Sub:Digital System Design Sub Code:17EE35

Q1a.Simplify the following Boolean function using K-map.
F(v,w,x,y,z)=∑m(3,7,8,10,11,12,14,15,17,19,21,23,25,27,29,31)+ ∑d(2,6,26,30) 10M
b.Using Quine-McCluskey method,simplify f(a,b,c,d)= ∑m(2,3,4,5,13,15)+dc(8,9,10,11) 10M

OR

Q2a.Simplify the Boolean expression using a 3 variable VEM with d as MEV.
F(a,b,c,d)= ∑m(1,3,7,11,15)+ ∑d(0,2,5) 10M
b.Use a logic circuit that has 4 inputs,the output will only be high,when the majority of the inputs are high.Use K-map to simplify 10M

Module 2

Q3a.Design and implement a 2 bit comparator 8M
b.Write the compressed truth table for a 4 to 2 line priority encoder with a valid output and simplify the same using K-map.Design the logic circuit as well. 6M
c.Implement the following Boolean function using a 4:1 Mux with A and B as select lines.
Y=f(A,B,C,D)= ∑m(0,1,2,4,6,9,12,14) 6M

OR

Q4a.Design and implement a 4 bit Carry look ahead adder 10M
b.Design a 4 to 16 decoder by cascading 2 to 4 decoders. 5M
c.Design an 8:1 Mux Tree using only 2:1 Multiplexers. 5M

Module 3

Q5a.Analyse the application of SR Flip Flop as switch debouncer with waveforms. 5M
b.Design a 4 bit twisted ring counter 5M
c.With a neat logic diagram,explain working of a Master slave JK Flip-Flop along with waveforms.Also brief about Race-around condition 10M

OR

Q6a.Differentiate Synchronous and Asynchronous counters 5M
b.Write short note on Shift Registers. 5M
c.Design Synchronous Mod-6 counter using SR Flip-Flops. 10M

Module 4

Q7a.With suitable example explain Mealy and Moore model in a sequential circuit analysis 10M
b.A sequential circuit has one input and one output. The state diagram is as shown below in Fig Q7b.Design a sequential circuit using D-FlipFlop. 10M

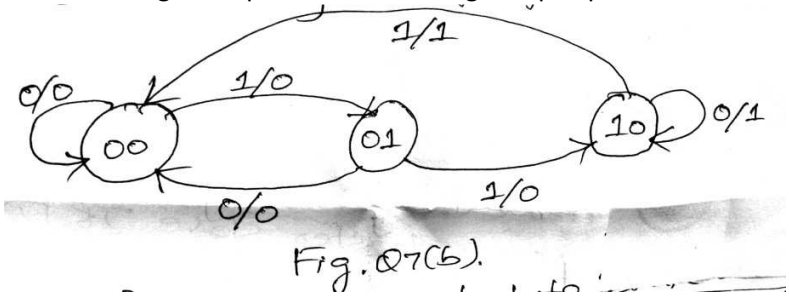

Fig. Q7(b).

Q8aDefine State,present state,Next state,State diagram and state table wit examples 10M

b.Design the sequential logic circuit for a single input and single output system fro the state diagram using JKFF.Analyze through state table and excitation table. 10M

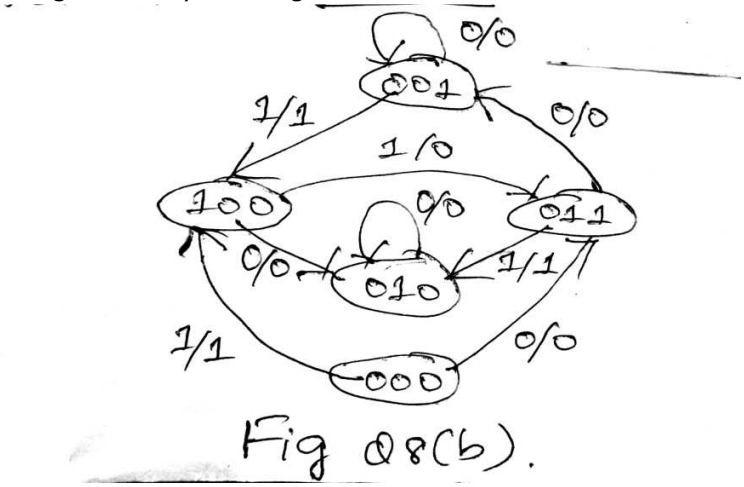

Fig Q8(b).

Module 5

Q9a.Mention various types of HDL description styles.Explain behavioral type with full adder example.10M

b.Compare VHDL and Verilog. 4M

c.Explain various data types of VHDL and Verilog. 6M

Q10a.Explain the various shift and rotate operators used in HDL with examples 10M

b.Write VHDL code to implememt 4:1 Multiplexer 6M

c.Implement a single bit Comparator for all input combinations in VHDL 4M