Visvesvaraya Technological University, Belagavi

CBCS Scheme: 2015-16

Model Question Paper

VLSI Design (15EI/BM/ML551)

Time: 3 hrs. **Max. Marks: 80**

Note: Answer any FIVE full questions, choosing one full question from each module.

Module 1

1. a. State and explain Moore's Law. **(04 Marks)**
   b. Give the comparison between CMOS and Bipolar technologies **(06 Marks)**
   c. Define Transconductance. Obtain the expression for transconductance of MOS transistors. **(06 Marks)**

OR

2. a. Give the Speed and Power performance analysis of the currently available technologies. **(04 Marks)**
   b. With figures, explain the CMOS p-well process. **(06 Marks)**
   c. Discuss the BiCMOS fabrication steps in n-well process. **(06 Marks)**

Module 2

3. a. With circuit and transfer characteristics, explain the working of nMOS inverter. **(06 Marks)**
   b. Obtain the pull-up to pull-down ratio for nMOS inverter driven through one or more pass transistors. **(10 Marks)**

OR

4. a. Define Latch-Up. Discuss the Latch-Up effect using circuit model. **(05 Marks)**
   b. Estimate the Rise time and Fall time of CMOS inverter with equations and model. **(06 Marks)**
   c. Write a note on BiCMOS drivers. **(05 Marks)**

Module 3

5. a. List the basic layers of MOS circuits. **(04 Marks)**
   b. With an example, explain nMOS design style. **(07 Marks)**
   c. With equations, explain the limitations of scaling in depletion width. **(05 Marks)**

OR

6. a. Write the stick diagrams for the following:
   i) p-well CMOS inverter ii) Simple n-well based BiCMOS inverter **(04 Marks)**
   b. With figures, explain the CMOS Lambda-based design rules. **(08 Marks)**
   c. Give the scaling factor for the following parameters:
   i) Gate Capacitance, C_g ii) Gate Delay, T_d
   iii) Switching energy per gate, E_g iv) Power-Speed product, P_T **(04 Marks)**

Module 4

7. a. With circuit and equations, discuss the Dynamic CMOS logic. **(08 Marks)**
   b. Describe the 4-bit Dynamic CMOS shift register with stick diagram. **(08 Marks)**

OR

8. a. Write a detailed note on the Parity generator with structured design and stick diagram. **(08 Marks)**
   b. Give the types of basic Bus architecture. **(04 Marks)**
   c. With block diagram, explain the subunits and basic interconnections for data path. **(04 Marks)**

Module 5

9. a. Explain the subsystem of 4-bit Data path for ALU. **(05 Marks)**
   b. With equations, explain the arrangement of 4-bit serial parallel multiplier. **(06 Marks)**
   c. Describe the three transistor dynamic RAM cell with circuit. **(05 Marks)**

OR

10. a. Discuss the implementation of ALU functions with an adder. **(08 Marks)**
    b. Give the circuit model for inverter driving another inverter on a Δoutput transition. **(04 Marks)**
    c. Write a note on CAD tools used for design and simulations. **(04 Marks)**

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