

ADVANCED ENGINEERING MATHEMATICS

[As per Choice Based Credit System (CBCS) scheme]

SEMESTER – I

Subject Code	16ELD11	IA Marks	20
Number of Lecture Hours/Week	04	Exam Marks	80
Total Number of Lecture Hours	50	Exam Hours	03

CREDITS – 04**Course objectives:** This course will enable students to:

- Acquaint with principles of linear algebra, calculus of variations, probability theory and random process.
- Apply the knowledge of linear algebra, calculus of variations, probability theory and random process in the applications of electronics and communication engineering sciences.

Modules	Teaching Hours	Revised Bloom's Taxonomy (RBT) Level
Module -1		
Linear Algebra-I Introduction to vector spaces and sub-spaces, definitions, illustrative examples and simple problems. Linearly independent and dependent vectors-definition and problems. Basis vectors, dimension of a vector space. Linear transformations- definition, properties and problems. Rank-Nullity theorem (without proof). Matrix form of linear transformations-Illustrative examples.	10 Hours (Text 1 & Ref. 1)	L1,L2
Module -2		
Linear Algebra-II Computation of Eigen values and Eigen vectors of real symmetric matrices-Given's method. Orthogonal vectors and orthogonal bases. Gram-Schmidt orthogonalization process. QR decomposition, singular value decomposition, least square approximations.	10 Hours (Text 1 & Ref. 1)	L1,L2
Module -3		

<p>Calculus of Variations Concept of functional-Eulers equation. functional dependent on first and higher order derivatives, functional on several dependent variables. Isoperimetric problems-variation problems with moving boundaries.</p>	<p>10 Hours (Text 2 & Ref. 2)</p>	<p>L1,L2</p>
<p>Module -4</p>		
<p>Probability Theory Review of basic probability theory. Definitions of random variables and probability distributions, probability mass and density functions, expectation, moments, central moments, characteristic functions, probability generating and moment generating functions-illustrations. Binomial, Poisson, Exponential, Gaussian and Rayleigh distributions-examples.</p>	<p>10 Hours (Text 3 & Ref. 3)</p>	<p>L1,L2</p>
<p>Module -5</p>		
<p>Joint probability distributions Definition and properties of CDF, PDF, PMF, conditional distributions. Expectation, covariance and correlation. Independent random variables. Statement of central limit theorem-Illustrative examples. Random process- Classification, stationary and ergodic random process. Auto correlation function-properties, Gaussian random process.</p>	<p>10 Hours (Text 3 & Ref. 3)</p>	<p>L1,L2</p>
<p>Course Outcomes: After studying this course, students will be able to:</p> <ol style="list-style-type: none"> 1. Understand vector spaces, basis, linear transformations and the process of obtaining matrix of linear transformations arising in magnification and rotation of images. 2. Apply the techniques of QR and singular value decomposition for data compression, least square approximation in solving inconsistent linear systems. 3. Utilize the concepts of functionals and their variations in the applications of communication systems, decision theory, synthesis and optimization of digital circuits. 4. Learn the idea of random variables (discrete/continuous) and probability distributions in analyzing the probability models arising in control systems and system communications. 5. Apply the idea of joint probability distributions and the role of parameter-dependent random variables in random process. 		

Question paper pattern:

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

1. David C.Lay, Steven R. Lay and J.J.McDonald: Linear Algebra and its Applications, 5th Edition, Pearson Education Ltd., 2015.
2. E. Kreyszig, “Advanced Engineering Mathematics”, 10th edition, Wiley, 2015.
3. Scott L.Miller, DonaldG. Childers: “Probability and Random Process with application to Signal Processing”, Elsevier Academic Press, 2nd Edition,2013.

Reference books:

1. Richard Bronson: “Schaum’s Outlines of Theory and Problems of Matrix Operations”, McGraw-Hill, 1988.
2. Elsgolts, L.:”Differential Equations and Calculus of Variations”, MIR Publications, 3rd Edition, 1977.
3. T.Veerarajan: “Probability, Statistics and Random Process“, 3rd Edition, Tata McGraw Hill Co.,2008.

Web links:

1. <http://nptel.ac.in/courses.php?disciplineId=111>
2. [http://www.class-central.com/subject/math\(MOOCs\)](http://www.class-central.com/subject/math(MOOCs))
3. <http://ocw.mit.edu/courses/mathematics/>
4. www.wolfram.com

<u>DIGITAL VLSI DESIGN</u>			
[As per Choice Based Credit System (CBCS) scheme]			
SEMESTER –I			
Subject Code	16EVE12	IA Marks	20
Number	04	Exam Marks	80
Total Number of	50	Exam Hours	03
CREDITS – 04			
<p>Course objectives: This course will enable students to:</p> <ol style="list-style-type: none"> 1. Explain VLSI Design Methodologies 2. Learn Static and Dynamic operation principles, analysis and design of inverter circuit. 3. Infer state of the art Semiconductors Memory circuits. 4. Outline the comprehensive coverage of Methodologies and Design practice that are used to reduce the Power Dissipation of large scale digital circuits. 5. Illustrate VLSI and ASIC design. 			
Modules		Teaching Hours	Revised Bloom's Taxonomy (RBT) Level
Module -1			
<p>MOS Transistor: The Metal Oxide Semiconductor (MOS) Structure, The MOS System under External Bias, Structure and Operation of MOS Transistor, MOSFET Current-Voltage Characteristics, MOSFET Scaling and Small-Geometry Effects.</p> <p>MOS Inverters-Static Characteristics: Introduction, Resistive-Load Inverter, Inverters with n_Type MOSFET Load.</p>		10 Hours	L1, L2
Module -2			

<p>MOS Inverters-Static Characteristics: CMOS Inverter.</p> <p>MOS Inverters: Switching Characteristics and Interconnect Effects: Introduction, Delay-Time Definition, Calculation of Delay Times, Inverter Design with Delay Constraints, Estimation of Interconnect Parasitics, Calculation of Interconnect Delay, Switching Power Dissipation of CMOS Inverters.</p>	<p>10 Hours</p>	<p>L2, L3</p>
<p>Module -3</p>		
<p>Semiconductor Memories: Introduction, Dynamic Random Access Memory (DRAM), Static Random Access Memory (SRAM), Nonvolatile Memory, Flash Memory, Ferroelectric Random Access Memory (FRAM).</p>	<p>10 Hours</p>	<p>L1, L2, L3</p>
<p>Module -4</p>		
<p>Dynamic Logic Circuits: Introduction, Basic Principles of Pass Transistor Circuits, Voltage Bootstrapping, Synchronous Dynamic Circuit Techniques, Dynamic CMOS Circuit Techniques, High Performance Dynamic CMOS Circuits.</p> <p>BiCMOS Logic Circuits: Introduction, Bipolar Junction Transistor (BJT): Structure and Operation, Dynamic Behavior of BJTs, Basic BiCMOS Circuits: Static Behavior, Switching Delay in BiCMOS Logic Circuits, BiCMOS Applications.</p>	<p>10 Hours</p>	<p>L1,L2, L3, L4</p>
<p>Module -5</p>		
<p>Chip Input and Output (I/O) Circuits: Introduction, ESD Protection, Input Circuits, Output Circuits and L(di/dt) Noise, On-Chip Clock Generation and Distribution, Latch-Up and Its Prevention.</p> <p>Design for Manufacturability: Introduction, Process Variations, Basic Concepts and Definitions, Design of Experiments and Performance Modeling.</p>	<p>10 Hours</p>	<p>L2, L3</p>

Course outcomes:

After studying this course, students will be able to:

1. Analyse issues of On-chip interconnect Modelling and Interconnect delay calculation.
2. Analyse the Switching Characteristics in Digital Integrated Circuits.
3. Use the Dynamic Logic circuits in state of the art VLSI chips.
4. Study critical issues such as ESD protection, Clock distribution, Clock buffering, and Latch phenomenon
5. Use Bipolar and Bi-CMOS circuits in very high speed design.

Graduate Attributes (as per NBA):

- Engineering Knowledge.
- Problem Analysis.
- Design / development of solutions (partly).
- Interpretation of data.

Question Paper Pattern

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

Sung Mo Kang & Yosuf Leblebici, "CMOS Digital Integrated Circuits: Analysis and Design", Tata McGraw-Hill, Third Edition.

Reference Books:

1. Neil Weste and K. Eshragian, "Principles of CMOS VLSI Design: A System Perspective", Second Edition, Pearson Education (Asia) Pvt. Ltd. 2000.
2. Wayne, Wolf, "Modern VLSI Design: System on Silicon" Prentice Hall PTR/Pearson Education, Second Edition, 1998.
3. Douglas A Pucknell & Kamran Eshragian, "Basic VLSI Design" PHI 3rd Edition (original Edition – 1994).

ADVANCED EMBEDDED SYSTEM			
[As per Choice Based Credit System (CBCS) scheme]			
SEMESTER – I			
Subject Code	16EVE13	IA Marks	20
Number of Lecture Hours/Week	04	Exam Marks	80
Total Number of Lecture Hours	50	Exam Hours	03
CREDITS – 04			
<p>Course objectives: This course will enable students to:</p> <ul style="list-style-type: none"> • Understand the basic hardware components and their selection method based on the characteristics and attributes of an embedded system. • Describe the hardware software co-design and firmware design approaches • Explain the architectural features of ARM CORTEX M3, a 32 bit microcontroller including memory map, interrupts and exceptions. • Program ARM CORTEX M3 using the various instructions, for different applications 			
Modules		Teaching Hours	Revised Bloom's Taxonomy (RBT) Level
Module -1			
<p>Embedded System: Embedded vs General computing system, classification, application and purpose of ES. Core of an Embedded System, Memory, Sensors, Actuators, LED, Optocoupler, Communication Interface, Reset circuits, RTC, WDT, Characteristics and Quality Attributes of Embedded Systems (Selected Topics from Ch -1, 2, 3 of Text 1).</p>		10 Hours	L1, L2, L3
Module -2			
<p>Hardware Software Co-Design, embedded firmware design approaches, computational models, embedded firmware development languages, Integration and testing of Embedded Hardware and firmware, Components in embedded system development environment (IDE), Files generated during compilation, simulators, emulators and debugging (Selected Topics From Ch-7, 9, 12, 13 of Text 1).</p>		10 Hours	L1, L2, L3, L4

Module -3		
ARM-32 bit Microcontroller: Thumb-2 technology and applications of ARM, Architecture of ARM Cortex M3, Various Units in the architecture, General Purpose Registers, Special Registers, exceptions, interrupts, stack operation, reset sequence (Ch 1, 2, 3 of Text 2).	10 Hours	L1, L2, L3
Module -4		
Instruction Sets: Assembly basics, Instruction list and description, useful instructions, Memory Systems, Memory maps, Cortex M3 implementation overview, pipeline and bus interface (Ch-4, 5, 6 of Text 2).	10 Hours	L1, L2, L3, L4
Module -5		
Exceptions, Nested Vector interrupt controller design, SysTick Timer, Cortex-M3 Programming using assembly and C language, CMSIS (Ch-7, 8, 10 of Text 2).	10 Hours	L1, L2, L3
<p>Course Outcomes: After studying this course, students will be able to:</p> <ul style="list-style-type: none"> • Understand the basic hardware components and their selection method based on the characteristics and attributes of an embedded system. • Explain the hardware software co-design and firmware design approaches. • Acquire the knowledge of the architectural features of ARM CORTEX M3, a 32 bit microcontroller including memory map, interrupts and exceptions. • Apply the knowledge gained for Programming ARM CORTEX M3 for different applications. 		
<p>Graduate Attributes (as per NBA)</p> <ul style="list-style-type: none"> • Engineering Knowledge. • Problem Analysis. • Design/Development of solutions 		
<p>Question paper pattern:</p> <ul style="list-style-type: none"> • The question paper will have 10 full questions carrying equal marks. • Each full question consists of 16 marks with a maximum of four sub questions. • There will be 2 full questions from each module covering all the topics of the module • The students will have to answer 5 full questions, selecting one full question from each module. 		
<p>Text Books:</p> <ol style="list-style-type: none"> 1. K. V. Shibu, "Introduction to embedded systems", TMH education Pvt. Ltd. 2009. 2. Joseph Yiu, "The Definitive Guide to the ARM Cortex-M3", 2nd edn, Newnes, (Elsevier), 2010. 		
<p>Reference Book: James K. Peckol, "Embedded systems- A contemporary design tool", John Wiley, 2008.</p>		

LOW POWER VLSI DESIGN

[As per Choice Based Credit System (CBCS) scheme]

SEMESTER –I

Subject Code	16EVE14	IA Marks	20
Number of Lecture Hours/Week	04	Exam Marks	80
Total Number of Lecture Hours	50	Exam Hours	03

CREDITS – 04**Course objectives:** This course will enable students to:

- Know the basics and advanced techniques in low power design which is a hot topic in today's market where the power plays a major role.
- Describe the various power reduction and the power estimation methods.
- Explain power dissipation at all layers of design hierarchy from technology, circuit, logic, architecture and system
- Apply State-of-the art approaches to power estimation and reduction.
- Practice the low power techniques using current generation design style and process technology

Modules	Teaching Hours	Revised Bloom's Taxonomy (RBT) Level
Module -1		
<p>Introduction: Need for low power VLSI chips, charging and discharging capacitance, short circuit current in CMOS leakage current, static current, basic principles of low power design, low power figure of merits.</p> <p>Simulation power analysis: SPICE circuit simulation, discrete transistor modeling and analysis, gate level logic simulation, architecture level analysis, data correlation analysis in DSP systems, Monte Carlo simulation.</p>	10 Hours (Text1)	L1, L2
Module -2		

<p>Probabilistic power analysis: Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy.</p> <p>Circuit: Transistor and gate sizing, equivalent pin ordering, network restructuring and reorganization, special latches and flip flops, low power digital cell library, adjustable device threshold voltage.</p>	<p>10 Hours (Text 1)</p>	<p>L1, L2, L3</p>
<p>Module -3</p>		
<p>Logic: Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic (Text 1).</p> <p>Low power Clock Distribution: Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip & package co design of clock network (Text 2).</p>	<p>10 Hours</p>	<p>L1, L2, L3</p>
<p>Module -4</p>		
<p>Low power Architecture & Systems: Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation (Text 1).</p> <p>Low power arithmetic components: Introduction, circuit design style, adders, multipliers, division (Text 2).</p>	<p>10 Hours</p>	<p>L1- L4</p>
<p>Module -5</p>		
<p>Low power memory design: Introduction, sources and reductions of power dissipation in memory subsystem, sources of power dissipation in DRAM and SRAM (Text 2).</p> <p>Algorithm & Architectural Level Methodologies: Introduction, design flow, Algorithmic level analysis & optimization, Architectural level estimation & synthesis (Text 2).</p> <p>Advanced Techniques: Adiabatic computation, pass transistor, Asynchronous circuits (Text 1).</p>	<p>10 Hours</p>	<p>L1-L4</p>

Course outcomes:

After studying this course, students will be able to:

- Identify the sources of power dissipation in CMOS circuits.
- Perform power analysis using simulation based approaches and probabilistic analysis.
- Use optimization and trade-off techniques that involve power dissipation of digital circuits.
- Make the power design a reality by making power dimension an integral part of the design process
- Use practical low power design techniques and their analysis at various levels of design abstraction and analyse how these are being captured in the latest design automation environments.

Graduate Attributes (as per NBA):

- Engineering Knowledge.
- Problem Analysis.
- Design / development of solutions (partly).
- Interpretation of data.

Question paper pattern:

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

1. Gary K. Yeap, "Practical Low Power Digital VLSI Design", Kluwer Academic, 1998.
2. Jan M.Rabaey, Massoud Pedram, "Low Power Design Methodologies" Kluwer Academic, 2010.

Reference Books:

1. Kaushik Roy, Sharat Prasad, "Low-Power CMOS VLSI Circuit Design" Wiley, 2000
2. A.P.Chandrasekaran and R.W.Broadersen, "Low power digital CMOS design", Kluwer Academic, 1995.
3. A Bellamour and M I Elmasri, " Low power VLSI CMOS circuit design", Kluwer Academic, 1995.

DIGITAL SYSTEM DESIGN USING VERILOG
 [As per Choice Based Credit System (CBCS) scheme]
 SEMESTER – I

Subject Code	16EVE151	IA Marks	20
Number of Lecture Hours/Week	03	Exam Marks	80
Total Number of Lecture Hours	40	Exam Hours	03
CREDITS – 03			
<p>Course objectives: This course will enable students to:</p> <ul style="list-style-type: none"> • Understand the concepts of Verilog Language • Design the digital systems as an activity in a larger systems design context. • Study the design and operation of semiconductor memories frequently used in application specific digital system. • Inspect how effectively IC's are embedded in package and assembled in PCB's for different application • Design and diagnosis of processors and I/O controllers they can be used in embedded systems 			
Modules		Teaching Hours	Revised Bloom's Taxonomy (RBT) Level
Module -1			
Introduction and Methodology: Digital Systems and Embedded Systems, Binary representation and Circuit Elements, Real-World Circuits, Models, Design Methodology.		8 Hours	L1, L2
Module -2			
Number Basics: Unsigned and Signed Integers, Fixed and Floating-point Numbers. Sequential Basics: Storage elements, Counters, Sequential Data paths and Control, Clocked Synchronous Timing Methodology.		8 Hours	L1, L2
Module -3			
Memories: Concepts, Memory Types, Error Detection and Correction. Implementation Fabrics: ICs, PLDs, Packaging and Circuit Boards, Interconnection and Signal Integrity.		8 Hours	L1, L2
Module -4			

<p>Processor Basics: Embedded Computer Organization, Instruction and Data, Interfacing with memory. I/O interfacing: I/O devices, I/O controllers, Parallel Buses, Serial Transmission, I/O software.</p>	8 Hours	L2, L3
Module -5		
<p>Accelerators: Concepts, case study, Verification of accelerators. Design Methodology: Design flow, Design optimization, Design for test.</p>	8 Hours	L2, L3
<p>Course outcomes: After studying this course, students will be able to:</p> <ol style="list-style-type: none"> 1. Design embedded systems, using small microcontrollers, larger CPUs/DSPs, or hard or soft processor cores. 2. Design & Construct the combinational circuits using discrete gates and programmable logic devices. 3. Describe Verilog model for sequential circuits and test pattern generation 4. Explore the different types of semiconductor memories and their usage for specific chip design 5. Design and synthesis of different types of processor and I/O controllers that are used in embedded system design 		
<p>Graduate Attributes (as per NBA):</p> <ul style="list-style-type: none"> o Engineering Knowledge. o Problem Analysis. o Design / development of solutions (partly). o Interpretation of data. 		
<p>Question paper pattern:</p> <ul style="list-style-type: none"> • The question paper will have 10 full questions carrying equal marks. • Each full question consists of 16 marks with a maximum of four sub questions. • There will be 2 full questions from each module covering all the topics of the module • The students will have to answer 5 full questions, selecting one full question from each module. 		
<p>Text Book: Peter J. Ashenden, “Digital Design: An Embedded Systems Approach Using VERILOG”, Elsevier, 2010.</p>		
<p>Reference Book: Verilog HDL: A Guide to Digital Design and Synthesis, Second Edition by Samir Palnitkar.</p>		

NANOELECTRONICS [As per Choice Based Credit System (CBCS) scheme] SEMESTER – I			
Subject Code	16EVE152	IA Marks	20
Number of Lecture Hours/Week	03	Exam Marks	80
Total Number of Lecture Hours	40	Exam Hours	03
CREDITS – 03			
<p>Course objectives: This course will enable students to:</p> <ul style="list-style-type: none"> • Enhance basic engineering science and technological knowledge of nanoelectronics. • Explain basics of top-down and bottom-up fabrication process, devices and systems. • Describe technologies involved in modern day electronic devices. • Appreciate the complexities in scaling down the electronic devices in the future. 			
Modules		Teaching hours	Revised Bloom's Taxonomy (RBT)
Module -1			
<p>Introduction: Overview of nanoscience and engineering. Development milestones in microfabrication and electronic industry. Moores law and continued miniaturization, Classification of Nanostructures, Electronic properties of atoms and solids: Isolated atom, Bonding between atoms, Giant molecular solids, Free electron models and energy bands, crystalline solids, Periodicity of crystal lattices, Electronic conduction, effects of nanometerlength scale, Fabrication methods: Top down processes, Bottom up processes methods for templating the growth of nanomaterials, ordering of nanosystems (Text 1).</p>		8 Hours	L1, L2
Module -2			
<p>Characterization: Classification, Microscopic techniques, Field ion microscopy, scanning probe techniques, diffraction techniques: bulk and surface diffraction techniques (Text 1).</p>		8 Hours	L2,L3

Module -3		
<p>Characterization: spectroscopy techniques: photon, radiofrequency, electron, surface analysis and dept profiling: electron, mass, Ion beam, Reflectometry, Techniques for property measurement: mechanical, electron, magnetic, thermal properties.</p> <p>Inorganic semiconductor nanostructures: overview of semiconductor physics. Quantum confinement in semiconductor nanostructures: quantum wells, quantum wires, quantum dots, super-lattices, band offsets, electronic density of states (Text 1).</p>	8 Hours	L1-L3
Module -4		
<p>Fabrication techniques: requirements of ideal semiconductor, epitaxial growth of quantum wells, lithography and etching, cleaved-edge over growth, growth of vicinal substrates, strain induced dots and wires, electrostatically induced dots and wires, Quantum well width fluctuations, thermally annealed quantum wells, semiconductor nanocrystals, collidal quantum dots, self-assembly techniques.</p> <p>Physical processes: modulation doping, quantum hall effect, resonant tunneling, charging effects, ballistic carrier transport, Inter band absorption, intraband absorption, Light emission processes, phonon bottleneck, quantum confined stark effect, nonlinear effects, coherence and dephasing, characterization of semiconductor nanostructures: optical electrical and structural (Text 1).</p>	8 Hours	L1-L3
Module -5		
<p>Methods of measuring properties: atomic, crystallography, microscopy, spectroscopy (Text 2).</p> <p>Applications: Injection lasers, quantum cascade lasers, single-photon sources, biological tagging, optical memories, coulomb blockade devices, photonic structures, QWIP's, NEMS, MEMS (Text 1).</p>	8 Hours	L1-L4

Course outcomes:

After studying this course, students will be able to:

- Know the principles behind Nanoscience engineering and Nanoelectronics.
- Apply the knowledge to prepare and characterize nanomaterials.
- Know the effect of particles size on mechanical, thermal, optical and electrical properties of nanomaterials.
- Design the process flow required to fabricate state of the art transistor technology.
- Analyze the requirements for new materials and device structure in the future technologies.

Graduate Attributes (as per NBA):

- Engineering Knowledge.
- Problem Analysis.
- Design / development of solutions (partly).
- Interpretation of data.

Question paper pattern:

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

1. Ed Robert Kelsall, Ian Hamley, Mark Geoghegan, “Nanoscale Science and Technology”, John Wiley, 2007.
2. Charles P Poole, Jr, Frank J Owens, “Introduction to Nanotechnology”, John Wiley, Copyright 2006, Reprint 2011.

Reference Book:

Ed William A Goddard III, Donald W Brenner, Sergey E. Lyshevski, Gerald J Iafrate, “Hand Book of Nanoscience Engineering and Technology”, CRC press, 2003.

ASIC DESIGN			
[As per Choice Based Credit System (CBCS) scheme]			
SEMESTER – I			
Subject Code	16EVE153	IA Marks	20
Number of Lecture Hours/Week	03	Exam Marks	80
Total Number of Lecture Hours	40	Exam Hours	03
CREDITS – 03			
<p>Course objectives: This course will enable students to:</p> <ul style="list-style-type: none"> • Explain ASIC methodologies and programmable logic cells to implement a function on IC. • Analyse back-end physical design flow, including partitioning, floor-planning, placement, and routing. • Gain sufficient theoretical knowledge for carrying out FPGA and ASIC designs. • Design CAD algorithms and explain how these concepts interact in ASIC design. 			
Modules		Teaching Hours	Revised Bloom's Taxonomy (RBT)Level
Module -1			
<p>Introduction to ASICs, Full custom, Semi-custom and Programmable ASICs, ASIC Design flow, ASIC cell libraries. CMOS Logic: Datapath Logic Cells: Data Path Elements, Adders: Carry skip, Carry bypass, Carry save, Carry select, Conditional sum, Multiplier (Booth encoding), Data path Operators, I/O cells.</p>		08 Hours	L1-L2
Module -2			
<p>ASIC Library Design: Logical effort: Predicting Delay, Logical area and logical efficiency, Logical paths, Multi stage cells, Optimum delay and number of stages. Programmable ASIC Logic Cells: MUX as Boolean function generators, Actel ACT: ACT 1, ACT 2 and ACT 3 Logic Modules, Xilinx LCA: XC3000 CLB, Altera FLEX and MAX.</p>		08 Hours	L1-L3
Module -3			

<p>Programmable ASIC I/O Cells: Xilinx and Altera I/O Block. Low-level design entry: Schematic entry: Hierarchical design, Netlist screener. ASIC Construction: Physical Design, CAD Tools. Partitioning: Goals and objectives, Constructive Partitioning, Iterative Partitioning Improvement, KL, FM and Look Ahead algorithms.</p>	<p>08 Hours</p>	<p>L1-L4</p>
<p>Module -4</p>		
<p>Floor planning and placement: Goals and objectives, Floor planning tools, Channel definition, I/O and Power planning and Clock planning. Placement: Goals and Objectives, Min-cut Placement algorithm, Iterative Placement Improvement, Physical Design Flow.</p>	<p>08 Hours</p>	<p>L1-L4</p>
<p>Module -5</p>		
<p>Routing: Global Routing: Goals and objectives, Global Routing Methods, Back-annotation. Detailed Routing: Goals and objectives, Measurement of Channel Density, Left-Edge and Area-Routing Algorithms. Special Routing, Circuit extraction and DRC.</p>	<p>08 Hours</p>	<p>L1-L4</p>
<p>Course outcomes: After studying this course, students will be able to:</p> <ol style="list-style-type: none"> 1. Describe the concepts of ASIC design methodology, data path elements, logical effort and FPGA architectures. 2. Analyze the design of FPGAs and ASICs suitable for specific tasks, perform design entry and explain the physical design flow. 3. Design data path elements for ASIC cell libraries and compute optimum path delay. 4. Create floorplan including partition and routing with the use of CAD algorithms. 		
<p>Graduate Attributes (as per NBA):</p> <ul style="list-style-type: none"> ○ Engineering Knowledge. ○ Problem Analysis. ○ Design / development of solutions (partly). ○ Interpretation of data. 		
<p>Question paper pattern:</p> <ul style="list-style-type: none"> • The question paper will have 10 full questions carrying equal marks. • Each full question consists of 16 marks with a maximum of four sub questions. • There will be 2 full questions from each module covering all the topics of the module • The students will have to answer 5 full questions, selecting one full question from each module. 		

Text Book:

Michael John Sebastian Smith, "Application - Specific Integrated Circuits" Addison-Wesley Professional; 2005.

Reference Books:

1. Neil H.E. Weste, David Harris, and Ayan Banerjee, "CMOS VLSI Design: A Circuits and Systems Perspective", 3rd edition, Addison Wesley/ Pearson education, 2011.
2. Vikram Arkalgud Chandrasetty, "VLSI Design: A Practical Guide for FPGA and ASIC Implementations", Springer, 2011, ISBN: 978-1-4614-1119-2.
3. Rakesh Chadha, Bhasker J., "An ASIC Low Power Primer", Springer, ISBN: 978-1-4614-4270-7.

ADVANCED COMPUTER ARCHITECTURE
[As per Choice Based Credit System (CBCS) scheme]
SEMESTER – I

Subject Code	16ELD154	IA Marks	20
Number of Lecture Hours/Week	03	Exam Marks	80
Total Number of Lecture Hours	40	Exam Hours	03

CREDITS – 03

Course objectives: This course will enable students to:

- Understand the basic concepts for parallel processing
- Analyze program partitioning and flow mechanisms
- Apply pipelining concept for the performance evaluation
- Learn the advanced processor architectures for suitable applications

Modules	Teaching Hours	Revised Bloom's Taxonomy (RBT) Level
Module -1		
Parallel Computer Models: Classification of parallel computers, Multiprocessors and multicomputers, Multivector and SIMD computers. Program and Network Properties, Conditions of parallelism, Data and resource Dependences, Hardware and software parallelism.	8 Hours (Text 1)	L2, L3, L4
Module -2		
Program partitioning and scheduling, Grain Size and latency, Program flow mechanisms, Control flow versus data flow, Data flow Architecture, Demand driven mechanisms, Comparisons of flow mechanisms, Principles of Scalable Performance, Performance Metrics and Measures, Parallel Processing Applications, Speedup Performance Laws, Scalability Analysis and Approaches.	8 Hours (Text 1)	L2, L3, L4
Module -3		
Advanced Processors: Advanced processor technology, Instruction-set Architectures, CISC Scalar Processors, RISC Scalar Processors, Superscalar Processors, VLIW Architectures, Pipelining, Linear pipeline processor, nonlinear pipeline processor, Instruction pipeline design.	8 Hours (Text 1)	L1, L2, L3
Module -4		

Mechanisms for instruction pipelining, Dynamic instruction scheduling, Branch Handling techniques, branch prediction, Arithmetic Pipeline Design, Computer arithmetic principles, Static Arithmetic pipeline, Multifunctional arithmetic pipelines.	8 Hours (Text 1)	L2, L3, L4
Module -5		
Multithread and Dataflow Architecture: Principles of Multithreading, Scalable and Multithreaded Architecture, Data flow Architecture, Symmetric shared memory architecture, distributed shared memory architecture.	8 Hours (Text 1 & 2)	L1, L2, L3
<p>Course outcomes: At the end of this course, the students will be able to:</p> <ul style="list-style-type: none"> • Understand the basic concepts for parallel processing • Analyze program partitioning and flow mechanisms • Apply pipelining concept for the performance evaluation • Learn the advanced processor architectures for suitable applications 		
<p>Graduating Attributes (as per NBA)</p> <ul style="list-style-type: none"> • Engineering Knowledge • Problem Analysis • Design / development of solutions 		
<p>Question paper pattern:</p> <ul style="list-style-type: none"> • The question paper will have 10 full questions carrying equal marks. • Each full question consists of 16 marks with a maximum of four sub questions. • There will be 2 full questions from each module covering all the topics of the module • The students will have to answer 5 full questions, selecting one full question from each module. 		
<p>Text Books:</p> <ol style="list-style-type: none"> 1. Kai Hwang, “Advanced computer architecture”, TMH. 2007. 2. Kai Hwang and Zu, “Scalable Parallel Computers Architecture”, MGH, 2008. 		
<p>Reference Books:</p> <ol style="list-style-type: none"> 1. M.J. Flynn, “Computer Architecture, Pipelined and Parallel Processor Design”, Narosa Publishing, 2002. 2. D.A.Patterson, J.L.Hennessy, “Computer Architecture: A quantitative approach”, Morgan Kauffmann feb, 2002. 		

VLSI and ES LAB - 1

[As per Choice Based Credit System (CBCS) scheme]

SEMESTER – I

Laboratory Code	16EVEL16	IA Marks	20
Number of Lecture Hours/Week	01Hr Tutorial (Instructions) + 02 Hours Laboratory	Exam Marks	80
		Exam Hours	03

CREDITS – 02

Course objectives: This course will enable students to:

- Learn Verilog Code Programming for the design of digital circuits
- Use FPGA/CPLD board and Logic Analyzer or Chipscope to verify the results
- Learn Assembly language programming for different applications using ARM-Cortex M3 Kit and Keil uvision- 4 tool.
- Learn C language programming for different applications using ARM- Cortex M3 Kit and Keil uvision-4 tool.

Laboratory Experiments:

**Revised
Bloom's
Taxonomy**

- 1) **Digital Design Experiments:** Using Verilog code and any Compiler. Download code to FPGA/CPLD board and verify the output using Logic Analyzer or Chipscope
- a) Design and verify an 8 to 3 programmable priority encoder
 - b) Design and verify 3-bit Arbitrary Counter and repeat the given sequence
 - c) Design and Verify BCD adder and subtractor
 - d) Design and verify a sequential block to generate a sequence (say 11101) using appropriate FSM.
 - e) Design and verify 8 bit Ripple carry adder and Carry skip adder.
 - f) Design and verify a Linear feedback shift register based on a given polynomial expression
 - g) Design and verify the following 8 bit multipliers. Also report on area delay trade-off
 - i) Serial Multiplier
 - ii) Parallel Multiplier
 - h) Design and verify a parameterized FIFO
 - i) Design and verify register file which has 32-entry 3-ports having explicit address decoder. The ports are dedicated for read and write and will take one clock cycle for read or write operation

L2,L3,L4,L5

<p>2) ARM Cortex M3 Programs: (Programming to be done using Keil uvision 4 and download the program on to a M3 evaluation board such as NXP LPC1768 or ATMEL ATSAM3U)</p> <ol style="list-style-type: none"> a) Write an Assembly language program to calculate the sum and display the result for the addition of first ten numbers. SUM = 10+9+8+.....+1 b) Write a Assembly language program to link multiple object files and link them together c) Write an Assembly language program to store data in RAM d) Write a C program to Output the “Hello World” message using UART e) Write a C program to Design a Stopwatch using interrupts 	<p>L2,L3,L4</p>
<p>Course outcomes: On the completion of this laboratory course, the students will be able to:</p> <ul style="list-style-type: none"> • Develop Verilog Code for the design of digital circuits • Use FPGA/CPLD board and Logic Analyzer or Chipscope to verify the results • Develop Assembly language programs for different applications using ARM-Cortex M3 Kit and Keiluvision-4 tool. • Develop C language programs for different applications using ARM-Cortex M3 Kit and Keil uvision-4 tool 	
<p>Graduate Attributes (as per NBA)</p> <ul style="list-style-type: none"> • Engineering Knowledge. • Problem Analysis. • Design/Development of solutions. 	
<p>Conduct of Practical Examination:</p> <ul style="list-style-type: none"> • All laboratory experiments are to be included for practical examination. • For examination, two questions using different tool to be set. • Students are allowed to pick one experiment from the lot. • Strictly follow the instructions as printed on the cover page of answer script for breakup of marks. • Change of experiment is allowed only once and Marks allotted to the procedure part to be made zero. 	