# VISVESVARAYA TECHNOLOGICAL UNIVERSITY
## ವಿಶ್ವೇಶ್ವರಯ್ಯ ತಾಂತ್ರಿಕ ವಿಶ್ವವಿದ್ಯಾಲಯ
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**Dr. Satish Annigeri**
**Registrar In-Charge**
Ref: VTU/TEQIP 3/2019/ 123

Date: 10 JUL 2019

**CIRCULAR**

**Sub:** Faculty Development Program – Reg.
**Ref:** Hon'ble Vice Chancellor approval dated: 03/07/2019

With reference to the above cited subject, this is to inform that Faculty Development Program on "AI, Machine Learning and it's Hardware prototyping" is scheduled from 29th July to 4th August 2019, at VTU Campus Belagavi. This is arranged for Faculty members of VTU PG Centre Belagavi and VTU RRC Research Scholars.

**Guidelines:**

- There is no Registration Fee.
- Participants have to make their own Food Arrangements. Tea will be served on the days of the workshop.
- Accommodation will be provided in the Hostels at Nominal Charges, subjected to availability.
- No. of participants is restricted to 25 only.
- All participants will get course completion certificate from Coreel Technologies Pvt. Ltd., on successful completion.
- Resource Persons are from Mathworks and Coreel Technologies.
- Selected candidates will be intimated through e-mail.

Interested Faculty Members/VTU RRC Research Scholars may complete the enclosed Form and send to the below address on or before 20th July 2019. Also, the scanned copy of the same shall be sent to teqip@vtu.ac.in

TEQIP Cell
Visvesvaraya Technological University
"Jnana Sangama", Belagavi – 590018
Karnataka, India

**REGISTRAR**

**To,**

1. Department of E&C & CS, VTU PG Centre Belagavi.
2. RRC Office, VTU Belagavi.

**Encl:**

1. Registration Form, NoC and Declaration by the candidate
2. Contents of the workshop

**Copy for information to:**

1. The Secretary to Vice Chancellor, VTU, Belagavi.
2. The PS to Registrar, VTU, Belagavi.
3. The Finance Officer, VTU, Belagavi.
4. The TEQIP Co-ordinator, VTU, Belagavi.

## REGISTRATION FORM

| | |
|---|---|
| Name | |
| USN | |
| Designation | |
| Department and Organization | |
| Contact Details<br>(Email ID and Contact No.) | |
| Area of Research | |

## NO OBJECTION CERTIFICATE

The applicant Prof./ Mr./Ms._____from our institution will be permitted to attend Faculty Development Program on "AI, Machine Learning and it's Hardware prototyping" scheduled from 29th July to 4th August 2019, at VTU Campus Belagavi.

Place:
Date:

Signature
(Head of the Institution with seal)

## DECLARATION BY THE CANDIDATE

I agree to maintain the discipline and submit the deliverables of the entire course of Faculty Development Program on "AI, Machine Learning and it's Hardware prototyping" scheduled from 29th July to 4th August 2019 and I shall participate in the course for entire duration, if selected.

Place:
Date:

Signature of the Participant

(Scanned copy to be submitted in through email to teqip@vtu.ac.in)

CoreEL Technologies

# COURSE OUTLINE

## Day 1 - Machine Learning with MATLAB

### Importing and Organizing Data (2 hrs)

Bring data into MATLAB and organize it for analysis, including normalizing data and removing observations with missing values.

- Data types
- Tables
- Categorical data
- Data preparation

### Finding Natural Patterns in Data (2 hrs)

Use unsupervised learning techniques to group observations based on a set of explanatory variables and discover natural patterns in a data set.

- Unsupervised learning
- Clustering methods
- Cluster evaluation and interpretation

### Building Classification Models (3 hrs)

Use supervised learning techniques to perform predictive modeling for classification problems. Evaluate the accuracy of a predictive model.

- Supervised learning
- Training and validation
- Classification methods

## Day 2 - Machine Learning with MATLAB-Contd.

### Improving Predictive Models (2 hrs)

Reduce the dimensionality of a data set. Improve and simplify machine learning models.

- Cross validation
- Hyperparameter optimization
- Feature transformation
- Feature selection
- Ensemble learning

### Building Regression Models (2.5 hrs)

Use supervised learning techniques to perform predictive modeling for continuous response variables.

- Parametric regression methods
- Nonparametric regression methods
- Evaluation of regression models

### Creating Neural Networks (2.5 hrs)

Create and train neural networks for clustering and predictive modeling. Adjust network architecture to improve performance.

- Clustering with Self-Organizing Maps
- Classification with feed-forward networks
- Regression with feed-forward networks

## Day 3 - Deep Learning with MATLAB

### Transfer Learning for Image Classification (2.5 hrs)

Perform image classification using pretrained networks. Use transfer learning to train customized classification networks.

- Pretrained networks
- Image datastores
- Transfer learning
- Network evaluation

### Interpreting Network Behavior (1.5 hrs)

Gain insight into how a network is operating by visualizing image data as it passes through the network. Apply this technique to different kinds of images.

- Activations
- Feature extraction for machine learning

### Creating Networks (2 hrs)

Build convolutional networks from scratch. Understand how information is passed between network layers and how different types of layers work.

- Training from scratch
- Neural networks
- Convolution layers and filters

### Training a Network (1 hrs)

Understand how training algorithms work. Set training options to monitor and control training.

- Network training
- Training progress plots
- Validation

## Day 4 - Deep Learning with MATLAB-Contd.

### Improving Network Performance (2 hrs)

Choose and implement modifications to training algorithm options, network architecture, or training data to improve network performance.

- Training options
- Directed acyclic graphs
- Augmented datastores

### Performing Image Regression (1 hrs)

Create convolutional networks that can predict continuous numeric responses.

- Transfer learning for regression
- Evaluation metrics for regression networks

### Detecting Objects in Images (1 hrs)

Train networks to locate and label specific objects within images.

- Object detection

### Classifying Sequence Data (2 hrs)

Build and train networks to perform classification on ordered sequences of data, such as time series or sensor data.

- Long short-term memory networks
- Sequence classification
- Sequence preprocessing
- Categorical sequences

**Generating Sequences of Output (1 hrs)**

Use recurrent networks to create sequences of predictions.

- Sequence to sequence classification
- Sequence forecasting

## Day 5:

Day 5 is agenda divided into two sections

- First section is HDL code conversion and its FPGA implementation.
- Second Section is Machine Learning algorithm implemented on Nvidia Platform

## MATLAB TO FPGA IMPLEMENTATION DESIGN FLOW

**Code Generation from MATLAB (1.5 hrs)**

Enabling HDL Code Generation from MATLAB

- Introduction to HDL Coder
- HDL Coder environment setup
- Hands on session on HDL Code conversion.

Lab 1: Hands on: Filter design using program and app, Visualization of filter's response FDA tool features generation of HDL Coder. Generate HDL code for the specified design.

**Enabling HDL Code Generation with HDL CODER and Verification using HDL VERIFER (1.5 hrs)**

Lab 2: Hands on session on HDL Code generation from MATLAB functions for an adder

- Automatic HDL code generation
- Flow of FPGA Design
- Working with functions

Lab 3: Demonstration on HDL Code generation from MATLAB functions for image edge detection and deploying it on Zed Board FPGA.

## MATLAB TO NVIDIA GPU IMPLEMENTATION DESIGN FLOW

**Architecture and Overview of Nvidia GPU (30 mins)**

- Overview of Nvidia GPU
- Architecture of Nvidia GPU
- NVIDIA DRIVE Support from GPU Coder

**Code Generation from MATLAB (30 mins)**

Enabling CUDA Code Generation from MATLAB

- Introduction to CUDA Coder
- Generate Fast, Flexible CUDA Coder
- Generate Code from supported toolboxes and functions

**Deploy End-To-End Algorithms on Nvidia Tx2 Platform (2 hrs)**

Demonstration on Enabling MATLAB to Deploy Machine Learning Algorithms on Nvidia Tx2 Platform.

**Day 6:**

- Xilinx FPGA Design Flow.
- Overview of 7-series FPGA Architecture with one hands on example deployed on Nexys A7 Board.
- Demonstration of Image Processing using Nexys A7 Board
- Embedded System Design using ZED Board and ZCU104 Board.
- Demonstration of audio processing Design using Vivado HLS on ZED Board.

**Day 7:**

- Xilinx SDSoC Flow
- Demonstration of Machine learning algorithm implementation using Xilinx SDSoC on ZCU104 Board.