VISVESVARAYA TECHNOLOGICAL UNIVERSITY
ವಿಶ್ವೇಶ್ವರಯ್ಯ ತಾಂತ್ರಿಕ ವಿಶ್ವವಿದ್ಯಾಲಯ
"Jnana Sangama", Belagavi - 590 018, Karnataka State, INDIA

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Dr. H. N. Jagannatha Reddy B.E., M.E., Ph.D.
Registrar

Ref: VTU/BGM/PG/VLSI/2017-18/12027 **Date:** 27 MAR 2018

CIRCULAR

Sub: VGST sponsored Faculty Development Program on "System Design using SystemVerilog" – Reg.

With reference to the above, it is to inform that, Center for PG Studies, Dept. of VLSI Design and Embedded Systems, VTU Belagavi is organizing VGST sponsored Faculty Development Program on "System Design using SystemVerilog" from 24.04.2018 to 27.04.2018.

SystemVerilog is a hardware design and verification language (HDVL). As per the literature SystemVerilog will become the dominant HDL and provide significant benefits to the current and future generation of hardware designers, architects and verification engineers. The objective of this FDP is to create a platform for faculty members to get an experience in the field of System Design using SystemVerilog. This FDP aims to provide good theoretical and practical knowledge to the faculty members to carry out their research work and to impart better training to students.

The interested faculty members shall register for the FDP by using the link https://goo.gl/forms/5Fo4UcRH2bsP5ltH3

There is no registration fee. However the hard copy of the No Objection Certificate has to be submitted in advance to the address mentioned below:

Dr. Meghana Kulkarni
Dept. of VLSI Design and Embedded Systems,
Center for PG Studies,
"Jnana Sangama" Visvesvaraya Technological University,
Belagavi-590018, Karnataka.
E-mail: meghanak@vtu.ac.in
Mobile: 9480398197

The important dates are

Last date for online registration and hard copy of NoC submission	12th April 2018
Confirmation to the participants	16th April 2018

Hence, you are requested to bring this circular to the notice of the concerned faculty in your college and inform them to participate in this Program.

Brochure of the event is enclosed for your reference.

27/03/18
REGISTRAR

To,

1. The Principal of All Affiliated/Constituent/Autonomous Engineering Colleges Under VTU, Belagavi
2. The PG Coordinators of All VTU PG Centres of VTU, Belagavi

Copy to:

1. Hon'ble Vice- Chancellor through Secretary to VC, VTU, Belagavi for information.
2. The Finance Officer, VTU, Belagavi for information.

NO OBJECTION CERTIFICATE

The applicant Prof./Dr./Mr./Ms._____ from our institution will be permitted to attend the VGST Sponsored Faculty Development Program on _____ to be held during _____to _____at Center of Post Graduate Studies, Visvesvaraya Technological University (VTU), Belagavi.

Place:
Date: Signature
(Head of the Institution with seal)

DECLARATION BY THE CANDIDATE

I agree to maintain the discipline for the entire course of VGST Sponsored Faculty Development Program scheduled from _____to_____ and I shall participate in the course for entire duration, if selected.

Place:
Date: Signature of the Participant

Scanned copy to be submitted through email to meghanak@vtu.ac.in and hard copy to be submitted to the address given below in advance.

ADDRESS OF COMMUNICATION

Dr. Meghana Kulkarni
Program Coordinator
Dept. of VLSI Design and Embedded Systems
Visvesvaraya Technological University
"Jnana Sangama", Belagavi – 590018
Karnataka, India
Mob: 9480398197
Email :meghanak@vtu.ac.in

ADVISORY COMITTEE

1. **Dr. Karisiddappa**
   Hon'ble Vice- Chancellor, VTU, Belagavi
2. **Dr. H. N. Jagannatha Reddy,**
   Registrar, VTU, Belagavi
3. **Dr. Satish Annigeri,**
   Registrar (Evaluation), VTU, Belagavi
4. **Smt. M. A. Sapana,**
   Finance Officer, VTU Belagavi.

PROGRAM CHAIR

Dr. Anand V. Shivapur
Regional Director and PG Coordinator,
VTU Belagavi.

Dr. T. C. Thanuja
Prof. and Head
Dept. of VLSI Design and Embedded Systems
VTU Belagavi.

ORGANIZING COMITTEE

Mr. Mahesh Neelgar
Assistant Professor,
Dept. of VLSI Design and Embedded Systems
CPGS, VTU, Belagavi.

Miss. Anuradha Parvatikar
Faculty,
Dept. of VLSI Design and Embedded Systems
CPGS, VTU, Belagavi.

VISVESVARAYA TECHNOLOGICAL UNIVERSITY

"JNANA SANGAMA", BELAGAVI

VGST Sponsored

FACULTY DEVELOPMENT PROGRAM on System Design using SystemVerilog

24th to 27th April 2018

Organized By
Dept. of VLSI Design and Embedded Systems
Center for PG Studies, VTU Belagavi.

In Association with

C-Quad Computers
Belagavi

CO-ORDINATOR

Dr. Meghana Kulkarni
Associate Professor
Dept. of VLSI Design and Embedded Systems,
CPGS, VTU, Belagavi

ABOUT VTU

Visvesvaraya Technological University (VTU) is one of the largest Technological Universities in India with 12B certification from UGC. It came into existence in the year 1998 to cater the needs of Indian industries for trained technical manpower with practical experience and sound theoretical knowledge. University has successfully achieved the tremendous task of bringing various colleges affiliated earlier to different Universities, with different syllabi, different procedures and different traditions under one umbrella.

It has four regional centers across the State of Karnataka in Belagavi, Bengaluru, Kalaburagi and Mysuru respectively. University is comprised of a multi-disciplinary and multi-level institution offering wide ranging programmes in engineering, technology and Management.

VTU is the first university in the country to adopt Innovative steps in the examination reforms by adopting Digital Evaluation System.

Centre for Post Graduate Studies

Centre for Post Graduate studies, Belagavi was established in the year 2002 with all necessary infrastructure required for imparting quality education. There are five full time M.Tech. programs, MBA and MCA. All the programs have well qualified and experienced faculty members.

VLSI Design and Embedded Systems

VLSI Design and Embedded Systems program was established in the year 2003 in the VTU campus. All faculty members have wide professional expertise and are actively involved in research and technical activities. The department has well equipped laboratories. The area of research includes VLSI Design, Embedded Systems, and VLSI for communication etc.

ABOUT THE PROGRAM

SystemVerilog is a hardware design and verification language (HDVL). As per the literature SystemVerilog will become the dominant HDL and provide significant benefits to the current and future generation of hardware designers, architects and verification engineers.

The objective of this FDP is to create a platform for faculty members to get an experience in the field of System Design using SystemVerilog. This FDP aims to provide good theoretical and practical knowledge to the faculty members to carry out their research work and to impart better training to students.

RESOURCE PERSONS

1. Dr. U. V. Wali, CEO, C-QUAD Computers, Belagavi.
2. Mr. Venugopal Kolathur, Chief Architect, Co-Founder, Vavya Labs Pvt. Ltd. Belagavi.
3. Mr. Hemant Mallapur, Cofounder and EVP Engineering, Saankhya Labs, Bangaluru.
4. Prakash G., Lead Application Engineer, Coreel Technologies, Bengaluru.

WHO CAN APPLY?

Faculty members of Constituent & Affiliated Engineering Colleges of VTU/ VTU Regional Centres and Industry Personnel.

REGISTRATION FEES

There is no Registration fee.

Registration Link is:

https://goo.gl/forms/5Fo4UcRH2bsP5ltH3

TOPICS TO BE COVERED

- Verification Guidelines.
- Taking an IC from Idea to market
- Software Aspects of SoC.
- Basics of Verilog and SystemVerilog.
- Brief description on latest Simualtor and synthesis tools.
- Advanced System Verilog Constructs.
- Simulation of Systemverilog Code for basic design using Questasim Simulator.
- Simulator tool flow and Improved designs flow model
- Synthesis & Implementation of SystemVerilog designs in Xilinx Vivado Software
- Introduction of different types of Testbench Architectures
- Code Coverage and Functional coverage reports
- Bus functional Models and Verification IP methods
- Introduction to Universal Verification Methodology(UVM)
- Design & Implementation of AMBA (AHP to APB) Protocol.

VENUE AND IMPORTANT DATES

Center for PG Studies,Visvesvaraya Technological University, “Jnana Sangama”, Belagavi-18

Last date for online registration and hard copy of NoC submission	**12th April 2018**
Confirmation to the participants	**16th April 2018**

SELECTION OF PARTICIPANTS

The batch size of the participants is limited to about 50. Selected candidates will be intimated by e-mail.

ACCOMODATION

Shortlisted/Selected outstation participants will be provided accommodation on sharing basis at VTU Hostels subjected to availability.