SCHEME OF TEACHING AND EXAMINATION FOR
M.TECH. COMPUTER ENGINEERING

I Semester

Elective – I
10SCE151 Advances in Database Management Systems
10SCE152 Computer Graphics & Visualization
10SCE153 Data structures & Algorithms in C++

Note: The Internal Assessment marks of 50 for the core subjects with 2 hours of practical will have 30 marks for theory and 20 marks for practical work

I SEMESTER

Advances in Operating Systems

Subject Code : 10SCE11 IA Marks : 50
No of Lecture Hrs/Week : 4 Exam hours : 3
Total No of Lecture Hours : 52 Exam Marks : 100

1. Introduction, Review
Operating Systems Strategies: User’ perspectives, technologies and examples of Batch Systems, Timesharing Systems, Personal computer systems, Embedded systems, and small communicating computers; The genesis of modern operating systems.

2. Using the Operating Systems
The programmer’s abstract machine; Resources; Processes and threads; Writing concurrent programs.

3. Operating Systems Organization
Basic functions; General implementation considerations; Contemporary OS kernels.

4. Design Strategies
Design considerations; Monolithic kernels; Modular organization; Microkernel; Layered organizations; Operating Systems for distributed system.

5. Real World Examples
Linux, Windows NT/2000/XP: Kernel

6. Distributed Systems: Networking; The Need for a Protocol Architecture; The TCP/IP Sockets; Linux Networking; Client/Server Computing; Distributed Message Passing; Remote Procedure Calls; Clusters; Windows Vista Cluster Server; Linux Clusters; Distributed Process Management; Process Migration; Distributed Global States; Distributed Mutual Exclusion; Distributed Deadlock.

Laboratory Work:
(The following programs can be executed on any available and suitable platform)
1. Design, develop and execute a program using any thread library to create the number of threads specified by the user; each thread independently generates a random integer as an upper limit, and then computes and prints the number of primes less than or equal to that upper limit along with that upper limit.

2. Rewrite above program such that the processes instead of threads are created and the number of child processes created is fixed as two. The program should make use of kernel timer to measure and print the real time, processor time, user space time and kernel space time for each process.

3. Design, develop and implement a process with a producer thread and a consumer thread which make use of a bounded buffer (size can be prefixed at a suitable value) for communication. Use any suitable synchronization construct.

4. Design, develop, and execute a program to solve a system of n linear equations using Successive Over-relaxation method and n processes which use Shared Memory API.

5. Design, develop, and execute a program to demonstrate the use of RPC.

Text Books:


Reference Books:


ADVANCED DIGITAL DESIGN

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<th>Subject Code: 10SCE12</th>
<th>L.A. Marks</th>
<th>50</th>
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<tr>
<td>Hours/Week: 04</td>
<td>Exam Hours: 03</td>
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<tr>
<td>Total Hours: 52</td>
<td>Exam Marks: 100</td>
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1. **Introduction**: Design methodology – An introduction; IC technology options.

2. **Logic Design with Verilog**: Structural models of combinational logic; Logic simulation, Design verification, and Test methodology; Propagation delay; Truth-Table models of Combinational and sequential logic with Verilog

3. **Logic Design with Behavioral Models**: Behavioral modeling; A brief look at data types for behavioral modeling; Boolean-Equation – Based behavioral models of combinational logic; Propagation delay and continuous assignments; Latches and Level – Sensitive circuits in Verilog; Cyclic behavioral models of Flip-Flops and Latches; Cyclic behavior and edge detection; A comparison of styles for behavioral modeling; Behavioral models of multiplexers, encoders, and decoders; Dataflow models of a Linear-Feedback Shift Register; Modeling digital machines with repetitive algorithms; Machines with multi-cycle operations; Design documentation with functions and tasks; Algorithmic state machine charts for behavioral modeling; ASMD charts; Behavioral models of counters, shift registers and register files; Switch debounce, metastability and synchronizers for asynchronous signals; Design example.

4. **Synthesis of Combinational and Sequential Logic**: Introduction to synthesis; Synthesis of combinational logic; Synthesis of sequential logic with latches; Synthesis of three-state devices and bus interfaces; Synthesis of sequential logic with flip-flops; Synthesis of explicit state machines; Registered logic; State encoding; Synthesis of implicit state machines, registers and counters; Resets; Synthesis of gated clocks and clock enables; Anticipating the results of synthesis; Synthesis of loops; Design traps to avoid; Divide and conquer: Partitioning a design.

5. **Programmable Logic and Storage Devices**: Programmable logic devices; Storage devices; PLA; PAL; Programmability of PLDs; CPLDs; FPGAs; Verlog-Based design flows for FPGAs; Synthesis with FPGAs.

**Laboratory Work:**
1. Design, develop, and verify a Verilog module that implements a JK Edge-Triggered Flip-Flop with Active-Low Preset and Clear Inputs.
2. Design, develop, and verify a Verilog module that produces a 4-bit output indicating the number of 1s in an 8-bit input word.
3. Design, develop, and verify a Verilog module that implements a bidirectional ring counter capable of counting in either direction, beginning with first active clock edge after reset.
4. Design, develop, and verify a Verilog module that implements a decade counter.
5. Design, develop, and verify a Verilog module that implements a Universal Shift Register.
6. Design, develop, and verify a Verilog module that implements a Hamming Encoder that produces a 7-bit Hamming code given a 4-bit input word.
7. Design, develop, and verify a Verilog module that implements a modulo-6 counter.
8. Synthesize and verify a cell-based implementation of a ring counter.

TEXT BOOKS:

REFERENCE BOOKS:
2. Relevant Web Sites.

MICROCONTROLLER-BASED SYSTEMS

Subject Code: 10SCE13
Hours/Week: 04
Total Hours: 52

L.A. Marks : 50
Exam Hours: 03
Exam Marks: 100

1. Introduction: Microcontrollers and embedded processors; Overview of the 8051 family.
2. 8051 Assembly Language Programming: Inside the 8051; Introduction to 8051 ALP; Assembling and running an 8051 program; The PC and ROM space in 8051; Data types, directives, flag bits, PSW register, register banks, and the stack, Jump and loop instructions; Call instructions; Time delay for various 8051 family members; I/O programming; I/O bit manipulation programming. Immediate and register addressing modes; Accessing memory using various addressing modes. Bit addresses for I/O and RAM; Extra 128 bytes of on-chip RAM in 8052. Arithmetic instructions; Signed numbers and arithmetic operations; Logic and compare instructions; rotate instruction and serialization; BCD, ASCII, and other application programs.
3. Programming in C: Programming in C: Data types and time delays; I/O programming; Logic operations; Data conversion programs; Accessing code ROM space; Data serialization.
4. Pin Description, Timer Programming: Pin description of 8051; Intel Hex file; Programming the 8051 timers; Counter programming; Programming Timers 0 and 1 in C.
5. Serial Port Programming, Interrupt Programming: Basics of serial communications; 8051 connections to RS232; Serial port programming in assembly and in C. 8051 interrupts; Programming timer interrupts; Programming external hardware interrupts; Programming the serial communications interrupt; Interrupt priority in 8051 / 8052; Interrupt programming in C.
6. Interfacing LCD, Keyboard, ADC, DAC and Sensors: LCE interfacing; Keyboard interfacing; Parallel and serial ADC; DAC interfacing; Sensor interfacing and signal conditioning
7. Interfacing to External Memory, Interfacing with 8255: Memory address decoding; Interfacing 8031 / 8051 with external ROM; 8051 data memory space; Accessing external data memory in C. Interfacing with 8255; Programming 8255 in C.
8. DS12887 RTC Interfacing and Programming, Applications: DS12887 RTC interfacing; DS12887 RTC programming in C; Alarm, SQW, and IRQ features of DS12886. Relays and opto-isolators; Stepper motor interfacing; DC motor interfacing and PWM.

TEXT BOOKS:

REFERENCE BOOKS:

Computer Systems Performance Analysis

Subject Code : 10SCE14  IA Marks : 50
No of Lecture Hrs/Week : 4  Exam hours : 3
Total No of Lecture Hours : 52  Exam Marks : 100


3. Monitors, Program Execution Monitors and Accounting Logs: Monitors: Terminology and classification; Software and hardware monitors, Software versus hardware monitors, Firmware and hybrid monitors, Distributed System Monitors, Program Execution Monitors and Accounting Logs, Program Execution Monitors, Techniques for Improving Program Performance, Accounting Logs, Analysis and Interpretation of Accounting log data, Using accounting logs to answer commonly asked questions.

4. Capacity Planning and Benchmarking: Steps in capacity planning and management; Problems in Capacity Planning; Common Mistakes in Benchmarking; Benchmarking Games; Load Drivers; Remote-Terminal Emulation; Components of an RTE; Limitations of RTEs.


6. Queuing Models: Introduction: Queuing Notation; Rules for all Queues; Little’s Law, Types of Stochastic Process. Analysis of Single Queue: Birth-Death Processes; M/M/1 Queue; M/M/m Queue; M/M/m/B Queue with finite buffers; Results for other M/M/1 Queuing Systems. Queuing Networks: Open and Closed Queuing Networks; Product form networks, queuing Network models of Computer Systems. Operational Laws: Utilization Law; Forced Flow Law; Little’s Law; General Response Time Law; Interactive Response Time Law; Bottleneck Analysis; Mean Value Analysis and Related Techniques; Analysis of Open Queuing Networks; Mean Value Analysis; Approximate MVA; Balanced Job Bounds; Convolution Algorithm, Distribution of Jobs in a System, Convolution Algorithm for Computing G(N), Computing Performance using G(N), Timesharing Systems, Hierarchical Decomposition of Large Queuing Networks; Load Dependent Service Centers, Hierarchical Decomposition, Limitations of Queuing Theory.

Text Book:

Reference Books:

ELECTIVE - I

Advances in Database Management Systems

Subject Code : 10SCE151  IA Marks : 50
No of Lecture Hrs/Week : 4  Exam hours : 3
Total No of Lecture Hours : 52  Exam Marks : 100
1. Review of Relational Data Model and Relational Database Constraints: Relational model concepts; Relational model constraints and relational database schemas; Update operations, transactions and dealing with constraint violations.

2. Object and Object-Relational Databases: Overview of Object-Oriented Concepts – Objects, Encapsulation, Type and class hierarchies, complex objects; Object model of ODMG, Object definition Language ODL; Object Query Language OQL; Overview of C++ language binding; Conceptual design of Object database. Overview of object relational features of SQL; Object-relational features of Oracle; Implementation and related issues for extended type systems; The nested relational model.


4. Parallel and Distributed Databases: Architectures for parallel databases; Parallel query evaluation; Parallelizing individual operations; Parallel query optimizations; Introduction to distributed databases; Distributed DBMS architectures; Storing data in a Distributed DBMS; Distributed catalog management; Distributed Query processing; Updating distributed data; Distributed transactions; Distributed Concurrency control and Recovery.

5. Data Warehousing, Decision Support and Data Mining: Introduction to decision support; OLAP, multidimensional model; Window queries in SQL; Finding answers quickly; Implementation techniques for OLAP; Data Warehousing: Views and Decision support; View materialization; Maintaining materialized views. Introduction to Data Mining; Counting co-occurrences; Mining for rules; Tree-structured rules; Clustering; Similarity search over sequences; Incremental mining and data streams; Additional data mining tasks.

6. More Recent Applications: Mobile databases; Multimedia databases; Geographical Information Systems; Genome data management.

TEXT BOOKS:

REFERENCE BOOKS:

Computer Graphics and Visualization

Subject Code : 10SCE152 IA Marks : 50
No of Lecture Hrs/Week : 4 Exam hours : 3
Total No of Lecture Hours : 52 Exam Marks : 100

1. Introduction: Applications of computer graphics; A graphics system; Images: Physical and synthetic; Imaging systems; The synthetic camera model; The programmer’s interface; Graphics architectures; Programmable pipelines; Performance characteristics. Graphics Programming: The Sierpinski gasket; Programming two-dimensional applications.

2. The OpenGL: The OpenGL API; Primitives and attributes; Color; Viewing; Control functions; The Gasket program; Polygons and recursion; The three-dimensional gasket; Plotting implicit functions.

3. Input and Interaction: Interaction; Input devices; Clients and servers; Display lists; Display lists and modeling; Programming event-driven input; Menus; Picking: A simple CAD program; Building interactive models; Animating interactive programs; Design of interactive programs; Logic operations.

4. Geometric Objects and Transformations: Scalars, points, and vectors; Three-dimensional primitives; Coordinate systems and frames; Modeling a colored cube; Affine transformations; Rotation, translation and scaling. Transformations in homogeneous coordinates; Concatenation of transformations; OpenGL transformation matrices; Interfaces to three-dimensional applications; Quaternions.

5. Viewing: Classical and computer viewing; Viewing with a computer; Positioning of the camera; Simple projections; Projections in OpenGL; Hidden-surface removal; Interactive mesh displays; Parallel-projection matrices; Perspective-projection matrices; Projections and shadows.

6. Lighting and Shading: Light and matter; Light sources: The Phong lighting model; Computation of vectors; Polygonal shading: Approximation of a sphere by recursive subdivisions; Light sources in OpenGL; Specification of materials in OpenGL; Shading of the sphere model; Global illumination.
7. **Curves and surfaces**: Representation of curves and surfaces; Design criteria; Parametric cubic polynomial curves; Interpolation; Hermite curves and surfaces; Bezier curves and surfaces; Cubic B-Splines; General B-Splines; Rendering curves and surfaces; Curves and surfaces in OpenGL.

**Text Book:**

**Reference Books:**
DATA STRUCTURES & ALGORITHMS IN C++

Subject Code: 10SCE153
L.A. Marks : 50

Hours/Week : 04
Exam Hours: 03

Total Hours : 52
Exam Marks: 100

1. Algorithm Analysis: Mathematical Background, Model, What to Analyze, Running Time Calculations.
5. Priority Queues (Heaps): Model, Simple Implementation, Binary Heap, Applications of Priority Queues, Priority Queues in the standard Library.

TEXT BOOKS:

REFERENCE BOOKS: