I – SEMESTER
CMOS VLSI DESIGN

Subject Code : 12EC021     IA Marks : 50
No. of Lecture Hours /week : 04     Exam Hours : 03
Total no. of Lecture Hours : 52     Exam Marks : 100

MOS Transistor Theory: n MOS / p MOS transistor, threshold voltage equation, body effect, MOS device design equation, sub threshold region, Channel length modulation, mobility variation, Tunneling, punch through, hot electron effect MOS models, small signal AC Characteristics, CMOS inverter, βn / βp ratio, noise margin, static load MOS inverters, differential inverter, transmission gate, tristate inverter, BiCMOS inverter. (Ref.1 Chap.2)

CMOS Process Technology: Lambda Based Design rules, scaling factor, semiconductor Technology overview, basic CMOS technology, p well / n well / twin well process. Current CMOS enhancement (oxide isolation, LDD, refractory gate, multilayer inter connect), Circuit elements, resistor, capacitor, interconnects, sheet resistance & standard unit capacitance concepts delay unit time, inverter delays, driving capacitive loads, propagate delays, MOS mask layer, stick diagram, design rules and layout, symbolic diagram, mask feints, scaling of MOS circuits. (Ref.3 Chap.4, 5)


CMOS Analog Design: Introduction, Single Amplifier. Differential Amplifier, Current mirrors, Band gap references, basis of cross operational amplifier. (Ref.5 Chap.3.2, 4.2, 5.1)

Dynamic CMOS and clocking: Introduction, advantages of CMOS over NMOS, CMOS/SOS technology, CMOS/bulk technology, latch up in bulk CMOS., static CMOS design, Domino CMOS structure and design, Charge
sharing, Clocking- clock generation, clock distribution, clocked storage elements. (Ref.2 Chap.7)

Reference Books:


2. Wayne. Wolf, “Modern VLSI design: System on Silicon” Pearson Education”, 2\textsuperscript{nd} Edition


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LABORATORY EXPERIMENTS

CMOS VLSI DESIGN LAB:
(Use any of the EDA Tools)

DIGITAL DESIGN

ASIC-DIGITAL DESIGN FLOW
1. Write Verilog Code for the following circuits and their Test Bench for verification, observe the waveform and synthesize the code with
technological library with given Constraints*. Do the initial timing verification with gate level simulation.

1. An inverter
2. A Buffer
3. Transmission Gate
4. Basic/universal gates
5. Flip flop - RS, D, JK, MS, T
6. Serial & Parallel adder
7. 4-bit counter [Synchronous & Asynchronous counter]
8. Successive approximation register [SAR]

*An appropriate constraint should be given

1. Using SPICE how do you measure the power for a digital circuit.
2. Using a suitable simulator determine the logic propagation delay available in a cycle for a traditional domino pipeline using 500 ps clock cycle. Assume there is zero clock skew.
3. Simulate the worst-case propagation delay of an 8-bit dynamic NOR gate driving a fanout of 4.
4. Simulate a pseudo-nMOS inverter in which the pMOS transistor is half the width of the nMOS transistor. What are the rising, falling and average logical efforts? What is Vol?
5. Simulate a static CMOS circuit to compute \( f = (A+B)(C+D) \) with least delay.
   Each input can present a maximum of 30 lambda of transistor width. The output must drive a load equivalent to 500 lambda of transistor width. Choose transistor size to achieve least delay and estimate the this delay in t.

PART - B
ANALOG DESIGN

Analog Design Flow
1. Design an Inverter with given specifications*, completing the design flow mentioned below:
   a. Draw the schematic and verify the following
      i) DC Analysis
      ii) Transient Analysis
   b. Draw the Layout and verify the DRC, ERC
   c. Check for LVS
   d. Extract RC and back annotate the same and verify the Design
2. Design the following circuits with given specifications*, completing the design flow mentioned below:
   a. Draw the schematic and verify the following
      i) DC Analysis
      ii) AC Analysis
      iii) Transient Analysis
   b. Draw the Layout and verify the DRC, ERC
   c. Check for LVS
   d. Extract RC and back annotate the same and verify the Design.
      i) A Single Stage differential amplifier
      ii) Common source and Common Drain amplifier.

3. Design an op-amp with given specification* using given differential amplifier Common source and Common Drain amplifier in library** and completing the design flow mentioned below:
   a. Draw the schematic and verify the following
      i) DC Analysis
      ii) AC Analysis
      iii) Transient Analysis
   b. Draw the Layout and verify the DRC, ERC
   c. Check for LVS
   d. Extract RC and back annotate the same and verify the Design.

4. Design a 4 bit R-2R based DAC for the given specification and completing the design flow mentioned using given op-amp in the library**.
   a. Draw the schematic and verify the following
      i) DC Analysis
      ii) AC Analysis
      iii) Transient Analysis
   b. Draw the Layout and verify the DRC, ERC
   c. Check for LVS
   d. Extract RC and back annotate the same and verify the Design.

5. For the SAR based ADC mentioned in the figure below draw the mixed signal schematic and verify the functionality by completing ASIC Design FLOW.
   [Specifications to GDS-II]
Appropriate specification should be given.
** Applicable Library should be added & information should be given to the Designer.
*** An appropriate constraint should be given
6. Design a simple 8-bit ADC converter using any one of the tools given above.
7. Design a simple NAND/NOR gate using any one of the tools given above.
*(Any other experiments may be added in supportive of the course)*

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**SoC Design**

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Goal of the course – Today, VLSI chips are entire “system-on-chip” designs, which include processors, memories, peripheral controllers, and connectivity sub-systems. The course aims to provide an appreciation for the motivation behind SoC design, the challenges of SoC design, and the overall SoC design flow.

**Motivation for SoC Design** - Review of Moore’s law and CMOS Scaling, benefits of system-on-chip integration in terms of cost, power, and performance. Comparison on System-on-Board, System-on-Chip, and System-in-Package. Typical goals in SoC design – cost reduction, power
reduction, design effort reduction, performance maximization. (Ref.2 Chap.2, Ref .6 Chap-3.5, publication-3,5)

**System On Chip Design Process:** A canonical SoC Design, SoC Design flow waterfall vs spiral, top down vs Bottom up. Specification requirement, Types of Specification , System Design process, System level design issues, Soft IP Vs Hard IP, IP verification and integration, hardware-software codesign, Design for timing closure, Logic design issues Verification strategy, On chip buses and interfaces, Low Power, Hardware Accelerators in an SOC. (Ref -4, chap-2,3 Publication-1,5)

**Embedded Memories**—cache memories, flash memories, embedded DRAM. Topics related to cache memories. Cache coherence. MESI protocol and Directory-based coherence. (Ref -3, chap: 10.5, Ref -6, chap 10)


**MPSoCs:** What,Why,How MPSoCs. Techniques for designing MPSoCs, Performance and flexibility for MPSoCs design, (Ref -5, Chap-1, 2, 5, Publication-4)

Case study: A Low Power Open Multimedia Application Platform for 3G Wireless (Publication-6)

Reference Books:


ADVANCED EMBEDDED SYSTEMS

Subject Code : 12EC118  IA Marks : 50
No. of Lecture Hours /week : 04  Exam Hours : 03
Total no. of Lecture Hours : 52  Exam Marks : 100


Characteristics and Quality Attributes of Embedded Systems:


Embedded Firmware Design and Development: Embedded Firmware Design Approaches, Embedded Firmware Development Languages
Real-Time Operating System (RTOS) based Embedded System Design: Operating System Basics, Types of OS, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling, Threads, Processes and Scheduling: Putting them altogether, Task Communication, Task Synchronization, Device Drivers, How to Choose an RTOS
The Embedded System Development Environment: The Integrated Development Environment (IDE), Types of Files Generated on Cross-compilation, Disassembler/Decompiler, Simulators, Emulators and Debugging, Target Hardware Debugging, Boundary Scan.

**REFERENCE BOOKS:**


Lab Experiments:

I. Advanced Embedded Systems

1. Use any EDA (Electronic Design Automation) tool to learn the Embedded Hardware Design and for PCB design.
2. Familiarize the different entities for the circuit diagram design.
3. Familiarize with the layout design tool, building blocks, component placement, routings, design rule checking etc.

II. Embedded Programming Concepts (RTOS)

1. Create ‘n’ number of child threads. Each thread prints the message “ I’m in thread number …” and sleeps for 50 ms and then quits. The main thread waits for complete execution of all the child threads and then quits. Compile and execute in Linux.
2. Implement the multithread application satisfying the following:
   i. Two child threads are created with normal priority.
   ii. Thread 1 receives and prints its priority and sleeps for 50ms and then quits.
   iii. Thread 2 prints the priority of the thread 1 and rises its priority to above normal and retrieves the new priority of thread 1, prints it and then quits.
   iv. The main thread waits for the child thread to complete its job and quits.
3. Implement the usage of anonymous pipe with 512 bytes for data sharing between parent and child processes using handle inheritance mechanism.
4. Test the program below using multithread application-
i. The main thread creates a child thread with default stack size and name ‘Child_Thread’.
ii. The main thread sends user defined messages and the message ‘WM_QUIT’ randomly to the child thread.
iii. The child thread processes the message posted by the main thread and quits when it receives the ‘WM_QUIT’ message.
iv. The main thread checks the termination of the child thread and quits when the child thread complete its execution.
v. The main thread continues sending the random messages to the child thread till the ‘WM_QUIT’ message is sent to child thread.
vi. The messaging mechanism between the main thread and child thread is synchronous.

5. Test the program application for creating an anonymous pipe with 512 bytes of size and pass the ‘Read Handle’ of the pipe to a second process using memory mapped object. The first process writes a message ‘Hi from Pipe Server’. The 2nd process reads the data written by the pipe server to the pipe and displays it on the console. Use event object for indicating the availability of data on the pipe and mutex objects for synchronizing the access in the pipe.

6. Create a POSIX based message queue for communicating between two tasks as per the requirements given below:-
   i. Use a named message queue with name ‘MyQueue’.
   ii. Create two tasks(Task1 & Task2) with stack size 4000 & priorities 99 & 100 respectively.
   iii. Task 1 creates the specified message queue as Read Write and reads the message present, if any, from the message queue and prints it on the console.
   iv. Task2 open the message queue and posts the message ‘Hi from Task2’.
Handle all possible error scenarios appropriately.

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VLSI Design Verification

Subject Code : 12EC130  IA Marks : 50
No. of Lecture Hours /week : 04  Exam Hours : 03
Total no. of Lecture Hours : 52  Exam Marks : 100

Note: Today, the complexity of the VLSI integrated circuits that are being designed is so large that pre-silicon verification presents a major challenge to the design team. The fact that IP from multiple sources are integrated today to create a system-on-chip design further complicates the matter. Simulation
based verification techniques that were developed in the past are considered inadequate to-day, since they require too many test cases and require too much development time and run-time. Raising the level of abstraction to design can help bring down the simulation cost. Formal specification and verification techniques are another way to address the challenge of design verification.

**Importance of Design Verification:** What is verification? What is a testbench? The importance of verification, Reconvergence model, Formal verification, Equivalence checking, Model checking, Functional verification. Functional verification approaches: Black box verification, white box verification, grey box verification. Testing versus verification: scan based testing, design for verification. Verification reuse. The cost of verification. [Ref1- Chapter1]


**The verification plan:** The role of verification plan: specifying the verification plan, defining the first success. Levels of verification: unit level verification, reusable components verification, ASIC and FPGA verification, system level verification, board level verification, verifying strategies, verifying responses. From specification to features: component level feature, system level features, Error types to look for?, prioritise, design for verification. Directed testbench approaches group into testcases, from testcases to testbenches, measuring progress. Coverage driven random based approach: Measuring progress, From features to functional coverage, from features to testbench, From features to generators, directed testcases. [Ref1-Chapter3]
**Static Timing Verification.** Concept of static timing analysis. Cross talk and noise. Limitations of STA, slew of a waveform, skew between the signals, timing arcs and unateness, Min and Max timing paths, clock domains, operating conditions, critical path analysis, false paths, timing models. [Ref2 Chapter 1, 2, 3, 8]

**Physical Design Verification.** Layout rule checks and electrical rule checks. Parasitic extraction. Antenna [Ref4 Chapter 8]

**Crosstalk and Noise:** Cross talk glitch analysis, crosstalk delay analysis, timing verification [Ref4 Chapter 8]

**IP-Reuse in modern-day SoC.** SoC Integration and the problem of verification of IP-based designs. Verification IP and their importance. (Ref. 5)

**Formal Verification:** SAT BDDs, Symbolic Model Checking with BDDs, Model Checking using SAT, Equivalence Checking. [Ref3 Chapter 1, 2]

**REFERENCE BOOKS:**


3. S.Minato “ Binary decision diagram and applications for VLSI CAD”, Kulwer Academic pub November 1996


5. [http://www.cse.psu.edu/~vijay/verify/instructors.html](http://www.cse.psu.edu/~vijay/verify/instructors.html)
Introduction and Methodology:
Digital Systems and Embedded Systems, Binary representation and Circuit Elements, Real-World Circuits, Models, Design Methodology.

Combinational Basics:
Boolean Functions and Boolean Algebra, Binary Coding, Combinational Components and Circuits, Verification of Combinational Circuits.

Number Basics:
Unsigned and Signed Integers, Fixed and Floating-point Numbers.

Sequential Basics:
Storage elements, Counters, Sequential Datapaths and Control, Clocked Synchronous Timing Methodology.

Memories:
Concepts, Memory Types, Error Detection and Correction. Implementation Fabrics: ICs, PLDs, Packaging and Circuit Boards, Interconnection and Signal Integrity.

Processor Basics:
Embedded Computer Organization, Instruction and Data, Interfacing with memory.

I/O interfacing:
I/O devices, I/O controllers, Parallel Buses, Serial Transmission, I/O software.

Accelerators:
Concepts, case study, Verification of accelerators.

Design Methodology:
Design flow, Design optimization, Design for test,

Reference Books:
Introduction: Overview of nanoscience and engineering, Development milestones in microfabrication and electronic industry, Moore's law and continued miniaturization, Classification of Nano structures, Electronic properties of atoms and solids: isolated atom, Bonding between atoms, Giant molecular solids, Free electron models and energy bands, crystalline solids, Periodicity of crystal lattices, Electronic conduction, effects of nanometer length scale, Fabrication methods: Top down processes, Bottom up processes methods for templating the growth of nanomaterials, ordering of nanosystems.

Characterization: Classification, Microscopic techniques, Field ion microscopy, scanning probe techniques, diffraction techniques: bulk, surface, spectroscopy techniques: photon, radiofrequency, electron, surface analysis and dept profiling: electron, mass, Ion beam, Reflectometry, Techniques for property measurement: mechanical, electron, magnetic, thermal properties.


Fabrication techniques: requirements of ideal semiconductor, epitaxial growth of quantum wells, lithography and etching, cleaved edge overgrowth, growth of vicinal substrates, strain induced dots and wires, electrostatically induced dots and wires, Quantum well width fluctuations, thermally annealed quantum wells, semiconductor nanocrystals, colloidal quantum dots, self-assembly techniques.

Physical processes: modulation doping, quantum hall effect, resonant tunneling, charging effects, ballistic carrier transport, Inter band absorption, intraband absorption, Light emission processes, phonon bottleneck, quantum
confined stark effect, nonlinear effects, coherence and dephasing, characterization of semiconductor nanostructures: optical electrical and structural.

Methods of measuring properties: structure:

Applications: Injection lasers, quantum cascade lasers, single photon sources, biological tagging, optical memories, coulomb blockade devices, photonic structures, QWIP’s, NEMS, MEMS.

References:

ASIC DESIGN

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Note: All Designs Will Be Based On VHDL
**Introduction:** Full Custom with ASIC, Semi custom ASICs, Standard Cell based ASIC, Gate array based ASIC, Channeled gate array, Channel less gate array, structured get array, Programmable logic device, FPGA design flow, ASIC cell libraries

**Data Logic Cells:** Data Path Elements, Adders, Multiplier, Arithmetic Operator, I/O cell, Cell Compilers

**ASIC Library Design:** Logical effort: practicing delay, logical area and logical efficiency logical paths, multi stage cells, optimum delay, optimum no. of stages, library cell design.

**Low-Level Design Entry:** Schematic Entry: Hierarchical design. The cell library, Names, Schematic, Icons & Symbols, Nets, schematic entry for ASIC’S, connections, vectored instances and buses, Edit in place attributes, Netlist, screener, Back annotation

**Programmable ASIC:** programmable ASIC logic cell, ASIC I/O cell

**A Brief Introduction to Low Level Design Language:** an introduction to EDIF, PLA Tools, an introduction to CFI designs representation. Half gate ASIC. Introduction to Synthesis and Simulation;

**ASIC Construction Floor Planning and Placement And Routing:** Physical Design, CAD Tools, System Partitioning, Estimating ASIC size, partitioning methods. Floor planning tools, I/O and power planning, clock planning, placement algorithms, iterative placement improvement, Time driven placement methods. Physical Design flow global Routing, Local Routing, Detail Routing, Special Routing, Circuit Extraction and DRC.

**REFERENCE BOOKS:**

II – SEMESTER

DESIGN OF ANALOG & MIXED MODE VLSI CIRCUITS

Subject Code : 12EC025  IA Marks : 50
No. of Lecture Hours /week : 04  Exam Hours : 03
Total no. of Lecture Hours : 52  Exam Marks : 100

MOSFET Modelling for Basic Analog Design: Derivation of MOS I/V Characteristics ($I_D$, $R_{ON}$, $g_m$), second order effects, MOS device Models.
[Ref 1. Chapter 2]

Single stage Amplifier: CS stage with resistive load, diode connected load, current source load, triode load, CS stage with source degeneration, Source follower, Common-gate stage, Cascode stage, Folded Cascode, Choice of device models. [Ref 1. Chapter 3]

Frequency Response of CS Stage: General considerations: Miller effect, Association of poles with nodes, Frequency response of Common Source Stage. [Ref 1. Chapter 6]

Differential Amplifiers & Current Mirrors: Basic differential Pair, Common mode response, Differential pair with MOS loads, Gilbert cell. Basic current mirrors, Cascode Current mirrors, Active current mirrors. [Ref 1. Chapter 4, 5]


Oscillators & Phase Locked Loop: Ring Oscillators, LC Oscillators, VCO, Mathematical Model of VCO. Simple PLL, Charge pump PLL, Non-ideal effects in PLL, Delay locked loops and applications. [Ref 1. Chapter 14, 15]
**Bandgap Reference & Switched Capacitor Circuits:** General Considerations, Supply Independent biasing, Temperature independent biasing, PTAT Current Generation, Constant Gm biasing. Sampling Switches, Switched Capacitor Amplifiers. [Ref 1. Chapter 11, 12]

**Data Converter Architectures:** DAC & ADC Specifications, (Qualitative Analysis of )Resistor String DAC, R-2R Ladder Networks, Current Steering DAC, Charge Scaling DAC, Cyclic DAC, Pipeline DAC, Flash ADC, Pipeline ADC, Integrating ADC, Successive Approximation ADC. [Ref 2. Chapter 28,29]

**REFERENCE BOOK:**


**LABORATORY EXPERIMENTS:**

ALL EXPERIMENTS MUST BE IMPLEMENTED USING VLSI TOOLS LIKE CADANCE/SYNOPSIS/MENTAGRAPHICS.

1. Design the MOS transistor circuits for DC & AC small signal parameters, completing the design flow mentioned below:
   a. Draw the schematic and verify the following
      i) DC Analysis
      ii) AC Analysis
      iii) Transient Analysis
   b. Draw the Layout and verify the DRC, ERC
   c. Check for LVS.

2. Design a **TWO** stage **op-amp** with given specification* using given differential amplifier Common source and Common Drain amplifier in library* and completing the design flow mentioned below:
   a. Draw the schematic and verify the following
i) DC Analysis
ii) AC Analysis
iii) Transient Analysis
b. Draw the layout and verify the DRC, ERC
c. Check for frequency response, slew rate, offset effects and Noise.
3. Design a simple sample and hold circuit and measure the switching times.
4. Design a PLL and measure all the parameters.
5. Design a simple ADC/DAC and measure the data conversion time.
   Assume the 95 nanometer technology.
6. Design 3-8 decoder using MOS technology.
ANY EXPERIMETNS CAN BE ADDED TO SUPPLEMENT THE THEORY. ABOVE IS THE ONLY GUIDE LINES.

REAL TIME OPERATING SYSTEMS

Subject Code : 12EC126  IA Marks : 50
No. of Lecture Hours /week : 04  Exam Hours : 03
Total no. of Lecture Hours : 52  Exam Marks : 100


Processing: Preemptive Fixed-Priority Policy, Feasibility, Rate Monotonic least upper bound, Necessary and Sufficient feasibility, Deadline – Monotonic Policy, Dynamic priority policies.

Memory: Physical hierarchy, Capacity and allocation, Shared Memory, ECC Memory, Flash file systems.
Multi-resource Services:
Blocking, Deadlock and livestock, Critical sections to protect shared
resources, priority inversion.

Soft Real-Time Services:
Missed Deadlines, QoS, Alternatives to rate monotonic policy, Mixed hard
and soft real-time services.

Embedded System Components:
Firmware components, RTOS system software mechanisms, Software
application components.

Debugging Components:
Exceptions assert, Checking return codes, Single-step debugging, kernel
scheduler traces, Test access ports, Trace ports, Power-On self test and
diagnostics, External test equipment, Application-level debugging.

Performance Tuning:
Basic concepts of drill-down tuning, hardware – supported profiling and
tracing, Building performance monitoring into software, Path length,
Efficiency, and Call frequency, Fundamental optimizations.

High availability and Reliability Design:
Reliability and Availability, Similarities and differences, Reliability, Reliable
software, Available software, Design trade offs, Hierarchical applications for
Fail-safe design.

Design of RTOS – PIC microcontroller. (Chap 13 of book Myke Predko)

Reference Books:
1. “Real-Time Embedded Systems and Components”, Sam Siewert,
2. “Programming and Customizing the PIC microcontroller”, Myke
3. “Programming for Embedded Systems”, Dreamtech Software Team,

Real Time Operating Systems:
Laboratory Experiments -
USE LINUX/SOLARIS/QNX OS ONLY.

1. Implement simple IPC protocol.
2. Implement Semaphore and Mutex for any given applications.
3. Communicate between 2 PCs using Socket programming or message passing techniques (i.e., MPI).
4. Create ‘n’ number of child threads. Each thread prints the message “I’m in thread number …” and sleeps for 50 ms and then quits. The main thread waits for complete execution of all the child threads and then quits. Compile and execute in Linux.

5. Implement the multithread application satisfying the following:
   i. Four child threads are created with normal priority.
   ii. Thread 1& 2 receives and prints its priority and sleeps for 50ms and then quits.
   iii. Thread 3&4 prints the priority of the thread 1 &2 and rises its priority to above normal and retrieves the new priority of thread 1, prints it and then quits.
   iv. The main thread waits for the child thread to complete its job and quits.
6. Implement the usage of send and receive primitives with 512 bytes for data sharing between parent and child processes using handle inheritance mechanism.

7. Test the program below using multithread application:
   1. The main thread creates a child thread with default stack size and name ‘Child_Thread’.
   2. The main thread sends user defined messages and the message ‘WM_QUIT’ randomly to the child thread.
   3. The child thread processes the message posted by the main thread and quits when it receives the ‘WM_QUIT’ message.
   4. The main thread checks the termination of the child thread and quits when the child thread complete its execution.
   5. The main thread continues sending the random messages to the child thread till the ‘WM_QUIT’ message is sent to child thread.
   6. The messaging mechanism between the main thread and child thread is synchronous.

8. Test the program application for creating an anonymous pipe with 512 bytes of size and pass the ‘Read Handle’ of the pipe to a second process using memory mapped object. The first process writes a message ‘Hi from Pipe'
Server'. The 2nd process reads the data written by the pipe server to the pipe and displays it on the console. Use event object for indicating the availability of data on the pipe and mutex objects for synchronizing the access in the pipe. For synchronization semaphore/mutex can be used.

9. Create a POSIX based message queue for communicating between several tasks as per the requirements given below:
   i. Use a named message queue with name 'MyQueue'.
   ii. Create N tasks with stack size 4000 & priorities (n-1) & n respectively. N can be any number but more than 4.
   iii. Tasks creates the specified message queue as Read Write and reads the message present, if any, from the message queue and prints it on the console.
   iv. Tasks open the message queue and posts the message 'Hi from Task(n-1)'.
   v. Handle all possible error scenarios appropriately.

MINI PROJECTS: (optional)
1. Implement protocol converter (refer book 3 given in the RTOS theory)
2. Implement System Calls for the RTOS using RTLinux.
3. Implement an IP phone.
4. Implement Device Driver.

ANY EXPERIMENTS CAN BE ADDED TO SUPPLEMENT THE THEORY. ABOVE IS THE ONLY GUIDE LINES.

ADVANCED MICROCONTROLLEERS

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Note: Microcontrollers have become prevalent in a number of applications such as instrumentation, industrial electronics, automotive electronics, robotics, etc. Advances in VLSI technology permit the integration of not only the processor but also the analog electronics, memory and peripherals necessary for system implementation; this allows low-cost system implementation. Some microcontrollers used in industrial electronics also
provide some digital signal processing capability to further reduce the system cost.
Power dissipation is often a consideration in many systems and modern microcontrollers address it through the support of several low-power modes of operation. The aim of the course is to introduce advanced microcontrollers (16-bit and 32-bit).

**Motivation for advanced microcontrollers** – Low Power embedded systems, On-chip peripherals, low-power RF capabilities. Examples of applications.

**MSP430 – 16-bit Microcontroller family**. CPU architecture, Instruction set, Interrupt mechanism, Clock system, Memory subsystem, bus –architecture. The assembly language and ‘C’ programming for MSP-430 microcontrollers. On-chip peripherals, WDT, Comparator, Op-Amp, Timer, Basic Timer, Real Time Clock (RTC), ADC, DAC, Digital I/O. Using the low-power features of MSP430. Clock system, low-power modes, Clock request feature, Low-power programming and interrupts.


**Applications** – Wireless Sensor Networking with MSP430 and Low-Power RF circuits; Pulse Width Modulation(PWM) in Power Supplies.

**References Books:**

4. *Sample Programs for MSP430* downloadable from msp430.com
LOW POWER VLSI DESIGN

Subject Code : 12EC047  IA Marks : 50
No. of Lecture Hours /week : 04  Exam Hours : 03
Total no. of Lecture Hours : 52  Exam Marks : 100

Introduction : Need for low power VLSI chips, Sources of power dissipation on Digital Integrated circuits. Emerging Low power approaches, Physics of power dissipation in CMOS devices.

Device & Technology Impact on Low Power: Dynamic dissipation in CMOS, Transistor sizing & gate oxide thickness, Impact of technology Scaling, Technology & Device innovation

Power estimation, Simulation Power analysis: SPICE circuit simulators, gate level logic simulation, capacitive power estimation, static state power, gate level capacitance estimation, architecture level analysis, data correlation analysis in DSP systems, Monte Carlo simulation.

Probabilistic power analysis: Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy.

Low Power Design Circuit level: Power consumption in circuits. Flip Flops & Latches design, high capacitance nodes, low power digital cells library

Logic level: Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic

Low power Architecture & Systems: Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power arithmetic components, low power memory design.

Low power Clock Distribution: Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip & package co design of clock network

REFERENCE BOOKS:


ELECTIVE –II

DESIGN OF VLSI SYSTEMS

Subject Code : 12EC027  IA Marks : 50
No. of Lecture Hours /week : 04  Exam Hours : 03
Total no. of Lecture Hours : 52  Exam Marks : 100


Chip Design Methods: Behavioral synthesis, RTL synthesis, Logic optimization and structural tools layout synthesis, layout synthesis, EDA Tools for System


Data Path Sub System Design: Introduction, Addition, Subtraction, Comparators, Counters, Boolean logical operations, coding, shifters, Multiplication, Parallel Prefix computations

Array Subsystem Design: SRAM, Special purpose RAMs, DRAM, Read only memory, Content Addressable memory, Programmable logic arrays.

Control Unit Design: Finite State Machine (FSM) Design, Control Logic Implementation: PLA control implementation, ROM control implementation.
Special Purpose Subsystems: Packaging, power distribution, I/O, Clock, Transconductance amplifier, follower integrated circuits, etc

Design Economics: Nonrecurring and recurring engineering Costs, Fixed Costs, Schedule, Person power, example


VLSI Applications: Case Study: RISC microcontroller, ATM Switch, etc.

REFERENCE BOOKS:


VLSI Design Automation

Subject Code : 12EC010 IA Marks : 50
No. of Lecture Hours /week : 04 Exam Hours : 03
Total no. of Lecture Hours : 52 Exam Marks : 100

Logic Synthesis & Verification: Introduction to combinational logic synthesis, Binary Decision Diagram, Hardware models for High-level synthesis.

VLSI Automation Algorithms:
Partitioning: problem formulation, classification of partitioning algorithms, Group migration algorithms, simulated annealing & evolution, other partitioning algorithms

25
Placement, Floor Planning & Pin Assignment: problem formulation, simulation base placement algorithms, other placement algorithms, constraint based floor planning, floor planning algorithms for mixed block & cell design. General & channel pin assignment

Global Routing: Problem formulation, classification of global routing algorithms, Maze routing algorithm, line probe algorithm, Steiner Tree based algorithms, ILP based approaches

Detailed Routing: problem formulation, classification of routing algorithms, single layer routing algorithms, two layer channel routing algorithms, three layer channel routing algorithms, and switchbox routing algorithms

Over The Cell Routing & Via Minimization: two layers over the cell routers, constrained & unconstrained via minimization

Compaction: problem formulation, one-dimensional compaction, two dimension based compaction, hierarchical compaction

REFERENCE BOOKS:


MODERN DSP

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Goal of the course – Advances in Digital Signal Processing involve variable sampling rates and thus the multirate signal processing and hence their
applications in communication systems and signal processing. It is intended to introduce a basic course in multirate signal processing especially meant for students of branches eligible for M Tech courses in EC related disciplines.

**Introduction and Discrete Fourier Transforms:** Signals, Systems and Processing. Classification of Signals, The Concept of Frequency in Continuous-Time and Discrete-Time Signals, Analog-to-Digital and Digital-to-Analog Conversion, Frequency-Domain Sampling: The Discrete Fourier Transform, Properties of the DFT, Linear Filtering Methods Based on the DFT (Ref.1 Chap. 1 & 7)

**Design of Digital Filters:** General Considerations, Design of FIR Filters, Design of IIR Filters from Analog Filters, Frequency Transformations. (Ref.1 Chap.10)

**Multirate Digital Signal Processing:** Introduction, Decimation by a factor ‘D’, Interpolation by a factor ‘I’, Sampling rate Conversion by a factor ‘I/D’, implementation of Sampling rate conversion, Multistage implementation of Sampling rate conversion, Sampling rate conversion of Band Pass Signals, Sampling rate conversion by an arbitrary factor, Applications of Multirate Signal Processing, Digital Filter banks, Two Channel Quadrature Mirror Filter banks, M-Channel QMF bank. (Ref.1 Chap.11)

**Adaptive Filters:** Applications of Adaptive Filters, Adaptive Direct Form FIR Filters- The LMS Algorithm, Adaptive Direct Form Filters-RLS Algorithm. (Ref.1 Chap.13)

**References:**

III – SEMESTER
CMOS RF CIRCUIT DESIGN

Subject Code : 12EC020  IA Marks : 50
No. of Lecture Hours /week : 04  Exam Hours : 03
Total no. of Lecture Hours : 52  Exam Marks : 100


RF Modulation: Analog and digital modulation of RF circuits, Comparison of various techniques for power efficiency, Coherent and non-coherent detection, Mobile RF communication and basics of Multiple Access techniques. Receiver and Transmitter architectures, Direct conversion and two-step transmitters. RF Testing: RF testing for heterodyne, Homodyne, Image reject, Direct IF and sub sampled receivers.

BJT and MOSFET Behavior at RF Frequencies: BJT and MOSFET behavior at RF frequencies, modeling of the transistors and SPICE model, Noise performance and limitations of devices, integrated parasitic elements at high frequencies and their monolithic implementation.

Circuits Design: Overview of RF Filter design, Active RF components & modeling, Matching and Biasing Networks. Basic blocks in RF systems and their VLSI implementation, Low noise Amplifier design in various technologies, Design of Mixers at GHz frequency range, Various mixers-working and implementation. Oscillators- Basic topologies VCO and definition of phase noise, Noise power and trade off. Resonator VCO designs, Quadrature and single sideband generators. Radio frequency Synthesizers- PLLS, Various RF synthesizer architectures and frequency dividers, Power Amplifier design, Liberalization techniques, Design issues in integrated RF filters.
REFERENCE BOOKS:


ELECTIVE - III

SYNTHESIS AND OPTIMIZATION OF DIGITAL CIRCUITS

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Introduction: Microelectronics, semiconductor technologies and circuit taxonomy, Microelectronic design styles, computer aided synthesis and optimization.

Graphs: Notation, undirected graphs, directed graphs, combinatorial optimization, Algorithms, tractable and intractable problems, algorithms for linear and integer programs, graph optimization problems and algorithms, Boolean algebra and Applications.

Hardware Modeling: Hardware Modeling Languages, distinctive features, structural hardware language, Behavioral hardware language, HDLs used in synthesis, abstract models, structures logic networks, state diagrams, data flow and sequencing graphs, compilation and optimization techniques.

Two Level Combinational Logic Optimization: Logic optimization, principles, operation on two level logic covers, algorithms for logic minimization, symbolic minimization and encoding property, minimization of Boolean relations.
Multiple Level Combinational Optimizations: Models and transformations for combinational networks, algebraic model, Synthesis of testable network, algorithm for delay evaluation and optimization, rule based system for logic optimization.

Sequential Circuit Optimization: Sequential circuit optimization using state based models, sequential circuit optimization using network models.

Schedule Algorithms: A model for scheduling problems, Scheduling with resource and without resource constraints, Scheduling algorithms for extended sequencing models, Scheduling Pipe lined circuits.

Cell Library Binding: Problem formulation and analysis, algorithms for library binding, specific problems and algorithms for library binding (lookup table F.P.G.As and Antifuse based F.P.G.As), rule based library binding.


REFERENCE BOOKS:


IMAGE AND VIDEO PROCESSING

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Introduction: 2D systems, Mathematical preliminaries – Fourier Transform, Z Transform, Optical & Modulation transfer function, Matrix theory,
Random signals, Discrete Random fields, Spectral density function. (Ref.1, Chap.2)

**Image Perception:** Light, Luminance, Brightness, Contrast, MTF of the visual system, Visibility function, Monochrome vision models, Fidelity criteria, Color representation, Chromaticity diagram, Color coordinate systems, Color difference measures, Color vision model, Temporal properties of vision. (Ref.1, Chap.3)

**Image Sampling and Quantization:** Introduction, 2D sampling theory, Limitations in sampling & reconstruction, Quantization, Optimal quantizer, Compander, Visual quantization. (Ref.1, Chap.4)

**Image Transforms:** Introduction, 2D orthogonal & unitary transforms, Properties of unitary transforms, DFT, DCT, DST, Hadamard, Haar, Slant, KLT, SVD transform. (Ref.1, Chap.5)

**Image Representation by Stochastic Models:** Introduction, one-dimensional Causal models, AR models, Non-causal representations, linear prediction in two dimensions. (Ref.1, Chap.6)

**Image Enhancement:** Point operations, Histogram modeling, spatial operations, Transform operations, Multi-spectral image enhancement, false color and Pseudo-color, Color Image enhancement. (Ref.1, Chap.7)

**Image Filtering & Restoration:** Image observation models, Inverse & Wiener filtering, Fourier Domain filters, Smoothing splines and interpolation, Least squares filters, generalized inverse, SVD and Iterative methods, Maximum entropy restoration, Bayesian methods, Coordinate transformation & geometric correction, Blind de-convolution. (Ref.1, Chap.8)

**Image Analysis & Computer Vision:** Spatial feature extraction, Transform features, Edge detection, Boundary Extraction, Boundary representation, Region representation, Moment representation, Structure, Shape features, Texture, Scene matching & detection, Image segmentation, Classification Techniques. (Ref.1, Chap.9)

**Image Reconstruction from Projections:** Introduction, Radon Transform, Back projection operator, Projection theorem, Inverse Radon transform, Fourier reconstruction, Fan beam reconstruction, 3D tomography. (Ref.1, Chap.10)

**Image Data Compression:** Introduction, Pixel coding, Predictive techniques, Transform coding, Inter-frame coding, coding of two tone images, Image compression standards. (Ref.1, Chap.11)

**Video Processing:** Fundamental Concepts in Video – Types of video signals, Analog video, Digital video, Color models in video, Video Compression Techniques – Motion compensation, Search for motion vectors, H.261,
H.263, MPEG 1, MPEG 2, MPEG 4, MPEG 7 and beyond, Content based video indexing. (Ref.4)

Reference Books:

AUTOMOTIVE ELECTRONICS

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Actuators – Fuel Metering Actuator, Fuel Injector, Ignition Actuator

Electronic Engine Control – Engine parameters, variables, Engine Performance terms, Electronic Fuel Control System, Electronic Ignition control, Idle speed control, EGR Control


Vehicle Motion Control – Cruise Control, Chassis, Power Brakes, Anti-lock Brake System (ABS), Electronic Steering Control, Power Steering, Traction Control, Electronically controlled suspension

Automotive Instrumentation – Sampling, Measurement & Signal Conversion of various parameters.


Future Automotive Electronic Systems – Alternative Fuel Engines, Collision Avoidance Radar warning Systems, Low tire pressure warning system, Radio navigation, Advance Driver Information System

Reference Books: -


ELECTIVE-IV

RF AND MICROWAVE CIRCUIT DESIGN

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Wave Propagation in N/W:

Introduction, reasons for using RF/Micro waves, applications, RF waves, RF and Microwave circuit design, introduction to component basics, analysis of
simple circuit phasor domain, RF impedance matching, properties of waves, transmission media, micro strip lines, high frequency parameters, formulation of S-parameters, properties, transmission matrix, generalized S-parameters.

**Passive Circuit design:**
Introduction, Smith chart, scales, applications of Smith chart, design of matching N/Ws, definition of impedance matching, matching using lumped and distributed elements.

**Basic consideration in active N/Ws and design of amplifiers, oscillators, and detectors:**
Stability considerations, gain considerations, noise considerations. Linear and non linear design, introduction, types of amplifiers, design of different types of amplifiers, multi stage small signal amplifiers, design of transistor oscillators, detector losses, detector design.

**Mixers, phase shifters and RF and Microwave IC design:**
Mixer types, conversion loss for SSB mixers, one diode mixer, phase shifters, digital phase shifters, semiconductor phase shifters, RF and microwave IC design, MICs, MIC materials, types of MICs, hybrid vs monolithic ICs, chip materials.

**Text Book:**

**Ref Book:**

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**ADVANCES IN VLSI DESIGN**

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**Review of MOS Circuits:** MOS and CMOS static plots, switches, comparison between CMOS and B1 - CMOS.
MESFETS: MESFET and MODFET operations, quantitative description of MESFETS.

MIS Structures and MOSFETS: MIS systems in equilibrium, under bias, small signal operation of MESFETS and MOSFETS.

Short Channel Effects and Challenges to CMOS: Short channel effects, scaling theory, processing challenges to further CMOS miniaturization

Beyond CMOS: Evolutionary advances beyond CMOS, carbon Nano tubes, conventional vs. tactile computing, computing, molecular and biological computing Mole electronics-molecular Diode and diode- diode logic .Defect tolerant computing,

Super Buffers, Bi-CMOS and Steering Logic: Introduction, RC delay lines, super buffers- An NMOS super buffer, tri state super buffer and pad drivers, CMOS super buffers, Dynamic ratio less inverters, large capacitive loads, pass logic, designing of transistor logic, General functional blocks - NMOS and CMOS functional blocks.


System Design: CMOS design methods, structured design methods, Strategies encompassing hierarchy, regularity, modularity & locality, CMOS Chip design Options, programmable logic, Programmable inter connect, programmable structure, Gate arrays standard cell approach, Full custom Design.

Reference Books:

RF MEMS

Review – Introduction to MEMS. Fabrication for MEMS, MEMS transducers and Actuators. Microsensing for MEMS, Materials for MEMS. (Ref.1, Chap.1)

MEMS materials and fabrication techniques – Metals, Semiconductors, thin films, Materials for Polymer MEMS, Bulk Machining for silicon based MEMS, Surface machining for silicon based MEMS, Micro Stereo Lithography for Polymer MEMS. (Ref.1, Chap.2)

RF MEMS Switches and micro – relays. Switch Parameters, Basics of Switching, Switches for RF and microwave Applications, Actuation mechanisms, micro relays and micro actuators, Dynamics of Switch operation, MEMS Switch Design and design considerations. MEMS Inductors and capacitors. (Ref.1, Chap.3 & 4)

Micromachined RF Filters and Phase shifters. RF Filters, Modeling of Mechanical Filters, Micromachanical Filters, SAW filters – Basics, Design considerations. Bulk Acoustic Wave Filters, Micromachined Filters for Millimeter Wave frequencies. Micromachined Phase Shifters, Types and Limitations, MEMS and Ferroelectric Phase shifters, Applications. (Ref.1, Chap.5 & 6)

Micromachined transmission lines and components. Micromachined Transmission Lines – Losses in Transmission lines, coplanar lines, Meicroshield and membrane supported lines, Microshield components, Micromachined waveguides, directional couplers and mixers, Resonators and Filters. (Ref.1, Chap.7)

Micromachined antennas. Design, Fabrication and Measurements. Integration and Packaging for RF MEMS. Roles and types of Packages, Flip Chip Techniques, Multichip module packaging and Wafer bonding, Reliability issues and Thermal issues. (Ref.1, Chap.8 & 9)

Reference Books:
