<table>
<thead>
<tr>
<th>Subject Code</th>
<th>Name of the Subject</th>
<th>Teaching hours/week</th>
<th>Duration of Exam in Hours</th>
<th>Marks for</th>
<th>Total Marks</th>
<th>CREDITS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Lecture</td>
<td>Practical / Field Work / Assignment / Tutorials</td>
<td>I.A.</td>
<td>Exam</td>
<td></td>
</tr>
<tr>
<td>14ELD11</td>
<td>Advanced Mathematics</td>
<td>4</td>
<td>2</td>
<td>3</td>
<td>50</td>
<td>100</td>
</tr>
<tr>
<td>14EVE12</td>
<td>Digital VLSI Design</td>
<td>4</td>
<td>2</td>
<td>3</td>
<td>50</td>
<td>100</td>
</tr>
<tr>
<td>14EVE13</td>
<td>Advanced Embedded Systems</td>
<td>4</td>
<td>2</td>
<td>3</td>
<td>50</td>
<td>100</td>
</tr>
<tr>
<td>14ELD14</td>
<td>Digital Circuits and Logic Design</td>
<td>4</td>
<td>2</td>
<td>3</td>
<td>50</td>
<td>100</td>
</tr>
<tr>
<td>14ELD15X</td>
<td>Elective - I</td>
<td>4</td>
<td>2</td>
<td>3</td>
<td>50</td>
<td>100</td>
</tr>
<tr>
<td>14ELD16</td>
<td>Digital Electronics Lab -1</td>
<td>--</td>
<td>3</td>
<td>3</td>
<td>25</td>
<td>50</td>
</tr>
<tr>
<td>14ELD17</td>
<td>Seminar on Advanced topics from refereed journals</td>
<td>--</td>
<td>3</td>
<td>--</td>
<td>25</td>
<td>--</td>
</tr>
</tbody>
</table>

**Total**  
20 16 18 300 550 850 23

**Elective-1**

<table>
<thead>
<tr>
<th>Subject Code</th>
<th>Name of the Subject</th>
</tr>
</thead>
<tbody>
<tr>
<td>14 ELD 151</td>
<td>Digital System Design using Verilog</td>
</tr>
<tr>
<td>14 ELD 152</td>
<td>Automotive Electronics</td>
</tr>
<tr>
<td>14 ELD 153</td>
<td>NanoElectronics</td>
</tr>
<tr>
<td>14 EVE 154</td>
<td>ASIC Design</td>
</tr>
<tr>
<td>14 ELD 155</td>
<td>Simulation, Modeling and Analysis</td>
</tr>
</tbody>
</table>
### Scheme of Teaching and Examination for M.Tech. Electronics

**II Semester**

<table>
<thead>
<tr>
<th>Subject Code</th>
<th>Name of the Subject</th>
<th>Lecture</th>
<th>Practical/Field Work/Assignment/Tutorials</th>
<th>Duration of Exam in Hours</th>
<th>Marks for Total Marks</th>
<th>CREDITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>14ELD21</td>
<td>Modern DSP</td>
<td>4</td>
<td>2</td>
<td>3</td>
<td>50</td>
<td>100</td>
</tr>
<tr>
<td>14ELD22</td>
<td>Coding Theory</td>
<td>4</td>
<td>2</td>
<td>3</td>
<td>50</td>
<td>100</td>
</tr>
<tr>
<td>14ELD23</td>
<td>Digital Signal Compression</td>
<td>4</td>
<td>2</td>
<td>3</td>
<td>50</td>
<td>100</td>
</tr>
<tr>
<td>14ELD24</td>
<td>Real Time Operating Systems</td>
<td>4</td>
<td>2</td>
<td>3</td>
<td>50</td>
<td>100</td>
</tr>
<tr>
<td>14ELD25X</td>
<td>Elective-2</td>
<td>4</td>
<td>2</td>
<td>3</td>
<td>50</td>
<td>100</td>
</tr>
<tr>
<td>14ELD26</td>
<td>Digital Electronics Lab -2</td>
<td></td>
<td>3</td>
<td>3</td>
<td>25</td>
<td>50</td>
</tr>
<tr>
<td>14ELD27</td>
<td>Seminar on Advanced topics from refereed journals</td>
<td>--</td>
<td>3</td>
<td>--</td>
<td>25</td>
<td>--</td>
</tr>
</tbody>
</table>

**Project Phase-I(6 week Duration)**

**Total**  

<table>
<thead>
<tr>
<th>Teaching hours/week</th>
<th>Marks for</th>
<th>Total Marks</th>
<th>CREDITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lecture</td>
<td>I.A.</td>
<td>Exam</td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>16</td>
<td>18</td>
<td></td>
</tr>
<tr>
<td></td>
<td>300</td>
<td>550</td>
<td>850</td>
</tr>
</tbody>
</table>

**Elective -2:**

<table>
<thead>
<tr>
<th>Subject Code</th>
<th>Subject</th>
</tr>
</thead>
<tbody>
<tr>
<td>14 ELD 251</td>
<td>VLSI Design and Verification</td>
</tr>
<tr>
<td>14 ELD 252</td>
<td>Synthesis &amp; Optimization of Digital Circuits</td>
</tr>
<tr>
<td>14 ELD 253</td>
<td>MEMS</td>
</tr>
<tr>
<td>14 ECS 254</td>
<td>Multimedia Communication</td>
</tr>
<tr>
<td>14 ECS 255</td>
<td>Spread Spectrum Communication</td>
</tr>
</tbody>
</table>

**Between the II Semester and III Semester, after availing a vacation of 2 weeks.**
### III Semester: INTERNSHIP #

<table>
<thead>
<tr>
<th>Course Code</th>
<th>Subject</th>
<th>Teaching hours/week</th>
<th>Duration of the Exam in Hours</th>
<th>Marks for</th>
<th>Total Marks</th>
<th>CREDITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>14ELD31</td>
<td>Midterm Presentation on Internship (After 8 weeks from the date of commencement) *</td>
<td>-</td>
<td>-</td>
<td>25</td>
<td>25</td>
<td>1</td>
</tr>
<tr>
<td>14ELD32</td>
<td>Report on Internship (After 16 weeks from the date of commencement)</td>
<td>-</td>
<td>-</td>
<td>75</td>
<td>75</td>
<td>15</td>
</tr>
<tr>
<td>14ELD33</td>
<td>Evaluation and Viva-voce</td>
<td>-</td>
<td>3</td>
<td>–</td>
<td>50</td>
<td>4</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td></td>
<td></td>
<td></td>
<td><strong>100</strong></td>
<td><strong>50</strong></td>
<td><strong>20</strong></td>
</tr>
</tbody>
</table>

* The student shall make a midterm presentation of the activities undertaken during the first 8 weeks of internship to a panel comprising Internship Guide, a senior faculty from the department and Head of the Department.

# The College shall facilitate and monitor the student internship program.

The internship report of each student shall be submitted to the University.
### IV Semester

<table>
<thead>
<tr>
<th>Subject Code</th>
<th>Subject</th>
<th>Teaching hours/week</th>
<th>Duration of Exam in Hours</th>
<th>Marks for Total Marks</th>
<th>CREDITS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Lecture</td>
<td>Practical / Field Work / Assignment / Tutorials</td>
<td>I.A.</td>
<td>Exam</td>
</tr>
<tr>
<td>14ELD41</td>
<td>Advanced Computer Architecture</td>
<td>4</td>
<td>2</td>
<td>3</td>
<td>50</td>
</tr>
<tr>
<td>14ELD42X</td>
<td>Elective-3</td>
<td>4</td>
<td>2</td>
<td>3</td>
<td>50</td>
</tr>
<tr>
<td>14ELD43</td>
<td>Evaluation of Project Phase-I</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>25</td>
</tr>
<tr>
<td>14ELD44</td>
<td>Phase-II : Midterm evaluation of Project</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>25</td>
</tr>
<tr>
<td>14ELD45</td>
<td>Evaluation of Project Work and Viva-voce</td>
<td>-</td>
<td>-</td>
<td>3</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td><strong>Total</strong></td>
<td><strong>8</strong></td>
<td><strong>04</strong></td>
<td><strong>09</strong></td>
<td><strong>150</strong></td>
</tr>
</tbody>
</table>

**Elective -3:**

- 14 EVE 421 Advances in VLSI Design
- 14 ELD 422 Image and Video Processing
- 14 ECS 423 RF and Microwave Circuit Design
- 14 ELD 424 Cryptographic Systems
- 14 ELD 425 Advanced Microcontrollers
Note:

1) Project Phase – I: 6 weeks duration shall be carried out between II and III Semesters. Candidates in consultation with the guides shall carry out literature survey / visit to Industries to finalize the topic of dissertation.

2) Project Phase – II: 16 weeks duration during III Semester. Evaluation shall be taken during the Second week of the IV Semester. Total Marks shall be 25.


Marks of Evaluation of Project:

- The I.A. Marks of Project Phase – I & II shall be sent to the University along with Project Work report at the end of the Semester.

4) During the final viva, students have to submit all the reports.

5) The Project Valuation and Viva-Voce will be conducted by a committee consisting of the following:

   a) Head of the Department (Chairman)
   b) Guide
   c) Two Examiners appointed by the university. (Out of two external examiners at least one should be present).
Advanced Mathematics

Subject Code : 14ELD11  IA Marks : 50
No. of Lecture Hours / Week : 04  Exam. Hours : 03
Total No. of Lecture Hours : 50  Exam. Marks : 100

Matrix Theory
QR EL Decomposition – Eigen values using shifted QR algorithm- Singular Value EL Decomposition - Pseudo inverse- Least square approximations

Calculus of Variations
Concept of Functionals- Euler’s equation – functional dependent on first and higher order derivatives – Functionals on several dependent variables – Iso perimetric problems- Variational problems with moving boundaries

Transform Methods
Laplace transform methods for one dimensional wave equation – Displacements in a string – Longitudinal vibration of a elastic bar – Fourier transform methods for one dimensional heat conduction problems in infinite and semi infinite rod.

Elliptic Equation
Laplace equation – Properties of harmonic functions – Fourier transform methods for laplace equations. Solution for Poisson equation by Fourier transforms method

Linear and Non Linear Programming
Simplex Algorithm- Two Phase and Big M techniques – Duality theory- Dual Simplex method. Non Linear Programming –Constrained extremal problems- Lagranges multiplier method- Kuhn- Tucker conditions and solutions
Reference Books:
# Digital VLSI Design

<table>
<thead>
<tr>
<th>Subject Code</th>
<th>14EVE12</th>
<th>IA Marks</th>
<th>50</th>
</tr>
</thead>
<tbody>
<tr>
<td>No. of Lecture Hours /week</td>
<td>04</td>
<td>Exam Hours</td>
<td>03</td>
</tr>
<tr>
<td>Total no. of Lecture Hours</td>
<td>50</td>
<td>Exam Marks</td>
<td>100</td>
</tr>
</tbody>
</table>


MOS Inverters: Static Characteristics: Introduction, Resistive-Load Inverter, Inverters with n_Type MOSFET Load, CMOS Inverter.


BiCMOS Logic Circuits: Introduction, Bipolar Junction Transistor (BJT): Structure and Operation, Dynamic Behavior of BJTs, Basic BiCMOS Circuits: Static Behavior, Switching Delay in BiCMOS Logic Circuits, BiCMOS Applications.


Reference Books:

Advanced Embedded Systems


Embedded Firmware Design and Development: Embedded Firmware Design Approaches, Embedded Firmware Development Languages

Real-Time Operating System (RTOS) based Embedded System Design: Operating System Basics, Types of OS, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling, Threads, Processes and Scheduling: Putting them altogether, Task Communication, Task Synchronization, Device Drivers, How to Choose an RTOS

The Embedded System Development Environment: The Integrated Development Environment (IDE), Types of Files Generated on Cross compilation, Disassembler/ELDompiler, Simulators, Emulators and Debugging, Target Hardware Debugging, Boundary Scan.
Reference Books:

Digital Circuits and Logic Design

Subject Code    : 14ELD14 IA Marks : 50
No. of Lecture Hours /week : 04 Exam Hours : 03
Total no. of Lecture Hours : 50 Exam Marks : 100

Threshold Logic: Introductory Concepts, Synthesis of Threshold Networks

Reliable Design and Fault Diagnosis Hazards: Fault Detection in Combinational Circuits, Fault-Location Experiments, Boolean Differences, Fault Detection by Path Sensitizing, Detection of Multiple Faults, Failure-Tolerant Design, Quadded Logic

Capabilities, Minimization, and Transformation of Sequential Machines: The Finite- State Model, Further Definitions, Capabilities and Limitations of Finite – State Machines, State Equivalence and Machine Minimization, Simplification of Incompletely Specified Machines.


Reference Books:
2. Charles Roth Jr., “Digital Circuits and logic Design”,
Digital System Design Using Verilog

Subject Code : 14 ELD151
IA Marks : 50
No. of Lecture Hours /week : 04
Exam Hours : 03
Total no. of Lecture Hours : 50
Exam Marks : 100


Combinational Basics: Boolean Functions and Boolean Algebra, Binary Coding, Combinational Components and Circuits, Verification of Combinational Circuits.

Number Basics: Unsigned and Signed Integers, Fixed and Floating-point Numbers.

Sequential Basics: Storage elements, Counters, Sequential Datapaths and Control, Clocked Synchronous Timing Methodology.

Memories: Concepts, Memory Types, Error Detection and Correction.

Implementation Fabrics: ICs, PLDs, Packaging and Circuit Boards, Interconnection and Signal Integrity.

Processor Basics: Embedded Computer Organization, Instruction and Data, Interfacing with memory.

I/O interfacing: I/O devices, I/O controllers, Parallel Buses, Serial Transmission, I/O software.

Accelerators: Concepts, case study, Verification of accelerators.

Design Methodology: Design flow, Design optimization, Design for test.

REFERENCE BOOKS:

Automotive Electronics

Subject Code : 14ELD152       IA Marks  : 50
No. of Lecture Hours /week : 04       Exam Hours  : 03
Total no. of Lecture Hours : 50       Exam Marks  : 100


Actuators – Fuel Metering Actuator, Fuel Injector, Ignition Actuator

Exhaust After-Treatment Systems – AIR, Catalytic Converter, Exhaust Gas Recirculation (EGR), Evaporative Emission Systems

Electronic Engine Control – Engine parameters, variables, Engine Performance terms, Electronic Fuel Control System, Electronic Ignition control, Idle speed control, EGR Control


Vehicle Motion Control – Cruise Control, Chassis, Power Brakes, Antilock Brake System (ABS), Electronic Steering Control, Power Steering, Traction Control, Electronically controlled suspension

Automotive Instrumentation – Sampling, Measurement & Signal Conversion of various parameters


Future Automotive Electronic Systems – Alternative Fuel Engines, Collision Avoidance Radar warning Systems, Low tire pressure warning system, Radio navigation, Advance Driver Information System
Reference Books:


Characterization: Classification, Microscopic techniques, Field ion microscopy, scanning probe techniques, diffraction techniques: bulk, surface, spectroscopy techniques: photon, radiofrequency, electron, surface analysis and dept profiling: electron, mass, Ion beam, Reflectometry, Techniques for property measurement: mechanical, electron, magnetic, thermal properties.


Fabrication techniques: requirements of ideal semiconductor, epitaxial growth of quantum wells, lithography and etching, cleaved edgeover growth, growth of vicinal substrates, strain induced dots and wires, electrostatically induced dots and wires, Quantum well width fluctuations, thermally annealed quantum wells, semiconductor nanocrystals, collidal quantum dots, self-assembly techniques.

Physical processes: modulation doping, quantum hall effect, resonanttunneling, charging effects, ballistic carrier transport, Inter band absorption, intraband absorption, Light emission processes, phonon bottleneck, quantumconfined stark effect, nonlinear effects, coherence and dephasing, characterization of semiconductor nanostructures: optical electrical and structural.

Methods of measuring properties-structure:atomic,crystallography,microscopy,spectroscopy. Properties of nanoparticles: metalnano clusters, semiconducting nanoparticles, rare gas and molecularclusters, methods of synthesis(RF, chemical, thermolysis, pulsed laser methods) Carbon nanostructures and its applications(field emission and shielding, computers, fuelcells, sensors, catalysis).Self assembling nanostructured

**Applications:** Injectionlasers, quantumcascadelasers, singlephotonsources, biologicaltagging, opticalmemories, coulomb blockade devices, photonic structures, QWIP’s, NEMS, MEMS.

**Reference Books:**

ASIC Design

Subject Code : 14EVE154
No. of Lecture Hours /week : 04
Total no. of Lecture Hours : 50
IA Marks : 50
Exam Hours : 03
Exam Marks : 100

Note: All Designs Will Be Based On VHDL

Introduction: Full Custom with ASIC, Semi custom ASICS, Standard Cell based ASIC, Gate array based ASIC, Channelled gate array, Channel less gate array, structured get array, Programmable logic device, FPGA design flow, SIC cell libraries.

Data Logic Cells: Data Path Elements, Adders, Multiplier, Arithmetic Operator, I/O cell, Cell Compilers

ASIC Library Design: Logical effort: practicing delay, logical area and logical efficiency logical paths, multi stage cells, optimum delay, optimum no. of stages, library cell design.


Programmable ASIC: programmable ASIC logic cell, ASIC I/O cell.

A Brief Introduction to Low Level Design Language: an introduction to EDIF, PLA Tools, an introduction to CFI designs representation. Half gate ASIC. Introduction to Synthesis and Simulation.

ASIC Construction Floor Planning and Placement And Routing: Physical Design, CAD Tools, System Partitioning, Estimating ASIC size, partitioning methods. Floor planning tools, I/O and power planning, clock planning, placement algorithms, iterative placement improvement, Time driven placement methods. Physical Design flow global Routing, Local Routing, Detail Routing, Special Routing, Circuit Extraction and DRC.

Reference Books:
Basic simulation modeling: nature of simulation, system models, discrete event simulation, single server simulation, alternative approaches, other types of simulation.

Building valid, credible and detailed simulation models. Techniques for increasing model validity and credibility, comparing real world observations

Selecting input probability distributions. Useful probability distributions, assessing sample independence, activity I, II and III. Models of arrival process.

Random numbers generators: linear congruential, other kinds, testing random number generators. Random variate generation: approaches, continuous random variates, discrete random variates, correlated random variates.


Reference Books:
Digital Electronics Lab -1

Subject Code : 14ELD16  
IA Marks : 25
No. of Lecture Hours /week : 03  
Exam Hours : 03
Total no. of Lecture Hours : 42  
Exam Marks : 50

Design Using Cadence ORCAD

1. Design of 3½ Digit Digital Voltmeter
2. Design of Monolithic function Generator.
3. Design of Regulator Power supplies.
4. Design of Batch counter using TTL ICs.
5. Design of DAC and ADC.
7. Design of Programmable Timers.
8. Design of filters and resonance circuits.

VLSI DIGITAL DESIGN

FPGA DIGITAL DESIGN

VLSI Front End Design programs:
Programming can be done using any compiler. Download the programs on FPGA/CPLD boards and performance testing may be done using pattern generator (32 channels and logic analyzer)/Chipscope pro apart from verification by simulation with any of the front end tools

1. Write Verilog code for the design of 8-bit
   i. Carry Ripple Adder
   ii. Carry LookAhead adder
   iii. Carry Skip Adder
iv. BCD Adder & Subtracter

2. Write Verilog Code for 8-bit
   i. Array Multiplication (Signed and Unsigned)
   ii. Booth Multiplication (Radix-4)

3. Write Verilog code for 4/8-bit
   i. Magnitude Comparator
   ii. LFSR
   iii. Parity Generator
   iv. Universal Shift Register

4. Write Verilog Code for 3-bit Arbitrary Counter to generate 0,1,2,3,6,5,7 and repeats.

5. Design a Mealy and Moore Sequence Detector using Verilog to detect Sequence.
   Eg 11101 (with and without overlap) any sequence can be specified

6. Design a FIFO and LIFO buffers in Verilog and Verify its Operation.

7. Design a coin operated public Telephone unit using Mealy FSM model with following operations
   i. The calling process is initiated by lifting the receiver.
   ii. Insert 1 Rupee Coin to make a call.
   iii. If line is busy, placing the receiver on hook should return a coin
   iv. If line is through, the call is allowed for 60 seconds at the 45th second prompt another 1 Rupee coin to be inserted, to continue the call.
   v. If user doesn't insert the coin within 60 seconds the call should be terminated.
   vi. The system is ready to accept new call request when the receiver is placed on the hook.
   vii. The FSM goes 'out of order' state when there is a Line Fault.

Note: Implementing the above designs on Xilinx/Altera/Cypress/equivalent based FPGA/CPLD kits
Modern DSP

Goal of the course – Advances in Digital Signal Processing involve variable sampling rates and thus the multirate signal processing and hence their applications in communication systems and signal processing. It is intended to introduce a basic course in multirate signal processing especially meant for students of branches eligible for M Tech courses in EC related disciplines.

Introduction and Discrete Fourier Transforms: Signals, Systems and Processing, Classification of Signals, The Concept of Frequency in Continuous-Time and Discrete-Time Signals, Analog-to-Digital and Digital-to-Analog Conversion, Frequency-Domain Sampling: The Discrete Fourier Transform, Properties of the DFT, Linear Filtering Methods Based on the DFT (Ref.1 Chap. 1 & 7)

Design of Digital Filters: General Considerations, Design of FIR Filters, Design of IIR Filters from Analog Filters, Frequency Transformations. (Ref.1 Chap.10)

Multirate Digital Signal Processing: Introduction, EL Dimation by a factor ‘D’, Interpolation by a factor ‘I’, Sampling rate Conversion by a factor ‘I/D’, implementation of Sampling rate conversion, Multistage implementation of Sampling rate conversion, Sampling rate conversion of Band Pass Signals, Sampling rate conversion by an arbitrary factor, Applications of Multirate Signal Processing, Digital Filter banks, Two Channel Quadrature Mirror Filter banks, M-Channel QMF bank. (Ref.1 Chap.11)

Adaptive Filters: Applications of Adaptive Filters, Adaptive Direct Form FIR Filters- The LMS Algorithm, Adaptive Direct Form Filters-RLS Algorithm. (Ref.1 Chap.13)

Reference Books:

Source coding: Uniquely EL Dodable codes, Instantaneous codes and its construction, Average length of a code, Bounds for Average Length, Kraft's Inequality, R-ary compact codes. Code efficiency, Redundancy. Shannon-Fano and Huffman code.

Algebra: Groups, rings and fields, properties of finite fields, Galois field arithmetic and its realization, Vector spaces, Matrices.


Reference Books:

Digital Signal Compression

Introduction: Compression techniques, Modeling & coding, Distortion criteria, Differential Entropy, Rate Distortion Theory, Vector Spaces, Information theory, Models for sources, Coding – uniquely ELDodable codes, Prefix codes, Kraft McMillan Inequality

Quantization: Quantization problem, Uniform Quantizer, Adaptive Quantization, Non-uniform Quantization; Entropy coded Quantization, Vector Quantization, LBG algorithm, Tree structured VQ, Structured VQ, Variations of VQ – Gain shape VQ, Mean removed VQ, Classified VQ, Multistage VQ, Adaptive VQ, Trellis coded quantization


Transform Coding: Transforms – KLT, DCT, DST, DWHT; Quantization and coding of transform coefficients, Application to Image compression – JPEG, Application to audio compression.


Wavelet Based Compression: Wavelets, Multiresolution analysis & scaling function, Implementation using filters, Image compression – EZW, SPIHT, JPEG 2000

Analysis/Synthesis Schemes: Speech compression – LPC-10, CELP, MELP, Image Compression – Fractal compression

Video Compression: Motion compensation, Video signal representation, Algorithms for video conferencing & videophones – H.261, H. 263, Asymmetric applications – MPEG 1, MPEG 2, MPEG 4, MPEG 7, Packet video

Reference Books:

Real Time Operating Systems

<table>
<thead>
<tr>
<th>Subject Code</th>
<th>14ELD24</th>
<th>IA Marks</th>
<th>50</th>
</tr>
</thead>
<tbody>
<tr>
<td>No. of Lecture Hours /week</td>
<td>04</td>
<td>Exam Hours</td>
<td>03</td>
</tr>
<tr>
<td>Total no. of Lecture Hours</td>
<td>50</td>
<td>Exam Marks</td>
<td>100</td>
</tr>
</tbody>
</table>


**Processing**: Preemptive Fixed-Priority Policy, Feasibility, Rate Monotonic, least upper bound, Necessary and Sufficient feasibility, Deadline – Monotonic Policy, Dynamic priority policies.

**I/O Resources**: Worst-case Execution time, Intermediate I/O, Execution efficiency, I/O Architecture.

**Memory**: Physical hierarchy, Capacity and allocation, Shared Memory, ECC Memory, Flash file systems.

**Multi-resource Services**: Blocking, Deadlock and livestock, Critical sections to protect shared resources, priority inversion.

**Soft Real-Time Services**: Missed Deadlines, QoS, Alternatives to rate monotonic policy, Mixed hard and soft real-time services.

**Embedded System Components**: Firmware components, RTOS system software mechanisms, Software application components.


**Performance Tuning**: Basic concepts of drill-down tuning, hardware – supported profiling and tracing, Building performance monitoring into software, Path length, Efficiency, and Call frequency, Fundamental optimizations.

**High availability and Reliability Design**: Reliability and Availability, Similarities and differences, Reliability, Reliable software, Available software, Design tradeoffs, Hierarchical applications for Fail-safe design.

**Design of RTOS – PIC microcontroller.** (Chap 13 of book MykePredko)
Reference Books:

Note: Today, the complexity of the VLSI integrated circuits that are being designed is so large that pre-silicon verification presents a major challenge to the design team. The fact that IP from multiple sources are integrated today to create a system-on-chip design further complicates the matter. Simulation-based verification techniques that were developed in the past are considered inadequate today, since they require too many test cases and require too much development time and run-time. Raising the level of abstraction to design can help bring down the simulation cost. Formal specification and verification techniques are another way to address the challenge of design verification.

**Importance of Design Verification:** What is verification? What is a test bench? The importance of verification, Reconvergence model, Formal verification, Equivalence checking, Model checking, Functional verification.[Ref1- Chapter1]

**Functional verification approaches:** Black box verification, white box verification, grey box verification. Testing versus verification: scan based testing, design for verification. Verification reuse. The cost of verification.[Ref1- Chapter1]

**Verification Tools:** Linting tools: Limitations of linting tools, linting verilog source code, linting VHDL source code, linting OpenVera and e-source code, code reviews. Simulators: Stimulus and response, Event based simulation, cycle based simulation, Co-simulators, verification intellectual property: hardware modelers, waveform viewers.[Ref1-Chapter2]

**Code Coverage:** statement coverage, path coverage, expression coverage, FSM coverage, what does 100% coverage mean? Functional coverage: Item Coverage, cross coverage, Transition coverage, what does 100% functional mean? Verification languages: Assertions: simulation based assertions, formal assertions proving. Metrics: Code related metrics, Quality related metrics, interpreting metrics.[Ref1-Chapter2]

**The verification plan:** The role of verification plan: specifying the verification plan, defining the first success. Levels of verification: unit level verification, reusable components verification, ASIC and FPGA verification, system level verification, board level verification, verifying strategies, verifying responses. [Ref1-Chapter3]
From specification to features: component level feature, system level features, Error types to look for?, prioritise, design for verification. Directed test bench approaches group into test cases, from test cases to test benches, measuring progress. Coverage driven random based approach: Measuring progress, From features to functional coverage, from features to test bench, From features to generators, directed test cases. [Ref1-Chapter3]

Static Timing Verification: Concept of static timing analysis. Cross talk and noise. Limitations of STA. slew of a wave form, Skew between the signals, Timing arcs and unateness, Min and Max timing paths, clock domains, operating conditions, critical path analysis, falsepaths, Timing models. [Ref2 Chapter 1, 2, 3, 8]

Physical Design Verification: Layout rule checks and electrical rule checks. Parasitic extraction. Antenna, Crosstalk and Noise: Cross talk glitch analysis, crosstalk delayanalysis, timing verification [Ref4 Chapter 8]

IP-Reuse in modern-day SoC: SoC Integration and the problem of verification of IP-based designs. Verification IP and their importance, Formal Verification: SAT BDDs, Symbolic Model Checking with BDDs, Model Checking using SAT, Equivalence Checking. [Ref 5, Ref3 Chapter 1, 2]

Reference Books:

3. S.Minato “Binary Decision diagram and applications for VLSICAD”, Kulwer Academic pub November 1996
Introduction: Microelectronics, semiconductor technologies and circuit taxonomy, Microelectronic design styles, computer aided synthesis and optimization.

Graphs: Notation, undirected graphs, directed graphs, combinatorial optimization, Algorithms, tractable and intractable problems, algorithms for linear and integer programs, graph optimization problems and algorithms, Boolean algebra and Applications.

Hardware Modeling: Hardware Modeling Languages, distinctive features, structural hardware language, Behavioural hardware language, HDLs used in synthesis, abstract models, structures logic networks, state diagrams, dataflow and sequencing graphs, compilation and optimization techniques.

Two Level Combinational Logic Optimization: Logic optimization, principles, operation on two level logic covers, algorithms for logic minimization, symbolic minimization and encoding property, minimization of Boolean relations.

Multiple Level Combinational Optimizations: Models and transformations for combinational networks, algebraic model, Synthesis of testable network, algorithm for delay evaluation and optimization, rule based system for logic optimization.

Sequential Circuit Optimization: Sequential circuit optimization using state based models, sequential circuit optimization using network models.

Schedule Algorithms: A model for scheduling problems, Scheduling wither source and without resource constraints, Scheduling algorithms for extended sequencing models, Scheduling Pipe lined circuits.

Cell Library Binding: Problem formulation and analysis, algorithms for library binding, specific problems and algorithms for library binding (lookup table F.P.G.As and Anti fuse based F.P.G.As), rule based library binding.

Reference Books:
Overview of MEMS & Microsystems: MEMS & Microsystems, Typical MEMS and Micro system products — features of MEMS, The multidisciplinary nature of Microsystems design and manufacture, Applications of Microsystems in automotive industry, health care industry, aerospace industry, industrial products, consumer products and telecommunications.

Scaling Laws in Miniaturization: Introduction to scaling, scaling in geometry, scaling in rigid body dynamics, scaling electrostatic forces, electromagnetic forces, electricity, scaling in fluid mechanics & heat transfer.

Transduction Principles in MEMS & Microsystems: Introduction, Micro sensors — thermal, radiation, mechanical, magnetic and bio — sensors, Micro actuation, MEMS with micro actuators.


Micro System Design and Modeling: Introduction, Design considerations: Process design, Mechanical design, Modeling using CAD tools: ANSYS / Multiphysics or Intellisuite or MEMS CAD, Features and Design considerations of RF MEMS, Design considerations of Optical MEMS (MOEMS), Design and Modeling: case studies - i) Cantilever beam ii) Micro switches iii) MEMS based SMART antenna in mobile applications for maximum reception of signal in changing communication conditions and iv) MEMS based micro mirror array for control and switching in optical communications.

Micro system packaging: Over view of mechanical packaging of micro electronics micro system packaging, Interfaces in micro system packaging, Packaging technologies.
Reference Books:

Multimedia Communication

Subject Code    : 14ECS254      IA Marks  : 50
No. of Lecture Hours /week : 04        Exam Hours  : 03
Total no. of Lecture Hours  : 50        Exam Marks  : 100

Multimedia Communications: multimedia information representation, multimedia networks, multimedia applications, network QoS and application QoS.

Information Representation: text, images, audio and video, Text and image compression, compression principles, text compression, image compression. Audio and video compression, audio compression, video compression, video compression principles, video compression standards: H.261, H.263, P1.323, MPEG 1, MPEG 2, Other coding formats for text, speech, image and video.

Detailed Study of MPEG 4: coding of audiovisual objects, MPEG 4 systems, MPEG 4 audio and video, profiles and levels. MPEG 7 standardization process of multimedia content description, MPEG 21 multimedia framework, Significant features of JPEG 2000, MPEG 4 transport across the Internet.

Synchronization: notion of synchronization, presentation requirements, reference model for synchronization, Introduction to SMIL, Multimedia operating systems, Resource management, process management techniques.

Multimedia Communication Across Networks: Layered video coding, error resilient video coding techniques, multimedia transport across IP networks and relevant protocols such as RSVP, RTP, RTCP, DVMRP, multimedia in mobile networks, multimedia in broadcast networks.

Reference Books:

Spread Spectrum Communication

Review of digital communication concepts, direct sequence and frequency hop spread spectrum systems.

Hybrid direct sequence/frequency hop spread spectrum. Complex envelop representation of spread spectrum signals.


Spread spectrum communication system model, Performance of spread spectrum signals in jamming environments, Performance of spread spectrum communication systems with and without forward error correction.

Diversity reception in fading channels, Cellular radio concept, CDMA cellular systems. Examples of CDMA cellular systems. Multicarrier CDMA systems. CDMA standards

Reference Books:

Digital Electronics Lab -2

Graphical Programming using LabVIEW
Design of 4 bit Adders (CLA, CSA, CMA, Parallel adders)
Design of Binary Subtractors
Design of Encoder (8X3), ELDoder(3X8)
Design of Multiplexer (8X1), and Demultiplexer (1X8)
Design of code converters & Comparator
Design of FF (SR, D, T, JK, and Master Slave with delays)
Design of registers using latches and flip-flops
Design of 8 bit Shift registers
Design of Asynchronous & Synchronous Counters

ARM-CORTEX M3

[Programming to be done using Keiluvision 4 and download the program on to a M3 evaluation board such as NXP LPC1768 or ATMEL ATSAM3U].

Write an Assembly language program to calculate 10+9+8+....+1
Write a Assembly language program to link Multiple object files and link them together.
Write a Assembly language program to store data in RAM.
Write a C program to Output the "Hello World" message using UART.
Write a C program to Design a Stopwatch using interrupts.
Write an Exception vector table in C
Write an Assembly Language Program for locking a Mutex.
Write a SVC handler in C. Use the wrapper code to extract the correct stack frame starting location. The C handler can then use this to extract the stacked PC location and the stacked register values.
Advanced Computer Architecture

<table>
<thead>
<tr>
<th>Subject Code</th>
<th>14ELD41</th>
<th>IA Marks</th>
<th>50</th>
</tr>
</thead>
<tbody>
<tr>
<td>No. of Lecture Hours /week</td>
<td>04</td>
<td>Exam Hours</td>
<td>03</td>
</tr>
<tr>
<td>Total no. of Lecture Hours</td>
<td>50</td>
<td>Exam Marks</td>
<td>100</td>
</tr>
</tbody>
</table>

Introduction and Review of Fundamentals of Computer Design: Introduction; Classes computers; Defining computer architecture; Trends in Technology; Trends in power in Integrated Circuits; Trends in cost; Dependability, Measuring, reporting and summarizing Performance; Quantitative Principles of computer design; Performance and Price-Performance; Fallacies and pitfalls; Case studies.

Some topics in Pipelining, Instruction –Level Parallelism, Its Exploitation and Limits on ILP: Introduction to pipelining, ILP; Crosscutting issues, fallacies, and pitfalls with respect to pipelining; Basic concepts and challenges of ILP; Case study of Pentium 4, Fallacies and pitfalls.

Introduction to limits in ILP; Performance and efficiency in advanced multiple-issue processors.

Memory Hierarchy Design, Storage Systems: Review of basic concepts; Crosscutting issues in the design of memory hierarchies; Case study of AMD Opteron memory hierarchy; Fallacies and pitfalls in the design of memory hierarchies. Introduction to Storage Systems; Advanced topics in disk storage.

Definition and examples of real faults and failures; I/O performance, reliability measures, and benchmarks; Queuing theory; Crosscutting issues; Designing and evaluating an I/O system – The Internet archive cluster; Case study of NetAA FAS6000 filer; Fallacies and pitfalls.


Reference Books:
Advances in VLSI Design

Review of MOS Circuits: MOS and CMOS static plots, switches, comparison between CMOS and Bi-CMOS.

MESFETS: MESFET and MODFET operations, quantitative description of MESFETS.

MIS Structures and MOSFETS: MIS systems in equilibrium, under bias, small signal operation of MESFETS and MOSFETS.

Short Channel Effects and Challenges to CMOS: Short channel effects, scaling theory, processing challenges to further CMOS miniaturization

Beyond CMOS: Evolutionary advances beyond CMOS, carbon Nanotubes, conventional vs. tactile computing, computing, molecular and biological computing. Mole electronics-molecular Diode and diode-diode logic. Defect tolerant computing.

Super Buffers, Bi-CMOS and Steering Logic: Introduction, RC delay lines, super buffers- An NMOS super buffer, tri state super buffer and pad drivers, CMOS super buffers, Dynamic ratio less inverters, large capacitive loads, pass logic, designing of transistor logic, General functional blocks -NMOS and CMOS functional blocks.


System Design: CMOS design methods, structured design methods, Strategies encompassing hierarchy, regularity, modularity & locality. CMOS Chip design Options, programmable logic, Programmable inter connect, programmable structure, Gate arrays standard cell approach, Full custom design.

Reference Books:

Image and Video Processing

Introduction: 2D systems, Mathematical preliminaries – Fourier Transform, Z Transform, Optical & Modulation transfer function, Matrix theory, Random signals, Discrete Random fields, Spectral density function. (Ref.1, Chap.2)

Image Perception: Light, Luminance, Brightness, Contrast, MTF of the visual system, Visibility function, Monochrome vision models, Fidelity criteria, Color representation, Chromaticity diagram, Color coordinate systems, Color difference measures, Color vision model, Temporal properties of vision. (Ref.1, Chap.3)

Image Sampling and Quantization: Introduction, 2D sampling theory, Limitations in sampling & reconstruction, Quantization, Optimal quantizer, Compander, Visual quantization. (Ref.1, Chap.4)

Image Transforms: Introduction, 2D orthogonal & unitary transforms, Properties of unitary transforms, DFT, DCT, DST, Hadamard, Haar, Slant, KLT, SVD transform. (Ref.1, Chap.5)

Image Representation by Stochastic Models: Introduction, one dimensional Causal models, AR models, Non-causal representations, linear prediction in two dimensions. (Ref.1, Chap.6)

Image Enhancement: Point operations, Histogram modeling, spatial operations, Transform operations, Multi-spectral image enhancement, false color and Pseudo-color, Color Image enhancement. (Ref.1, Chap.7)

Image Filtering & Restoration: Image observation models, Inverse & Wiener filtering, Fourier Domain filters, Smoothing splines and interpolation, Least squares filters, generalized inverse, SVD and Iterative methods, Maximum entropy restoration, Bayesian methods, Coordinate transformation & geometric correction, Blind de-convolution. (Ref.1, Chap.8)

Image Analysis & Computer Vision: Spatial feature extraction, Transform features, Edge detection, Boundary Extraction, Boundary representation, Region representation, Moment representation, Structure, Shape features, Texture, Scene matching & detection, Image segmentation, Classification Techniques. (Ref.1, Chap.9)
**Image Reconstruction from Projections:** Introduction, Radon Transform, Back projection operator, Projection theorem, Inverse Radon transform, Fourier reconstruction, Fan beam reconstruction, 3D tomography. (Ref. 1, Chap. 10)

**Image Data Compression:** Introduction, Pixel coding, Predictive techniques, Transform coding, Inter-frame coding, coding of two tone images, Image compression standards. (Ref. 1, Chap. 11)

**Video Processing:** Fundamental Concepts in Video – Types of video signals, Analog video, Digital video, Color models in video, Video Compression Techniques – Motion compensation, Search for motion vectors, H.261, H.263, MPEG 1, MPEG 2, MPEG 4, MPEG 7 and beyond, Content based video indexing. (Ref. 4)

**Reference Books:**


RF and Microwave Circuit Design

Subject Code : 14ECS423
No. of Lecture Hours /week : 04
Total no. of Lecture Hours : 50
IA Marks : 50
Exam Hours : 03
Exam Marks : 100

Wave Propagation in Networks: Introduction to RF/Microwave Concepts and applications; RF Electronics Concepts; Fundamental Concepts in Wave Propagation; Circuit Representations of two port RF/MW networks


Basic Considerations in Active Networks: Stability Consideration in Active networks, Gain Considerations in Amplifiers, Noise Considerations in Active Networks.


Reference Books:
Cryptographic Systems

Overview: Services, Mechanisms and attack models, Model for network security, Symmetric cipher model, Substitution techniques, Transposition techniques, Rotor machine, Steganography.

Block Ciphers and DES: Block cipher design principles, Block cipher modes of operation. Differential and Linear cryptanalysis 3DES, Rijndael system, AES, IDEA Fermat’s and Euler’s theorem, Big-O notation, Chinese Remainder Theorem, Fields, Group-isomorphism, Discrete Logarithm, Pohlig-Hellman algorithm, Pollard’s p-1 factorization, pollard rho factorization algorithm.


Other Public Key Crypto Systems and Key Management: Key management, Diffie-Hellman key exchange, DH with multiple participants, Elliptic curve arithmetic, Elliptic curve cryptography, Analog of Massey –Omura, Analog of ElGamal crypto systems. Elliptic curve factorization - pollard’s p-1 method, Lenstra’s elliptic curve factorization algorithm, Hyper elliptic curve cryptography.

Message Authentication and Hash Functions: Authentication requirements, Authentication functions, Message authentication codes, Hash functions, Security of hash functions and MAC.


Reference Books:

Advanced Microcontrollers

Subject Code    : 14 ELD425       IA Marks  : 50
No. of Lecture Hours /week : 04       Exam Hours : 03
Total no. of Lecture Hours  : 50       Exam Marks : 100

Note: Microcontrollers have become prevalent in a number of applications such as instrumentation, industrial electronics, automotive electronics, robotics, etc. Advances in VLSI technology permit the integration of not only the processor but also the analog electronics, memory and peripherals necessary for system implementation; this allows low-cost system implementation. Some microcontrollers used in industrial electronics also provide some digital signal processing capability to further reduce the system cost.

Power dissipation is often a consideration in many systems and modern microcontrollers address it through the support of several low-power modes of operation. The aim of the course is to introduce advanced microcontrollers (16-bit and 32-bit).

Motivation for advanced microcontrollers – Low Power embedded systems, On-chip peripherals, low-power RF capabilities. Examples of applications.

MSP430 – 16-bit Microcontroller family. CPU architecture, Instruction set, Interrupt mechanism, Clock system, Memory subsystem, bus – architecture. The assembly language and „C” programming for MSP-430 microcontrollers. On-chip peripherals. WDT, Comparator, Op-Amp, Timer, Basic Timer, Real Time Clock (RTC), ADC, DAC, Digital I/O. Using the low-power features of MSP430. Clock system, low-power modes, Clock request feature, Low-power programming and interrupts.


Applications – Wireless Sensor Networking with MSP430 and Low-Power RF circuits; Pulse Width Modulation(PWM) in Power Supplies.

Reference Books:


4. **Sample Programs for MSP430** downloadable from msp430.com