### I Semester

<table>
<thead>
<tr>
<th>Subject Code</th>
<th>Name of the Subject</th>
<th>Teaching hours/week</th>
<th>Duration of Exam in Hours</th>
<th>Marks for</th>
<th>Total Marks</th>
<th>CREDITS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Lecture</td>
<td>Practical / Field Work / Assignment/ Tutorials</td>
<td></td>
<td>I.A.</td>
<td>Exam</td>
</tr>
<tr>
<td>14ELD11</td>
<td>Advanced Mathematics</td>
<td>4</td>
<td>2</td>
<td>3</td>
<td>50</td>
<td>100</td>
</tr>
<tr>
<td>14ELD12</td>
<td>Digital Circuits and Logic Design</td>
<td>4</td>
<td>2</td>
<td>3</td>
<td>50</td>
<td>100</td>
</tr>
<tr>
<td>14EIE13</td>
<td>Advanced Embedded Systems</td>
<td>4</td>
<td>2</td>
<td>3</td>
<td>50</td>
<td>100</td>
</tr>
<tr>
<td>14EIE14</td>
<td>Advanced Control Systems</td>
<td>4</td>
<td>2</td>
<td>3</td>
<td>50</td>
<td>100</td>
</tr>
<tr>
<td>14EIE15X</td>
<td>Elective - 1</td>
<td>4</td>
<td>2</td>
<td>3</td>
<td>50</td>
<td>100</td>
</tr>
<tr>
<td>14EIE16</td>
<td>Advanced Embedded Systems Lab</td>
<td>--</td>
<td>3</td>
<td>3</td>
<td>25</td>
<td>50</td>
</tr>
<tr>
<td>14EIE17</td>
<td>Seminar on Advanced topics from refereed journals</td>
<td>--</td>
<td>3</td>
<td>--</td>
<td>25</td>
<td>--</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td></td>
<td>20</td>
<td>16</td>
<td>18</td>
<td>300</td>
<td>550</td>
</tr>
</tbody>
</table>

**Elective-1:**

<table>
<thead>
<tr>
<th>Subject Code</th>
<th>Name of the Subject</th>
</tr>
</thead>
<tbody>
<tr>
<td>14ELD151</td>
<td>Digital System Design Using Verilog</td>
</tr>
<tr>
<td>14EIE152</td>
<td>Probability and Random Process</td>
</tr>
<tr>
<td>14ELD153</td>
<td>Nanoelectronics</td>
</tr>
<tr>
<td>14ECS154</td>
<td>CMOS VLSI Design</td>
</tr>
<tr>
<td>14ELD155</td>
<td>Simulation, Modeling and Analysis</td>
</tr>
</tbody>
</table>
**VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELGAUM**
**SCHEME OF TEACHING AND EXAMINATION FOR**
**M.Tech. Industrial Electronics**

### II Semester

<table>
<thead>
<tr>
<th>Subject Code</th>
<th>Name of the Subject</th>
<th>Teaching hours/week</th>
<th>Duration of Exam in Hours</th>
<th>Marks for</th>
<th>Total Marks</th>
<th>CREDITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>14EIE21</td>
<td>Synthesis &amp; Optimization of Digital Circuits</td>
<td>Lecture 4</td>
<td>Practical / Field Work / Assignment/ Tutorials 2</td>
<td>Duration of Exam in Hours 3</td>
<td>I.A. 50</td>
<td>Exam 100</td>
</tr>
<tr>
<td>14EIE22</td>
<td>Modern DSP</td>
<td>Lecture 4</td>
<td>Practical / Field Work / Assignment/ Tutorials 2</td>
<td>Duration of Exam in Hours 3</td>
<td>I.A. 50</td>
<td>Exam 100</td>
</tr>
<tr>
<td>14EIE23</td>
<td>Automotive Electronics</td>
<td>Lecture 4</td>
<td>Practical / Field Work / Assignment/ Tutorials 2</td>
<td>Duration of Exam in Hours 3</td>
<td>I.A. 50</td>
<td>Exam 100</td>
</tr>
<tr>
<td>14EIE24</td>
<td>Design of Power Converters</td>
<td>Lecture 4</td>
<td>Practical / Field Work / Assignment/ Tutorials 2</td>
<td>Duration of Exam in Hours 3</td>
<td>I.A. 50</td>
<td>Exam 100</td>
</tr>
<tr>
<td>14EIE25X</td>
<td>Elective-2</td>
<td>Lecture 4</td>
<td>Practical / Field Work / Assignment/ Tutorials 2</td>
<td>Duration of Exam in Hours 3</td>
<td>I.A. 50</td>
<td>Exam 100</td>
</tr>
<tr>
<td>14EIE26</td>
<td>Modern Digital Signal Processing Lab</td>
<td>Lecture 3</td>
<td>Practical / Field Work / Assignment/ Tutorials 3</td>
<td>Duration of Exam in Hours 3</td>
<td>I.A. 25</td>
<td>Exam 50</td>
</tr>
<tr>
<td>14EIE27</td>
<td>Seminar on Advanced topics from refereed journals</td>
<td>Lecture --</td>
<td>Practical / Field Work / Assignment/ Tutorials 3</td>
<td>Duration of Exam in Hours --</td>
<td>I.A. 25</td>
<td>Exam --</td>
</tr>
</tbody>
</table>

**Total**

<table>
<thead>
<tr>
<th>Lecture</th>
<th>Practical / Field Work / Assignment/ Tutorials</th>
<th>Duration of Exam in Hours</th>
<th>I.A.</th>
<th>Exam</th>
<th>Total Marks</th>
<th>CREDITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>20</td>
<td>16</td>
<td>18</td>
<td>300</td>
<td>550</td>
<td>850</td>
<td>23</td>
</tr>
</tbody>
</table>

**Elective - 2:**

<table>
<thead>
<tr>
<th>Subject Code</th>
<th>Name of the Subject</th>
</tr>
</thead>
<tbody>
<tr>
<td>14EIE251</td>
<td>Advanced Power Electronic Converters and Applications</td>
</tr>
<tr>
<td>14EIE252</td>
<td>Real Time Operating Systems</td>
</tr>
<tr>
<td>14EIE253</td>
<td>Medical Imaging</td>
</tr>
<tr>
<td>14ECS254</td>
<td>Multimedia Communication</td>
</tr>
<tr>
<td>14EIE255</td>
<td>PLCs and Industrial Automation</td>
</tr>
</tbody>
</table>

**Between the II Semester and III Semester, after availing a vocation of 2 weeks.**
## VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELGAUM
### SCHEME OF TEACHING AND EXAMINATION FOR
#### M.Tech. Industrial Electronics

### III Semester: INTERNSHIP #

<table>
<thead>
<tr>
<th>Course Code</th>
<th>Subject</th>
<th>Teaching hours/week</th>
<th>Duration of the Exam in Hours</th>
<th>Marks for Total</th>
<th>Total Marks</th>
<th>CREDITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>14EIE31</td>
<td>Midterm Presentation on Internship (After 8 weeks from the date of commencement) *</td>
<td>-</td>
<td>-</td>
<td>25</td>
<td>-</td>
<td>25</td>
</tr>
<tr>
<td>14EIE 32</td>
<td>Report on Internship (After 16 weeks from the date of commencement)</td>
<td>-</td>
<td>-</td>
<td>75</td>
<td>75</td>
<td>12</td>
</tr>
<tr>
<td>14EIE 33</td>
<td>Evaluation and Viva-voce</td>
<td>-</td>
<td>-</td>
<td>50</td>
<td>50</td>
<td>4</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td></td>
<td>-</td>
<td>-</td>
<td><strong>100</strong></td>
<td><strong>50</strong></td>
<td><strong>150</strong></td>
</tr>
</tbody>
</table>

* The student shall make a midterm presentation of the activities undertaken during the first 8 weeks of internship to a panel comprising Internship Guide, a senior faculty from the department and Head of the Department.
# The College shall facilitate and monitor the student internship program.
The internship report of each student shall be submitted to the University.
### IV Semester

<table>
<thead>
<tr>
<th>Subject Code</th>
<th>Subject</th>
<th>Teaching hours/week</th>
<th>Duration of Exam in Hours</th>
<th>Marks for Total Marks</th>
<th>CREDITS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Lecture 4</td>
<td>Practical / Field Work / Assignment / Tutorials 2</td>
<td>I.A. 50</td>
<td>Exam 100</td>
</tr>
<tr>
<td>14EIE41</td>
<td>RF and Microwave Circuit Design</td>
<td></td>
<td>3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>14EIE42X</td>
<td>Elective-3</td>
<td></td>
<td>3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>14EIE43</td>
<td>Evaluation of Project Phase-I</td>
<td>-</td>
<td>-</td>
<td>25</td>
<td>-</td>
</tr>
<tr>
<td>14EIE44</td>
<td>Phase-II : Midterm evaluation of Project #</td>
<td>-</td>
<td>-</td>
<td>25</td>
<td>-</td>
</tr>
<tr>
<td>14EIE45</td>
<td>Evaluation of Project Work and Viva-voce</td>
<td>–</td>
<td>3</td>
<td>-</td>
<td>100+10</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Total 8</td>
<td>04</td>
<td>09</td>
<td>150</td>
</tr>
</tbody>
</table>

Grand Total (I to IV Sem.): 2400 Marks; 94 Credits

### Elective-3:

<table>
<thead>
<tr>
<th>Subject Code</th>
<th>Subject</th>
</tr>
</thead>
<tbody>
<tr>
<td>14EVE421</td>
<td>Advances in VLSI Design</td>
</tr>
<tr>
<td>14EVE424</td>
<td>Advanced Computer Architecture</td>
</tr>
<tr>
<td>14EIE422</td>
<td>Process Control Instrumentation</td>
</tr>
<tr>
<td>14ELD425</td>
<td>Advanced Microcontrollers</td>
</tr>
<tr>
<td>14EIE423</td>
<td>Low Power VLSI Design</td>
</tr>
</tbody>
</table>
Note:

1) Project Phase – I: 6 weeks duration shall be carried out between II and III Semesters. Candidates in consultation with the guides shall carryout literature survey / visit to Industries to finalize the topic of dissertation.

2) Project Phase – II: 16 weeks duration during III Semester. Evaluation shall be taken during the Second week of the IV Semester. Total Marks shall be 25.


**Marks of Evaluation of Project:**

- The I.A. Marks of Project Phase – I & II shall be sent to the University along with Project Work report at the end of the Semester.

4) During the final viva, students have to submit all the reports.

5) The Project Valuation and Viva-Voce will be conducted by a committee consisting of the following:

   a) Head of the Department (Chairman)
   b) Guide
   c) Two Examiners appointed by the university. (Out of two external examiners at least one should be present).
Advanced Mathematics

Matrix Theory
QR EI Decomposition – Eigen values using shifted QR algorithm- Singular Value EI Decomposition - Pseudo inverse- Least square approximations

Calculus of Variations
Concept of Functionals- Euler’s equation – functional dependent on first and higher order derivatives – Functionals on several dependent variables – Isoperimetric problems- Variational problems with moving boundaries

Transform Methods
Laplace transform methods for one dimensional wave equation – Displacements in a string – Longitudinal vibration of a elastic bar – Fourier transform methods for one dimensional heat conduction problems in infinite and semi infinite rod.

Elliptic Equation
Laplace equation – Properties of harmonic functions – Fourier transform methods for laplace equations. Solution for Poisson equation by Fourier transforms method

Linear and Non Linear Programming
Simplex Algorithm- Two Phase and Big M techniques – Duality theory- Dual Simplex method. Non Linear Programming –Constrained extremal problems- Lagranges multiplier method- Kuhn- Tucker conditions and solutions

Reference Books:
Digital Circuits and Logic Design

Subject Code    : 14ELD12
No. of Lecture Hours /week : 04
Total no. of Lecture Hours  : 50
IA Marks : 50
Exam Hours : 03
Exam Marks : 100

Threshold Logic: Introductory Concepts, Synthesis of Threshold Networks

Reliable Design and Fault Diagnosis Hazards: Fault Detection in Combinational Circuits, Fault-Location Experiments, Boolean Differences, Fault Detection by Path Sensitizing, Detection of Multiple Faults, Failure-Tolerant Design, Quadded Logic

Capabilities, Minimization, and Transformation of Sequential Machines: The Finite-State Model, Further Definitions, Capabilities and Limitations of Finite – State Machines, State Equivalence and Machine Minimization, Simplification of Incompletely Specified Machines.


Reference Books:

2. Charles Roth Jr., “Digital Circuits and logic Design”,
**Advanced Embedded Systems**

Subject Code : 14EIE13  
IA Marks : 50  
No. of Lecture Hours /week : 04  
Exam Hours : 03  
Total no. of Lecture Hours : 50  
Exam Marks : 100

**Typical Embedded System:** Core of the Embedded System, Memory, Sensors and Actuators, Communication Interface, Embedded Firmware, Other System Components Characteristics and Quality Attributes of Embedded Systems


**Embedded Firmware Design and Development:** Embedded Firmware Design Approaches, Embedded Firmware Development Languages, Real-Time Operating System (RTOS) based Embedded System Design.

**Operating System Basics,** Types of OS, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling, Threads, Processes and Scheduling: Putting them altogether, Task Communication, Task Synchronization, Device Drivers, How to Choose an RTOS

**The Embedded System Development Environment:** The Integrated Development Environment (IDE), Types of Files Generated on Cross-compilation, Disassembler/Decompiler, Simulators, Emulators and Debugging, Target Hardware Debugging, Boundary Scan.


**Reference Books:**

Advanced Control Systems

Digital Control Systems: Review of difference equations and Z — transforms, Z- transfer function (Pulse transfer function), Z-.. Transforms analysis sampled data systems, Stability analysis (Jury’s Stability Test and Bilinear Transformation), Pulse transfer functions and different configurations for closed loop Discrete-time control systems

Modern Control Theory: I, State model for continuous time and discrete time systems, Solutions of state equations (for both continuous and discrete systems), Concepts of controllability and observability (For both continuous and discrete systems), Pole Placement by state feedback (for both continuous and discrete systems), Full order and reduced order observes (for both continuous and discrete systems), Dead beat control by state feedback, Optimal control problems using state variable approach, State Regulator and output regulator, Concepts of Model reference control systems, Adaptive Control systems and design

Non Linear Control Systems: Common nonlinearities, Singular Points, Stability of nonlinear systems - Phase plane analysis and describing function analysis, Liapunoy’s stability criterion, Popov’s criterion

Reference Books:

1. K.Ogata, “Modern Control Engineering”, PHI

Combinational Basics: Boolean Functions and Boolean Algebra, Binary Coding, Combinational Components and Circuits, Verification of Combinational Circuits.

Number Basics: Unsigned and Signed Integers, Fixed and Floating-point Numbers.

Sequential Basics: Storage elements, Counters, Sequential Datapaths and Control, Clocked Synchronous Timing Methodology.

Memories: Concepts, Memory Types, Error Detection and Correction.

Implementation Fabrics: ICs, PLDs, Packaging and Circuit Boards, Interconnection and Signal Integrity.

Processor Basics: Embedded Computer Organization, Instruction and Data, Interfacing with memory.

I/O interfacing: I/O devices, I/O controllers, Parallel Buses, Serial Transmission, I/O software.

Accelerators: Concepts, case study, Verification of accelerators.

Design Methodology: Design flow, Design optimization, Design for test.

REFERENCE BOOKS:

Probability and Random Process

Subject Code : 14EIE152
IA Marks : 50
No. of Lecture Hours / Week : 04
Exam. Hours : 03
Total No. of Lecture Hours : 50
Exam. Marks : 100

Introduction to probability theory: Experiments, Sample space, Events, Axioms, Assigning probabilities, Joint and conditional, Baye's theorem, Independence, Discrete random variables, Engineering example

Random variables, Distributions, Density functions: CDF, PDF, Gaussian random variable, Uniform, Exponential, Laplace, Gamma, Erlang, Chi-square, Rayleigh, Rician and Cauchy types of random variables.

Operation on a single random variable: Expected value, EV of random variables, EV of functions of random variables, Central moments, Conditional expected values.

Characteristics functions: Probability generating functions, Moment generating function, Engineering applications, Scalar quantization, Entropy and source coding.

Pairs of random variables: Joint PDF, Joint probability mass functions, Conditional distribution, Density and mass functions, EV involving pairs of random variables, Independent random variables, Complex random variables, Engineering application.

Multiple random variables: Joint and conditional PMF, CDF, PDF, EV involving multiple random variables, Gaussian random variable in multiple dimension, Engineering application, Linear prediction.

Random process: Definition and characterisation, Mathematical tools for studying random processes, Stationery and Ergodic random processes, Properties of ACF.

Reference books:
Introduction: Overview of nanoscience and engineering. Development milestones in micro fabrication and electronic industry, Moores law and continued miniaturization, Classification of Nanostructures, Electronic properties of atoms and solids: Isolated atom, Bonding between atoms, Giant molecular solids, Free electron models and energy bands, crystalline solids, Periodicity of crystal lattices, Electronic conduction, effects of nanometer length scale, Fabrication methods: Top down processes, Bottom up processes methods for templating the growth of nanomaterials, ordering of nanosystems.

Characterization: Classification, Microscopic techniques, Field ion microscopy, scanning probe techniques, diffraction techniques: bulk, surface, spectroscopy techniques: photon, radiofrequency, electron, surface analysis and dept profiling: electron, mass, Ion beam, Reflectrometry, Techniques for property measurement: mechanical, electron, magnetic, thermal properties.

Inorganic semiconductor nanostructures: overview of semiconductor physics, Quantum confinement in semiconductor nanostructures: quantum wells, quantum wires, quantum dots, superlattices, band offsets, electronic density of states.

Fabrication techniques: requirements of ideal semiconductor, epitaxial growth of quantum wells, lithography and etching, cleaved edge overgrowth, growth of vicinal substrates, strain induced dots and wires, electrostatically induced dots and wires, Quantum well width fluctuations, thermally annealed quantum wells, semiconductor nanocrystals, colloidal quantum dots, self-assembly techniques.

Physical processes: modulation doping, quantum hall effect, resonant tunneling, charging effects, ballistic carrier transport, Inter band absorption, intraband absorption, Light emission processes, phonon bottleneck, quantum confined stark effect, nonlinear effects, coherence and dephasing, characterization of semiconductor nanostructures: optical electrical and structural.

Methods of measuring properties-structure: atomic, crystallography, microscopy, spectroscopy. Properties of nanoparticles: metal nano clusters, semiconducting nanoparticles, rare gas and molecular clusters, methods of synthesis(RF, chemical, thermolysis, pulsed laser methods)

Applications: Injection lasers, quantum cascade lasers, singe photon sources, biological tagging, optical memories, coulomb blockade devices, photonic structures, QWIP’s, NEMS, MEMS.

References:


CMOS VLSI Design

Subject Code : 14ECS154
IA Marks : 50
No. of Lecture Hours / Week : 04
Exam. Hours : 03
Total No. of Lecture Hours : 50
Exam. Marks : 100

MOS transistor theory: NMOS/PMOS transistor, Threshold voltage equation, Body effect, MOS device design equation, Sub threshold region, Channel length modulation, Mobility variations, tunnelling, Punch through, Hot electron effect MOS models, Small signal AC characteristic, CMOS inverters, An/Ap ratio, noise margin, Static load MOS inverters, Differential inverter, Transmission gate, Tristate inverter, BiCMOS inverter.

CMOS process Technology: Lambda based design rules, Scaling factor, Semiconductor technology overview, Basic CMOS technology, p-well/n-well/twin-well process. Current CMOS enhancement (oxide isolation, LDD, refractory gate, Multilayer interconnect), Circuit element, resistor, Capacitor, Interconnects, Sheet resistance and standard unit capacitance concept delay unit time, Inverter delays driving capacitive loads, Propagate delays, MOS mask layer, Stick diagram, design rules and layout, Symbolic diagrams, MOS feints, Scaling of MOS circuits.

Basic of Digital CMOS design: Combinational MOS logic circuits -Introduction, CMOS logic circuits with the a MOS load, CMOS logic circuits, Complex logic circuits, transmission gate, Sequential MOS logic circuits - Introduction, Behaviour of high stable elements, SR latch circuits, Clocked latch and flip-flop circuits, CMOS D-latch and triggered flip-flop, Dynamic logic circuits - Introduction, principles of pass transistor circuits, Voltage bootstrapping synchronous dynamic circuit techniques, Dynamic CMOS circuit techniques.

CMOS analog design: Introduction, Single amplifier, Differential amplifier, Current mirrors, Bandgap references, Basis of cross operational amplifier.

Dynamic CMOS and clocking: Introduction, Advantages of CMOS over NMOS, CMOS/SOS technology, CMOS/bulk technology, Latchup in bulk CMOS, Static CMOS design, Domino CMOS structure and design, Charge sharing, Clocking - Clock generation, Clock distribution, Clocked storage elements.

Reference books:


Simulation Modelling and Analysis

Subject Code : 14ELD155
No. of Lecture Hours /week : 04
Total no. of Lecture Hours : 50
IA Marks : 50
Exam Hours : 03
Exam Marks : 100

Basic simulation modeling: nature of simulation, system models, discrete event simulation, single server simulation, alternative approaches, other types of simulation.

Building valid, credible and detailed simulation models. Techniques for increasing model validity and credibility, comparing real world observations.

Selecting input probability distributions. Useful probability distributions, assessing sample independence, activity I, II and III. Models of arrival process.

Random numbers generators: linear congruential, other kinds, testing random number generators. Random variate generation: approaches, continuous random variates, discrete random variates, correlated random variates.


Reference Books:
Advanced Embedded System Lab

Subject Code : 14EIE16
IA Marks : 25
No. of Lecture Hours /week : 03
Exam Hours : 03
Total no. of Lecture Hours : 42
Exam Marks : 50

- Use the EDA (Electronic Design Automation) tools to learn the Embedded Hardware Design and for PCB design.
- Familiarize the different entities for the circuit diagram design.
- Familiarize with the layout design tool, building blocks, component placement, routings, design rule checking etc.

Embedded Programming Concepts (RTOS):
1. Create ‘n’ number of child threads. Each thread prints the message “I’m in thread number …” and sleeps for 50 ms and then quits. The main thread waits for complete execution of all the child threads and then quits. Compile and execute in Linux.

2. Implement the multithread application satisfying the following:
   a. Two child threads are created with normal priority.
   b. Thread 1 receives and prints its priority and sleeps for 50ms and then quits.
   c. Thread 2 prints the priority of the thread 1 and rises its priority to above normal and retrieves the new priority of thread 1, prints it and then quits.
   d. The main thread waits for the child thread to complete its job and quits.

3. Implement the usage of anonymous pipe with 512 bytes for data sharing between parent and child processes using handle inheritance mechanism.

4. Test the program below using multithread application:
   a. The main thread creates a child thread with default stack size and name ‘Child_Thread’.
   b. The main thread sends user defined messages and the message ‘WM_QUIT’ randomly to the child thread.
   c. The child thread processes the message posted by the main thread and quits when it receives the ‘WM_QUIT’ message.
d. The main thread checks the termination of the child thread and quits when the child thread complete its execution.
e. The main thread continues sending the random messages to the child thread till the ‘WM_QUIT’ message is sent to child thread.
f. The messaging mechanism between the main thread and child thread is synchronous.

5. Test the program application for creating an anonymous pipe with 512 bytes of size and pass the ‘Read Handle’ of the pipe to a second process using memory mapped object. The first process writes a message ‘Hi from Pipe Server’. The 2nd process reads the data written by the pipe server to the pipe and displays it on the console. Use event object for indicating the availability of data on the pipe and mutex objects for synchronizing the access in the pipe.

6. Create a POSIX based message queue for communicating between two tasks as per the requirements given below:
   a. Use a named message queue with name ‘MyQueue’.
   b. Create two tasks(Task1 & Task2) with stack size 4000 & priorities 99 & 100 respectively.
   c. Task 1 creates the specified message queue as Read Write and reads the message present, if any, from the message queue and prints it on the console.
   d. Task2 open the message queue and posts the message ‘Hi from Task2’.
   e. Handle all possible error scenarios appropriately.
Synthesis and Optimization of Digital Circuits

Subject Code : 14EIE21
IA Marks : 50
No. of Lecture Hours /week : 04
Exam Hours : 03
Total no. of Lecture Hours : 50
Exam Marks : 100

Introduction: Microelectronics, semiconductor technologies and circuit taxonomy, Microelectronic design styles, computer aided synthesis and optimization.

Graphs: Notation, undirected graphs, directed graphs, combinatorial optimization, Algorithms, tractable and intractable problems, algorithms for linear and integer programs, graph optimization problems and algorithms, Boolean algebra and Applications.

Hardware Modeling: Hardware Modeling Languages, distinctive features, structural hardware language, Behavioral hardware language, HDLs used in synthesis, abstract models, structures logic networks, state diagrams, data flow and sequencing graphs, compilation and optimization techniques.

Two Level Combinational Logic Optimization: Logic optimization, principles, operation on two level logic covers, algorithms for logic minimization, symbolic minimization and encoding property, minimization of Boolean relations.

Multiple Level Combinational Optimizations: Models and transformations for combinational networks, algebraic model, Synthesis of testable network, algorithm for delay evaluation and optimization, rule based system for logic optimization.

Sequential Circuit Optimization: Sequential circuit optimization using state based models, sequential circuit optimization using network models.

Schedule Algorithms: A model for scheduling problems, Scheduling with resource and without resource constraints, Scheduling algorithms for extended sequencing models, Scheduling Pipe lined circuits.

Cell Library Binding: Problem formulation and analysis, algorithms for library binding, specific problems and algorithms for library binding (lookup table F.P.G.As and Antifuse based F.P.G.As), rule based library binding.

Reference Books:

Modern DSP

Subject Code : 14EIE22
No. of Lecture Hours /week : 04
Total no. of Lecture Hours : 50
IA Marks = 50
Exam Hours : 03
Exam Marks : 100

**Goal of the course** – Advances in Digital Signal Processing involve variable sampling rates and thus the multirate signal processing and hence their applications in communication systems and signal processing. It is intended to introduce a basic course in multirate signal processing especially meant for students of branches eligible for M Tech courses in EC related disciplines.

**Introduction and Discrete Fourier Transforms:** Signals, Systems and Processing, Classification of Signals, The Concept of Frequency in Continuous-Time and Discrete-Time Signals, Analog-to-Digital and Digital-to-Analog Conversion, Frequency-Domain Sampling: The Discrete Fourier Transform, Properties of the DFT, Linear Filtering Methods Based on the DFT (Ref.1 Chap. 1 & 7).

**Design of Digital Filters:** General Considerations, Design of FIR Filters, Design of IIR Filters from Analog Filters, Frequency Transformations. (Ref.1 Chap. 10)

**Multirate Digital Signal Processing:** Introduction, Decimation by a factor ‘D’, Interpolation by a factor ‘I’, Sampling rate Conversion by a factor ‘I/D’, implementation of Sampling rate conversion, Multistage implementation of Sampling rate conversion, Sampling rate conversion of Band Pass Signals, Sampling rate conversion by an arbitrary factor, Applications of Multirate Signal Processing, Digital Filter banks, Two Channel Quadrature Mirror Filter banks, M-Channel QMF bank. (Ref.1 Chap. 11)

**Adaptive Filters:** Applications of Adaptive Filters, Adaptive Direct Form FIR Filters- The LMS Algorithm, Adaptive Direct Form Filters-RLS Algorithm. (Ref.1 Chap. 13)

**Reference Books:**


Actuators – Fuel Metering Actuator, Fuel Injector, Ignition Actuator

Exhaust After-Treatment Systems – AIR, Catalytic Converter, Exhaust Gas Recirculation (EGR), Evaporative Emission Systems

Electronic Engine Control – Engine parameters, variables, Engine Performance terms, Electronic Fuel Control System, Electronic Ignition control, Idle speed control, EGR Control


Vehicle Motion Control – Cruise Control, Chassis, Power Brakes, Antilock Brake System (ABS), Electronic Steering Control, Power Steering, Traction Control, Electronically controlled suspension

Automotive Instrumentation – Sampling, Measurement & Signal Conversion of various parameters


Future Automotive Electronic Systems – Alternative Fuel Engines, Collision Avoidance Radar warning Systems, Low tire pressure warning system, Radio navigation, Advance Driver Information System
Reference Books:


Design of Power Converters

Subject Code : 14EIE24
No. of Lecture Hours /week : 04
Total no. of Lecture Hours : 50
IA Marks : 50
Exam Hours : 03
Exam Marks : 100

**Introduction** to power electronic applications like UPS, SMPS, power factor converters, motor control, lighting;

**Converters:** AC to DC converters; DC to DC converters; Inverters;

**Drive circuits for power devices:** Magnetics for switched mode converters;

**Thermal design for switched mode converters:** current mode control; controller designs;

**Switched Mode Power Supply Circuits:** regulation in isolated SMPS; magnetic amplifiers; application case studies.

**Reference Books:**


Advanced Power Electronic Converters and Applications

1. Introduction
1.1 Overview of the field.
1.2 Principles of Steady State Converter Analysis
   a) Inductor Volt-Second Balance, Capacitor Charge Balance, and the Small-Ripple Approximation
   b) Boost Converter Example
   c) Cuk Converter Example
   d) Estimating the Output voltage ripple and inductor current ripple in converters Containing Two-Pole Low-Pass Filters

2. DC - DC Switch-Mode Converters: Dynamic Modeling and Control
2.1 Small-signal modeling:
   2.1.1 Averaging Method
   2.1.2 Discrete Method
      a) Buck Converter
      b) Boost Converter
      c) Buck-Boost Converter
      d) Cuk Converter
2.2 Closed-loop Controller Design
   2.2.1 Power Stage Design
   2.2.2 Feedback Design
   2.2.3 Commercial PWM Controller IC
2.3 Measurement of Loop Gains
   2.3.1 Voltage Injection
   2.3.2 Current Injection

3. Resonant Converters
3.1 Half- and Full-bridge Dc-DC Resonant Converters
3.2 The Series Resonant Converter
3.3 The Parallel Resonant Converter
3.4 Principle of Operation of the Resonant Switch Concept:
   a) Zero-Current Switching
   b) Zero-Voltage Switching

4. Pulse Width Modulation (PWM) Inverter Modulation Strategies
4.1 Sine Pulse Width Modulation (SPWM)
4.2 Sine with third harmonic
4.3 Space Vector modulation
4.4 Selective Harmonic Elimination PWM
4.5 Delta Modulation
4.6 Predictive Current Control Technique

5. Storage systems
Types of batteries used in solar, UPS, EV applications, Fuel cells, Ultra capacitors and future sources; Different types of chargers and various methods of charging.

6. Practical Converter Design Considerations and Applications
6.1 Input Filter Design: EMI issues; Effect of Input Filter on Converter Transfer Functions; Buck Converter Example.
6.2 Magnetics: Review of Basic Magnetics; Loss Mechanisms in Magnetic Devices
   a) Inductor Design: Filter Inductor Design Constraints; Step-by-Step Design
Procedure; Forward and Fly back Transformer Design Examples; Planar Inductor.
b) Transformer Design: Basic Constraints; Step-by-Step Design Procedure; AC
Inductor Design; Multiple-Output Full-Bridge Buck Converter Example; Planar
Transformer Design

6.3 **Snubber Circuits:** Function and Types of Snubber Circuits; Diode Snubbers; Need for Snubbers with Transistors; Turn-On and Turn-Off Snubbers.

6.4 **Power factor, power factor correction:** why is it and why must it be corrected?, power factor correction in switching power supplies, continuous versus discontinuous mode boost topology for power factor correction, study of FAN9611 chip for power factor correction.

6.5 **High Brightness LED Drivers:** Review for suitable power converters in automotive, general light, LCD/LED TV and laptop applications (From Web/Application notes)

6.6 **Digital control of power converters:** Merits and demerits of digital control over analog control, Different types of digital pulse width modulation techniques, problems of limit cycle oscillations, Digital soft-start realization, Digital PID compensation converter (From Web/Application notes)

**Reference Books:**
Real Time Operating Systems

Subject Code : 14EIE252
IA Marks : 50
No. of Lecture Hours /week : 04
Exam Hours : 03
Total no. of Lecture Hours : 50
Exam Marks : 100


Processing: Preemptive Fixed-Priority Policy, Feasibility, Rate Monotonic least upper bound, Necessary and Sufficient feasibility, Deadline – Monotonic Policy, Dynamic priority policies.

I/O Resources:

Memory:
Physical hierarchy, Capacity and allocation, Shared Memory, ECC Memory, Flash filesystems.

Multi-resource Services:
Blocking, Deadlock and livestock, Critical sections to protect shared resources, priority inversion.

Soft Real-Time Services:
Missed Deadlines, QoS, Alternatives to rate monotonic policy, Mixed hard and soft real-time services.

Embedded System Components:
Firmware components, RTOS system software mechanisms, Software application components.

Debugging Components:

Performance Tuning:
Basic concepts of drill-down tuning, hardware – supported profiling and tracing, Building performance monitoring into software, Path length, Efficiency, and Call frequency, Fundamental optimizations.

**High availability and Reliability Design:**
Reliability and Availability, Similarities and differences, Reliability, Reliable software, Available software, Design trade offs, Hierarchical applications for Fail-safe design.

**Design of RTOS – PIC microcontroller.** (Chap 13 of book Myke Predko)

**Reference Books:**
Medical Imaging

Subject Code : 14EIE253  
IA Marks : 50  
No. of Lecture Hours /week : 04  
Exam Hours : 03  
Total no. of Lecture Hours : 50  
Exam Marks : 100

A number of new, imaging techniques and modalities in imaging area have revolutionized the Medicare In this Course principles of various imaging modalities are to be discussed (Ref.1 Chap.1)

**X-Rays**: X ray diagnostic methods, Conventional x-ray radiography fluoroscopy and angiography computed tomography: Recent developments in x-ray unit characteristics. Biological effects ionizing radiation (Ref.1 Chap.1)

**Computed Tomography**: Basic principles, system components and truncations of scanning systems, Medical applications and safety precautions, Discussion on reconstruction algorithms (Ref.1 Chap.1)

**Ultrasound**: Functional block diagram of basic pulse echo system for diagnostic purposes, A mode, B mode and M mode principles of echocardiography (Ref.1 Chap.2)

**Radio Nuclide Imaging**: Principles, schematic functional diagram and components of gamma, Medical applications, safety precautions. (Ref.1 Chap.3)

**Magnetic Resonance Imaging**: Basic principles, Signals excitation and detection, Schematic functional diagram of MRI scanner with its sub systems, Magnet gradient systems, RF transmitter- receiver system, medical applications, safety precautions. (Ref.1 Chap.4)

**Reference Books:**

1. Kirk Shung, Michael B, Smith, Benjamin M W Tsui, “**Principles of medical imaging**”, Academic press
Multimedia communication

Multimedia Communications: multimedia information representation, multimedia networks, multimedia applications, network QoS and application QoS. (Ref.1 Chap. 1)

Information Representation: text, images, audio and video, Text and image compression, compression principles, text compression, image compression. Audio and video compression, audio compression, video compression, video compression principles, video compression standards: H.261, H.263, P1.323, MPEG 1, MPEG 2, Other coding formats for text, speech, image and video.(Ref 1 Chap 3 &4)

Detailed Study of MPEG 4: coding of audiovisual objects, MPEG 4 systems, MPEG 4 audio and video, profiles and levels. MPEG 7 standardization process of multimedia content description, MPEG 21 multimedia framework, Significant features of JPEG 2000, MPEG 4 transport across the Internet. (Ref2. Chap.5)

Synchronization: Notion of synchronization, presentation requirements, reference model for synchronization, Synchronization specification. Multimedia operating systems, Resource management, process management techniques. (Ref. 3. Cahp 9 & 11)

Multimedia Communication Across Networks: Layered video coding, error resilient video coding techniques, multimedia transport across IP networks and relevant protocols such as RSVP, RTP, RTCP, DVMRP, multimedia in mobile networks, multimedia in broadcast networks. (Ref.2 Chap. 6)

Assignments / Practicals can be given on writing the programs to encode and decode the various kinds of data by using the algorithms. Students can collect several papers from journals/conferences/Internet on a specific area of multimedia communications and write a review paper and make a presentation.

Reference Books:

PLCs and Industrial Automation

Introduction: What Is A PLC, Technical Definition Of PLC, What Are Its Advantages, Characteristic Functions Of A PLC, Chronological Evolution Of PLC, Types Of PLC, Unitary PLC Modular PLC, SMEEl PLC, Medium PLC, Large PLC, Block Diagram Of PLC, Input / Output (I / O) Section, Processor Section, Power Supply, Memory, Central Processing Unit, Processor Software / Executive Software, Multitasking, Languages, Ladder Language.

Bit Logic Instructions: Introduction, Input And Output Contact Program, Symbols, Numbering System Of Inputs And Outputs, Program Format, Introduction To Logic, Equivalent Ladder Diagram Of AND Gate, Equivalent Ladder Diagram Of OR Gate, Equivalent Ladder Diagram Of NOT Gate, Equivalent Ladder Diagram Of XOR Gate, Equivalent Ladder Diagram Of NAND Gate, Equivalent Ladder Diagram Of NOR Gate, Equivalent Ladder Diagram To Demonstrate De Morgan Theorem, Ladder Design

Plc Timers And Counters: Timer And Its Classification, Characteristics Of PLC Timer, Functions In Timer, Resetting – Retentive And Non-Retentive, Classification Of PLC Timer, On Delay, And Off Delay Timers, Timer-On Delay, Timer Off Delay, Retentive And Non-Retentive Timers, Format Of a Timer Instruction, PLC Counter, Operation Of PLC Counter, Counter Parameters, Counter Instructions. Overview, Count Up (CTU), Count Down (CTD).


Plc Input Output (I/O) Modules And Power Supply: Introduction, Classification Of I/O, I/O System Overview, Practical I/O System And Its Mapping, Addressing Local And Expansion I/O, Input-Output Systems, Direct I/O Parallel I/O Systems,


**Reference Books:**

Using MATLAB

1 Question based on response of LTI systems to different inputs

A LTI system is defined by the difference equation $y[n]=x[n]+x[n-1]+x[n-2]$.

(a) Determine the impulse response of the system and sketch it.

(b) Determine the output $y[n]$ of the system when the input is $x[n]=u[n]$.

(c) Determine the output of the system when the input is a complex exponential (Eg. $x[n]=2e^{j0.2\pi n}$).

2 Question on design of simple digital filter using the relationship between pole and zeros and the frequency response of the system

Design a simple digital FIR filter with real coefficients to remove a narrowband (i.e., sinusoidal) disturbance with frequency $F_0=50$ Hz. Let $F_s=300$ Hz be the sampling frequency.

(a) Determine the desired zeros and poles of the filter.

(b) Determine the filter coefficients with the gain $K=1$

(c) Sketch the magnitude of the frequency response.

3 Question on simple digital filtering using the relationship between pole and zeros and the frequency response of the system

Design an IIR filter with real coefficients with same specifications mentioned in Q2 and repeat the steps (a) to (c).

4 Question to understand the effect of time domain windowing

Generate a signal with two frequencies $x(t)=3\cos(2\pi F_1 t) + 2\cos(2\pi F_2 t)$ sampled at $F_s=8$ kHz. Let $F_1=1$ kHz and $F_2=F_1+\Delta$ and the overall data length be $N=256$ points.

(a) From theory, determine the minimum value of $\Delta$ necessary to distinguish between the two frequencies.

(b) Verify this result experimentally. Using the rectangular window, look at the DFT with several values of $\Delta$ so that you verify the resolution.

(c) Repeat part (b) using a Hamming window. How did the resolution change?
5  Comparison of DFT and DCT (in terms of energy compactness)
   Generate the sequence \( x[n] = n - 64 \) for \( n = 0, \ldots, 127 \).
   (a) Let \( X[k] = \text{DFT}\{x[n]\} \). For various values of \( L \), set to zero the “high frequency coefficients” \( X[64-L] = \ldots = X[64] = \ldots = X[64+L] = 0 \) and take the inverse DFT. Plot the results.
   (b) Let \( X_{\text{DCT}}[k] = \text{DCT}\{x[n]\} \). For the same values of \( L \), set to zero the “high frequency coefficients” \( X_{\text{DCT}}[127-L] = \ldots = X_{\text{DCT}}[127] \). Take the inverse DCT for each case and compare the reconstruction with the previous case.

6  Filter design
   Design a discrete time low pass filter with the specifications given below:
   Sampling frequency = 2 kHz.
   Pass band edge = 260 Hz
   Stop band edge = 340 Hz
   Max. pass band attenuation = 0.1 dB
   Minimum stop band attenuation = 30 dB
   Use the following design methodologies:
   Hamming windowing
   Kaiser windowing
   Applying bilinear transformation to a suitable, analog Butterworth filter.
   Compare the obtained filters in terms of performance (accuracy in meeting specifications) and computational complexity.

Using DSP Processor
   1. Write an ALP to obtain the response of a system using linear convolution whose input and impulse response are specified.
   2. Write an ALP to obtain the impulse response of the given system, given the difference equation.
   4. Design of equiripple filters.
   5. Application of frequency transformation in filter design.
6. Computation of FFT when N is not a power of 2.
7. Sampling rate conversion and plot of spectrum.
8. Analysis of signals by STFT and WT.
10. Record of machinery noise like fan or blower or diesel generator and obtaining its spectrum.
RF and Microwave Circuit Design

Subject Code : 14EIE41
No. of Lecture Hours /week : 04
Total no. of Lecture Hours : 50
IA Marks : 50
Exam Hours : 03
Exam Marks : 100

Wave Propagation in Networks: Introduction to RF/Microwave Concepts and applications; RF Electronics Concepts; Fundamental Concepts in Wave Propagation; Circuit Representations of two port RF/MW networks


Basic Considerations in Active Networks: Stability Consideration in Active networks, Gain Considerations in Amplifiers, Noise Considerations in Active Networks.


Reference Books:

Advances in VLSI Design

<table>
<thead>
<tr>
<th>Subject Code</th>
<th>12EVE421</th>
<th>IA Marks</th>
<th>50</th>
</tr>
</thead>
<tbody>
<tr>
<td>No. of Lecture Hours /week</td>
<td>04</td>
<td>Exam Hours</td>
<td>03</td>
</tr>
<tr>
<td>Total no. of Lecture Hours</td>
<td>50</td>
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<td>100</td>
</tr>
</tbody>
</table>

**Review of MOS Circuits:** MOS and CMOS static plots, switches, comparison between CMOS and BI-CMOS.

**MESFETS:** MESFET and MODFET operations, quantitative description of MESFETS.

**MIS structures and MOSFETS:** MIS systems in equilibrium, under bias, small signal operation of MESFETS and MOSFETS.

**Short channel effects and challenges to CMOS:** Short channel effects, scaling theory, processing challenges to further CMOS miniaturization

**Beyond CMOS:** Evolutionary advances beyond CMOS, carbon Nano tubes, conventional vs. tactile computing, computing, molecular and biological computing Mole electronics-molecular Diode and diode- diode logic. Defect tolerant computing,

**Super Buffers, Bi-CMOS and Steering Logic:** Introduction, RC delay lines, super buffers- An NMOS super buffer, tri state super buffer and pad drivers, CMOS super buffers, Dynamic ratio less inverters, large capacitive loads, pass logic, designing of transistor logic, General functional blocks - NMOS and CMOS functional blocks.

**Special Circuit Layouts and Technology Mapping:** Introduction, Talley circuits, NAND-NAND, NOR- NOR, and AOI Logic, NMOS, CMOS Multiplexers, Barrel shifter, Wire routing and module lay out.

**System Design:** CMOS design methods, structured design methods, Strategies encompassing hierarchy, regularity, modularity & locality, CMOS Chip design Options, programmable logic, Programmable inter connect, programmable structure, Gate arrays standard cell approach, Full custom Design.

**Reference Books:**

Process Control Instrumentation

Subject Code : 14EIE422
IA Marks : 50
No. of Lecture Hours /week : 04
Exam Hours : 03
Total no. of Lecture Hours : 50
Exam Marks : 100

Introduction to process control, objects and benefits, mathematical modeling;

Principles, modeling analysis for process control; Dynamic behavior of typical process systems;

PID controller tuning for dynamic performance, stability analysis and controller tuning;

Digital implementation of process control;

Temperature measurement using IC temperature sensor, thermocouple & RTD; Measurement of strain, force, displacement weight, flow and pressure;

Signal conditioning & transmission. 4-20mA current transmitter for LVDT, signal conditioning for low level DC & AC signals, concept of shielding, grounding & EMI

Reference Books:

2. Anvekar & Sonde, “Electronic Data Converters”, TMH
Low Power VLSI Design

Introduction: Need for low power VLSI chips, Sources of power dissipation on Digital Integrated circuits. Emerging Low power approaches, Physics of power dissipation in CMOS devices.

Device & Technology Impact on Low Power: Dynamic dissipation in CMOS, Transistor sizing & gate oxide thickness, Impact of technology Scaling, Technology & Device innovation

Power estimation, Simulation Power analysis: SPICE circuit simulators, gate level logic simulation, capacitive power estimation, static state power, gate level capacitance estimation, architecture level analysis, data correlation analysis in DSP systems, Monte Carlo simulation.

Probabilistic power analysis: Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy.

Low Power Design Circuit level: Power consumption in circuits. Flip Flops & Latches design, high capacitance nodes, low power digital cells library

Logic level: Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic

Low power Architecture & Systems: Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power arithmetic components, low power memory design.

Low power Clock Distribution: Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip & package co design of clock network


Reference Books:
Parallel Computer Models: The state of computing, Classification of parallel computers, Multiprocessors and multicomputers, Multivector and SIMD computers.

Program and Network Properties: Conditions of parallelism, Data and resource Dependences, Hardware and software parallelism, Program partitioning and scheduling, Grain Size and latency, Program flow mechanisms, Control flow versus data flow, Data flow Architecture, Demand driven mechanisms, Comparisons of flow mechanisms


Advanced Processors: Advanced processor technology, Instruction-set Architectures, CISC Scalar Processors, RISC Scalar Processors, Superscalar Processors, VLIW Architectures, Vector and Symbolic processors

Pipelining: Linear pipeline processor, nonlinear pipeline processor, Instruction pipeline Design, Mechanisms for instruction pipelining, Dynamic instruction scheduling, Branch Handling techniques, branch prediction, Arithmetic Pipeline Design, Computer arithmetic principles, Static Arithmetic pipeline, Multifunctional arithmetic pipelines

Memory Hierarchy Design: Cache basics & cache performance, reducing miss rate and miss penalty, multilevel cache hierarchies, main memory organizations, design of memory hierarchies.

Multiprocessor Architectures: Symmetric shared memory architectures, distributed shared memory architectures, models of memory consistency, cache coherence protocols (MSI, MESI, MOESI), scalable cache coherence, overview of directory based approaches, design challenges of directory protocols, memory based directory protocols, cache based directory protocols, protocol design tradeoffs, synchronization

Multithread and Dataflow Architecture: Principles of Multithreading, Scalable and Multithreaded Architecture, Dataflow Architecture

Reference Books:
Advanced Microcontrollers

<table>
<thead>
<tr>
<th>Subject Code</th>
<th>14ELD425</th>
<th>IA Marks</th>
<th>50</th>
</tr>
</thead>
<tbody>
<tr>
<td>No. of Lecture Hours /week</td>
<td>04</td>
<td>Exam Hours</td>
<td>03</td>
</tr>
<tr>
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<td>50</td>
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<td>100</td>
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Note: Microcontrollers have become prevalent in a number of applications such as instrumentation, industrial electronics, automotive electronics, robotics, etc. Advances in VLSI technology permit the integration of not only the processor but also the analog electronics, memory and peripherals necessary for system implementation; this allows low-cost system implementation. Some microcontrollers used in industrial electronics also provide some digital signal processing capability to further reduce the system cost.

Power dissipation is often a consideration in many systems and modern microcontrollers address it through the support of several low-power modes of operation. The aim of the course is to introduce advanced microcontrollers (16-bit and 32-bit).

**Motivation for advanced microcontrollers** – Low Power embedded systems, On-chip peripherals, low-power RF capabilities. Examples of applications.

**MSP430 – 16-bit Microcontroller family.** CPU architecture, Instruction set, Interrupt mechanism, Clock system, Memory subsystem, bus – architecture. The assembly language and „C” programming for MSP-430 microcontrollers. On-chip peripherals. WDT, Comparator, Op-Amp, Timer, Basic Timer, Real Time Clock (RTC), ADC, DAC, Digital I/O. Using the low-power features of MSP430. Clock system, low-power modes, Clock request feature, Low-power programming and interrupts.


**Applications** – Wireless Sensor Networking with MSP430 and Low-Power RF circuits; Pulse Width Modulation(PWM) in Power Supplies.

**Reference Books:**

4. Sample Programs for MSP430 downloadable from msp430.com