Syllabus of III to VIII Semesters B.E.
(With effect from 2018-19)

Electronics & Telecommunication Engineering

Visvesvaraya Technological University, Belagavi.
ವಿಶ್ವೇಶ್ವರಯ್ಯ ತಾಂತ್ರಿಕ ವಿಶ್ವವಿದ್ಯಾಲಯ, ಬೆಳಗಾವಿ

Visvesvaraya Technological University, Belagavi.

Regulations Governing the Degree of Bachelor of Engineering/
Technology (B.E./B.Tech.)
Under Outcome Based Education (OBE) & Choice Based Credit System (CBCS)

Effective from the Academic Year 2018 – 19

DEFINITIONS OF KEYWORDS

The following are the definitions/descriptions that have been followed for the different terms used in the Regulations of B.E./B.Tech. Programmes:

1) **Programme:** Is an educational programme in a particular stream/ branch of Engineering/branch of specialization leading to award of the Degree. It involves events/activities, comprising of lectures/ tutorials/ laboratory work/ field work, outreach activities/ project work/ vocational training/ viva voce/ seminars/ internship/ assignments/ presentations/ self-study etc., or a combination of some of these.

2) **Branch:** Means Specialization or discipline of B.E./B.Tech. Degree Programme, like Civil Engineering, Mechanical Engineering, Textile Engineering, etc.

3) **Semester:** Refers to one of the two sessions of an academic year (vide: serial number 4), each session being of sixteen weeks duration (with working days greater than or equal to ninety).The odd and even semesters shall be as per the University academic calendar.

4) **Academic Year:** Refers to the sessions of two consecutive semesters (odd followed by an even) including periods of vacation.

5) **Course:** Refers to usually referred to as 'papers' and is a component of a programme. All Courses need not carry the same weight. The Courses should define learning objectives and learning outcomes. A Course may be designed to comprise lectures/ tutorials/ laboratory work/ field work/ outreach activities/project work/ vocational training/ viva voce/ seminars/ term papers/assignments/ presentations/ self-study etc., or a combination of some of these.

6) **Credit:** Refers to a unit by which the Course work is measured. It determines the number of hours of instructions required per week. One credit is equivalent to one hour of lecture or two hours of laboratory/practical Courses/ tutorials/ fieldwork per week etc.

7) **Audit Courses:** Means the Knowledge/ Skill enhancing Courses without the benefit of a grade or credit for a Course.

8) **Choice Based Credit System (CBCS):** Refers to customizing the Course work, through Core, Elective and soft skill Courses, to provide necessary support for the students to achieve their goals.

9) **Course Registration:** Refers to formal registration for the Courses of a semester (Credits) by every student under the supervision of a Faculty Advisor (also called Mentor, Counsellor etc.,) in each semester for the Institution to maintain proper record.

10) **Course Evaluation:** Means Continuous Internal Evaluation (CIE) and Semester End Examinations (SEE) to constitute the major evaluations prescribed for each Course. CIE and SEE to carry 40 % and 60 % respectively, to enable each Course to be evaluated for 100 marks, irrespective of its Credits.

11) **Continuous Internal Evaluation (CIE):** Refers to evaluation of students' achievement in the learning process. CIE shall be by the Course Instructor and includes tests, homework, problem solving, group discussion, quiz, mini-project and seminar throughout the semester, with a weightage for the different components being fixed by the University.

12) **Semester End Examinations (SEE):** Refers to the examinations conducted by the University covering the entire Course Syllabus. For this purpose, Syllabi to be modularized and SEE questions to be set from each module, with a choice confined to the concerned module only. SEE is also termed as University examination.

13) **First Attempt:** Refers to a student who has completed all formalities and has become eligible to attend the SEE and has attended at least one head of passing, such attempt shall be considered as first attempt.

14) **Credit Based System (CBS):** Refers to quantification of Course work, after a student completes teaching – learning process, followed by passing in both CIE and SEE. Under CBS, the requirement for awarding degree is prescribed in terms of total number of credits to be earned by the students.

15) **Credit Representation:** Refers to the Credit Values for different academic activities considered, as per the Table.1. Credits for seminar, project phases, project viva–voce and internship shall be as specified in the Scheme of Teaching and Examinations.

Table 1: Credit Values				
Theory/ Lectures (L) (hours/week/ Semester)	Tutorials (T) (hours/week/ Semester)	Laboratory/Practical (P) (hours/week/Semester)	Credits (L:T:P)	Total Credits
4	0	0	4:0:0	4
3	0	0	3:0:0	3
2	2	0	2:1:0	3
2	0	2	2:0:1	3
2	2	2	2:1:1	4
0	0	6	0:0:3	3
NOTE: Activities like, practical training, study tour and participation in Guest lectures not to carry Credits.				

16) **Letter Grade:** It is an index of the performance of students in a said Course. Grades are denoted by letters S, A, B, C, D, E and F.

17) **Grading:** Grade refers to qualitative measure of achievement of a student in each Course, based on the percentage of marks secured in CIE and SEE. Grading is done by Absolute Grading [Refer: 18 OB

6.0]. The rubrics attached to letter grades are as follows:
S – Outstanding, A – Excellent, B – Very Good, C – Good, D – Above Average, E – Average and F – Fail.

18) **Grade Point (GP):** Refers to a numerical weightage allotted to each letter grade on a 10-point scale as under.

Letter Grade and corresponding Grade Points on a typical 10 – Point scale							
Letter	S	A	B	C	D	E	F
Grade	10	09	08	07	06	04	00

19) **Passing Standards:** Refers to passing a Course only when getting GP greater than or equal to 04 (as per serial number 18).
20) **Credit Point:** Is the product of grade point (GP) and number of credits for a Course i.e.,
   Credt points (CrP)=GP×Credits for the Course.
21) **Semester Grade Point Average (SGPA):** Refers to the measure of academic performance of student/s in a semester. [Refer:18 OB 6.2]
22) **Cumulative Grade Point Average (CGPA):** Is a measure of overall cumulative performance of a student over all semesters. [Refer:18OB6.2]
23) **Grade Card:** Refers to the certificate showing the grades earned by a student. A grade card shall be issued to all the registered students after every semester end examination. The grade card will display the Programme details (Course code, title, number of credits, grades secured) along with SGPA of that semester and CGPA earned till that semester.
24) **University:** Visvesvaraya Technological University (VTU), Belagavi.

Visvesvaraya Technological University, Belagavi.

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18OB1.0	**Title, Duration and Credits of the Programme of Study.**
18OB1.1	The Programme of study shall be called the degree of Bachelor of Engineering / Bachelor of Technology, abbreviated as B.E. / B.Tech.
18OB1.2	(a) The Programme to which students are admitted to First semester of B.E./B.Tech. Programme shall be of four academic year duration divided into eight semesters. The actual Teaching and Learning days shall be for at least 90 working days in a semester.
	(b) The Programme to which students are admitted to third semester of B.E./B.Tech. Programme under lateral entry shall be of three academic year duration, divided into six semesters. The actual Teaching and Learning days shall be at least 90 working days in a semester.
	(c) The Programme (conducted during evening) to which students are admitted to third semester of B.E./B.Tech. Programme under lateral entry scheme shall be of three academic year duration, divided into six semesters. The actual Teaching and Learning days shall be for at least 90 working days in a semester. The deficit contact hours of the Programme, conducted during evening on all working days, shall be compensated on all Sundays (except on general holidays).
18OB1.3	The calendar of events in respect of the Programme of study shall be notified by the University in advance.
18OB1.4	Maximum Duration for Programme Completion:
	(a) In case of students admitted to First semester of First year B.E./B.Tech. Programme
	(i) Students admitted to First year first semester B.E./B.Tech. shall complete the Programme within a period of eight academic years from the date of first admission, failing which they have to discontinue the Programme.
	(ii) A student who has not obtained eligibility to third semester even after three academic years from the date of first admission to first semester shall discontinue the Programme or get readmitted to first semester of first year B.E./B.Tech. with a revised University Seat Number having the same year of admission but serial number of the student starting with SIX hundred series (6XX).
	(iii) A student who has joined first year (to I or II semester) as a

	repeater and has not obtained eligibility to third semester even after three academic years from the date of readmission to first year shall discontinue the Programme or get readmitted to first semester of first year B.E./B.Tech., subject to the provision of 18OB1.4 (a)(i), with a revised University Seat Number having the same year of admission but serial number of the student starting with SIX hundred series (6XX).
(iv)	A student, who has been readmitted to First year as per [as per 18OB1.4 (a) (ii)and (iii)], does not get eligibility to third semester even after two academic years from the date of readmission, he/she shall discontinue the Programme or seek fresh admission following the prevailing admission procedure at that time.
(v)	A student who gets admitted to III semester from I year in three or less the three years shall complete the Programme, with or without break, within a period of eight academic years from the date of first admission, failing which they have to discontinue the Programme or seek fresh admission following the prevailing admission procedure at that time.
(b)	In case of lateral entry students admitted to Third semester of Second year B.E./B.Tech. Programme
(i)	Students admitted to second year third semester B.E./ B.Tech. shall complete the Programme within a period of six academic years from the date of first admission, failing which they have to discontinue the Programme.
(ii)	A student who has not obtained eligibility to fifth semester even after two academic years from the date of first admission to third semester shall discontinue the Programme or get readmitted to third semester of second year B.E./B.Tech. with a revised University Seat Number having the same year of admission but serial number of the student starting with SEVEN hundred series (7XX).
(iii)	A student who has joined second year (to III or IV semester) as a repeater and has not obtained eligibility to fifth semester even after three academic years from the date of readmission to second year shall discontinue the Programme or get readmitted to third semester of second year B.E./B.Tech., subject to the provision of 18OB1.4 (b) (i), with a revised University Seat Number having the same year of admission but serial number of the student starting with SEVEN hundred series (7XX).
(iv)	A student, who has been readmitted to second year as per [as per 18OB1.4 (b) (ii) and (iii)], does not get eligibility to fifth semester even after two academic years from the date of readmission to second year, he/she shall discontinue the Programme or seek fresh admission following the prevailing admission procedure at that time.

	(v) A student who gets admitted to V semester from II year in two or less the two years shall complete the Programme, with or without break, within a period of six academic years from the date of first admission, failing which they have to discontinue the Programme or seek fresh admission following the prevailing admission procedure at that time.
18OB1.5	Prescribed Number of Credits for the Programme [to be read along with 18OB12.2]: (a) The number of credits to be completed by students admitted to first semester of B.E./B.Tech. Programme shall be 175. (b) The number of credits to be completed by students admitted to third semester of B.E./B.Tech. Programme under lateral entry scheme shall be 135. (c) A student shall be eligible to get Undergraduate degree with Honours, if he/she earns additional 20 credits, as per VTU norms issued from time to time regarding the earning of additional credits.[To be read along with Regulations Governing the award of Honours' at B.E./B.Tech. Degree Programmes.]
18OB1.6	(a) Definition of Credits: (a.1) 1 hour Lecture (L) per week per semester = 1 Credit (a.2) 2 hour Tutorial (T) per week per semester = 1 Credit (a.3) 2 hour Practical/Laboratory/Drawing (P) per week per semester = 1 Credit. (a.4) Teaching – Learning hours for Credit Courses: (a.5) Four credit theory courses shall be designed for 50 hours of Teaching – Learning process. (a.6) Three credit theory courses shall be designed for 40 hours of Teaching – Learning process.
18OB2.0	**Eligibility for Admission to B.E./B.Tech. Programmes (As per the Government orders issued from time to time)**
18OB2.1	(a) Day Engineering College (Eligibility: Candidates who have Passed Second PUC/ Twelfth standard) (i) Passed Second PUC/12th standard/Equivalent examination with English as one of the Languages and obtained a minimum of 45 % of Marks in aggregate in Physics and Mathematics along with Chemistry/Bio-Technology/ Biology/ Electronics/ Computer. 40 % for SC, ST, Category – 1, 2A, 2B, 3A and 3B category candidates of Karnataka only. (ii) Those students, who have passed a qualifying examination other than the PUC II examination of the Pre-University Education Board of Karnataka, have to obtain eligibility certificate for seeking admission to B.E./B.Tech. Degree Programme from Visvesvaraya Technological University, Belagavi.

	(b) Day Engineering College (Eligibility: Candidates who have Passed 3 year Diploma)
	(i) A candidate who has passed any Engineering diploma examination or equivalent examination and obtained an aggregate minimum of 45 % marks taken together in all the subjects of the final year (Fifth and Sixth semester) diploma examination (qualified examination) is eligible for admission to B.E./B.Tech. Programmes,in respective branch of Engineering (as notified by the Government of Karnataka for admission to 3rd semester / 2nd year B.E./B.Tech.) and 40 % of marks in qualified examination in case of SC, ST and Backward Classes of Karnataka candidates.
	(ii) Those candidates who have completed Engineering Diploma from other than Karnataka state shall provide the Equivalence/ Eligibility Certificate issued from the Director of Technical Education, Karnataka.
	(c) Evening Engineering College (Eligibility: Candidates who have Passed 3 year Diploma):
	(i) A candidate who has passed any Engineering diploma examination or equivalent examination and obtained an aggregate minimum of 45 % marks taken together in all the subjects of the final year (Fifth and Sixth semesters) diploma examination (qualified examination) is eligible for admission to B.E./B.Tech. Programmes, in respective branch of Engineering (as notified by the Government of Karnataka for admission to 3rd semester / 2nd year B.E./B.Tech.) and 40 % of marks in qualified examination in case SC, ST and Backward Classes of Karnataka candidates.
	In addition to this a candidate after passing the diploma, must have minimum of Two years full-time work experience as on 1st September of the year of admission, in a registered firm/Company/Industry/Educational Institution /Government/Autonomous Organizations in the branch of Engineering/Technology, in which the candidates holds a diploma, and in which admission is sought by him/her.
	Professional experience refers to the experience earned as an employee on regular basis in Government, Government Undertaking, Public Sector Undertaking, Corporation or Private company registered under the Directorate of Industries and Commerce or the Directorate of Small Scale Industries or Government, Government recognized Institutions as technical staff.
	Provided that the period of apprenticeship undergone shall also be treated as professional experience , if sponsored by the Board of Apprenticeship Training, Southern Region, Chennai or by Government, Government Undertakings and Public Sector Undertakings.

	Note: In case where genuineness of the employment certificate is questionable, such candidates have to produce supportive documents specifying the registration details of the Industry/Company (e.g., SSI Registration) and or identity cards provided to them together with latest salary certificate and provident fund certificate. However, the employer has to fill up the NOC duly signed by the company authority.
	(d) Day Engineering College (Eligibility: Candidates who have Passed B.Sc Degree)
	Passed B.Sc. Degree from a recognized University as defined by UGC, with at least 45% marks (40% in case of candidates belonging to reserved category) and passed 10+2 examination with Mathematics as a subject.
	Note: A Faculty/ Employee working on Full Time basis in an Institution/ Organization and pursuing/ pursued any Full Time Course for the same duration as that of Regular Shift ("Single Shift/ Regular Shift" means where, educational activities of the Technical Institution are conducted between say, 9 am and 5 pm.) shall be considered as invalid for the purpose of employment/ higher studies.
	However, the Faculty/ Employee shall pursue a Programme (Course) as Part Time for longer duration, in the same City, only if, a University is offering a Part Time Programme for longer duration. [Page 74, 6.1, Chapter VI, Norms and Requirements, Approval Process Handbook 2019-20]
18OB2.2	With regard to the qualification earned from foreign countries, Equivalence certificate from the University/ Association of Indian Universities is mandatory for admission to B.E./B.Tech. Programmes. In case of any dispute about the equivalence in qualification earned from foreign countries, the decision of the University Equivalence Committee shall be the final in establishing the eligibility of the student.
18OB3.0	**Courses**
18OB3.1	There shall be the following types of Courses:
	(a) Humanities, Social Sciences and Management (HSMC): These are mandatory for all disciplines.
	(b) Basic Sciences (BSC): Physics, Chemistry and Mathematics. These are mandatory for all disciplines.
	(c) Engineering Sciences (ESC): Materials, Workshop, Drawing, and Basics of Electrical/ Electronics/ Instrumentation/ Civil/ Mechanical/ Computer Engineering etc. These are mandatory for all disciplines.
	(d) Professional Courses (PCC) – Core: Are the professional Core Courses, relevant to the chosen specialization/ branch. The core Courses are to be compulsorily studied by students

	and are mandatory to complete them to fulfill the requirements of a Programme.
	(e) Professional Elective Courses (PEC): Are the professional Electives, relevant to the chosen specialization / branch and can be chosen from the pool of papers. It shall be supportive to the discipline providing extended scope/enabling an exposure to some other discipline /domain and nurturing student proficiency skills.
	(f) Open Elective Courses (OEC): Are the Elective Courses from other technical areas and/ or from emerging fields.
	(g) Project Work (PROJ): Mini project and Main Project. Carried out at the Institution or elsewhere without affecting with the regular classwork.
	(h) Seminar: Deliverable at the Institution under the supervision of a Faculty.
	(i) Internship: Preferably at an industry/R and D organization/IT company/Government organization or elsewhere of significant repute for a specified period as mentioned in Scheme of Teaching and Examinations.
	(j) Mandatory Courses (MC): These Courses are mandatory, without the benefit of a grade or credit, for students admitted to B.E./B.Tech. Programme. A pass in each mandatory Course is required to qualify for the award of degree.
18OB3.2	The minimum number of students registered to any Elective Course offered by the Departments shall be not less than ten.
	However, the above condition shall not be applicable to Programmes having class strength of less than 10. In such cases, only one elective course shall be offered.
18OB3.3	A student shall exercise his option in respect of Elective Course/s and registered for the same at the beginning of the concerned semester. The student may be permitted to opt for a change of Elective Course/s within 15 days from the date of commencement of the semester as per the calendar of the University.
18OB3.4	**Course Registration:**
	In order to maintain proper academic record of each student at the Institution, every student shall register for the Courses of a semester (Credits) under the supervision of a Faculty Advisor (also called Mentor, Counselor, etc.,) in each semester.
18OB4.0	**Internship/Professional Practice**
18OB4.1	Internship / Professional Practice
	The Internship shall be completed during the period specified in the Scheme of Teaching and Examinations.
	1) The internship shall preferably be at an industry/R and D organization/IT company/ Government organization of

	significant repute for a specified period as mentioned in Scheme of Teaching and Examinations.
	2) The Department/college shall nominate staff member/s to facilitate, Guide and supervise students under internship.
	3) The students shall report progress of the internship to the Guide in regular intervals and seek his/her advice. The Guide shall maintain the progress record of the candidates undergoing internship.
	4) After the completion of Internship, students shall submit a report with completion certificate and attendance certificate to the Head of the Department with the approval of both internal and external Guides.
	5) There shall be 40 marks for CIE and 60 marks for SEE. The minimum requirement of CIE marks shall be 50% of the maximum marks.
	6) The internal Guide shall be the internal examiner for the SEE.
	7) The external Guide for Internship shall be the external examiner for SEE. Examination for internship shall be conducted at the college and the date shall be fixed in consultation with the external Guide. The Examiners shall jointly award the SEE marks. [To be read along with 18OB8.9 (f)]
	8) In case the external Guide expresses his inability to conduct the Examination, the Principal /Chief Superintendent of the Institute shall appoint a senior faculty of the Department to conduct the Examination along with the internal Guide.
	9) Non-availability of Internal guide due to inevitable situations for the conduct of SEE, the Principal /Chief Superintendent of respective institute shall appoint a senior faculty of the Department to conduct the Examination.
	10) The students are permitted to carry out the internship anywhere in India or abroad. The University will not provide any kind of financial assistance to any student for carrying out the Internship.
18OB 5.0	**Technical Seminar and Project**
18 OB 5.1	Technical Seminar: Technical Seminar is one of the head of passing.
	(i) Each candidate shall deliver Technical seminar as per the Scheme of Teaching and Examinations on the topic chosen from the relevant field.
	(ii) The Head of the Department shall make arrangements for the conduct of seminars through concerned faculty members of the Department. The committee, constituted for the purpose by the Head of the Department, shall award the CIE marks for the seminar. The committee shall consist of two senior faculty members of the Department and the senior most acting as the

	Chairperson. [To be read along with 18OB8.2 (e)]
18OB 5.2	Project: Project (Mini and Main) is one of the head of passing. Mini Project Work and Main Project Work shall preferably be batch wise, the strength of each batch shall not exceed a maximum of four students. [To be read along with 18OB 8.2 (f), (g) 18OB8.9 (f) and the details mentioned in Scheme of Teaching and Examinations.]
18OB 5.3	Examinations in Mini Project Work and Main Project Work shall be conducted batch-wise.
18OB 6.0	**Computation of SGPA and CGPA**
18OB 6.1	(i) The University adopts absolute grading system wherein the marks are converted to grades, and every semester results shall be declared in terms of Semester Grade Point Average (SGPA) considering all the courses appeared in that Semester End Examinations including backlog course/s/arrear papers (refers to courses other than the current semester courses that have not yet been completed), and Cumulative Grade Point Average (CGPA). The CGPA will be calculated for every semester, except for the first semester. (ii) The grading system with the letter grades and the assigned range of marks under absolute grading system shall be as given below:

Level	Outstanding	Excellent	Very Good	Good	Above Average	Average	Fail
Letter Grade	S	A	B	C	D	E	F
Grade Points	10	9	8	7	6	4	00
Percentage of Marks Scored in a Course	≥ 90	<90 ≥80	< 80 ≥70	< 70 ≥60	< 60 ≥ 45	< 45 ≥40	< 40
	(90 -100)	(80 - 89)	(70 - 79)	(60 - 69)	(45 - 59)	(40 - 44)	(0 - 39)

	(iii) A student obtaining Grade F in a Course shall be considered fail and is required to reappear in the subsequent SEE. Whatever the letter grade secured by the student during his /her reappearance shall be awarded. The number of attempts taken to clear Course/s shall be indicated in the grade card.
18OB6.2	Computation of SGPA and CGPA The following expressions shall be used to compute the Semester Grade Point Average (SGPA) and Cumulative Grade Point Average (CGPA) respectively:

The following expressions shall be used to compute the Semester Grade Point Average (SGPA) and Cumulative Grade Point Average (CGPA) respectively:

$$SGPA = \frac{\sum[Course\ Credits\ \times Grade\ Points]\ for\ all\ the\ Courses\ in\ that\ Semester}{\sum[Course\ Credits\ ]\ for\ all\ the\ Courses\ in\ that\ Semester}$$

$$CGPA = \frac{\sum[Course\ Credits\ \times Grade\ Points]\ for\ all\ Courses\ excluding\ those\ with\ F\ grades\ until\ that\ Semester}{\sum[Course\ Credits\ ]\ for\ all\ Courses\ excluding\ those\ with\ F\ grades\ until\ that\ semester}$$

The SGPA and CGPA shall be rounded off to 2 decimal points and reported in the grade cards.

(a) SGPA and CGPA Calculations: An Illustrative Example for one academic year						
(Odd :I, Semester Even: II)	Course Code	Credits	Grade	Grade Points	Credit Points	SGPA, CGPA
I	XX101	5:0:0 = 5	B	8	5 × 8 = 40	$SGPA = \frac{117}{25}$ = **4.68**
I	XX102	3:2:0 = 5	Absent(F)	0	5 × 0 = 00	
I	XX103	3:0:0 = 3	A	9	3 × 9 = 27	
I	XX104	0:1:1 = 2	F	0	2 × 0 = 00	
I	XX105	4:1:0 = 5	D	6	5 × 6 = 30	
I	XX106	5:0:0 = 5	E	4	5 × 4 = 20	
	Total	25 (18*)	Total		117	

(18*): Total credits of the semester excluding the credits of the courses under F grade. Considered for the calculation of CGPA of the two consecutive semesters under consideration.

II	XX107	3:1:1 = 5	C	7	5 × 7 = 35	$SGPA = \frac{157}{25}$ = **6.28**
II	XX108	4:0:0 = 4	B	8	4 × 8 = 32	
II	XX109	3:0:0 = 3	D	6	3 × 6 = 18	
II	XX110	4:1:0 = 5	E	4	5 × 4 = 20	
II	XX111	2:1:1 = 4	A	9	4 × 9 = 36	CGPA $= \frac{(117 + 157)}{18 + 23}$ = 274/41 = **6.68**
II	XX112	2:0:0 = 2	F	0	2 × 0 = 00	
II	XX113	0:2:0 = 2	B	8	2 × 8 = 16	
	Total	25 (23*)	Total		157	

(23*): Total credits of the semester excluding the credits of the courses under F grade. Considered for the calculation of CGPA of the two consecutive semesters under consideration.

If the Student secures letter grades as detailed below after reappearance to SEE, then the SGPA and CGPA shall be calculated as indicated below.

I	XX102	3:2:0 = 5	D	6	5 × 6 = 30	SGPA (I Semester) $= \frac{(117 + 30 + 14)}{25}$ = 161/25 = **6.44**
I	XX104	0:1:1 = 2	C	7	2 × 7 = 14	
II	XX112	2:0:0 = 2	D	6	2 × 6 = 12	SGPA (II Semester) = (157 + 12)/25 = 169/25 = **6.76**

(b) CGPA Calculation of the Programme: An Illustrative Example								
Semester	I	II	III	IV	V	VI	VII	VIII
Credits of the semester	20	20	24	24	25	24	20	18
SGPA	7.00	8.50	9.20	6.86	8.18	7.73	8.68	9.40
CGPA $= \frac{20 \times 7.00 + 20 \times 8.50 + 24 \times 9.20 + 24 \times 6.86 + 25 \times 8.18 + 24 \times 7.73 + 20 \times 8.68 + 18 \times 9.40}{175}$ = **8.16**								

180B6.3	Grade Card: Based on the secured letter grades, grade points, SGPA and CGPA, a grade card for each semester and a consolidated grade card indicating the performance in all semesters shall be issued.
18OB7.0	**Conversions of CGPA into Percentage of marks and Class Equivalence**
18OB7.1	Formula for the conversion of CGPA into percentage of marks. Percentage of marks secured, $P = [CGPA\ Earned - 0.75] \times 10$ Illustration for a CGPA of 8.20: $P = [CGPA\ Earned\ 8.20 - 0.75] \times 10 = 74.5\%$
18OB7.2	Class Equivalence: Subsequent to the conversion of final CGPA, after successful completion of the Programme, into percentage of marks (P), a graduating student is reckoned to have passed in (i) First Class with Distinction (FCD) if $P \geq 70\%$ (ii) First Class (FC) if $P \geq 60\%$ but $<70\%$ and (iii) Second Class (SC) if $P < 60\%$.
18OB8.0	**Continuous Internal Evaluation, Semester End Evaluation and Minimum CIE and SEE Marks**
18OB8.1	Continuous Internal Evaluation Marks and Minimum CIE Marks: (a) For Vyavaharika Kannada (Balake Kannada)/Aadalitha Kannada (Samskruthika Kannada) the maximum CIE marks shall be 100. For the award of credit, the minimum CIE marks to be secured shall be 40 % of the maximum marks i.e., 40 marks. (b) For Project work phase -1 and Technical seminar the maximum CIE marks shall be 100. For the award of credit, the minimum CIE marks to be secured shall be 50 % of the maximum marks i.e., 50 marks. (c) For Practical/ Mini-project/Internship/Project work– Phase 2 the maximum CIE marks shall be 40. To appear for the SEE, the minimum CIE marks to be secured shall be 50 % of the maximum marks i.e., 20 marks. (d) For all other theory Courses of the Programme, the maximum CIE marks shall be 40. To appear for the SEE, the minimum CIE marks to be secured shall be 40 % of the maximum marks i.e., 16 marks. (f) For Additional Mathematics I and II (to be completed by diploma lateral entry students) the maximum CIE marks shall be 40. To appear for the SEE, the minimum CIE marks to be secured shall be 40 % of the maximum marks i.e., 16 marks. (g) For Engineering Graphics and Elements of Civil Engineering and Mechanics (of First Year Engineering and to be completed by B.Sc graduates under lateral entry)the

	maximum CIE marks shall be 40. To appear for the SEE, the minimum CIE marks to be secured shall be respectively 50 % and 40 % of the maximum marks i.e., 20 and 16 marks.
18OB8.2	Continuous Internal Evaluation Procedure: [To be read along with 18 OB 8.1and 8.3]
	(a) Theory Courses:
	(i) CIE Marks in each theory Course [including 'Technical English I and II', 'Constitution of India, Professional Ethics and Cyber Law', 'Environmental Studies', 'Additional Mathematics I and II'], shall be the sum of marks prescribed for tests and assignments. Marks prescribed for tests shall be 30 and that for assignments 10.
	(ii) The CIE marks awarded for tests in the theory Courses shall be based on three tests generally conducted at the end of fifth, tenth and fifteenth week of each semester. Each test shall be conducted for a maximum of 50 marks and the final test marks shall be the average of three tests, proportionately reduced to a maximum of 30 marks.
	(iii) The remaining 10 marks shall be awarded based on the evaluation of assignments/unit tests/written quizzes that support to cover both lower and higher order thinking skills as per Revised Bloom's Taxonomy.
	(iv) Final CIE marks awarded shall be the sum of 18OB8.2
	(a) (ii) and (iii) for a maximum of 40 marks.
	(v) The candidates shall write the tests, assignments/unit-tests /written quizzes in Blue Books which shall be preserved by the Principal/ Head of the Department for at least six months after the announcement of University results and shall be made available for verification at the direction of the Registrar (Evaluation).
	(b) Engineering Graphics/ Drawing/Fieldwork Courses:
	The CIE marks awarded for I year Engineering Graphics Course shall be based on
	(i) Classwork for 24 marks (sketching and Computer Aided Engineering Drawing).
	(ii) Two Tests conducted in the same pattern as that of SEE for 16 marks (The marks secured can be taken as best of the two tests).
	(iii) Final CIE marks awarded for Engineering Graphics shall be the sum of 18OB8.2 (b) (i) and (ii) for a maximum of 40 marks.
	(iv) The CIE marks awarded for higher semester Drawings/ Design Drawings offered by various branches shall be based on the evaluation of the sheets and one test in the ratio 60:40.

(v) The CIE marks awarded for field work (like Surveying Practice) shall be based on the evaluation of the associated field work and one test in the ratio 60:40.

(c) Practical Courses:

The CIE marks awarded in case of Practical, shall be based on the weekly evaluation of laboratory journals/ reports after the conduction of every experiment and one practical test in the ratio 60:40.

(d) Internship:

The CIE marks awarded for internship shall be based on the evaluation of Internship Report, Presentation skill and Question and Answer session in the ratio 50:25:25.

(e) Technical Seminar

The CIE marks awarded for Technical Seminar shall be based on the evaluation of Seminar Report, Presentation skill and Question and Answer session in the ratio 50:25:25.

(f) Mini - Project

The CIE marks awarded for Mini - Project, shall be based on the evaluation of Mini - Project Report, Project Presentation skill and Question and Answer session in the ratio 50:25:25. The marks awarded for Mini - Project report shall be the same for all the batch mates.

(g) Main Project Work

(i) Project Work Phase – 1

The CIE marks awarded for project work phase -1 shall be based on the evaluation of project work phase -1 Report, Project Presentation skill and Question and Answer session in the ratio 50:25:25. The marks awarded for the Project report shall be the same for all the batch mates.

(ii) Project Work Phase - 2

The CIE marks awarded for project work phase -2 shall be based on the evaluation of project work phase -2 Report, Project Presentation skill and Question and Answer session in the ratio 50:25:25. The marks awarded for Project report shall be the same for all the batch mates.

(h) Vyavaharika Kannada (Balake Kannada)/Aadalitha Kannada (Samskruthika Kannada)

(i) CIE Marks in Vyavaharika Kannada (Balake Kannada)/Aadalitha Kannada (Samskruthika Kannada) shall be the sum of marks prescribed for tests and assignments. Marks prescribed for tests shall be 75 and that for the assignments be 25.

	(ii) The CIE marks awarded for the tests shall be based on three tests generally conducted at the end of fifth, tenth and fifteenth week of each semester. Each test shall be conducted for a maximum of 25 marks and the final CIE marks shall be the sum of the marks of all the three tests.
	(iii) The remaining 25 marks shall be awarded based on the evaluation of assignments/oral discussions/ quizzes that supports communication skills.
	(iv) Final marks awarded shall be the sum of 18OB8.2 (h) (ii) and (iii) for a maximum of 100 marks.
	(v) Students shall write the tests in Blue Books and complete the exercises/activates/ questions given in the University Kannada textbook. These shall be preserved by the Principal/ Head of the Department for at least six months after the announcement of University results and shall be made available for verification at the direction of the Registrar (Evaluation).
18OB8.3	(a) The CIE marks in the case of Internship/Technical Seminar/Mini-Project and Project Work Phase 1 and 2 shall be awarded by a committee consisting of the Head of the concerned Department and two senior faculty members of the Department, one of whom shall be the Guide.
	(b) A committee constituted by the Head of the Department of Humanities and Social Science shall inspect and authenticate the award the CIE marks for the Course Vyavaharika Kannada (Balake Kannada)/Aadalitha Kannada (Samskruthika Kannada). The committee shall consist of two senior faculty members of the Department and the senior most acting as the Chairperson.
18OB8.4	(i) Students satisfying the attendance requirement but failing to secure the minimum percentage of CIE marks, in any Course/s, shall not be eligible for the SEE conducted by the University and they shall be considered as fail in that Course /those Courses. However, they can appear for University examinations conducted in other Courses of the same semester and backlog Course/s if any.
	(ii) Students who have satisfied the attendance requirement but not the CIE requirements shall be permitted to register afresh and appear for SEE after satisfying the CIE requirements in the same Course/s (with or without satisfying the attendance requirement) when offered during subsequent semester/s.
	(iii) Each appearance to SEE to complete a course shall be treated as an attempt.
18OB8.5	CIE marks of those students, who come under 18OB8.4, shall also be sent to the Registrar (Evaluation) along with other course CIE Marks.

18OB8.6	(i) The final list, incorporating corrections (if any), of CIE marks awarded to the students in the Theory/Practical/Internship/ Technical Seminar / Mini – Project/Project work –phase 1 and 2, shall be displayed on the notice board of the college much before the closure of the semester.
	(ii)The institution shall enter the CIE marks of each semester in the format of the VTU online CIE marks portal and submit a certified copy of the same to the University Examination Section within the stipulated date notified by University. Every page of the CIE marks sheet (hardcopy) shall bear the signatures of the concerned Teacher/Teachers, Head of the Department and Principal.
18OB8.7	Any corrections or overwriting of CIE marks shall bear the signature(s) of concerned Teacher(s) and in such cases the Head of the Department shall indicate the number of corrections on every sheet and attest it with his/her signature.
18OB8.8	CIE marks shall reach the University before the commencement of examination as per the notification from the office of the Registrar (Evaluation) from time to time. After the submission of CIE marks to the University, any request under any circumstances for change of CIE marks shall not be considered.
18OB8.9	Semester End Examination Marks and Passing standards
	(a) University examination for all Courses under SEE shall be conducted for a maximum of 100 Marks. The marks secured by the students for 100 marks shall be proportionately reduced to a maximum of 60 marks to add the same with the CIE marks for the award of letter grade.
	(b) The University examinations for all the Programmes of study shall be conducted at the end of each semester for all the eight semesters.
	(c) Students having no backlog course/s, may not have more than one examination on the same day. However, students having backlog course/s may face a situation where they may have
	(i) Two examinations scheduled at the same time of the day,
	(ii) to take two examinations on the same day, one during the morning session and the other in the afternoon session, and
	(iii) Examinations on consecutive days.
	As changing the examination dates is not an option, the examination timetable shall not be modified/ altered/ adjusted in any of the above three cases. In the first case, the students shall select any one of the clashing courses and in second and third cases, the students shall manage the examinations as per their decision.
	(d) The pattern of the SEE question paper for Courses Technical English I and II, Constitution of India, Professional Ethics and Cyber Law, and Environmental Studies shall be objective type [Multiple Choice Questions (MCQ)].

	(e) For a pass in a theory Course/Drawing, students shall secure a minimum 35 % of the maximum marks prescribed for the University examination and in total 40 % of the Course maximum marks, i.e., the sum of the CIE and SEE marks prescribed for the Course. (f) For a pass in Practical/ Mini-project / Internship/Technical Seminar/Project work, students shall secure a minimum of 40 % of the Course maximum marks prescribed for the University examination (SEE). (g) Students who satisfy the conditions 18OB8.9 (e) and (f), and obtain any grade from S to E in a Course shall be considered to have passed that Course. (h) A student shall be declared fail if the candidate (h.a) Fails to satisfy the conditions 18OB8.9 (g). (h.b) Absents himself / herself to the University examination. (h.c) Is held guilty of examination malpractice and for any other reasons, and declared the performance of any Course/s null and void by a competent authority. (i) If a student secures F grade in any of the Course/s, he/she shall reappear for that Course/s during the subsequent SEE. The CIE marks awarded to the student at first attempt in the concerned Course/s shall be carried forward. Revised CIE marks is considered only in cases under the provision of 18OB8.4 (ii).
18OB8.10	Students who pass a Course of a semester as per 18OB8.9 (g) shall not be allowed to appear for any individual Course again, unless they opt for rejection of results of entire semester. However, students who have CGPA less than 5.00 at the end of academic Programme, subject to the provision 18OB1.4, shall be allowed to appear for only SEE of Course/s to make up the deficiency in CGPA.
18OB8.11	A student may, at his/her desire, can reject the total performance of a semester (including CIE marks) or reject only the result of his/her performance in University examinations of a semester. The rejection is permitted only once during the entire Programme of study.
18OB8.12	Students who desire to reject the SEE results of a semester shall reject the total performance (irrespective of the earned Course grades) in all the Courses of the semester either rejecting or retaining the CIE marks. However, rejection of the performance of VIII semester project shall not be permitted. (i) Students, who desire to reject the total SEE performance of an odd or even semester including CIE marks, have to repeat that odd or even semester of the prevailing scheme by taking readmission during the subsequent academic year/s. They shall also be governed by 18OB 12.1, 12.2 and 1.4.

	(ii) If the rejection of SEE results excluding CIE marks is of odd semester, students shall be allowed to take admission to the immediate next even semester.
	(iii) If the rejection of SEE results excluding CIE marks is of even semester, then students shall not be allowed to take admission to the next odd semester as per 18OB10.3. In such cases, students shall take admission to the next odd semester of the prevailing scheme during the subsequent academic year/s, after obtaining the eligibility to move to higher semester. They shall also be governed by 18OB 12.1, 12.2 and 1.4.
	(iv) Readmission to odd/even semester as per 18OB8.12 (i)and (iii) shall not be considered as fresh admission and therefore students shall continue to have the same University Seat Number, which was allotted earlier. The maximum duration of the programme (as per 18OB1.4) shall be counted with reference to old University Seat Number.
	(v) Applications for rejection and approval to reappear for University examinations shall be sent to the Registrar (Evaluation) through the Principal of the College within 30 days from the date of announcement of the results. Late submission of applications shall not be accepted for any reasons.
	(vi) Application for approval of readmission shall be sent to the Registrar through the Principal of College within 30 days from the date of the announcement of the results. Late submission of application shall not be accepted for any reasons.
18OB8.13	Students who opt for rejection of results of University examination shall be eligible for the award of degree and not for the award of ranks and Honours Degree.
18OB9.0	**Attendance Requirement**
18OB9.1	Each semester shall be considered as a unit for calculation of the attendance and the Candidates have to put in a minimum attendance of 85% in each Course with a provision of condonation of 10% of the attendance by the Vice-Chancellor on the specific recommendations of the Principal of the college where the candidate is studying, based on medical grounds, participation in University/State/ National/ International level sports and cultural activities, seminars, workshops, paper presentation etc., of significant value. The supporting documents for condoning the shortage of attendance shall be submitted along with the recommendations.
18OB9.2	(a) The basis for the calculation of attendance shall be the period prescribed by the University by its calendar of events and as notified by the Registrar (Evaluation) from time to time.

	(b) In case of late admissions, approved by competent authority (DTE/VTU), to I semester/ III semester (lateral entry scheme) of day college/III semester (lateral entry scheme) of Engineering Programme conducted during evening, the attendance shall be reckoned from the date of admission to the Programme.
18OB9.3	The Course Instructor/ Mentor/College shall inform the students as well as their parents /guardians about the attendance status periodically. Students who are facing the shortage of attendance shall be mentored to make up the shortage. Principals shall also notify every month, the list of candidates who are under short of attendance.
18OB9.4	A candidate, who does not satisfy the attendance requirement (in one or more Courses and including the Courses Additional Mathematics I and II) as mentioned in 18OB 9.1 shall not be eligible to appear for the Semester End Examinations of that semester and shall not be permitted to take admission to next higher semester. The candidate shall be required to repeat that semester during the subsequent year.
18OB10.0	**Vertical Progression (Promotion/ Eligibility to higher semesters)**
18OB10.1	There shall be no restriction for promotion from an odd semester to the next even semester, provided the student has fulfilled the attendance requirement.
18OB10.2	Along with the reasons specified at 18OB8.9 (h), a student shall be declared fail if he/she
	(i) Has not satisfied the CIE requirements of any Course/s.
	(ii) Has not registered for the SEE even after satisfying the attendance and CIE requirements.
18OB10.3	(A) Vertical Progression in case of students admitted to First year:
	(a) Students having not more than four F grades in the two semesters of first year of the Programme shall be eligible to move to second year.
	(a.1) Students having not more than four F grades in the four semesters of I and II year shall be eligible to move to III year.
	(a.2) Student who have earned all the prescribed credits of I year, and having not more than four F grades in the four semesters of II and III year shall be eligible to move to IV year.
	(B) Vertical Progression in case of Diploma students admitted to Second year (lateral entry)
	(a) Students having not more than four F grades (excluding the Fail or pass status of Additional Mathematics I and II) in the two semesters of II year of the Programme shall be eligible to move to III Year.

(a.1)	Students having not more than four F grades (excluding the Fail or pass status of Additional Mathematics I and II, if any) in the four semesters of II and III year shall be eligible to move to IV year.
(b)	The mandatory non – credit Courses Additional Mathematics I and II prescribed at III and IV semesters respectively, to lateral entry Diploma holders admitted to III semester of B.E./B.Tech. Programmes, shall attend the classes during the respective semesters to satisfy attendance and CIE requirements and to appear for the University examinations.
(i)	In case, any student fails to satisfy the attendance requirement of the Courses Additional
	Mathematics I and II, he/she shall not be eligible to appear for the Semester End Examinations of that semester and shall not be permitted to take admission to next higher semester. The candidate shall be required to repeat that semester during the subsequent year.
(ii)	Students who have satisfied the attendance requirement but not the CIE requirements of the Courses Additional Mathematics I and II shall be permitted to register afresh and appear for SEE after satisfying the CIE requirements in the same Course/s (with or without satisfying the attendance requirement) when offered during subsequent semester/s.
(c)	Completion of Additional Mathematics I and II, shall be mandatory for the award of degree.
(C)	Vertical Progression in case of B.Sc students admitted to Second year (lateral entry)
(a)	Students having not more than four F grades (excluding the Fail or pass status of Engineering Graphics and Design, and Civil Engineering and Mechanics of First Year Engineering Programme) in the two semesters of II year of the Programme shall be eligible to move to III Year.
(a.1)	Students having not more than four F grades (excluding the Fail or pass status of Engineering Graphics and Design, and Civil Engineering and Mechanics of First Year Engineering Programme, if any) in the four semesters of II and III year shall be eligible to move to IV year.
(b)	The prescribed mandatory non – credit Courses Engineering Graphics and Design, and Civil Engineering and Mechanics of First Year Engineering Programme to lateral entry B.Sc. holders admitted to III semester of B.E./B.Tech. Programmes, shall attend the classes during the respective semesters to complete CIE and attendance requirements and to appear for the University examinations.
(i)	In case, any student fails to satisfy the attendance requirement of the above said Courses, he/she shall not be eligible to appear for the Semester End Examinations of that semester

	and shall not be permitted to take admission to next higher semester. The candidate shall be required to repeat that semester during the subsequent year.
	(ii) Students who have satisfied the attendance requirement but not the CIE requirements of the above said Courses, shall be permitted to register afresh and appear for SEE after satisfying the CIE requirements in the same Course/s (with or without satisfying the attendance requirement) when offered during subsequent semester/s.
	(c) Completion of Engineering Graphics and Elements of Civil Engineering and Mechanics shall be mandatory for the award of degree.
	The Principal of each college shall make suitable arrangements in the timetable to facilitate the B.Sc students to attend the above mentioned courses to satisfy the CIE and attendance requirements and to appear for the University examinations.
18OB11.0	**Award of Degree**
18OB11.1	1. B.E./B.Tech. degree
	(a) Students shall be declared to have completed the Programme of B.E. / B.Tech. degree and is eligible for the award of degree, provided the students have undergone the stipulated Course work of all the semesters under the Scheme of Teaching and Examinations and has earned the prescribed number of credits as per the provision 18OB1.5. [To be read along with 18 OB 12.1 and 12.2]
	(b) For the award of degree, a CGPA ≥ 5.00 at the end of Programme shall be mandatory. [To be read with 18OB11.2 (1)]
	(c) Completion of Additional Mathematics I and II, shall be mandatory for the award of degree to lateral entry diploma students.
	(d) Completion of Engineering Graphics and Elements of Civil Engineering and Mechanics of First Year Engineering Programme shall be mandatory for the award of degree to lateral entry B.Sc graduates.
	(e)(i) Over and above the academic credits, every Day College regular student admitted to the 4 years Degree Programme and every student entering 4 years Degree Programme through lateral entry, shall earn 100 and 75 Activity Points respectively through AICTE Activity Point Programme for the award of degree. Students transferred from other Universities/ Autonomous colleges under VTU to fifth semester are required to earn 50 Activity Points from the year of entry to VTU. The Activity Points earned shall be reflected on the student's eight semester Grade Card.

	(ii) Activity Points (non-credit) have no effect on SGPA/CGPA and shall not be considered for vertical progression.
	In case students fail to earn the prescribed activity Points before the commencement of 8th semester examinations, Eighth semester Grade Card shall be issued only after earning the required activity Points. Students shall be admitted for the award of degree only after the release of the Eighth semester Grade Card.
	2. B.E./B.Tech. (Honours) degree
	(a) A student shall be declared to have completed the Programme of B.E. / B.Tech. degree and shall be eligible to get undergraduate BE/B.Tech degree with Honours, provided
	(i) The student has undergone the stipulated Course work of all the semesters under the same Scheme of Teaching and Examinations and has earned the prescribed number of credits as per the provision 18 OB1.5 (a) and (b).
	(ii) Has earned additional 20 or more credits through University approved online Courses.
	(iii) Satisfies the Regulations Governing the award of Honours at B.E./B.Tech. Degree Programmes.
18OB11.2	(1)Noncompliance of CGPA at the end of the Programme
	(a) Students who have completed all the courses of the Programme but not having a CGPA ≥ 5.00 at the end of the programme, shall not be eligible for the award of the degree.
	(b) In the cases of 18OB11.2 (1) (a), students shall be permitted to appear again for SEE in course/s [other than Internship, Technical seminar, Project (Mini and Main), and Laboratories] of any Semester/s without the rejection of CIE marks for any number of times, subject to the provision of maximum duration of the Programme to make up the CGPA equal to or greater than 5.00 for the award of the Degree.
	(c) In case, the students earn improved grade/s in all the reappeared course/s, the CGPA shall be calculated considering the improved grade/s. If it is ≥ 5.00, the students shall become eligible for the award of the degree. If CGPA <5.00, the students shall follow the procedure laid in 18OB11.2(1) (b).
	(d) In case, the students earn improved grade/s in some course/s and the same or lesser than the previously earned pass grade/s in the other reappeared course/s, the CGPA shall be calculated considering the improved grade/s and the pass grades earned before the reappearance. If it is ≥ 5.00, the students shall become eligible for the award of the degree. If CGPA <5.00, the students shall follow the procedure laid in 18OB11.2 (1) (b).

	(e) In case, the students earn improved grade/s in some courses and fail in the other reappeared course/s, the CGPA shall be calculated by considering the improved grade/s and the previously earned pass grade/s of the reappeared course/s in which the students have failed. If it is ≥ 5.00, the students shall become eligible for the award of the degree. If CGPA <5.00, the students shall follow the procedure laid in 18OB11.2 (1) (b).
	(f) In case, the students fail (i.e., earns F grade) in all the reappeared course/s, pass grade/s of the course/s earned by the students before reappearance shall be retained. In such cases, the students shall follow the procedure laid in 18OB11.2 (1) (b).
	(g) Students shall obtain written permission from the Registrar (Evaluation) to reappear in SEE to make up the CGPA equal to or greater than 5.00.
	(2) Noncompliance of Mini-project
	(a) The mini-project shall be considered as a head of passing and shall be considered for the award of degree. Those, who do not take-up/complete the mini-project shall be declared fail in that course and shall have to complete the same during subsequent University examinations after satisfying the Mini-project requirements. Also, mini-project shall be considered for eligibility to VII semester.
	(3) Noncompliance of Internship
	(a) All the students of B.E./B.Tech. shall have to undergo mandatory internship of 4 weeks during the vacation of VI and VII semesters and /or VII and VIII semesters. A University examination shall be conducted during VIII semester and the prescribed credits shall be included with the credits of VIII semester. Internship shall be considered as a head of passing and shall be considered for the award of degree. Those, who do not take-up/complete the internship shall be declared fail in that Course and shall have to complete the same during subsequent University examinations after satisfy the internship requirements.
18OB12.0	**Temporary Discontinuation/Break in the Programme/Change in Scheme of Study**
18OB12.1	**(a)** If a candidate, for any reason, temporarily discontinues the Programme or take a break from the Programme during any semester intentionally, he/she shall be permitted to continue the Programme by registering to the same semester of the prevailing scheme. The candidate, from that semester, shall attend and complete all the remaining Course works of all the semesters, adhering to the regulations of the prevailing

		scheme and subject to the provision 18OB1.4. Also the Candidates may have to complete additional Course/s, if any, as per the decision of concerned Board of Studies on establishing the equivalence between two schemes. A Grade card shall be issued to that effect. Additional Course/s shall not be considered for the eligibility criteria prescribed for promotion. Based on the individual cases, they shall be considered to decide the SGPA and CGPA to admit the student for the award of degree. Such candidates shall not be eligible for the award of rank / Honours degree.
	(b)	Candidates who take admission to any semester of the existing scheme from another scheme, as a repeater/fresher because of various reasons, shall attend and complete all the remaining semester/s of the Programme adhering to the regulations of the prevailing scheme, and shall complete additional Course/s, if any, as per the decision of concerned Board of Studies on establishing the equivalence between two schemes. A Grade card shall be issued to that effect. Additional Courses shall not be considered for the eligibility criteria prescribed for promotion. Based on the individual cases, they shall be considered to decide the SGPA and CGPA to admit the student for the award of degree. Such candidate shall not be eligible for the award of rank/Honours Degree.
	(c)	The credits to be earned by the candidates under 18OB12.1 (a and b) and 18OB14.1(b) and (c) shall be decided by the University along with the additional Course/s to be completed.
18OB12.2	(i)	The candidates who have temporarily discontinued the Programme of study or changed the scheme of study from one to another because of various reasons, or transferred from autonomous/other University to non-autonomous VTU constituent/affiliated college, shall be eligible for the award of degree provided the credits earned is equal to or greater than the credits decided by the University in the individual cases.
	(ii)	In case, the credits earned is less than the credits decided by the University in the individual cases, after the completion of all the semesters of the Programme under the prevailing scheme, the candidate shall register for a Course or courses not studied earlier and make up the credits earned equal to or greater than the required for the award of degree.
	(iii)	If the earned Programme credits are greater than the prescribed, the CGPA shall be proportionately reduced to the prescribed Programme credits.
18OB13.0	**Award of Prizes, Medals and Ranks**	
18OB13.1	For the award of Prizes and Medals, the conditions stipulated by the	

		Donor shall be considered subject to the provisions of the statutes framed by the University for such awards.
18OB13.2	(1)	For award of rank in a Specialization of Bachelor of Engineering/ Technology, the CGPA secured by the students from III to VIII semester shall be considered.
	(2)	The additional credits earned for the award of Honours degree shall not have any bearing for the Rank declaration.
	(3)	A student shall be eligible for a rank at the time of award of degree of Bachelor of Engineering/ Technology, provided that the student,
	(a)	(i) Has passed all the Courses of I to VIII semester in first attempt only in case of Candidates admitted to I year.
	(ii)	Has passed all the Courses (including Additional Mathematics I and II in case Diploma students/ Engineering Graphics and Elements of Civil Engineering and Mechanics in case of B.Sc graduates under lateral entry) of III to VIII semester in first attempt only in case of Candidates admitted under lateral entry scheme.
	(b)	Is not a repeater in any semester because of rejection of result of a semester/ shortage of attendance etc.
	(c)	Has completed all the Courses/semesters of the same Scheme of Teaching and Examinations without any break/discontinuity.
	(d)	Has completed all the semesters (I to VIII/III to VIII) in VTU constituent college or in any VTU affiliated non-autonomous college.
	(e)	Has not been transferred from any autonomous institution affiliated to VTU or from any other University.
	(4)	The total number of ranks awarded shall be 10% of total number of students appeared in VIII semester subject to a maximum of 10 ranks in a Specialization.
	(5)	For award of ranks in a Specialization, a minimum of 10 students should have appeared in the VIII semester examination.
	Illustration:	
	(a)	If 1228 students appeared for the VIII semester in Electronics and Communication Engineering Programme, the number of ranks to be awarded for Electronics and Communication Engineering shall be 10.
	(b)	If 90 students appeared for the VIII semester in Biomedical Engineering, the number of ranks to be awarded for Biomedical Engineering will be 09.
	(6)	In case of fractional number of ranks, it is rounded to higher integer only when the first decimal place is greater than or equal to 5.

18OB13.3	Ranks shall be awarded based on the merit of the students as determined by CGPA. If two or more students get the same CGPA, the tie shall be resolved by considering the number of times a student has obtained higher SGPA. If it is not resolved even at this stage, the number of times a student has obtained higher grades like S, A, B etc., shall be taken into account to decide the order of the rank.
18OB14.0	**Transfer of students**
18OB14.1	(a) (i) Transfer of students from one VTU affiliated non – autonomous college to another VTU non – autonomous affiliated college shall be permitted only at the beginning of third, fifth, and seventh semesters, subject to availability of seats within the permitted intake in respective Colleges with the approval of the Registrar, VTU subject to the provision 18OB10.3. (ii) The students seeking transfer as per 18OB14.1 (a) (i) shall have to obtain No Objection certificate for admission from the University and from both the colleges before the commencement of term as notified by VTU. (iii) Complete the Programme subject to the provision 18OB1.4. (b) Transfer of students from an autonomous to non – autonomous college, affiliated to VTU is permitted with the following conditions. (i) Transfer shall only be at the beginning of III and V semester B.E./B.Tech. Programme. (ii) No transfer shall be permitted to VII semester B.E./B.Tech. Programme. (iii) Students who are seeking transfer must have passed in all the Courses of the previous semesters. (iv) Obtain No Objection certificate for admission from the University and from both the colleges before commencement of term as notified by VTU. (v) Complete additional Course/s, if any, as per the decision of concerned Board of Studies on establishing the equivalence between two schemes. A Grade card shall be issued to that effect. Additional Course/s shall not be considered for the Eligibility criteria prescribed for promotion, calculation of SGPA and CGPA. However, a pass in the additional Courses, if any, is mandatory before the completion of Degree. (vi) Earn the credits decided by the University as per 18 OB 12.2. (vii) Complete the Programme subject to the provision 18OB1.4.

	(c) In the case of students seeking transfer from Universities other than VTU, the students must have passed in all the Courses of I and II semesters for admission to III semester and all the Courses of I to IV semesters for admission to V semester. No transfer shall be permitted to VII semester B.E./B.Tech. Programme of VTU from any other Universities.
	The students seeking admission from other Universities to VTU shall have to
	(i) Apply for establishment of equivalence with prescribed fees as notified by the VTU and obtain No Objection certificate for admission from the University before the commencement of term as notified by VTU.
	(ii) Produce No Objection certificate for admission from both the colleges before the commencement of term as notified by VTU.
	(iii) Complete additional Course/s, if any, as per the decision of concerned Board of Studies on establishing equivalence between two schemes. A Grade card shall be issued to that effect. Additional Course/s shall not be considered for the eligibility criterion prescribed for promotion, calculation of SGPA and CGPA. However, a pass in the additional Courses, if any, is mandatory before the completion of Degree.
	(iv) Earn the credits as decided by the University as per 18 OB 12.2.
	(v) Complete the Programme subject to the provision 18OB1.4.
18OB14.2	Transfer of students within the College from one branch to another branch at the start of III semester shall be permitted with the approval of the Registrar, VTU subject to the provisions made by the appropriate authorities.
18OB14.3	The University may prescribe fee for administration purpose, which shall be notified from time to time, for transfer from one college to another (Change of College) or one branch to another branch (change of branch within the college).
18OB15.0	**Applicability and Power to Modify**
18OB15.1	The regulations governing the Degree of Bachelor of Engineering / Technology of Visvesvaraya Technological University shall be a binding on all concerned.
18OB15.2	i) Notwithstanding anything contained in the foregoing, the University shall have the power to issue directions/ orders to address any difficulty.
	ii) Nothing in the foregoing may be construed as limiting the power of the University to amend, modify or repeal any or all of the above.

VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI
Scheme of Teaching and Examination 2018 – 19
Outcome Based Education (OBE) and Choice Based Credit System (CBCS)
(Effective from the academic year 2018 – 19)

Programme: B.E: Electronics &Telecommunication Engineering

III SEMESTER

Sl. No		Course and Course Code	Course Title	Teaching Department	Teaching Hours/Week Lecture Theory L	Tutorial T	Practical/Drawing P	Examination Duration in hours	CIE Marks	SEE Marks	Total Marks	Credits
1	BSC	18MAT31	Transform Calculus, Fourier Series and Numerical Techniques	Mathematics	2	2	--	03	40	60	100	3
2	PCC	18EC32	Network Theory		3	2	--	03	40	60	100	4
3	PCC	18EC33	Electronic Devices		3	0	--	03	40	60	100	3
4	PCC	18EC34	Digital System Design		3	0	--	03	40	60	100	3
5	PCC	18EC35	Computer Organization & Architecture		3	0	--	03	40	60	100	3
6	PCC	18EC36	Power Electronics & Instrumentation		3	0	--	03	40	60	100	3
7	PCC	18ECL37	Electronic Devices & Instrumentation Laboratory		--	2	2	03	40	60	100	2
8	PCC	18ECL38	Digital System Design Laboratory		--	2	2	03	40	60	100	2
9	HSMC	18KVK39/49	Vyavaharika Kannada (Kannada for communication)/	HSMC	--	2	--	--	100	--	100	1
		18KAK39/49	Aadalitha Kannada (Kannada for Administration)									
			OR									
		18CPC39/49	Constitution of India, Professional Ethics and Cyber Law		1	--	--	02	40	60		
			Examination is by objective type questions									
		TOTAL			17 OR 18	10 OR 08	04	24 OR 26	420 OR 360	480 OR 540	900	24

Note: BSC: Basic Science, PCC: Professional Core, HSMC: Humanity and Social Science, NCMC: Non-credit mandatory course.

18KVK39 Vyavaharika Kannada (Kannada for communication) is for non-Kannada speaking, reading and writing students and 18KAK39 Aadalitha Kannada (Kannada for Administration) is for students who speak, read and write Kannada.

Course prescribed to lateral entry Diploma holders admitted to III semester of Engineering programs

				02	01	--	03	40	60	100	0
10	NCMC	18MATDIP31	Additional Mathematics - I	Mathematics							

(a) The mandatory non – credit courses Additional Mathematics I and II prescribed for III and IV semesters respectively, to the lateral entry Diploma holders admitted to III semester of BE/B.Tech programs, shall attend the classes during the respective semesters to complete all the formalities of the course and appear for the University examination. In case, any student fails to register for the said course/fails to secure the minimum 40% of the prescribed CIE marks, he/she shall be deemed to have secured F grade. In such a case, the students have to fulfill the requirements during subsequent semester/s to appear for SEE.

(b) These Courses shall not be considered for vertical progression, but completion of the courses shall be mandatory for the award of degree.

Courses prescribed to lateral entry B. Sc degree holders admitted to III semester of Engineering programs

Lateral entrant students from B.Sc. Stream, shall clear the non-credit courses Engineering Graphics and Elements of Civil Engineering and Mechanics of the First Year Engineering Programme. These Courses shall not be considered for vertical progression, but completion of the courses shall be mandatory for the award of degree.

AICTE Activity Points to be earned by students admitted to BE/B. Tech/B. Plan day college programme (For more details refer to Chapter 6, AICTE Activity Point Programme, Model Internship Guidelines):

Over and above the academic grades, every Day College regular student admitted to the 4 years Degree programme and every student entering 4 years Degree programme through lateral entry, shall earn 100 and 75 Activity Points respectively for the award of degree through AICTE Activity Point Programme. Students transferred from other Universities to fifth semester are required to earn 50 Activity Points from the year of entry to VTU. The Activity Points earned shall be reflected on the student's eighth semester Grade Card.

The activities can be can be spread over the years, anytime during the semester weekends and holidays, as per the liking and convenience of the student from the year of entry to the programme. However, minimum hours' requirement should be fulfilled. Activity Points (non-credit) have no effect on SGPA/CGPA and shall not be considered for vertical progression.

In case students fail to earn the prescribed activity Points, Eighth semester Grade Card shall be issued only after earning the required activity Points. Students shall be admitted for the award of degree only after the release of the Eighth semester Grade Card.

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Programme: B.E: Electronics &Telecommunication Engineering

IV SEMESTER

Sl No		Course and Course code	Course Title	Teaching Department	Teaching Hours /Week			Duration in hours	CIE Marks	SEE Marks	Total Marks	Credits
					Lecture Theory L	Tutorial T	Practical/ Drawing P					
1	BSC	18MAT41	Complex Analysis, Probability and Statistical Methods	Mathematics	2	2	--	03	40	60	100	3
2	PCC	18EC42	Analog Circuits		3	2	--	03	40	60	100	4
3	PCC	18EC43	Control Systems		3	0	--	03	40	60	100	3
4	PCC	18EC44	Engineering Statistics & Linear Algebra		3	0	--	03	40	60	100	3
5	PCC	18EC45	Signals & Systems		3	0	--	03	40	60	100	3
6	PCC	18EC46	Microcontroller		3	0	--	03	40	60	100	3
7	PCC	18ECL47	Microcontroller Laboratory		--	2	2	03	40	60	100	2
8	PCC	18ECL48	Analog Circuits Laboratory		--	2	2	03	40	60	100	2
9	HSMC	18KVK39/49	Vyavaharika Kannada (Kannada for communication)	HSMC	--	2	--	--	100	--	100	1
		18KAK39/49	Aadalitha Kannada (Kannada for Administration)									
			OR									
		18CPC39/49	Constitution of India, Professional Ethics and Cyber Law		1	--	--	02	40	60		
					Examination is by objective type questions							
			TOTAL		17	10	04	24	420	480	900	24
					OR	OR		OR	OR	OR		
					18	08		26	360	540		

Note: BSC: Basic Science, PCC: Professional Core, HSMC: Humanity and Social Science, NCMC: Non-credit mandatory course.

18KVK39/49 Vyavaharika Kannada (Kannada for communication) is for non-Kannada speaking, reading and writing students and 18KAK39/49 Aadalitha Kannada (Kannada for Administration) is for students who speak, read and write Kannada.

Course prescribed to lateral entry Diploma holders admitted to III semester of Engineering programs

10	NCMC	18MATDIP41	Additional Mathematics – II	Mathematics	02	01	--	03	40	60	100	0

(a)The mandatory non – credit courses Additional Mathematics I and II prescribed for III and IV semesters respectively, to the lateral entry Diploma holders admitted to III semester of BE/B.Tech programs, shall attend the classes during the respective semesters to complete all the formalities of the course and appear for the University examination. In case, any student fails to register for the said course/ fails to secure the minimum 40% of the prescribed CIE marks, he/she shall be deemed to have secured F grade. In such a case, the students have to fulfill the requirements during subsequent semester/s to appear for SEE.

(b) These Courses shall not be considered for vertical progression, but completion of the courses shall be mandatory for the award of degree.

Courses prescribed to lateral entry B. Sc degree holders admitted to III semester of Engineering programs

Lateral entrant students from B.Sc. Stream, shall clear the non-credit courses Engineering Graphics and Elements of Civil Engineering and Mechanics of the First Year Engineering Programme. These Courses shall not be considered for vertical progression, but completion of the courses shall be mandatory for the award of degree.

AICTE activity Points: In case students fail to earn the prescribed activity Points, Eighth semester Grade Card shall be issued only after earning the required activity Points. Students shall be admitted for the award of degree only after the release of the Eighth semester Grade Card.

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Programme: B.E: Electronics &Telecommunication Engineering

V SEMESTER

Sl. No	Course and Course code		Course Title	Teaching Department	Teaching Hours /Week			Duration in hours	CIE Marks	SEE Marks	Total Marks	Credits
					Lecture Theory L	Tutorial T	Practical/ Drawing P					
1	HSMC	18ES51	Technological Innovation Management and Entrepreneurship		3	0	--	03	40	60	100	3
2	PCC	18EC52	Digital Signal Processing		3	2	--	03	40	60	100	4
3	PCC	18EC53	Principles of Communication Systems		3	2	--	03	40	60	100	4
4	PCC	18EC54	Information Theory & Coding		3	--	--	03	40	60	100	3
5	PCC	18EC55	Electromagnetic Waves		3	--	--	03	40	60	100	3
6	PCC	18EC56	Verilog HDL		3	--	--	03	40	60	100	3
7	PCC	18ECL57	Digital Signal Processing Laboratory		--	2	2	03	40	60	100	2
8	PCC	18ECL58	HDL Laboratory		--	2	2	03	40	60	100	2
9	HSMC	18CIV59	Environmental Studies	Civil/Environmental [Paper setting: Civil Engineering Board]	1	--	--	02	40	60	100	1
				TOTAL	**19**	**8**	**4**	**26**	**360**	**540**	**900**	**25**

Note: PCC: Professional Core, HSMC: Humanity and Social Science.

AICTE activity Points: In case students fail to earn the prescribed activity Points, Eighth semester Grade Card shall be issued only after earning the required activity Points. Students shall be admitted for the award of degree only after the release of the Eighth semester Grade Card.

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Programme: B.E: Electronics &Telecommunication Engineering

VI SEMESTER

Sl. No	Course and Course code		Course Title	Teaching Department	Teaching Hours /Week			Examination				Credits
					Theory Lecture L	Tutorial T	Practical/ Drawing P	Duration in hours	CIE Marks	SEE Marks	Total Marks	
1	PCC	18EC61	Digital Communication		3	2	--	03	40	60	100	4
2	PCC	18TE62	Microwave Theory & Antennas		3	2	--	03	40	60	100	4
3	PCC	18TE63	Computer Communication Networks		3	2	--	03	40	60	100	4
4	PEC	18XX64X	Professional Elective -1		3	--	--	03	40	60	100	3
5	OEC	18XX65X	Open Elective -A		3	--	--	03	40	60	100	3
6	PCC	18TEL66	CCN Laboratory		--	2	2	03	40	60	100	2
7	PCC	18TEL67	Analog & Digital Communication Laboratory		--	2	2	03	40	60	100	2
8	MP	18TEMP68	Mini-project		--	--	2	03	40	60	100	2
9	Internship	--	Internship	To be carried out during the vacation/s of VI and VII semesters and /or VII and VIII semesters.								
			TOTAL		15	10	6	24	320	480	800	24

Note: PCC: Professional core, PEC: Professional Elective, OE: Open Elective, MP: Mini-project.

Professional Elective -1

Course code under 18XX64X	Course Title
18EC641	Operating System
18EC642	Artificial Neural Networks
18EC643	Data Structures using C++
18TE644	Microcontroller and Embedded Systems
18TE645	Radio Frequency Integrated Circuits
18EC646	Python Application Programming

OPEN ELECTIVE group-B	
18EC651	Signal Processing
18EC652	Sensors &Signal Conditioning
18EC653	**Virtual Instrumentation**
18EC654	**Microcontrollers**
18EC655	**Basic VLSI Design**

Students can select any one of the open electives offered by other Departments except those that are offered by the parent Department (Please refer to the list of open electives under 18XX65X).

Selection of an open elective shall not be allowed if,

- The candidate has studied the same course during the previous semesters of the programme.
- The syllabus content of open elective is similar to that of the Departmental core courses or professional electives.
- A similar course, under any category, is prescribed in the higher semesters of the programme.

Registration to electives shall be documented under the guidance of Programme Coordinator/ Advisor/Mentor.

Mini-project work:

Based on the ability/abilities of the student/s and recommendations of the mentor, a single discipline or a multidisciplinary Mini- project can be assigned to an individual student or to a group having not more than 4 students.

CIE procedure for Mini-project:

(i) Single discipline: The CIE marks shall be awarded by a committee consisting of the Head of the concerned Department and two senior faculty members of the Department, one of whom shall be the Guide.

The CIE marks awarded for the Mini-project work, shall be based on the evaluation of project report, project presentation skill and question and answer session in the ratio 50:25:25.The marks awarded for the project report shall be the same for all the batch mates.

(ii) Interdisciplinary: Continuous Internal Evaluation shall be group wise at the college level with the participation of all the guides of the college.

The CIE marks awarded for the Mini-project, shall be based on the evaluation of project report, project presentation skill and question and answer session in the ratio 50:25:25.The marks awarded for the project report shall be the same for all the batch mates.

SEE for Mini-project:

(i) Single discipline: Contribution to the Mini-project and the performance of each group member shall be assessed individually in the semester end examination (SEE) conducted at the department.

(ii) Interdisciplinary: Contribution to the Mini-project and the performance of each group member shall be assessed individually in semester end examination (SEE) conducted separately at the departments to which the student/s belong to.

Internship: All the students admitted to III year of BE/B.Tech shall have to undergo mandatory internship of 4 weeks during the vacation of VI and VII semesters and /or VII and VIII semesters. A University examination shall be conducted during VIII semester and the prescribed credit shall be included in VIII semester. Internship shall be considered as a head of passing and shall be considered for the award of degree. Those, who do not take-up/complete the internship shall be declared fail and shall have to complete during subsequent University examination after satisfying the internship requirements.

AICTE activity Points: In case students fail to earn the prescribed activity Points, Eighth semester Grade Card shall be issued only after earning the required activity Points. Students shall be admitted for the award of degree only after the release of the Eighth semester Grade Card.

VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI
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Programme: B.E: Electronics &Telecommunication Engineering

VII SEMESTER

Sl. No		Course and Course code	Course Title	Teaching Department	Teaching Hours /Week				Examination				Credits
					Theory Lecture L	Tutorial T	Practical/ Drawing P	Duration in hours	CIE Marks	SEE Marks	Total Marks	
1	PCC	18TE71	Optical Communication		3	--	--	03	40	60	100	3
2	PCC	18TE72	Wireless Communication		3	--	--	03	40	60	100	3
3	PEC	18XX73X	Professional Elective - 2		3	--	--	03	40	60	100	3
4	PEC	18XX74X	Professional Elective - 3		3	--	--	03	40	60	100	3
5	OEC	18XX75X	Open Elective -B		3	--	--	03	40	60	100	3
6	PCC	18TEL76	Wireless Communication Laboratory		--	2	2	03	40	60	100	2
7	PCC	18TEL77	Microwave & Antennas Laboratory		--	2	2	03	40	60	100	2
8	Project	18TEP78	Project Work Phase - 1		--	2	2	--	100	--	100	1
9	Internship	--	Internship	(If not completed during the vacation of VI and VII semesters, it shall be carried out during the vacation of VII and VIII semesters)								
			TOTAL		15	04	06	21	38	420	800	20

Note: PCC: Professional core, PEC: Professional Elective.

Professional Elective - 2

Course code under 18XX73X

	Course Title
18EC731	Real Time Systems
18EC732	Satellite Communication
18EC733	Digital Image Processing
18EC734	DSP Algorithms & Architecture
18TE735	CMOS VLSI Design

Course code under 18XX74X	Course Title
18EC741	IOT & Wireless Sensor Networks
18EC742	Automotive Electronics
18EC743	Multimedia Communication
18EC744	Cryptography
18EC745	Machine Learning with Python
Open Elective –B	
18EC751	Communication Theory
18EC752	Neural Networks
18EC753	**ARM Embedded Systems**
18EC754	**Digital Systems Design using VHDL**

Students can select any one of the open electives offered by other Departments except those that are offered by the parent Department (Please refer to the list of open electives under 18XX75X).

Selection of an open elective shall not be allowed if,

- The candidate has studied the same course during the previous semesters of the programme.

- The syllabus content of open elective is similar to that of the Departmental core courses or professional electives.

- A similar course, under any category, is prescribed in the higher semesters of the programme.

Registration to electives shall be documented under the guidance of Programme Coordinator/ Advisor/Mentor.

Project work:

Based on the ability/abilities of the student/s and recommendations of the mentor, a single discipline or a multidisciplinary project can be assigned to an individual student or to a group having not more than 4 students. In extraordinary cases, like the funded projects requiring students from different disciplines, the project student strength can be 5 or 6.

CIE procedure for Project Work Phase - 1:

(i) Single discipline: The CIE marks shall be awarded by a committee consisting of the Head of the concerned Department and two senior faculty members of the Department, one of whom shall be the Guide.

The CIE marks awarded for the project work phase -1, shall be based on the evaluation of the project work phase -1 Report (covering Literature Survey, Problem identification, Objectives and Methodology), project presentation skill and question and answer session in the ratio 50:25:25.The marks awarded for the Project report shall be the same for all the batch mates.

(ii) Interdisciplinary: Continuous Internal Evaluation shall be group wise at the college level with the participation of all guides of the college. Participation of external guide/s, if any, is desirable.

The CIE marks awarded for the project work phase -1, shall be based on the evaluation of project work phase -1 Report, project presentation skill and question and answer session in the ratio 50:25:25.The marks awarded for the project report shall be the same for all the batch mates.

Internship: All the students admitted to III year of BE/B.Tech shall have to undergo mandatory internship of 4 weeks during the vacation of VI and VII semesters and /or VII and VIII semesters. A University examination shall be conducted during VIII semester and the prescribed credit shall be included in VIII semester. Internship shall be considered as a head of passing and shall be considered for the award of degree. Those, who do not take-up/complete the internship shall be declared fail and shall have to complete during subsequent University examination after satisfying the internship requirements.

AICTE activity Points: In case students fail to earn the prescribed activity Points, Eighth semester Grade Card shall be issued only after earning the required activity Points. Students shall be admitted for the award of degree only after the release of the Eighth semester Grade Card.

VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI
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Outcome Based Education (OBE) and Choice Based Credit System (CBCS)
(Effective from the academic year 2018 – 19)

Programme: B.E.: Electronics &Telecommunication Engineering   **VIII SEMESTER**

Sl. No	Course and Course code		Course Title	Teaching Department	Teaching Hours /Week				Examination					Credits
					Theory Lecture (L)	Tutorial (T)	Practical/ Drawing (P)	Duration in hours	CIE Marks	SEE Marks	Total Marks			
1	PCC	18TE81	Advanced Cellular Communication		3	--	--	03	40	60	100			3
2	PEC	18XX82X	Professional Elective - 4		3	--	--	03	40	60	100			3
3	Project	18TEP83	Project Work Phase - 2		--	--	2	03	40	60	100			8
4	Seminar	18TES84	Technical Seminar		--	--	2	03	100	--	100			1
5	Internship	18TEI85	Internship	Completed during the vacation/s of VI and VII semesters and /or VII and VIII semesters.)				03	40	60	100			3
			TOTAL		**06**	**--**	**04**	**15**	**260**	**240**	**500**			**18**

Note: PCC: Professional Core, PEC: Professional Elective.

Professional Elective - 4

Course code under 18XX82X	Course Title
18EC821	Network Security
18EC822	Micro Electro Mechanical Systems
18EC823	Radar Engineering
18TE24	Network Management
18TES25	Sustainable Telecommunication Networks

Project Work

CIE procedure for Project Work Phase - 2:

(i) Single discipline: The CIE marks shall be awarded by a committee consisting of the Head of the concerned Department and two senior faculty members of the Department, one of whom shall be the Guide.

The CIE marks awarded for the project work phase -2, shall be based on the evaluation of project work phase -2 Report, project presentation skill and question and answer session in the ratio 50:25:25. The marks awarded for the project report shall be the same for all the batch mates.

(ii) Interdisciplinary: Continuous Internal Evaluation shall be group wise at the college level with the participation of all guides of the college. Participation of external guide/s, if any, is desirable.

The CIE marks awarded for the project work phase -2, shall be based on the evaluation of project work phase -2 Report, project presentation skill and question and answer session in the ratio 50:25:25. The marks awarded for the project report shall be the same for all the batch mates.

SEE for Project Work Phase - 2:

(i) Single discipline: Contribution to the project and the performance of each group member shall be assessed individually in semester end examination (SEE) conducted at the department.

(ii) Interdisciplinary: Contribution to the project and the performance of each group member shall be assessed individually in semester end examination (SEE) conducted separately at the departments to which the student/s belongs to.

Internship: Those, who have not pursued /completed the internship, shall be declared as fail and have to complete during subsequent University examination after satisfying the internship requirements.

AICTE activity Points: In case students fail to earn the prescribed activity Points, Eighth semester Grade Card shall be issued only after earning the required activity Points. Students shall be admitted for the award of degree only after the release of the Eighth semester Grade Card.

Activity points of the students who have earned the prescribed AICTE activity Points shall be sent the University along with the CIE marks of 8th semester. In case of students who have not satisfied the AICTE activity Points at the end of eighth semester, the column under activity Points shall be marked NSAP (Not Satisfied Activity Points).

B. E. COMMON TO ALL PROGRAMMES

Choice Based Credit System (CBCS) and Outcome Based Education (OBE)

SEMESTER - III

TRANSFORM CALCULUS, FOURIER SERIES AND NUMERICAL TECHNIQUES

Course Code	: 18MAT31	CIE Marks	: 40
Lecture Hours/Week (L:T:P) : (2:2:0)		SEE Marks	: 60
Total Number of Lecture Hours : 40 (8 Hrs / Module)		Exam Hours	: 03

CREDITS – 03

Course Learning Objectives:

- To have an insight into Fourier series, Fourier transforms, Laplace transforms, Difference equations and Z-transforms.
- · To develop the proficiency in variational calculus and solving ODEs arising in engineering applications, using numerical methods.

Module-1

Laplace Transforms: Definition and Laplace transform of elementary functions. Laplace transforms of Periodic functions and unit-step function – problems.
Inverse Laplace Transforms: Inverse Laplace transform - problems, Convolution theorem to find the inverse Laplace transform (without proof) and problems, solution of linear differential equations using Laplace transform.

Module-2

Fourier Series: Periodic functions, Dirichlet's condition. Fourier series of periodic functions period 2π and arbitrary period. Half range Fourier series. Practical harmonic analysis, examples from engineering field.

Module-3

Fourier Transforms: Infinite Fourier transforms, Fourier sine and cosine transforms. Inverse Fourier transforms. Simple problems.
Difference Equations and Z-Transforms: Difference equations, basic definition, z-transform-definition, Standard z-transforms, Damping and shifting rules, initial value and final value theorems (without proof) and problems, Inverse z-transform. Simple problems.

Module-4

Numerical Solutions of Ordinary Differential Equations (ODEs): Numerical solution of ODEs of first order and first degree- Taylor's series method, Modified Euler's method. Range - Kutta method of fourth order, Milne's and Adam-Bashforth predictor and corrector method (No derivations of formulae), Problems.

Module-5

Numerical Solution of Second Order ODEs: Runge -Kutta method and Milne's predictor and corrector method.(No derivations of formulae).

Calculus of Variations: Variation of function and functional, variational problems, Euler's equation, Geodesics, hanging chain, problems.

Course Outcomes: At the end of the course the student will be able to:

1. Use Laplace transform and inverse Laplace transform in solving differential/ integral equation arising in network analysis, control systems and other fields of engineering.
2. Demonstrate Fourier series to study the behaviour of periodic functions and their applications in system communications, digital signal processing and field theory.
3. Make use of Fourier transform and Z-transform to illustrate discrete/ continuous function arising in wave and heat propagation, signals and systems.
4. Solve first and second order ordinary differential equations arising in engineering problems using single step and multistep numerical methods.
5. Determine the extremals of functionals using calculus of variations and solve problems arising in dynamics of rigid bodies and vibrational analysis.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

43

Textbooks

1. Advanced Engineering Mathematics, E. Kreyszig, John Wiley & Sons, 10th Edition, 2016
2. Higher Engineering Mathematics, B. S. Grewal, Khanna Publishers, 44th Edition, 2017
3. Engineering Mathematics, Srimanta Pal et al, Oxford University Press, 3rd Edition, 2016

Reference Books

1. Advanced Engineering Mathematics, C. Ray Wylie, Louis C. Barrett, McGraw-Hill Book Co, 6th Edition, 1995
2. Introductory Methods of Numerical Analysis, S. S. Sastry, Prentice Hall of India, 4th Edition 2010
3. Higher Engineering Mathematics, B.V. Ramana, McGraw-Hill, 11th Edition, 2010
4. A Text Book of Engineering Mathematics, N. P. Bali and Manish Goyal, Laxmi Publications, 2014
5. Advanced Engineering Mathematics, Chandrika Prasad and Reena Garg, Khanna Publishing, 2018

Web links and Video Lectures:

1. http://nptel.ac.in/courses.php?disciplineID=111
2. http://www.class-central.com/subject/math(MOOCs)
3. http://academicearth.org/
4. VTU EDUSAT PROGRAMME - 20

B. E. EC / TC
Choice Based Credit System (CBCS) and Outcome Based Education (OBE)
SEMESTER - III

NETWORK THEORY

Course Code : 18EC32	CIE Marks : 40
Lecture Hours/Week : 03 + 2 (Tutorial)	SEE marks : 60
Total Number of Lecture Hours : 50 (10 Hrs / Module)	Exam Hours : 03
CREDITS : 04	

Course Learning Objectives: This course will enable students to:

- Describe basic network concepts emphasizing source transformation, source shifting, mesh and nodal techniques to solve for resistance/ impedance, voltage, current and power.
- Explain network Thevenin's, Millman's, Superposition, Maximum Power transfer and Norton's Theorems and apply them in solving the problems related to Electrical Circuits.
- Explain the behavior of networks subjected to transient conditions.
- Use applications of Laplace transforms to network problems.
- Study two port network parameters like Z, Y, T and h and their inter-relationships and applications.
- Study of RLC Series and parallel tuned circuit.

Module – 1
Basic Concepts: Practical sources, Source transformations, Network reduction using Star – Delta transformation, Loop and node analysis with linearly dependent and independent sources for DC and AC networks.

L1, L2, L3, L4

Module – 2
Network Theorems:
Superposition, Millman's theorems, Thevenin's and Norton's theorems, Maximum Power transfer theorem.

L1, L2, L3, L4

Module – 3
Transient behavior and initial conditions: Behavior of circuit elements under switching condition and their Representation, evaluation of initial and final conditions in RL, RC and RLC circuits for AC and DC excitations.

L1 , L2 , L3

Module – 4

Laplace Transformation & Applications: Solution of networks, step, ramp and impulse responses, waveform Synthesis.

L1, L2, L3, L4

Module – 5

Two port network parameters: Definition of Z, Y, h and Transmission parameters, modelling with these parameters, relationship between parameters sets.
Resonance:
Series Resonance: Variation of Current and Voltage with Frequency, Selectivity and Bandwidth, Q-Factor, Circuit Magnification Factor, Selectivity with Variable Capacitance, Selectivity with Variable Inductance.
Parallel Resonance: Selectivity and Bandwidth, Maximum Impedance Conditions with C, L and f Variable, current in Anti-Resonant Circuit, The General Case-Resistance Present in both Branches.

L1, L2, L3, L4

Course Outcomes: At the end of the course, the students will be able to
1. Determine currents and voltages using source transformation/ source shifting/ mesh/ nodal analysis and reduce given network using star-delta transformation/source transformation/ source shifting.
2. Solve network problems by applying Superposition/ Thevenin's/ Norton's/ Maximum Power Transfer/ Millman's Network Theorems and electrical laws to reduce circuit complexities and to arrive at feasible solutions.
3. Calculate current and voltages for the given circuit under transient conditions and Apply Laplace transform to solve the given network.
4. Solve the given network using specified two port network parameters - Z, Y, T & h.
5. Understand the concept of resonance and determine the parameters that characterize series/parallel Resonant Circuits.

Question paper pattern:
- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:
1.	M.E. Van Valkenburg (2000) ―Network Analysis, Prentice Hall of India, 3rd edition, 2000, ISBN: 9780136110958.
2.	Roy Choudhury - Networks and Systems, 2nd edition, New Age International Publications, 2006, ISBN: 9788122427677

Reference Books:
1.	Hayt, Kemmerly and Durbin ―Engineering Circuit Analysis, TMH 7th Edition, 2010.
2.	J. David Irwin /R. Mark Nelms ―Basic Engineering Circuit Analysis John Wiley, 8th ed, 2006.
3.	Charles K Alexander and Mathew N O Sadiku ― Fundamentals of Electric Circuits, Tata McGraw-Hill, 3rd Ed, 2009.

ELECTRONIC DEVICES

Course Code	: 18EC33	CIE Marks : 40
Lecture Hours/Week	: 03	SEE marks : 60
Total Number of Lecture Hours : 40 (8 Hours / Module)		Exam Hours : 03

CREDITS – 03

Course Learning Objectives: This course will enable students to:

- Understand the basics of semiconductor physics and electronic devices.
- Describe the mathematical models BJTs and FETs along with the constructional details.
- Understand the construction and working principles of optoelectronic devices
- Understand the fabrication process of semiconductor devices and CMOS process integration.

Module-1

Semiconductors

Bonding forces in solids, Energy bands, Metals, Semiconductors and Insulators, Direct and Indirect semiconductors, Electrons and Holes, Intrinsic and Extrinsic materials, Conductivity and Mobility, Drift and Resistance, Effects of temperature and doping on mobility, Hall Effect.
(Text 1: 3.1.1, 3.1.2, 3.1.3, 3.1.4, 3.2.1, 3.2.3, 3.2.4, 3.4.1, 3.4.2, 3.4.3, 3.4.5).
L1,L2

Module-2

pn Junctions

Forward and Reverse biased junctions- Qualitative description of Current flow at a junction, reverse bias, Reverse bias breakdown- Zener breakdown, avalanche breakdown, Rectifiers. **(Text 1: 5.3.1, 5.3.3, 5.4, 5.4.1, 5.4.2, 5.4.3)** Optoelectronic Devices Photodiodes: Current and Voltage in an Illuminated Junction, Solar Cells, Photodetectors. Light Emitting Diode: Light Emitting materials**.**
(Text 1: 8.1.1, 8.1.2, 8.1.3, 8.2, 8.2.1),   **L1,L2**

Module – 3

Bipolar Junction Transistor

Fundamentals of BJT operation, Amplification with BJTS, BJT Fabrication, The coupled Diode model (Ebers-Moll Model), Switching operation of a transistor, Cutoff, saturation, switching cycle, specifications, Drift in the base region, Base narrowing, Avalanche breakdown.

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(Text 1: 7.1, 7.2, 7.3, 7.5.1, 7.6, 7.7.1, 7.7.2, 7.7.3)   **L1,L2**

Module-4
Field Effect Transistors
Basic pn JFET Operation, Equivalent Circuit and Frequency Limitations, MOSFET- Two terminal MOS structure- Energy band diagram, Ideal Capacitance – Voltage Characteristics and Frequency Effects, Basic MOSFET Operation- MOSFET structure, Current-Voltage Characteristics.
(Text 2: 9.1.1, 9.4, 9.6.1, 9.6.2, 9.7.1, 9.7.2, 9.8.1, 9.8.2).   **L1,L2**

Module-5
Fabrication of p-n junctions
Thermal Oxidation, Diffusion, Rapid Thermal Processing, Ion implantation, chemical vapour deposition, photolithography, Etching, metallization.
(Text 1: 5.1)
Integrated Circuits
Background, Evolution of ICs, CMOS Process Integration, Integration of Other Circuit Elements. **(Text 1: 9.1, 9.2, 9.3.1, 9.3.3).**   **L1,L2**

Course outcomes: After studying this course, students will be able to:
1. Understand the principles of semiconductor Physics
2. Understand the principles and characteristics of different types of semiconductor devices
3. Understand the fabrication process of semiconductor devices
4. Utilize the mathematical models of semiconductor junctions for circuits and systems.
5. Identify the mathematical models of MOS transistors for circuits and systems.

Question paper pattern:
- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

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Text Books:
1. Ben. G. Streetman, Sanjay Kumar Banerjee, "Solid State Electronic Devices", 7th Edition, Pearson Education, 2016, ISBN 978-93-325-5508-2.
2. Donald A Neamen, Dhrubes Biswas, "Semiconductor Physics and Devices", 4th Edition, McGraw Hill Education, 2012, ISBN 978-0-07-107010-2.

Reference Book:
1. S. M. Sze, Kwok K. Ng, "Physics of Semiconductor Devices", 3rd Edition, Wiley, 2018.
2. Adir Bar-Lev, "Semiconductor and Electronic Devices", 3rd Edition, PHI, 1993.

DIGITAL SYSTEM DESIGN

Course Code	: **18EC34**	CIE Marks : 40	
Lecture Hours/Week : 03		SEE marks : 60	
Total Number of Lecture Hours : 40 (8 Hours / Module)		Exam Hours : 03	
CREDITS – 03			

Course Learning Objectives: This course will enable students to:

- Illustrate simplification of Algebraic equations using Karnaugh Maps and Quine-Mc Clusky Techniques.
- Design Decoders, Encoders, Digital Multiplexer, Adders, Subtractors and Binary Comparators.
- Describe Latches and Flip-flops, Registers and Counters.
- Analyze Mealy and Moore Models.
- Develop state diagrams Synchronous Sequential Circuits.
- Appreciate the applications of digital circuits.

Module – 1

Principles of combinational logic: Definition of combinational logic, canonical forms,

Generation of switching equations from truth tables, Karnaugh maps-3,4,5 variables, Incompletely specified functions (Don't care terms) Simplifying Max term equations, Quine-McCluskey techniques – 3 & 4 variables

(Text 1 - Chapter 3)   **L1, L2, L3**

Module – 2

Analysis and design of combinational logic: Decoders, Encoders, Digital multiplexers, Adders and subtractors, Look ahead carry, Binary comparators.
(Text 1 - Chapter 4)
Programmable Logic Devices, Complex PLD, FPGA.
(Text 3 - Chapter 9, 9.6 to 9.8)   **L1, L2, L3**

Module -3

Flip-Flops and its Applications: Basic Bistable elements, Latches, The master-slave flip-flops (pulse-triggered flip-flops): SR flip-flops, JK flip-flops, Characteristic equations, Registers, binary ripple counters, and synchronous binary counters.**(Text 2 - Chapter 6)**   **L1, L2, L3**

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Sequential Circuit Design: Design of a synchronous counter, Design of a synchronous mod-n counter using clocked JK, D, T and SR flip-flops.
(Text 2 - Chapter 6)
Mealy and Moore models, State machine notation, Construction of state diagrams. **(Text 1 - Chapter 6)**   **L1, L2, L3**

Module -5

Applications of Digital Circuits: Design of a Sequence Detector, Guidelines for construction of state graphs, Design Example – Code Converter, Design of Iterative Circuits (Comparator), Design of Sequential Circuits using ROMs and PLAs, CPLDs and FPGAs, Serial Adder with Accumulator, Design of Binary Multiplier, Design of Binary Divider.
(Text 3 – 14.1, 14.3, 16.2, 16.3, 16.4, 18.1, 18.2, 18.3)   L1, L2, L3

Course Outcomes: After studying this course, students will be able to:
  1. Explain the concept of combinational and sequential logic circuits.
  2. Analyze and Design the combinational logic circuits.
  3. Describe and characterize flip-flops and its applications.
  4. Design the sequential circuits using SR, JK, D, T flip-flops and Mealy & Moore machines.
  5. Design applications of Combinational & Sequential Circuits.

Question paper pattern:
- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:
1.   John M Yarbrough -Digital Logic Applications and Design, Thomson Learning, 2001.
2.   Donald D. Givone ―Digital Principles and Design, McGraw Hill, 2002.
3.   Charles H Roth Jr., Larry L. Kinney ―Fundamentals of Logic Design, Cengage Learning, 7th Edition.

Reference Books:
1.   D. P. Kothari and J. S Dhillon, ―Digital Circuits and Design, Pearson, 2016.
2.   Morris Mano, ―Digital Design, Prentice Hall of India, Third Edition.
3.   K. A. Navas ―Electronics Lab Manual, Volume I, PHI, 5th Edition, 2015.

COMPUTER ORGANIZATION AND ARCHITECTURE

Course Code	: 18EC35	CIE Marks : 40
Lecture Hours/Week	: 03	SEE Marks : 60
Total Number of Lecture Hours : 40 (8 Hours / Module)		Exam Hours : 03

CREDITS– 03

Course Learning Objectives: This course will enable students to:
- Explain the basic sub systems of a computer, their organization, structure and operation.
- Illustrate the concept of programs as sequences of machine instructions.
- Demonstrate different ways of communicating with I/O devices
- Describe memory hierarchy and concept of virtual memory.
- Illustrate organization of simple pipelined processor and other computing systems.

Module 1

Basic Structure of Computers: Computer Types, Functional Units, Basic Operational Concepts, Bus Structures, Software, Performance – Processor Clock, Basic Performance Equation **(up to 1.6.2 of Chap 1 of Text).**
Machine Instructions and Programs: Numbers, Arithmetic Operations and Characters, IEEE standard for Floating point Numbers, Memory Location and Addresses, Memory Operations, Instructions and Instruction Sequencing **(up to 2.4.6 of Chap 2 and 6.7.1 of Chap 6 of Text). L1, L2, L3**

Module 2

Addressing Modes, Assembly Language, Basic Input and Output Operations, Stacks and Queues, Subroutines, Additional Instructions **(from 2.4.7 of Chap2, except 2.9.3, 2.11 & 2.12 of Text). L1, L2, L3**

Module 3

Input/Output Organization: Accessing I/O Devices, Interrupts – Interrupt Hardware, Enabling and Disabling Interrupts, Handling Multiple Devices, Controlling Device Requests, Direct Memory Access **(up to 4.2.4 and 4.4 except 4.4.1 of Chap 4 of Text). L1, L2, L3**

Module 4

Memory System: Basic Concepts, Semiconductor RAM Memories-Internal organization of memory chips, Static memories, Asynchronous DRAMS, Read Only Memories, Cash Memories, Virtual Memories, Secondary Storage-Magnetic Hard Disks **(5.1, 5.2, 5.2.1, 5.2.2, 5.2.3, 5.3, 5.5 (except 5.5.1 to 5.5.4), 5.7 (except 5.7.1), 5.9, 5.9.1 of Chap 5 of Text). L1, L2, L3**

Module 5

Basic Processing Unit: Some Fundamental Concepts, Execution of a Complete Instruction, Multiple Bus Organization, Hardwired Control, Microprogrammed Control **(up to 7.5 except 7.5.1 to 7.5.6 of Chap 7 of Text).**

L1,L2, L3

Course Outcomes: After studying this course, students will be able to:

1. Explain the basic organization of a computer system.

2. Describe the addressing modes, instruction formats and program control statement.

3. Explain different ways of accessing an input / output device including interrupts.

4. Illustrate the organization of different types of semiconductor and other secondary storage memories.

5. Illustrate simple processor organization based on hardwired control and micro programmed control.

Question paper pattern:

* Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
* Each full question can have a maximum of 4 sub questions.
* There will be 2 full questions from each module covering all the topics of the module.
* Students will have to answer 5 full questions, selecting one full question from each module
* The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

1. Carl Hamacher, Zvonko Vranesic, Safwat Zaky: Computer Organization, 5th Edition, Tata McGraw Hill, 2002.

Reference Books:

1. David A. Patterson, John L. Hennessy: Computer Organization and Design – The Hardware / Software Interface ARM Edition, 4th Edition, Elsevier, 2009.

2. William Stallings: Computer Organization & Architecture, 7th Edition, PHI, 2006.

3. Vincent P. Heuring & Harry F. Jordan: Computer Systems Design and Architecture, 2nd Edition, Pearson Education, 2004.

POWER ELECTRONICS AND INSTRUMENTATION

Course Code	: 18EC36	CIE Marks : 40
Lecture Hours/Week : 03		SEE marks : 60
Total Number of Lecture Hours : 40 (8 Hrs / Module)		Exam Hours : 03
CREDITS – 03		

Course Learning Objectives: This course will enable students to:

• Study and analysis of thyristor circuits with different triggering conditions.
• Learn the applications of power devices in controlled rectifiers, converters and inverters.
• Understand types of instrument errors.
• Develop circuits for multirange Ammeters and Voltmeters.
• Describe principle of operation of digital measuring instruments and Bridges.
• Understand the operation of Transducers, Instrumentation amplifiers and PLCs.

Module - 1

Introduction: History, Power Electronic Systems, Power Electronic Converters and Applications (**1.2, 1.3 1.5 & 1.6 of Text 1**).

Thyristors: Static Anode-Cathode characteristics and Gate characteristics of SCR, Turn-ON methods, Turn-OFF mechanisms (**2.3, 2.6 without 2.6.1), 2.7, 2.9 of text 1**),

Turn-OFF Methods: Natural and Forced Commutation – Class A and Class B types (**refer 2.10 without design considerations**),

Gate Trigger Circuit: Resistance Firing Circuit, Resistance capacitance firing circuit (**refer 3.5 up to 3.5.2 of Text 1**),

Unijunction Transistor: Basic operation and UJT Firing Circuit (**refer 3.6, up to 3.6.4, except 3.6.2**).

L1, L2

Module - 2

Phase Controlled Converter: Control techniques, Single phase half wave and full wave controlled rectifier with resistive and inductive loads, effect of freewheeling diode (**refer Chapter 6 of Text 1 up to 6.4.1 without derivations**).

Choppers: Chopper Classification, Basic Chopper operation: step-down, step-up and step-up/down choppers. (**refer Chapter 8 of Text 1 up to 8.3.3**)

L1, L2, L3

Inverters: Classification, Single phase Half bridge and full bridge inverters with R and RL load (**refer Chapter 9 of Text 1 up to 9.4.2 without Circuit Analysis**).

Switched Mode Power Supplies: Isolated Flyback Converter, Isolated Forward Converter (**only refer to the circuit operations in section 16.3 of Text 1 up to 16.3.2 except 16.3.1.3 and derivations**).

Principles of Measurement: Static Characteristics, Error in Measurement, Types of Static Error. (Text 2: 1.2-1.6)

Multirange Ammeters, Multirange voltmeter. (Text 2: 3.2, 4.4)

L1, L2, L3

Module - 4

Digital Voltmeter: Ramp Technique, Dual slope integrating Type DVM, Direct Compensation type and Successive Approximations type DVM (Text 2: 5.1-5.3, 5.5, 5.6)

Digital Multimeter: Digital Frequency Meter and Digital Measurement of Time, Function Generator.

Bridges: Measurement of resistance: Wheatstone's Bridge,   AC Bridges - Capacitance and Inductance Comparison bridge, Wien's bridge.
(Text 2: refer 6.2, 6.3 up to 6.3.2, 6.4 up to 6.4.2, 8.8, 11.2, 11.8-11.10, 11.14).

L1, L2

Module - 5

Transducers: Introduction, Electrical Transducer, Resistive Transducer, Resistive position Transducer, Resistance Wire Strain Gauges, Resistance Thermometer, Thermistor, LVDT.
(Text 2: 13.1-13.3, 13.5, 13.6 up to 13.6.1, 13.7, 13.8, 13.11).

Instrumentation Amplifier using Transducer Bridge, Temperature indicators using Thermometer, Analog Weight Scale (Text 2: 14.3.3, 14.4.1, 14.4.3).

Programmable Logic Controller: Structure, Operation, Relays and Registers (Text 2: 21.15, 21.15.2, 21.15.3, 21.15.5, 21.15.6).

L1, L2, L3

Course Outcomes: At the end of the course students should be able to:
1. Build and test circuits using power electronic devices.
2. Analyze and design controlled rectifier, DC to DC converters, DC to AC inverters and SMPS.
3. Analyze instrument characteristics and errors.
4. Describe the principle of operation and develop circuits for multirange Ammeters, Voltmeters and Bridges to measure passive component values and frequency.
5. Explain the principle, design and analyze the transducers for measuring physical parameters.

Question paper pattern:
* Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
* Each full question can have a maximum of 4 sub questions.
* There will be 2 full questions from each module covering all the topics of the module.
* Students will have to answer 5 full questions, selecting one full question from each module.
* The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:
1. M.D Singh and K B Khanchandani, Power Electronics, 2nd Edition, Tata Mc-Graw Hill, 2009, ISBN: 0070583897
2. H. S. Kalsi, "Electronic Instrumentation", McGraw Hill, 3rd Edition, 2012, ISBN: 9780070702066.

Reference Books:
1. Mohammad H Rashid, Power Electronics, Circuits, Devices and Applications, 3rd/4th Edition, Pearson Education Inc, 2014, ISBN: 978-93-325-1844-5.
2. L. Umanand, Power Electronics, Essentials and Applications, John Wiley India Pvt. Ltd, 2009.
3. David A. Bell, "Electronic Instrumentation & Measurements", Oxford University Press PHI 2nd Edition, 2006, ISBN 81-203-2360-2.
4. A. D. Helfrick and W.D. Cooper, "Modern Electronic Instrumentation and Measuring Techniques", Pearson, 1st Edition, 2015, ISBN: 9789332556065.

ELECTRONIC DEVICES AND INSTRUMENTATION LABORATORY

Course Code : **18ECL37**	CIE Marks : 40	SEE Marks : 60

Lecture Hours/Week: 02 Hours Tutorial (Instructions) + 02 Hours Laboratory

RBT Level : L1, L2, L3   Exam Hours : 03

CREDITS – 02

Course Learning Objectives: This laboratory course enables students to
- Understand the circuit schematic and its working.
- Study the characteristics of different electronic devices.
- Design and test simple electronic circuits as per the specifications using discrete electronic components.
- Familiarize with EDA software which can be used for electronic circuit simulation.

PART A : Experiments using Discrete components
1. Conduct experiment to test diode clipping (single/double ended) and clamping circuits (positive/negative).
2. Half wave rectifier and Full wave rectifier with and without filter and measure the ripple factor.
3. Characteristics of Zener diode and design a Simple Zener voltage regulator determine line and load regulation.
4. Characteristics of LDR and Photo diode and turn on an LED using LDR
5. Static characteristics of SCR.
6. SCR Controlled HWR and FWR using RC triggering circuit
7. Conduct an experiment to measure temperature in terms of current/ voltage using a temperature sensor bridge.
8. Measurement of Resistance using Wheatstone and Kelvin's bridge.

PART-B : Simulation using EDA software
(EDWinXP, PSpice, MultiSim, Proteus, Circuit Lab or any equivalent tool)
1. Input and Output characteristics of BJT Common emitter configuration and evaluation of parameters.
2. Transfer and drain characteristics of a JFET and MOSFET.
3. UJT triggering circuit for Controlled Full wave Rectifier.
4. Design and simulation of Regulated power supply.

Course Outcomes: On the completion of this laboratory course, the students will be able to:
1. Recognize and demonstrate functioning of semiconductor power devices.
2. Evaluate the characteristics, switching, power conversion and control by semiconductor power devices.
3. Analyze the response and plot the characteristics of transducers such as LDR, Photo diode, etc.
4. Design and test simple electronic circuits for measurement of temperature and resistance.
5. Use circuit simulation software for the implementation and characterization of electronic circuits and devices.

Conduct of Practical Examination:
- All laboratory experiments are to be considered for practical examination.
- For examination one question from **PART-A** and one question from **PART-B or** only one question from **PART-A** experiments based on the complexity, to be set.
- Students are allowed to pick one experiment from the lot.
- Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.
- Change of experiment is allowed only once and Marks allotted to the procedure part to be made zero.

Text Books
1. David A Bell, "Fundamentals of Electronic Devices and Circuits Lab Manual, 5th Edition, 2009, Oxford University Press.
2. Muhammed H Rashid, "Introduction to PSpice using OrCAD for circuits and electronics", 3rd Edition, Prentice Hall, 2003.

DIGITAL SYSTEM DESIGN LABORATORY

Course Code : **18ECL38**	CIE Marks : 40	SEE Marks : 60
Lecture Hours/Week: 02 Hours Tutorial (Instructions) + 02 Hours Laboratory		
RBT Level : L1, L2, L3, L4	Exam Hours : 03	
CREDITS – 02		

Course objectives: This laboratory course enables students to get practical experience in design, realization and verification of
- De Morgan's Theorem, SOP, POS forms
- Full/Parallel Adders, Subtractors and Magnitude Comparator
- Multiplexer using logic gates
- Demultiplexers and Decoders
- Flip-Flops, Shift registers and Counters.

NOTE:

1. Use discrete components to test and verify the logic gates.
2. The IC numbers given are suggestive; any equivalent ICs can be used.
3. For experiment No. 11 and 12 any open source or licensed simulation tool may be used.

Laboratory Experiments:

1. Verify (i) De Morgan's Theorem for 2 variables.

   (ii) The sum-of product and product-of-sum expressions using universal gates.

2. Design and implement

   (i) Half Adder & Full Adder using a) basic gates b) NAND gates

   (ii) Half subtractor & Full subtractor using a) basic gates b) NAND gates.

3. Design and implement

   (i) 4-bit Parallel Adder/Subtractor using IC 7483.

   (ii) BCD to Excess-3 code conversion and vice-versa.

4. Design and Implementation of

   (i) 1-bit Comparator.

   (ii) 5-bit Magnitude Comparator using IC 7485.

5. Realize

   (i) Adder & Subtractors using IC 74153.

   (ii) 4-variable function using IC74151(8:1MUX).

6. Realize

     (i) Adder &Subtractors using IC74139.

     (ii) Binary to Gray code conversion & vice-versa (74139)

7. Realize the following flip-flops using NAND Gates.

     Master-Slave JK, D & T Flip-Flops.

8. Realize the following shift registers using IC7474/7495

     (i) SISO (ii) SIPO (iii) PISO (iv) PIPO (v) Ring (vi) Johnson counter

9. Realize

     (i) Design Mod – N Synchronous Up Counter & Down Counter using 7476 JK Flip-flop

     (ii) Mod-N Counter using IC7490 / 7476

     (iii) Synchronous counter using IC74192

10. Design Pseudo Random Sequence generator using 7495.

11. Design Serial Adder with Accumulator and Simulate using Simulation tool.

12. Design Binary Multiplier and Simulate using Simulation tool.

Course Outcomes: On the completion of this laboratory course, the students will be able to:

1. Design, realize and verify De Morgan's Theorem, SOP, POS forms
2. Demonstrate the truth table of various expressions and combina- tional circuits using logic gates.
3. Design various combinational circuits such as adders, subtractors, com- parators, multiplexers and demultiplexers.
4. Construct flips-flops, counters and shift registers.
5. Simulate Serial adder and Binary Multiplier.

Conduct of Practical Examination:

•   All laboratory experiments are to be included for practical examination.

•   Students are allowed to pick one experiment from the lot.

•   Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.

•   Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

SEMESTER –II / III / IV
Aadalitha Kannada

Course Code : 18KAK39/49 CIE Marks : 100

Lecture Hours/Week (L:T:P) : (0: 2: 0)

Credits : 01

ಆಡಳಿತ ಕನ್ನಡ ಕಲಿಕೆಂಯು ಉದ್ದೇಶಗಳು:

* ಪದವಿ ವಿದ್ಯಾರ್ಥೀಳಾಗಿರುವುದರಿಂದ ಆಡಳಿತ ಕನ್ನಡದ ಪರಿಚಂಯು ವಂಾಡಿಕೊಡುವುದು.
* ವಿದ್ಯಾರ್ಥಿಗಳಲ್ಲಿ ಕನ್ನಡ ಭಾಷೆಯ ವ್ಯಾಕರಣದ ಬಗ್ಗೆ ಅರಿವು ಮೂಡಿಸುವುದು.
* ಕನ್ನಡ ಭಾಷಾ ರಚನೆಯಲ್ಲಿನ ನಯಮಗಳನ್ನು ಪರಿಚಯಿಸುವುದು.
* ಕನ್ನಡ ಭಾಷಾ ಬರಹದಲ್ಲಿ ಕಂಡುಬರುವ ದೋಷಗಳು ಹಾಗೂ ಅವುಗಳ ನವಾರಣೆ. ಮತ್ತು ಲೇಖನ ಚಿಹ್ನೆಗಳನ್ನು ಪರಿಚಯಿಸುವುದು.
* ಸಾಮಾನ್ಯ ಅರ್ಜಿಗಳು, ಸರ್ಕಾರಿ ಮತ್ತು ಅರೆ ಸರ್ಕಾರಿ ಪತ್ರವ್ಯವಹಾರದ ಬಗ್ಗೆ ಅರಿವು ಮೂಡಿಸುವುದು.
* ಭಾಷಾಂತರ ಮತ್ತು ಪ್ರಬಂಧ ರಚನೆ ಬಗ್ಗೆ ಅಸಕ್ತಿ ಮೂಡಿಸುವುದು.
* ಕನ್ನಡ ಭಾಷಾಭ್ಯಾಸ ಮತ್ತು ಸಾಮಾನ್ಯ ಕನ್ನಡ ಹಾಗೂ ಆಡಳಿತ ಕನ್ನಡದ ಪದಗಳ ಪರಿಚಯ ಮಾಡಿಕೊಡುವುದು.

ಪರಿವಿಡಿ (ಪಠ್ಯಪುಸ್ತಕದಲ್ಲಿರುವ ವಿಷಯಗಳ ಪಟ್ಟಿ)

ಅಧ್ಯಾಯ – 1 ಕನ್ನಡಭಾಷೆ – ಸಂಕ್ಷಿಪ್ತ ವಿವರಣೆ.

ಅಧ್ಯಾಯ – 2 ಭಾಷಾ ಪ್ರಯೋಗದಲ್ಲಾಗುವ ಲೋಪದೋಷಗಳು ಮತ್ತು ಅವುಗಳ ನವಾರಣೆ.

ಅಧ್ಯಾಯ – 3 ಲೇಖನ ಚಿಹ್ನೆಗಳು ಮತ್ತು ಅವುಗಳ ಉಪಯೋಗ.

ಅಧ್ಯಾಯ – 4 ಪತ್ರ ವ್ಯವಹಾರ.

ಅಧ್ಯಾಯ – 5 ಆಡಳಿತ ಪತ್ರಗಳು.

ಅಧ್ಯಾಯ – 6 ಸರ್ಕಾರದ ಆದೇಶ ಪತ್ರಗಳು.

ಅಧ್ಯಾಯ – 7 ಸಂಕ್ಷಿಪ್ತ ಪ್ರಬಂಧ ರಚನೆ (ಪ್ರೆಸ್ಸೆ ರೈಟಿಂಗ್), ಪ್ರಬಂಧ ಮತ್ತು ಭಾಷಾಂತರ.

ಅಧ್ಯಾಯ – 8 ಕನ್ನಡ ಶಬ್ದಸಂಗ್ರಹ.

ಅಧ್ಯಾಯ – 9 ಕಂಪ್ಯೂಟರ್ ಹಾಗೂ ಮಾಹಿತಿ ತಂತ್ರಜ್ಞಾನ.

ಅಧ್ಯಾಯ – 10 ಪಾರಿಭಾಷಿಕ ಆಡಳಿತ ಕನ್ನಡ ಪದಗಳು ಮತ್ತು ತಾಂತ್ರಿಕ/ ಕಂಪ್ಯೂಟರ್ ಪಾರಿಭಾಷಿಕ ಪದಗಳು.

ಆಡಳಿತ ಕನ್ನಡ ಕಲಿಕೆಂಯು ಫಲಿತಾಂಶಗಳು:

* ಆಡಳಿತ ಭಾಷೆ ಕನ್ನಡದ ಪರಿಚಂಯುವಾಗುತ್ತದೆ.
* ವಿದ್ಯಾರ್ಥಿಗಳಲ್ಲಿ ಕನ್ನಡ ಭಾಷೆಯ ವ್ಯಾಕರಣದ ಬಗ್ಗೆ ಅರಿವು ಮೂಡುತ್ತದೆ.
* ಕನ್ನಡ ಭಾಷಾ ರಚನೆಂಯುಲ್ಲಿನ ನಂಯುವುಗಳು ವುಂತ್ತು ಲೇಖನ ಚಿಹ್ನೆಗಳು ಪರಿಚಯಿಸಲ್ಪಡುತ್ತವೆ.

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- ಸಾಮಾನ್ಯ ಅರ್ಜಿಗಳು, ಸರ್ಕಾರಿ ಮತ್ತು ಅರೆ ಸರ್ಕಾರಿ ಪತ್ರವ್ಯವಹಾರದ ಬಗ್ಗೆ ಅರಿವು ಮೂಡುತ್ತದೆ.
- ಭಾಷಾಂತರ ಮತ್ತು ಪ್ರಬಂಧ್ ರಚನೆ ಬಗ್ಗೆ ಅಸಕ್ತಿ ವ್ಯೂಡುತ್ತದೆ.
- ಕನ್ನಡ ಭಾಷಾಭ್ಯಾಸ ಮತ್ತು ಸಾಮಾನ್ಯ ಕನ್ನಡ ಹಾಗೂ ಆಡಳಿತ ಕನ್ನಡದ ಪದಗಳು ಪರಿಚಯಿಸಲ್ಪಡುತ್ತವೆ.

ಪರೀಕ್ಷೆಯ ವಿಧಾನ : ನಿರಂತರ ಆಂತರಿಕ ವೌಲ್ಯಮಾಪನ – CIE (**Continuous Internal Evaluation**):
ಕಾಲೇಜು ಮಟ್ಟದಲ್ಲಿಯೆ ಆಂತರಿಕ ಪರೀಕ್ಷೆಯನ್ನು 100 ಅಂಕಗಳಿಗೆ ವಿಶ್ವವಿದ್ಯಾಲಯದ ನಿಯಮಗಳು ಮತ್ತು ನಿರ್ದೇಶನದಂತೆ ನಡೆಸತಕ್ಕದ್ದು.
ಪಠ್ಯಪುಸ್ತಕ : ಆಡಳಿತ ಕನ್ನಡ ಪಠ್ಯ ಪುಸ್ತಕ(**Kannada for Administration**)
ಸಂಪಾದಕರು
ಡಾ. ಎಲ್. ತಿಮ್ಮೇಶ
ಪ್ರೊ. ವಿ. ಕೇಶವಮೂರ್ತಿ
ಪ್ರಕಟಣೆ : ಪ್ರಸಾರಾಂಗ, ವಿಶ್ವೇಶ್ವರಯ್ಯ ತಾಂತ್ರಿಕ ವಿಶ್ವವಿದ್ಯಾಲಯ, ಬೆಳಗಾವಿ.

Vyavaharika Kannada

Course Code : 18KVK39/49	CIE Marks : 100
Lecture Hours/Week (L:T:P) : (0: 2: 0)	
Credits : 01	

Course Learning Objectives:

The course will enable the students to understand Kannada and communicate in Kannada language.

Table of Contents:

Chapter - 1: Vyavaharika kannada – Parichaya (Introduction to Vyavaharika Kannada).

Chapter - 2: Kannada Aksharamale haagu uchcharane (Kannada Alpabets and Pronunciation).

Chapter - 3: Sambhashanegaagi Kannada Padagalu (Kannada Vocabulary for Communication).

Chapter - 4: Kannada Grammar in Conversations (Sambhashaneyalli Kannada Vyakarana).

Chapter - 5: Activities in Kannada.

Course Outcomes:

At the end of the course, the student will be able to understand Kannada and communicate in Kannada language.

ಪರೀಕ್ಷೆಯ ವಿಧಾನ : ನಿರಂತರ ಆಂತರಿಕ ಮೌಲ್ಯಮಾಪನ CIE **(Continuous Internal Evaluation):**

ಕಾಲೇಜು ಮಟ್ಟದಲ್ಲಿಯೆ ಆಂತರಿಕ ಪರೀಕ್ಷೆಯನ್ನು 100 ಅಂಕಗಳಿಗೆ ವಿಶ್ವವಿದ್ಯಾಲಯದ ನಿಯಮಗಳು ಮತ್ತು ನಿರ್ದೇಶನದಂತೆ ನಡೆಸತಕ್ಕದ್ದು.

Textbook (ಪಠ್ಯಪುಸ್ತಕ): ವ್ಯಾವಹಾರಿಕ ಕನ್ನಡ ಪಠ್ಯ ಪುಸ್ತಕ **(Vyavaharika Kannada Text Book)** ಸಂಪಾದಕರು ಡಾ. ಎಲ್. ತಿಮ್ಮೇಶ ಪ್ರೊ. ವಿ. ಕೇಶವಮೂರ್ತಿ ಪ್ರಕಟಣೆ : ಪ್ರಸಾರಾಂಗ, ವಿಶ್ವೇಶ್ವರಯ್ಯ ತಾಂತ್ರಿಕ ವಿಶ್ವವಿದ್ಯಾಲಯ, ಬೆಳಗಾವಿ.

CONSTITUTION OF INDIA, PROFESSIONAL ETHICS AND CYBER LAW (CPC)

Course Code	: 18CPC39/49	CIE Marks : 40
Lecture Hours/Week (L:T:P)	: (1:0:0)	SEE Marks : 60
Credits : 01		Exam Hours : 02

Course Learning Objectives: To
- know the fundamental political codes, structure, procedures, powers, and duties of Indian government institutions, fundamental rights, directive principles, and the duties of citizens
- Understand engineering ethics and their responsibilities; identify their individual roles and ethical responsibilities towards society.
- Know about the cybercrimes and cyber laws for cyber safety measures.

Module-1
Introduction to Indian Constitution:
The Necessity of the Constitution, The Societies before and after the Constitution adoption. Introduction to the Indian constitution, The Making of the Constitution, The Role of the Constituent Assembly - Preamble and Salient features of the Constitution of India. Fundamental Rights and its Restriction and limitations in different Complex Situations. Directive Principles of State Policy (DPSP) and its present relevance in our society with examples. Fundamental Duties and its Scope and significance in Nation building.

Module-2
Union Executive and State Executive:
Parliamentary System, Federal System, Centre-State Relations. Union Executive – President, Prime Minister, Union Cabinet, Parliament - LS and RS, Parliamentary Committees, Important Parliamentary Terminologies. Supreme Court of India, Judicial Reviews and Judicial Activism. State Executives – Governor, Chief Minister, State Cabinet, State Legislature, High Court and Subordinate Courts, Special Provisions (Articles 370, 371,371J) for some States.

Module-3
Elections, Amendments and Emergency Provisions:
Elections, Electoral Process, and Election Commission of India, Election Laws. Amendments - Methods in Constitutional Amendments (How and Why) and Important Constitutional Amendments. Amendments – 7, 9, 10, 12, 42, 44,

61, 73, 74, 75, 86 and 91, 94, 95, 100, 101, 118 and some important Case Studies. Emergency Provisions, types of Emergencies and its consequences.
Constitutional special provisions:
Special Provisions for SC and ST, OBC, Women, Children and Backward Classes.

Module-4
Professional / Engineering Ethics:
Scope & Aims of Engineering & Professional Ethics - Business Ethics, Corporate Ethics, Personal Ethics. Engineering and Professionalism, Positive and Negative Faces of Engineering Ethics, Code of Ethics as defined in the website of Institution of Engineers (India): Profession, Professionalism, and Professional Responsibility. Clash of Ethics, Conflicts of Interest. Responsibilities in Engineering Responsibilities in Engineering and Engineering Standards, the impediments to Responsibility. Trust and Reliability in Engineering, IPRs (Intellectual Property Rights), Risks, Safety and liability in Engineering

Module-5
Internet Laws, Cyber Crimes and Cyber Laws:
Internet and Need for Cyber Laws, Modes of Regulation of Internet, Types of cyber terror capability, Net neutrality, Types of Cyber Crimes, India and cyber law, Cyber Crimes and the information Technology Act 2000, Internet Censorship. Cybercrimes and enforcement agencies.

Course Outcomes: On completion of this course, students will be able to,
 1. Describe and analyze the role and salient features of the Indian Constitution
 2. Understand the structure and powers of the Union and State Executives.
 3. Relate to the procedures and provisions in the electoral process.
 4. Develop Engineering and Professional ethics and adopt the responsibilities expected of an Engineer.
 5. Identify the cybercrimes and describe the cyber laws for cyber safety measures.

Question paper pattern for SEE and CIE:
- The SEE question paper will be set for 100 marks and the marks scored by the students will proportionately be reduced to 60. The pattern of the question paper will be objective type (MCQ).
- For the award of 40 CIE marks, refer the University regulations 2018.

Textbook/s
 1. Constitution of India, Professional Ethics and Human Rights, Shubham Singles, Charles E. Haries, and et al, Cengage Learning India, 2018

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2. Cyber Security and Cyber Laws, Alfred Basta and et. al., Cengage Learning India, 2018

Reference Books
1. Introduction to the Constitution of India, Durga Das Basu, Prentice – Hall, 2008.
2. Engineering Ethics, M. Govindarajan, S. Natarajan, V. S. Senthilkumar, Prentice – Hall, 2004

ADDITIONAL MATHEMATICS – I

Course Code	: 18MATDIP31	CIE Marks : 40	
Lecture Hours/Week (L:T:P) : (2:1:0)		SEE Marks : 60	
Credits : 0		Exam Hours : 03	

Course Learning Objectives:

- To provide basic concepts of complex trigonometry, vector algebra, differential and integral calculus.
- To provide an insight into vector differentiation and first order ODEs.

Module-1

Complex Trigonometry: Complex Numbers: Definitions and properties. Modulus and amplitude of a complex number, Argand's diagram, De-Moivre's theorem (without proof).
Vector Algebra: Scalar and vectors. Addition and subtraction and multiplication of vectors- Dot and Cross products, problems.

Module-2

Differential Calculus: Review of elementary differential calculus. Polar curves –angle between the radius vector and the tangent pedal equation- Problems. Maclaurin's series expansions, problems.
Partial Differentiation: Euler's theorem for homogeneous functions of two variables. Total derivatives - differentiation of composite function. Application to Jacobians of order two.

Module-3

Vector Differentiation: Differentiation of vector functions. Velocity and acceleration of a particle moving on a space curve. Scalar and vector point functions. Gradient, Divergence, Curl and Laplacian (Definitions only). Solenoidal and irrotational vector fields-Problems.

Module-4

Integral Calculus: Review of elementary integral calculus. Statement of reduction formulae for $\sin^n x, \cos^n x, and \sin^m x \times \cos^n x$ and evaluation of these with standard limits-Examples. Double and triple integrals, problems.

Module-5

Ordinary differential equations (ODEs): Introduction-solutions of first order and first degree differential equations: Variable Separable methods, exact and linear differential equations of order one. Application to Newton's law of cooling.

Course Outcomes: At the end of the course the student will be able to:
1. Apply concepts of complex numbers and vector algebra to analyze the problems arising in related area.
2. Use derivatives and partial derivatives to calculate rate of change of multivariate functions.
3. Analyze position, velocity and acceleration in two and three dimensions of vector valued functions.
4. Learn techniques of integration including the evaluation of double and triple integrals.
5. Identify and solve first order ordinary differential equations.

Question paper pattern:
- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Textbook
1. Higher Engineering Mathematics, B.S. Grewal, Khanna Publishers, 43rd Edition, 2015

Reference Books

1. Advanced Engineering Mathematics, E. Kreyszig, John Wiley & Sons, 10th Edition, 2015
2. Engineering Mathematics Vol.I, Rohit Khurana, Cengage Learning, 2015

B. E. Common to all Programmes
Choice Based Credit System (CBCS) and Outcome Based Education (OBE)
SEMESTER - IV

COMPLEX ANALYSIS, PROBABILITY AND STATISTICAL METHODS

Course Code	: 18MAT41	CIE Marks	: 40
Lecture Hours/Week (L:T:P) : (2:2:0)		SEE Marks	: 60
Total Number of Lecture Hours :40 (8 Hrs / Module)		Exam Hours	: 03
CREDITS : 03			

Course Learning Objectives:

- To provide an insight into applications of complex variables, conformal mapping and special functions arising in potential theory, quantum mechanics, heat conduction and field theory.
- To develop probability distribution of discrete, continuous random variables and joint probability distribution occurring in digital signal processing, design engineering and microwave engineering.

Module-1
Calculus of complex functions: Review of function of a complex variable, limits, continuity, and differentiability. Analytic functions: Cauchy-Riemann equations in Cartesian and polar forms and consequences.
Construction of analytic functions: Milne-Thomson method-Problems.

Module-2
Conformal transformations: Introduction. Discussion of transformations: $w = Z^2$, $w = e^z$, $w = z + 1/z$ $(z \neq 0)$. Bilinear transformations- Problems.
Complex integration: Line integral of a complex function-Cauchy's theorem and Cauchy's integral formula and problems.

Module-3
Probability Distributions: Review of basic probability theory. Random variables (discrete and continuous), probability mass/density functions. Binomial, Poisson, exponential and normal distributions- problems (No derivation for mean and standard deviation)-Illustrative examples.

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Module-4

Statistical Methods: Correlation and regression-Karl Pearson's coefficient of correlation and rank correlation -problems. Regression analysis- lines of regression –problems.

Curve Fitting: Curve fitting by the method of least squares- fitting the curves of the form-

$y = ax + b, y = ax^b$ and $y = ax^2 + bx + c$

Module-5

Joint probability distribution: Joint Probability distribution for two discrete random variables, expectation and covariance.

Sampling Theory: Introduction to sampling distributions, standard error, Type-I and Type-II errors. Test of hypothesis for means, student's t-distribution, Chi-square distribution as a test of goodness of fit.

Course Outcomes:

At the end of the course the student will be able to:

1. Use the concepts of analytic function and complex potentials to solve the problems arising in electromagnetic field theory.

2. Utilize conformal transformation and complex integral arising in aerofoil theory, fluid flow visualization and image processing.

3. Apply discrete and continuous probability distributions in analyzing the probability models arising in engineering field.

4. Make use of the correlation and regression analysis to fit a suitable mathematical model for the statistical data.

5. Construct joint probability distributions and demonstrate the validity of testing the hypothesis.

Question paper pattern:

*   Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
*   Each full question can have a maximum of 4 sub questions.
*   There will be 2 full questions from each module covering all the topics of the module.
*   Students will have to answer 5 full questions, selecting one full question from each module.
*   The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Textbooks

1. Advanced Engineering Mathematics, E. Kreyszig, John Wiley & Sons, 10th Edition, 2016
2. Higher Engineering Mathematics, B. S. Grewal, Khanna Publishers, 44th Edition, 2017
3. Engineering Mathematics, Srimanta Pal et. al., Oxford University Press, 3rd Edition, 2016

Reference Books
1. Advanced Engineering Mathematics, C. Ray Wylie, Louis C. Barrett, McGraw-Hill , 6th Edition 1995
2. Introductory Methods of Numerical Analysis, S.S.Sastry, Prentice Hall of India, 4th Edition 2010
3. Higher Engineering Mathematics, B. V. Ramana, McGraw-Hill, 11th Edition, 2010
4. A Text Book of Engineering Mathematics, N. P. Bali and Manish Goyal, Laxmi Publications, 2014

Web links and Video Lectures:
1. http://nptel.ac.in/courses.php?disciplineID=111
2. http://www.class-central.com/subject/math(MOOCs)
3. http://academicearth.org/
4. VTU EDUSAT PROGRAMME - 20

B. E. 2018 Scheme Fourth Semester Syllabus (EC / TC)

Choice Based Credit System (CBCS) and Outcome Based Education (OBE)

ANALOG CIRCUITS

Course Code	: **18EC42**	CIE Marks : 40
Lecture Hours/Week : 03 + 2 (Tutorial)		SEE marks : 60
Total Number of Lecture Hours : 50 (10 Hrs / Module)		Exam Hours : 03
CREDITS : 04		

Course Learning Objectives: This course will enable students to:
- Explain various BJT parameters, connections and configurations.
- Design and demonstrate the diode circuits and transistor amplifiers.
- Explain various types of FET biasing, and demonstrate the use of FET amplifiers.
- Construct frequency response of FET amplifiers at various frequencies.
- Analyze Power amplifier circuits in different modes of operation.
- Construct Feedback and Oscillator circuits using FET.

Module -1

BJT Biasing: Biasing in BJT amplifier circuits: The Classical Discrete circuit bias (Voltage-divider bias), Biasing using a collector to base feedback resistor. **Small signal operation and Models**: Collector current and transconductance, Base current and input resistance, Emitter current and input resistance, voltage gain, Separating the signal and the DC quantities, The hybrid Π model. **MOSFETs: Biasing in MOS amplifier circuits:** Fixing V_{GS}, Fixing V_G, Drain to Gate feedback resistor.
Small signal operation and modeling: The DC bias point, signal current in drain, voltage gain, small signal equivalent circuit models, transconductance. **[Text 1: 3.5(3.5.1, 3.5.3), 3.6(3.6.1 to 3.6.6), 4.5(4.5.1, 4.5.2, 4.5.3), 4.6(4.6.1 to 4.6.6)]**   **L1, L2,L3**

Module -2

MOSFET Amplifier configuration: Basic configurations, characterizing amplifiers, CS amplifier with and without source resistance R_S, Source follower. **MOSFET internal capacitances and High frequency model:** The gate capacitive effect, Junction capacitances, High frequency model.
Frequency response of the CS amplifier: The three frequency bands, high frequency response, Low frequency response.
Oscillators: FET based Phase shift oscillator, LC and Crystal Oscillators (no derivation)

[Text 1: 4.7(4.7.1 to 4.7.4, 4.7.6) 4.8(4.8.1, 4.8.2, 4.8.3), 4.9, 12.2.2, 12.3.1, 12.3.2] **L1, L2, L3**

Module -3

Feedback Amplifier: General feedback structure, Properties of negative feedback, The Four Basic Feedback Topologies, The series-shunt, series-series, shunt-shunt and shunt-series amplifiers (Qualitative Analysis).

Output Stages and Power Amplifiers: Introduction, Classification of output stages,, Class A output stage, Class B output stage: Transfer Characteristics, Power Dissipation, Power Conversion efficiency, Class AB output stage, Class C tuned Amplifier.

[Text 1: 7.1, 7.2, 7.3, 7.4.1, 7.5.1, 7.6 (7.6.1 to 7.6.3), 13.1, 13.2, 13.3 (13.3.1, 13.3.2, 13.3.3, 13.4, 13.7)] **L1, L2, L3**

Module -4

Op-Amp with Negative Feedback and general applications
Inverting and Non inverting Amplifiers – Closed Loop voltage gain, Input impedance, Output impedance, Bandwidth with feedback. DC and AC Amplifiers, Summing, Scaling and Averaging Amplifiers, Instrumentation amplifier, Comparators, Zero Crossing Detector, Schmitt trigger.

[Text 2: 3.3(3.3.1 to 3.3.6), 3.4(3.4.1 to 3.4.5) 6.2, 6.5, 6.6 (6.6.1), 8.2, 8.3, 8.4] **L1, L2, L3**

Module -5

Op-Amp Circuits: DAC - Weighted resistor and R-2R ladder, ADC-Successive approximation type, Small Signal half wave rectifier, Active Filters, First and second order low-pass and high-pass Butterworth filters, Band-pass filters, Band reject filters.

555 Timer and its applications: Monostable and a stable Multivibrators.

[Text 2: 8.11(8.11.1a, 8.11.1b), 8.11.2a, 8.12.2, 7.2, 7.3, 7.4, 7.5, 7.6, 7.8, 7.9, 9.4.1, 9.4.1(a), 9.4.3, 9.4.3(a)]

L1, L2, L3

Course Outcomes: At the end of this course students will demonstrate the ability to
1. Understand the characteristics of BJTs and FETs.
2. Design and analyze BJT and FET amplifier circuits.
3. Design sinusoidal and non-sinusoidal oscillators.
4. Understand the functioning of linear ICs.
5. Design of Linear IC based circuits.

Question paper pattern:
- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:
1. Microelectronic Circuits, Theory and Applications, Adel S Sedra, Kenneth C Smith, 6th Edition, Oxford, 2015. ISBN:978-0-19-808913-1
2. Op-Amps and Linear Integrated Circuits, Ramakant A Gayakwad, 4th Edition. Pearson Education, 2000. ISBN: 8120320581

Reference Books:
1. Electronic Devices and Circuit Theory, Robert L Boylestad and Louis Nashelsky, 11th Edition, Pearson Education, 2013, ISBN: 978-93-325-4260-0.
2. Fundamentals of Microelectronics, Behzad Razavi, 2nd Edition, John Weily, 2015, ISBN 978-81-265-7135-2
3. J.Millman & C.C. Halkias—Integrated Electronics, 2nd edition, 2010, TMH. ISBN 0-07-462245-5

CONTROL SYSTEMS

Course Code	: **18EC43**	CIE Marks : 40
Lecture Hours/Week : 3		SEE Marks : 60
Total Number of Lecture Hours : 40(8 Hrs/Module)		Exam Hours: 03

CREDITS – 03

Course Learning Objectives: This course will enable students to:

- Understand the basic features, configurations and application of control systems.
- Understand various terminologies and definitions for the control systems.
- Learn how to find a mathematical model of electrical, mechanical and electro- mechanical systems.
- Know how to find time response from the transfer function.
- Find the transfer function via Masons' rule.
- Analyze the stability of a system from the transfer function.

Module – 1
Introduction to Control Systems: Types of Control Systems, Effect of Feedback Systems, Differential equation of Physical Systems –Mechanical Systems, Electrical Systems, Electromechanical systems, Analogous Systems.
L1, L2, L3

Module – 2
Block diagrams and signal flow graphs: Transfer functions, Block diagram algebra and Signal Flow graphs.
L1, L2, L3

Module – 3
Time Response of feedback control systems: Standard test signals, Unit step response of First and Second order Systems. Time response specifications, Time response specifications of second order systems, steady state errors and error constants. Introduction to PI, PD and PID Controllers (excluding design).
L1, L2, L3

Module – 4
Stability analysis: Concepts of stability, Necessary conditions for Stability, Routh stability criterion, Relative stability analysis: more on the Routh stability criterion.
Introduction to Root-Locus Techniques, The root locus concepts, Construction of rootloci.

Frequency domain analysis and stability: Correlation between time and frequency response, Bode Plots, Experimental determination of transfer function.

<div align="right">

L1, L2, L3

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Module – 5

Introduction to Polar Plots, (Inverse Polar Plots excluded) Mathematical preliminaries, Nyquist Stability criterion, (Systems with transportation lag excluded)

Introduction to lead, lag and lead- lag compensating networks (excluding design).

Introduction to State variable analysis: Concepts of state, state variable and state models for electrical systems, Solution of state equations.

<div align="right">

L1, L2, L3

</div>

Course Outcomes: At the end of the course, the students will be able to

1. Develop the mathematical model of mechanical and electrical systems.
2. Develop transfer function for a given control system using block diagram reduction techniques and signal flow graph method.
3. Determine the time domain specifications for first and second order systems.
4. Determine the stability of a system in the time domain using Routh-Hurwitz criterion and Root-locus technique.
5. Determine the s stability of a system in the frequency domain using Nyquist and bode plots.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

1. J. Nagarath and M. Gopal, "Control Systems Engineering", New Age International(P) Limited, Publishers, Fifth edition- 2005, ISBN: 81 - 224 - 2008-7.

Reference Books:
1. "Modern Control Engineering", K. Ogata, Pearson Education Asia/ PHI, 4th Edition, 2002. ISBN 978 - 81 - 203 - 4010 - 7.
2. "Automatic Control Systems", Benjamin C. Kuo, John Wiley India Pvt. Ltd., 8th Edition, 2008.
3. "Feedback and Control System," Joseph J Distefano III et. al., Schaum's Outlines, TMH, 2nd Edition 2007.

ENGINEERING STATISTICS and LINEAR ALGEBRA

Course Code	: **18EC44**	CIE Marks : 40	
Lecture Hours/Week : 03		SEE Marks : 60	
Total Number of Lecture Hours: 40 (8 Hrs / Module)		Exam Hours : 03	
CREDITS – 03			

Course Learning Objectives: This course will enable students to:
- Understand and Analyze Single and Multiple Random Variables, and their extension to Random Processes.
- Familiarization with the concept of Vector spaces and orthogonality with a qualitative insight into applications in communications.
- Compute the quantitative parameters for functions of single and Multiple Random Variables and Processes.
- Compute the quantitative parameters for Matrices and Linear Transformations.

Module-1
Single Random Variables: Definition of random variables, cumulative distribution function continuous and discrete random variables; probability mass function, probability density functions and properties; Expectations, Characteristic functions, Functions of single Random Variables, Conditioned Random variables. Application exercises to Some special distributions: Uniform, Exponential, Laplace, Gaussian, Binomial, and Poisson distribution.
(Chapter 4 Text 1), **L1, L2, L3**

Module -2
Multiple Random variables: Concept, Two variable CDF and PDF, Two Variable expectations (Correlation, orthogonality, Independent), Two variable transformation, Two Gaussian Random variables, Sum of two independent Random Variables, Sum of IID Random Variables – Central limit Theorem and law of large numbers, Conditional joint Probabilities, Application exercises to Chi-square RV, Student-T RV, Cauchy and Rayleigh RVs.
(Chapter 5 Text 1), **L1, L2, L3**

Module-3
Random Processes: Ensemble, PDF, Independence, Expectations, Stationarity, Correlation Functions (ACF, CCF, Addition, and Multiplication), Ergodic Random Processes, Power Spectral Densities (Wiener Khinchin, Addition and Multiplication of RPs, Cross spectral densities), Linear Systems (output Mean, Cross correlation and Auto correlation of Input and output), Exercises with Noise. **(Chapter 6 Text 1)**, **L1, L2, L3**

Module -4

Vector Spaces: Vector spaces and Null subspaces, Rank and Row reduced form, Independence, Basis and dimension, Dimensions of the four subspaces, Rank-Nullity Theorem, Linear Transformations
Orthogonality: Orthogonal Vectors and Subspaces, Projections and Least squares, Orthogonal Bases and Gram- Schmidt Orthogonalization procedure.
(Refer Chapters 2 and 3 Text 2),   **L1, L2, L3**

Module -5

Determinants: Properties of Determinants, Permutations and Cofactors.
(Refer Chapter 4, Text 2)
Eigen values and Eigen vectors: Review of Eigenvalues and Diagonalization of a Matrix, Special Matrices (Positive Definite, Symmetric) and their properties, Singular Value Decomposition.
(Refer Chapter 5, Text 2),   **L1, L2, L3**

Course Outcomes: After studying this course, students will be able to:
1. Analyze and evaluate single and multiple random variables.
2. Identify and associate Random Variables and Random Processes in Communication events.
3. Analyze and model the Random events in typical communication events to extract quantitative statistical parameters.
4. Analyze and model typical signal sets in terms of a basis function set of Amplitude, phase and frequency.
5. Demonstrate by way of simulation or emulation the ease of analysis employing basis functions, statistical representation and Eigen values.

Question paper pattern:
- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:
1. Richard H Williams, "Probability, Statistics and Random Processes for Engineers" Cengage Learning, 1st Edition, 2003, ISBN 13: 978-0-534- 36888-3, ISBN 10: 0-534-36888-3.

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2.   Gilbert Strang, "Linear Algebra and its Applications", Cengage Learning, 4th Edition, 2006, ISBN 97809802327

Reference Books:

1.   Hwei P. Hsu, "Theory and Problems of Probability, Random Variables, and Random Processes" Schaums Outline Series, McGraw Hill. ISBN 10: 0-07- 030644-3.
2.   K. N. HariBhat, K Anitha Sheela, Jayant Ganguly, "Probability Theory and Stochastic Processes for Engineers", Cengage Learning India, 2019

SIGNALS AND SYSTEMS

Course Code	: **18EC45**	CIE Marks : 40
Lecture Hours/Week : 03		SEE Marks : 60
Total Number of Lecture Hours : 40 (8 Hours / Module)		Exam Hours : 03
CREDITS – 03		

Course Learning Objectives: This course will enable students to:

- Understand the mathematical description of continuous and discrete time signals and systems.
- Analyze the signals in time domain using convolution sum and Integral.
- Classify signals into different categories based on their properties.
- Analyze Linear Time Invariant (LTI) systems in time and transform domains.

Module-1

Introduction and Classification of signals: Definition of signal and systems, communication and control system as examples Classification of signals.

Basic Operations on signals: Amplitude scaling, addition, multiplication, differentiation, integration, time scaling, time shift and time reversal.

Elementary signals/Functions: Exponential, sinusoidal, step,impulse and ramp functions. Expression of triangular, rectangular and other waveforms in terms of elementary signals.,

L1, L2, L3

Module -2

System Classification and properties: Linear-nonlinear, Time variant -invariant, causal-noncausal, static-dynamic, stable-unstable, invertible.

Time domain representation of LTI System: Impulse response, convolution sum, convolution integral. Computation of convolution sum and convolution integral using graphical method for unit step and unit step, unit step and exponential, exponential and exponential, unit step and rectangular, and rectangular and rectangular.

L1, L2, L3

Module-3

LTI system Properties in terms of impulse response: System interconnection, Memory less, Causal, Stable, Invertible and Deconvolution, and step response.

Fourier Representation of Periodic Signals: CTFS properties and basic problems.

L1, L2, L3

Module -4

Fourier Representation of aperiodic Signals: Introduction to Fourier Transform & DTFT, Definition and basic problems.

82

Properties of Fourier Transform: Linearity, Time shift, Frequency shift, Scaling, Differentiation and Integration, Convolution and Modulation, Parseval's theorem and problems on properties of Fourier Transform.

L1, L2, L3

Module -5

The Z-Transforms: Z transform, properties of the region of convergence, properties of the Z-transform, Inverse Z-transform, Causality and stability, Transform analysis of LTI systems. **L1, L2, L3**

Course Outcomes: At the end of the course, students will be able to:
1. Analyze the different types of signals and systems.
2. Determine the linearity, causality, time-invariance and stability properties of continuous and discrete time systems.
3. Evaluate the convolution sum and integral.
4. Represent continuous and discrete signals & systems in frequency domain using Fourier representations.
5. Analyze discrete time signals and systems using Z-transforms.

Question paper pattern:
- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:
1. Simon Haykin and Barry Van Veen, "Signals and Systems", 2nd Edition, 2008, Wiley India. ISBN 9971-51-239-4.

Reference Books:
1. **Michael Roberts,** "Fundamentals of Signals & Systems", 2nd edition, Tata McGraw-Hill, 2010, ISBN 978-0-07-070221-9.
2. **Alan V Oppenheim, Alan S Willsky and S Hamid Nawab,** "Signals and Systems" Pearson Education Asia / PHI, 2nd edition, 1997. Indian Reprint 2002.
3. **H.P Hsu, R. Ranjan,** "Signals and Systems", Schaum's outlines, TMH, 2006.
4. **B. P. Lathi,** "Linear Systems and Signals", Oxford University Press, 2005.
5. **Ganesh Rao and Satish Tunga,** "Signals and Systems", Pearson/ Sanguine.

MICROCONTROLLER

Course Code	: **18EC46**	CIE Marks : 40
Lecture Hours/Week : 03		SEE Marks : 60
Total Number of Lecture Hours : 40 (8 Hours / Module)		Exam Hours:03

CREDITS – 03

Course Learning Objectives: This course will enable students to:

- Understand the difference between a Microprocessor and a Microcontroller and embedded microcontrollers.
- Familiarize the basic architecture of 8051 microcontroller.
- Program 8051microprocessor using Assembly Level Language and C.
- Understand the interrupt system of 8051 and the use of interrupts.
- Understand the operation and use of inbuilt Timers/Counters and Serial port of 8051.
- Interface 8051 to external memory and I/O devices using its I/O ports.

Module-1

8051 Microcontroller: Microprocessor vs Microcontroller, Embedded Systems, Embedded Microcontrollers, 8051 Architecture- Registers, Pin diagram, I/O ports functions, Internal Memory organization. External Memory (ROM & RAM) interfacing.

L1, L2

Module -2

8051 Instruction Set: Addressing Modes, Data Transfer instructions, Arithmetic instructions, Logical instructions, Branch instructions, Bit manipulation instructions. Simple Assembly language program examples (without loops) to use these instructions.

L1, L2

Module-3

8051 Stack, I/O Port Interfacing and Programming: 8051 Stack, Stack and Subroutine instructions. Assembly language program examples on subroutine and involving loops.

Interfacing simple switch and LED to I/O ports to switch on/off LED with respect to switch status. **L1, L2, L3**

Module -4

8051 Timers and Serial Port: 8051 Timers and Counters – Operation and Assembly language programming to generate a pulse using Mode-1 and a square wave using Mode-2 on a port pin. 8051 Serial Communication- Basics of Serial Data Communication, RS-232 standard, 9 pin RS232 signals, Simple Serial Port programming in Assembly and C to transmit a message and to receive data serially. **L1, L2, L3**

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Module -5

8051 Interrupts and Interfacing Applications: 8051 Interrupts. 8051 Assembly language programming to generate an external interrupt using a switch, 8051 C programming to generate a square waveform on a port pin using a Timer interrupt. Interfacing 8051 to ADC-0804, DAC, LCD and Stepper motor and their 8051 Assembly language interfacing programming.

L1, L2, L3

Course outcomes: At the end of the course, students will be able to:

1. Explain the difference between Microprocessors & Microcontrollers, Architecture of 8051 Microcontroller, Interfacing of 8051 to external memory and Instruction set of 8051.
2. Write 8051 Assembly level programs using 8051 instruction set.
3. Explain the Interrupt system, operation of Timers/Counters and Serial port of 8051.
4. Write 8051 Assembly language programs to generate square wave on 8051 I/O port pin using interrupt and C Programme to send & receive serial data using 8051 serial port.
5. Interface simple switches, simple LEDs, ADC 0804, LCD and Stepper Motor to 8051 using 8051 I/O ports.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. "The 8051 Microcontroller and Embedded Systems – using assembly and C", Muhammad Ali Mazidi and Janice Gillespie Mazidi and Rollin D. McKinlay; PHI, 2006 / Pearson, 2006.
2. "The 8051 Microcontroller", Kenneth J. Ayala, 3rd Edition, Thomson/ Cengage Learning.

Reference Books:
1. "The 8051 Microcontroller Based Embedded Systems", Manish K Patel, McGraw Hill, 2014, ISBN: 978-93-329-0125-4.
2. "Microcontrollers: Architecture, Programming, Interfacing and System Design", Raj Kamal, Pearson Education, 2005.

MICROCONTROLLER LABORATORY

Laboratory Code : **18ECL47**	CIE Marks : 40	SEE Marks : 60

Lecture Hours/Week : 02 Hours Tutorial (Instructions) + 02 Hours Laboratory

RBT Levels : L1, L2, L3	Exam Hours : 03

CREDITS 02

Course Learning Objectives: This laboratory course enables students to

- Understand the basics of microcontroller and its applications.
- Have in-depth knowledge of 8051 assembly language programming.
- Understand controlling the devices using C programming.
- The concepts of I/O interfacing for developing real time embedded systems.

Laboratory Experiments
I. PROGRAMMING
1. Data Transfer: Block Move, Exchange, Sorting, Finding largest element in an array.
2. Arithmetic Instructions - Addition/subtraction, multiplication and division, square, Cube – (16 bits Arithmetic operations – bit addressable).
3. Counters.
4. Boolean & Logical Instructions (Bit manipulations).
5. Conditional CALL & RETURN.
6. Code conversion: BCD – ASCII; ASCII – Decimal; Decimal - ASCII; HEX - Decimal and Decimal - HEX.
7. Programs to generate delay, Programs using serial port and on-Chip timer/counter.

II. INTERFACING
1. Interface a simple toggle switch to 8051 and write an ALP to generate an interrupt which switches on an LED (i) continuously as long as switch is on and (ii) only once for a small time when the switch is turned on.
2. Write a C program to (i) transmit and (ii) to receive a set of characters serially by interfacing 8051 to a terminal.
3. Write ALPs to generate waveforms using ADC interface.
4. Write ALP to interface an LCD display and to display a message on it.
5. Write ALP to interface a Stepper Motor to 8051 to rotate the motor.
6. Write ALP to interface ADC-0804 and convert an analog input connected to it.

Course Outcomes: On the completion of this laboratory course, the students will be able to:
1. Enhance programming skills using Assembly language and C.
2. Write Assembly language programs in 8051 for solving simple problems that manipulate input data using different instructions of 8051.
3. Interface different input and output devices to 8051 and control them using Assembly language programs.
4. Interface the serial devices to 8051 and do the serial transfer using C programming.
5. Develop applications based on Microcontroller 8051.

Conduct of Practical Examination:
- All laboratory experiments are to be included for practical examination.
- Students are allowed to pick one experiment from the lot.
- Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.
- Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

ANALOG CIRCUITS LABORATORY

Laboratory Code : **18ECL48**	CIE Marks : 40	SEE Marks : 60

Lecture Hours/Week : 02 Hours Tutorial (Instructions) + 02 Hours Laboratory

RBT Levels : L1, L2, L3	Exam Hours : 03

CREDITS 02

Course Learning Objectives: This laboratory course enables students to

- Understand the circuit configurations and connectivity of BJT and FET Amplifiers and Study of frequency response
- Design and test of analog circuits using OPAMPs
- Understand the feedback configurations of transistor and OPAMP circuits
- Use of circuit simulation for the analysis of electronic circuits.

Laboratory Experiments
PART A : Hardware Experiments
1. Design and setup the Common Source JFET/MOSFET amplifier and plot the frequency response.
2. Design and set up the BJT common emitter voltage amplifier with and without feedback and determine the gain- bandwidth product, input and output impedances.
3. Design and set-up BJT/FET i) Colpitts Oscillator and ii) Crystal Oscillator
4. Design active second order Butterworth low pass and high pass filters.
5. Design Adder, Integrator and Differentiator circuits using Op-Amp
6. Test a comparator circuit and design a Schmitt trigger for the given UTP and LTP values and obtain the hysteresis.
7. Design 4 bit R – 2R Op-Amp Digital to Analog Converter (i) using 4 bit binary input from toggle switches and (ii) by generating digital inputs using mod-16 counter.
8. Design Monostable and a stable Multivibrator using 555 Timer.

PART-B : Simulation using EDA software (EDWinXP, PSpice, MultiSim, Proteus, CircuitLab or any other equivalent tool can be used)
1. RC Phase shift oscillator and Hartley oscillator
2. Narrow Band-pass Filter and Narrow band-reject filter
3. Precision Half and full wave rectifier
4. Monostable and Astable Multivibrator using 555 Timer.

Course Outcomes: On the completion of this laboratory course, the students will be able to:
1. Analyze Frequency response of JFET/MOSFET amplifier.
2. Design BJT/FETs amplifier with and without feedback and evaluate their performance characteristics.
3. Apply the knowledge gained in the design of BJT/FET circuits in Oscillators.
4. Design analog circuits using OPAMPs for different applications.
5. Simulate and analyze analog circuits that uses ICs for different electronic applications.

Conduct of Practical Examination:
- All laboratory experiments are to be included for practical examination.
- Students are allowed to pick one experiment from the lot.
- Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.
- Change of experiment is allowed only once and Marks allotted to the procedure part to be made zero.

Reference Books:
1. David A Bell, "Fundamentals of Electronic Devices and Circuits Lab Manual, 5th Edition, 2009, Oxford University Press.

ADDITIONAL MATHEMATICS – II

Course Code	: **18MATDIP41**	CIE Marks	: 40
Lecture Hours/Week (L:T:P),	: (2:1:0)	SEE Marks	: 60
Credits	: 0	Exam Hours	: 03

Course Learning Objectives:

- To provide essential concepts of linear algebra, second & higher order differential equations along with methods to solve them.
- To provide an insight into elementary probability theory and numerical methods.

Module-1

Linear Algebra: Introduction - rank of matrix by elementary row operations - Echelon form. Consistency of system of linear equations - Gauss elimination method. Eigen values and Eigen vectors of a square matrix. Problems.

Module-2

Numerical Methods: Finite differences. Interpolation/extrapolation using Newton's forward and backward difference formulae (Statements only)- problems. Solution of polynomial and transcendental equations – Newton-Raphson and Regula-Falsi methods (only formulae)- Illustrative examples. Numerical integration: Simpson's one third rule and Weddle's rule (without proof) Problems.

Module-3

Higher order ODEs: Linear differential equations of second and higher order equations with constant coefficients. Homogeneous /non-homogeneous equations. Inverse differential operators. *[Particular Integral restricted to R(x)=* e^{ax}*, $\sin ax$ /$\cos ax$ for $f(D)y = R(x)$.]*

Module-4

Partial Differential Equations (PDEs):- Formation of PDEs by elimination of arbitrary constants and functions. Solution of non-homogeneous PDE by direct integration. Homogeneous PDEs involving derivative with respect to one independent variable only.

Module-5

Probability: Introduction. Sample space and events. Axioms of probability. Addition & multiplication theorems. Conditional probability, Bayes' theorem, problems.

Course Outcomes: At the end of the course the student will be able to:
1. Solve systems of linear equations using matrix algebra.
2. Apply the knowledge of numerical methods in modelling and solving engineering problems.
3. Make use of analytical methods to solve higher order differential equations.
4. Classify partial differential equations and solve them by exact methods.
5. Apply elementary probability theory and solve related problems.

Question paper pattern:
- The question paper will have ten full questions carrying equal marks.
- Each full question will be for 20 marks.
- There will be two full questions (with a maximum of four sub- questions) from each module.
- Each full question will have sub- question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

Textbook
1. Higher Engineering Mathematics, B.S. Grewal, Khanna Publishers, 43rd Edition, 2015

Reference Books
1. Advanced Engineering Mathematics, E. Kreyszig, John Wiley & Sons, 10th Edition, 2015
2. Engineering Mathematics, N. P. Bali and Manish Goyal, Laxmi Publishers, 7th Edition, 2007
3. Engineering Mathematics, Vol. I, Rohit Khurana, Cengage Learning, 1st Edition, 2015

Choice Based Credit System (CBCS) and Outcome Based Education (OBE)

SEMESTER – V

TECHNOLOGICAL INNOVATION MANAGEMENT AND ENTREPRENEURSHIP

Course Code	: **18ES51**	CIE Marks : 40
Lecture Hours/Week	: 03	SEE Marks : 60
Total Number of Lecture Hours : 40 (08 Hours / Module) Exam Hours : 03		
CREDITS 03		

Course Learning Objectives: This course will enable students to:
* Understand basic skills of Management
* Understand the need for Entrepreneurs and their skills
* Identify the Management functions and Social responsibilities
* Understand the Ideation Process, creation of Business Model, Feasibility Study and sources of funding

Module-1
Management: Nature and Functions of Management – Importance, Definition, Management Functions, Levels of Management, Roles of Manager, Managerial Skills, Management & Administration, Management as a Science, Art & Profession **(Selected topics of Chapter 1, Text 1).**
Planning: Planning-Nature, Importance, Types, Steps and Limitations of Planning; Decision Making – Meaning, Types and Steps in Decision Making (**Selected topics from Chapters 4 & 5, Text 1).**   **L1,L2**

Module-2
Organizing and Staffing: Organization-Meaning, Characteristics, Process of Organizing, Principles of Organizing, Span of Management (meaning and importance only), Departmentalisation, Committees–Meaning, Types of Committees; **Centralization Vs Decentralization of Authority and Responsibility; Staffing**-Need and Importance**,** Recruitment and Selection Process **(Selected topics from Chapters 7, 8 & 11,Text 1).**
Directing and Controlling: Meaning and Requirements of Effective Direction, Giving Orders; Motivation-Nature of Motivation, Motivation Theories (Maslow's Need-Hierarchy Theory and Herzberg's Two Factor Theory); Communication – Meaning, Importance and Purposes of Communication; Leadership-Meaning, Characteristics, Behavioural Approach of Leadership;

Coordination-Meaning, Types, Techniques of Coordination; Controlling – Meaning, Need for Control System, Benefits of Control, Essentials of Effective Control System, Steps in Control Process

(Selected topics from Chapters 15 to 18 and 9, Text 1). **L1,L2**

Module-3

Social Responsibilities of Business: Meaning of Social Responsibility, Social Responsibilities of Business towards Different Groups, Social Audit, Business Ethics and Corporate Governance **(Selected topics from Chapter 3, Text 1).**

Entrepreneurship: Definition of Entrepreneur, Importance of Entrepreneurship, concepts of Entrepreneurship, Characteristics of successful Entrepreneur, Classification of Entrepreneurs, Myths of Entrepreneurship, Entrepreneurial Development models, Entrepreneurial development cycle, Problems faced by Entrepreneurs and capacity building for Entrepreneurship **(Selected topics from Chapter 2, Text 2).** **L1,L2**

Module-4

Family Business: Role and Importance of Family Business, Contributions of Family Business in India, Stages of Development of a Family Business, Characteristics of a Family-owned Business in India, Various types of family businesses **(Selected topics from Chapter 4,(Page 71-75) Text 2).**

Idea Generation and Feasibility Analysis- Idea Generation; Creativity and Innovation; Identification of Business Opportunities; Market Entry Strategies; Marketing Feasibility; Financial Feasibilities; Political Feasibilities; Economic Feasibility; Social and Legal Feasibilities; Technical Feasibilities; Managerial Feasibility, Location and Other Utilities Feasibilities.**(Selected topics from Chapter 6(Page No. 111-117) & Chapter 7(Page No. 140-142), Text 2)** **L1,L2**

Module-5

Business model – Meaning, designing, analyzing and improvising; Business Plan – Meaning, Scope and Need; Financial, Marketing, Human Resource and Production/Service Plan; Business plan Formats; Project report preparation and presentation; Why some Business Plan fails? **(Selected topics from Chapter 8 (Page No 159-164, Text 2)**

Financing and How to start a Business? Financial opportunity identification; Banking sources; Nonbanking Institutions and Agencies; Venture Capital – Meaning and Role in Entrepreneurship; Government Schemes for funding business; Pre launch, Launch and Post launch requirements; Procedure for getting License and Registration; Challenges and Difficulties in Starting an Enterprise**(Selected topics from Chapter 7(Page No 147-149), Chapter 5(Page No 93-99) & Chapter 8(Page No. 166-172) Text 2)**

Project Design and Network Analysis: Introduction, Importance of Network

Analysis, Origin of PERT and CPM, Network, Network Techniques, Need for Network Techniques, Steps in PERT, CPM, Advantages, Limitations and Differences.
(Selected topics from Chapters 20, Text 3).   **L1,L2,L3**

Course Outcomes: After studying this course, students will be able to:
1. Understand the fundamental concepts of Management and Entrepreneurship and opportunities in order to setup a business
2. Identify the various organizations' architecture
3. Describe the functions of Managers, Entrepreneurs and their social responsibilities
4. Understand the components in developing a business plan
5. Recognize the various sources of funding and institutions supporting entrepreneurs

Text Books:
1.   Principles of Management – P.C Tripathi, P.N Reddy, McGraw Hill Education, 6th Edition, 2017. ISBN-13:978-93-5260-535-4.
2.   Entrepreneurship Development Small Business Enterprises- Poornima M Charantimath, Pearson Education 2008, ISBN 978-81-7758-260-4.
3.   Dynamics of Entrepreneurial Development and Management by Vasant Desai. HPH 2007, ISBN: 978-81-8488-801-2.
4.   Robert D. Hisrich, Mathew J. Manimala, Michael P Peters and Dean A. Shepherd, "Entrepreneurship", 8th Edition, Tata Mc-Graw Hill Publishing Co.Ltd.- New Delhi, 2012

Reference Book:
1.   Essentials of Management: An International, Innovation and Leadership perspective by Harold Koontz, Heinz Weihrich McGraw Hill Education, 10th Edition 2016. ISBN- 978-93-392-2286-4.

DIGITAL SIGNAL PROCESSING

Course Code	: **18EC52**	CIE Marks : 40
Lecture Hours/Week : 03 + 2 (Tutorial)		SEE marks : 60
Total Number of Lecture Hours : 50 (10 Hrs / Module)		Exam Hours : 03
CREDITS : 04		

Course Learning Objectives: This course will enable students to

- Understand the frequency domain sampling and reconstruction of discrete time signals.
- Study the properties and the development of efficient algorithms for the computation of DFT.
- Realization of FIR and IIR filters in different structural forms.
- Learn the procedures to design of IIR filters from the analog filters using impulse invariance and bilinear transformation.
- Study the different windows used in the design of FIR filters and design appropriate filters based on the specifications.
- Understand the architecture and working of DSP processor

Module-1

Discrete Fourier Transforms (DFT): Frequency domain sampling and Reconstruction of Discrete Time Signals, The Discrete Fourier Transform, DFT as a linear transformation, Properties of the DFT: Periodicity, Linearity and Symmetry properties, Multiplication of two DFTs and Circular Convolution, Additional DFT properties.
[Text 1],   **L1,L2,L3**

Module-2

Linear filtering methods based on the DFT: Use of DFT in Linear Filtering, Filtering of Long data Sequences.
Fast-Fourier-Transform (FFT) algorithms: Efficient Computation of the DFT: Radix-2 FFT algorithms for the computation of DFT and IDFT–decimation-in-time and decimation-in-frequency algorithms.
[Text 1],   **L1,L2, L3**

Module-3

Design of FIR Filters: Characteristics of practical frequency –selective filters, Symmetric and Antisymmetric FIR filters, Design of Linear-phase FIR filters using windows - Rectangular, Hamming, Hanning, Bartlett windows. Design of FIR filters using frequency sampling method. Structure for FIR Systems: Direct form, Cascade form and Lattice structures**.
[Text1],   **L1, L2, L3**

IIR Filter Design: Infinite Impulse response Filter Format, Bilinear Transformation Design Method, Analog Filters using Lowpass prototype transformation, Normalized Butterworth Functions, Bilinear Transformation and Frequency Warping, Bilinear Transformation Design Procedure, Digital Butterworth Filter Design using BLT. Realization of IIR Filters in Direct form I and II.
[Text 2],   **L1,L2,L3**

Module-5

Digital Signal Processors: DSP Architecture, DSP Hardware Units, Fixed point format, Floating point Format, IEEE Floating point formats, Fixed point digital signal processors, Floating point processors, FIR and IIR filter implementations in Fixed point systems.
[Text 2],   **L1, L2, L3**

Course Outcomes: After studying this course, students will be able to:
1.   Determine response of LTI systems using time domain and DFT techniques.
2.   Compute DFT of real and complex discrete time signals.
3.   Compute DFT using FFT algorithms and linear filtering approach.
4.   Design and realize FIR and IIR digital filters.
5.   Understand the DSP processor architecture.

Question paper pattern:
* Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
* Each full question can have a maximum of 4 sub questions.
* There will be 2 full questions from each module covering all the topics of the module.
* Students will have to answer 5 full questions, selecting one full question from each module.
* The total marks will be proportionally reduced to 60 marks as SEE marks is 60

Text Book:
1.   Proakis & Manolakis, "Digital Signal Processing – Principles Algorithms & Applications", 4th Edition, Pearson education, New Delhi, 2007. ISBN: 81-317-1000-9.
2.   Li Tan, Jean Jiang, "Digital Signal processing – Fundamentals and Applications", Academic Press, 2013, ISBN: 978-0-12-415893.

Reference Books:
1. Sanjit K Mitra, "Digital Signal Processing, A Computer Based Approach", 4th Edition, McGraw Hill Education, 2013,
2. Oppenheim & Schaffer, "Discrete Time Signal Processing" , PHI, 2003.
3. D.Ganesh Rao and Vineeth P Gejji, "Digital Signal Processing" Cengage India Private Limited, 2017, ISBN: 9386858231

PRINCIPLES OF COMMUNICATION SYSTEMS

Course Code	: **18EC53**	CIE Marks : 40
Lecture Hours/Week : 03 + 2 (Tutorial)		SEE marks : 60
Total Number of Lecture Hours : 50 (10 Hrs / Module)		Exam Hours : 03
CREDITS : 04		

Course Learning Objectives: This course will enable students to
* Understand and analyse concepts of Analog Modulation schemes viz; AM, FM, Low pass sampling and Quantization as a random process.
* Understand and analyse concepts digitization of signals viz; sampling, quantizing and encoding.
* Evolve the concept of SNR in the presence of channel induced noise and study Demodulation of analog modulated signals.
* Evolve the concept of quantization noise for sampled and encoded signals and study the concepts of reconstruction from these samples at a receiver.

Module-1
AMPLITUDE MODULATION: Introduction, Amplitude Modulation: Time & Frequency Domain description, Switching modulator, Envelop detector. **(3.1 – 3.2 in Text)**

DOUBLE SIDE BAND-SUPPRESSED CARRIER MODULATION: Time and Frequency Domain description, Ring modulator, Coherent detection, Costas Receiver, Quadrature Carrier Multiplexing. **(3.3 – 3.4 in Text)**

SINGLE SIDE–BAND AND VESTIGIAL SIDEBAND METHODS OF MODULATION: SSB Modulation, VSB Modulation, Frequency Translation, Frequency- Division Multiplexing,Theme Example: VSB Transmission of Analog and Digital Television. **(3.5 – 3.8 in Text)**

L1, L2, L3

Module-2
ANGLE MODULATION: Basic definitions, Frequency Modulation: Narrow Band FM, Wide Band FM, Transmission bandwidth of FM Signals, Generation of FM Signals, Demodulation of FM Signals, FM Stereo Multiplexing, Phase–Locked Loop: Nonlinear model of PLL, Linear model of PLL, Nonlinear Effects in FM Systems. The Superheterodyne Receiver **(4.1 – 4.6 of Text)**

L1, L2, L3

Module-3

[Review of Mean, Correlation and Covariance functions of Random Processes. (No questions to be set on these topics)]

NOISE - Shot Noise, Thermal noise, White Noise, Noise Equivalent Bandwidth **(5.10 in Text)**

NOISE IN ANALOG MODULATION: Introduction, Receiver Model, Noise in DSB-SC receivers. Noise in AM receivers, Threshold effect, Noise in FM receivers, Capture effect, FM threshold effect, FM threshold reduction, Pre-emphasis and De-emphasis in FM **(6.1 – 6.6 in Text)**

L1,L2,L3

Module-4

SAMPLING AND QUANTIZATION: Introduction, Why Digitize Analog Sources?, The Low pass Sampling process Pulse Amplitude Modulation. Time Division Multiplexing, Pulse-Position Modulation, Generation of PPM Waves, Detection of PPM Waves. **(7.1 – 7.7 in Text)**

L1,L2,L3

Module-5

SAMPLING AND QUANTIZATION (Contd): The Quantization Random Process, Quantization Noise, Pulse–Code Modulation: Sampling, Quantization, Encoding, Regeneration, Decoding, Filtering, Multiplexing; Delta Modulation **(7.8 – 7.10 in Text)**,

Application examples - (a) Video + MPEG **(7.11 in Text)** and (b) Vocoders **(refer Section 6.8 of Reference Book 1)**.

L1,L2,L3

Course Outcomes: After studying this course, students will be able to:
1. Analyze and compute performance of AM and FM modulation in the presence of noise at the receiver.
2. Analyze and compute performance of digital formatting processes with quantization noise.
3. Multiplex digitally formatted signals at Transmitter.
4. Demultiplex the signals and reconstruct digitally formatted signals at the receiver.
5. Design /Demonstrate the use of digital formatting in Multiplexers, Vocoders and Video transmission.

Question paper pattern:
• Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
• Each full question can have a maximum of 4 sub questions.
• There will be 2 full questions from each module covering all the topics

of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:
1.   "Communication Systems", Simon Haykin & Moher, 5th Edition, John Wiley, India Pvt. Ltd, 2010, ISBN 978 – 81 – 265 – 2151 – 7.

Reference Books:
1.   Modern Digital and Analog Communication Systems, B. P. Lathi, Oxford University Press, 4th edition.
2.   An Introduction to Analog and Digital Communication, Simon Haykin, John Wiley India Pvt. Ltd., 2008, ISBN 978–81–265–3653–5.
3.   Principles of Communication Systems, H.Taub & D.L.Schilling, TMH, 2011.
4.   Communication Systems, Harold P.E, Samy A. Mahmoud, Lee Elliott Stern, Pearson Edition, 2004.

INFORMATION THEORY and CODING

Course Code	: **18EC54**	CIE Marks	: 40
Lecture Hours/Week	: 3	SEE Marks	: 60
Total Number of Lecture Hours : 40 (8 Hrs / Module)		Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives: This course will enable students to
- Understand the concept of Entropy, Rate of information and order of the source with reference to dependent and independent source.
- Study various source encoding algorithms.
- Model discrete & continuous communication channels.
- Study various error control coding algorithms.

Module-1
Information Theory: Introduction, Measure of information, Information content of message, Average Information content of symbols in Long Independent sequences, Average Information content of symbols in Long dependent sequences, Markov Statistical Model for Information Sources, Entropy and Information rate of Markoff Sources
(Section 4.1, 4.2 of Text 1)   **L1, L2,L3**

Module-2
Source Coding: Encoding of the Source Output, Shannon's Encoding Algorithm**(Sections 4.3, 4.3.1 of Text 1),** Shannon Fano Encoding Algorithm **(Section 2.15 of Reference Book 4)**
Source coding theorem, Prefix Codes, Kraft McMillan Inequality property – KMI, Huffman codes **(Section 2.2 of Text 2)**
                                        L1, L2, L3

Module-3
Information Channels: Communication Channels, Discrete Communication channels Channel Matrix, Joint probabilty Matrix, Binary Symmetric Channel, System Entropies. **(Section 4.4, 4.5, 4.51,4.5.2 of Text 1)**

Mutual Information, Channel Capacity, Channel Capacity of Binary Symmetric Channel, **(Section 2.5, 2.6 of Text 2)**

Binary Erasure Channel, Muroga's Theorem **(Section 2.27, 2.28 of Reference Book 4)**
                                        L1, L2, L3

Module-4

Error Control Coding:
Introduction, Examples of Error control coding, methods of Controlling Errors, Types of Errors, types of Codes, Linear Block Codes: matrix description of Linear Block Codes, Error detection & Correction capabilities of Linear Block Codes, Single error correction Hamming code, Table lookup Decoding using Standard Array.

Binary Cyclic Codes: Algebraic Structure of Cyclic Codes, Encoding using an (n-k) Bit Shift register, Syndrome Calculation, Error Detection and Correction **(Sections 9.1, 9.2,9.3,9.3.1,9.3.2,9.3.3 of Text 1)** ,

L1, L2, L3

Module-5

Convolution Codes: Convolution Encoder, Time domain approach, Transform domain approach, Code Tree, Trellis and State Diagram, The Viterbi Algorithm) **(Section 8.5 – Articles 1, 2 and 3, 8.6- Article 1 of Text 2),**

L1, L2, L3

Course Outcomes: After studying this course, students will be able to:
1. Explain concept of Dependent & Independent Source, measure of information, Entropy, Rate of Information and Order of a source
2. Represent the information using Shannon Encoding, Shannon Fano, Prefix and Huffman Encoding Algorithms
3. Model the continuous and discrete communication channels using input, output and joint probabilities
4. Determine a codeword comprising of the check bits computed using Linear Block codes, cyclic codes & convolutional codes
5. Design the encoding and decoding circuits for Linear Block codes, cyclic codes, convolutional codes, BCH and Golay codes.

Question paper pattern:
- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:
1.   Digital and Analog Communication Systems, K. Sam Shanmugam, John Wiley India Pvt. Ltd, 1996.
2.   Digital Communication, Simon Haykin, John Wiley India Pvt. Ltd, 2008.

Reference Books:
1.   ITC and Cryptography, Ranjan Bose, TMH, II edition, 2007
2.   Principles of Digital Communication, J. Das, S. K. Mullick, P. K. Chatterjee, Wiley, 1986 - Technology & Engineering
3.   Digital Communications – Fundamentals and Applications, Bernard Sklar, Second Edition, Pearson Education, 2016, ISBN: 9780134724058.
4.   Information Theory and Coding, HariBhat, Ganesh Rao, Cengage, 2017.
5.   Error Correction Coding, Todd K Moon,Wiley Std. Edition, 2006

ELECTROMAGNETIC WAVES

Course Code	: **18EC55**	CIE Marks	: 40
Lecture Hours/Week	: 3	SEE Marks	: 60
Total Number of Lecture Hours : 40 (8 Hrs / Module)		Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives: This course will enable students to:

- Study the different coordinate systems, Physical significance of Divergence, Curl and Gradient.
- Understand the applications of Coulomb's law and Gauss law to different charge distributions and the applications of Laplace's and Poisson's Equations to solve real time problems on capacitance of different charge distributions.
- Understand the physical significance of Biot-Savart's, Ampere's Law and Stokes' theorem for different current distributions.
- Infer the effects of magnetic forces, materials and inductance.
- Know the physical interpretation of Maxwell's equations and applications for Plane waves for their behavior in different media.
- Acquire knowledge of Poynting theorem and its application of power flow.

Module-1

Revision of Vector Calculus – **(Text 1: Chapter 1)**

Coulomb's Law, Electric Field Intensity and Flux density: Experimental law of Coulomb, Electric field intensity, Field due to continuous volume charge distribution, Field of a line charge, Field due to Sheet of charge, Electric flux density, Numerical Problems. **(Text: Chapter 2.1 to 2.5, 3.1)**

L1, L2, L3

Module -2

Gauss's law and Divergence: Gauss law, Application of Gauss law to point charge, line charge, Surface charge and volume charge, Point (differential) form of Gauss law, Divergence. Maxwell's First equation (Electrostatics), Vector Operator ∇ and divergence theorem, Numerical Problems **(Text: Chapter 3.2 to 3.7)**.

Energy, Potential and Conductors: Energy expended or work done in moving a point charge in an electric field, The line integral, Definition of potential difference and potential, The potential field of point charge, Potential gradient, Numerical Problems **(Text: Chapter 4.1 to 4.4 and 4.6).** Current and Current density, Continuity of current. **(Text: Chapter 5.1, 5.2)**

L1, L2, L3

Module-3

Poisson's and Laplace's Equations: Derivation of Poisson's and Laplace's Equations, Uniqueness theorem, Examples of the solution of Laplace's equation, Numerical problems on Laplace equation **(Text: Chapter 7.1 to 7.3)**

Steady Magnetic Field: Biot-Savart Law, Ampere's circuital law, Curl, Stokes' theorem, Magnetic flux and magnetic flux density, Basic concepts Scalar and Vector Magnetic Potentials, Numerical problems. (**Text: Chapter 8.1 to 8.6)**

L1, L2, L3

Module -4

Magnetic Forces: Force on a moving charge, differential current elements, Force between differential current elements, Numerical problems **(Text: Chapter 9.1 to 9.3)**.

Magnetic Materials: Magnetization and permeability, Magnetic boundary conditions, The magnetic circuit, Potential energy and forces on magnetic materials, Inductance and mutual reactance, Numerical problems **(Text: Chapter 9.6 to 9.7)**.

Faraday' law of Electromagnetic Induction –Integral form and Point form, Numerical problems **(Text: Chapter 10.1)**

L1, L2, L3

Module -5

Maxwell's equations Continuity equation, Inconsistency of Ampere's law with continuity equation, displacement current, Conduction current, Derivation of Maxwell's equations in point form, and integral form, Maxwell's equations for different media, Numerical problems **(Text: Chapter 10.2 to 10.4)**

Uniform Plane Wave: Plane wave, Uniform plane wave, Derivation of plane wave equations from Maxwell's equations, Solution of wave equation for perfect dielectric, Relation between E and H, Wave propagation in free space, Solution of wave equation for sinusoidal excitation, wave propagation in any conducting media (γ, α, β, η) and good conductors, Skin effect or Depth of penetration, Poynting's theorem and wave power, Numerical problems. **(Text: Chapter 12.1 to 12.4)**

L1, L2, L3

Course Outcomes: After studying this course, students will be able to:

1. Evaluate problems on electrostatic force, electric field due to point, linear, volume charges by applying conventional methods and charge in a volume.

2. Apply Gauss law to evaluate Electric fields due to different charge distributions and Volume Charge distribution by using Divergence

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Theorem.

3.	Determine potential and energy with respect to point charge and capacitance using Laplace equation and Apply Biot-Savart's and Ampere's laws for evaluating Magnetic field for different current configurations

4.	Calculate magnetic force, potential energy and Magnetization with respect to magnetic materials and voltage induced in electric circuits.

5.	Apply Maxwell's equations for time varying fields, EM waves in free space and conductors and Evaluate power associated with EM waves using Poynting theorem

Question paper pattern:

·	Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.

·	Each full question can have a maximum of 4 sub questions.

·	There will be 2 full questions from each module covering all the topics of the module.

·	Students will have to answer 5 full questions, selecting one full question from each module.

·	The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

1.	W.H. Hayt and J.A. Buck, —Engineering Electromagnetics, 8th Edition, Tata McGraw-Hill, 2014, ISBN-978-93-392-0327-6.

Reference Books:

1.	Elements of Electromagnetics – Matthew N.O., Sadiku, Oxford university press, 4th Edn.

2.	Electromagnetic Waves and Radiating systems – E. C. Jordan and K.G. Balmain, PHI, 2nd Edn.

3.	Electromagnetics- Joseph Edminister, Schaum Outline Series, McGraw Hill.

4.	Fundamentals of Electromagnetics for Engineering - N. Narayana Rao, Pearson.

Verilog HDL

Course Code	: **18EC56**	CIE Marks	: 40
Lecture Hours/Week	: 03	SEE Marks	: 60
Total Number of Lecture Hours : 40 (08 Hrs/Module)		Exam Hours	: 03
CREDITS– 03			

Course Learning Objectives: This course will enable students to:
- Learn different Verilog HDL constructs.
- Familiarize the different levels of abstraction in Verilog.
- Understand Verilog Tasks, Functions and Directives.
- Understand timing and delay Simulation.
- Understand the concept of logic synthesis and its impact in verification

Module 1

Overview of Digital Design with Verilog HDL: Evolution of CAD, emergence of HDLs, typical HDL-flow, why Verilog HDL?, trends in HDLs.
Hierarchical Modeling Concepts: Top-down and bottom-up design methodology, differences between modules and module instances, parts of a simulation, design block, stimulus block.   **L1,L2,L3**

Module 2

Basic Concepts: Lexical conventions, data types, system tasks, compiler directives.
Modules and Ports: Module definition, port declaration, connecting ports, hierarchical name referencing   **L1,L2,L3**

Module 3

Gate-Level Modeling: Modeling using basic Verilog gate primitives, description of and/or and buf/not type gates, rise, fall and turn-off delays, min, max, and typical delays.
Dataflow Modeling: Continuous assignments, delay specification, expressions, operators, operands, operator types.   **L1,L2,L3**

Module 4

Behavioral Modeling: Structured procedures, initial and always, blocking and non-blocking statements, delay control, generate statement, event control, conditional statements, Multiway branching, loops, sequential and parallel blocks.
Tasks and Functions: Differences between tasks and functions, declaration, invocation, automatic tasks and functions.   **L1,L2,L3**

Module 5

Useful Modeling Techniques: Procedural continuous assignments, overriding parameters, conditional compilation and execution, useful system tasks.
Logic Synthesis with Verilog: Logic Synthesis, Impact of logic synthesis, Verilog HDL Synthesis, Synthesis design flow, Verification of Gate-Level Netlist. **(Chapter 14 till 14.5 of Text).** **L1,L2,L3**

Course Outcomes: At the end of this course, students will be able to
1. Write Verilog programs in gate, dataflow (RTL), behavioral and switch modeling levels of Abstraction.
2. Design and verify the functionality of digital circuit/system using test benches.
3. Identify the suitable Abstraction level for a particular digital design.
4. Write the programs more effectively using Verilog tasks, functions and directives.
5. Perform timing and delay Simulation and Interpret the various constructs in logic synthesis.

Question paper pattern:
- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:
1. Samir Palnitkar, "**Verilog HDL: A Guide to Digital Design and Synthesis**", Pearson Education, Second Edition.

Reference Books:
1. Donald E. Thomas, Philip R. Moorby, "The Verilog Hardware Description Language", Springer Science+Business Media, LLC, Fifth edition.
2. Michael D. Ciletti, "Advanced Digital Design with the Verilog HDL" Pearson (Prentice Hall), Second edition.
3. Padmanabhan, Tripura Sundari, "Design through Verilog HDL", Wiley, 2016 or earlier.

DIGITAL SIGNAL PROCESSING LABORATORY

Course Code : **18ECL57**	CIE Marks : 40	SEE Marks : 60

Lecture Hours/Week: 02 Hours Tutorial (Instructions) + 02 Hours Laboratory

RBT Level : L1, L2, L3	Exam Hours : 03

CREDITS – 02

Course Learning Objectives: This course will enable students to
- Simulate discrete time signals and verification of sampling theorem.
- Compute the DFT for a discrete signal and verification of its properties using MATLAB.
- Find solution to the difference equations and computation of convolution and correlation along with the verification of properties.
- Compute and display the filtering operations and compare with the theoretical values.
- Implement the DSP computations on DSP hardware and verify the result.

Laboratory Experiments

Following Experiments to be done using MATLAB / SCILAB / OCTAVE or equivalent:

1.   Verification of sampling theorem (use interpolation function).

2.   Linear and circular convolution of two given sequences, Commutative, distributive and associative property of convolution.

3.   Auto and cross correlation of two sequences and verification of their properties

4.   Solving a given difference equation.

5.   Computation of N point DFT of a given sequence and to plot magnitude and phase spectrum (using DFT equation and verify it by built-in routine).

6.   (i) Verification of DFT properties (like Linearity and Parseval's theorem, etc.)
       (ii) DFT computation of square pulse and Sinc function etc.

7. Design and implementation of Low pass and High pass FIR filter to meet the desired specifications (using different window techniques) and test the filter with an audio file. Plot the spectrum of audio signal before and after filtering.

8. Design and implementation of a digital IIR filter (Low pass and High pass) to meet given specifications and test with an audio file. Plot the spectrum of audio signal before and after filtering.

Following Experiments to be done using DSP kit
9. Obtain the Linear convolution of two sequences.
10. Compute Circular convolution of two sequences.
11. Compute the N-point DFT of a given sequence.
12. Determine the Impulse response of first order and second order system.
13. Generation of sine wave and standard test signals

Course Outcomes:
On the completion of this laboratory course, the students will be able to:
1. Understand the concepts of analog to digital conversion of signals and frequency domain sampling of signals.
2. Model the discrete time signals and systems and verify its properties and results.
3. Implement discrete computations using DSP processor and verify the results.
4. Realize the digital filters using a simulation tool and analyze the response of the filter for an audio signal.
5. Write programs using Matlab / Scilab/Octave to illustrate DSP concepts.

Conduct of Practical Examination:
1. All laboratory experiments are to be included for practical examination.
2. Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.
3. Change of experiment is allowed only once and Marks allotted to the procedure part to be made zero.

Reference Books:
1. Vinay K Ingle, John G Proakis, Digital Signal Processing using MATLAB, Fourth Edition, Cengage India Private Limited, 2017.

HDL LABORATORY

Course Code : **18ECL58**	CIE Marks : 40	SEE Marks : 60
Lecture Hours/Week: 02 Hours Tutorial (Instructions) + 02 Hours Laboratory		
RBT Level : L1, L2, L3	Exam Hours : 03	
CREDITS – 02		

Course Learning Objectives: This course will enable students to:
• Familiarize with the CAD tool to write HDL programs.
• Understand simulation and synthesis of digital design.
• Program FPGAs/CPLDs to synthesize the digital designs.
• Interface hardware to programmable ICs through I/O ports.
• Choose either Verilog or VHDL for a given Abstraction level.

Note: Programming can be done using any compiler. Download the programs on a FPGA/CPLD board and performance testing may be done using 32 channel pattern generator and logic analyzer apart from verification by simulation with tools such as Altera/Modelsim or equivalent.

PART A

1. Write Verilog program for the following combinational design along with test bench to verify the design:
   a. 2 to 4 decoder realization using NAND gates only (structural model)
   b. 8 to 3 encoder with priority and without priority (behavioural model)
   c. 8 to 1 multiplexer using case statement and if statements
   d. 4-bit binary to gray converter using 1-bit gray to binary converter 1-bit adder and subtractor
2. Model in Verilog for a full adder and add functionality to perform logical operations of XOR, XNOR, AND and OR gates. Write test bench with appropriate input patterns to verify the modeled behaviour.
3. Verilog 32-bit ALU shown in figure below and verify the functionality of ALU by selecting appropriate test patterns. The functionality of the ALU is presented in Table 1.
   a. Write test bench to verify the functionality of the ALU considering all possible input patterns
   b. The enable signal will set the output to required functions if enabled, if disabled all the outputs are set to tri-state
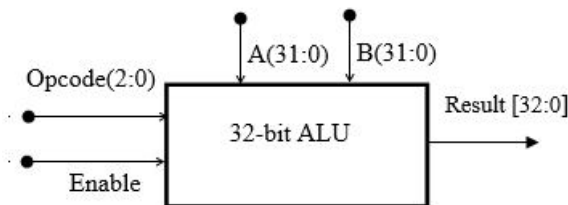   c. The acknowledge signal is set high after every operation is complete

Figure 1 ALU top level block diagram

Table 1 ALU Functions

Opcode (2:0)	ALU Operation	Remarks	
000	A + B	Addition of two numbers	Both A and B are in two's complement format
001	A − B	Subtraction of two numbers	
010	A + 1	Increment Accumulator by 1	A is in two's complement format
011	A - 1	Decrement accumulator by 1	
100	A	True	Inputs can be in any format
101	A Complement	Complement	
110	A OR B	Logical OR	
111	A AND B	Logical AND	

4.   Write Verilog code for SR, D and JK and verify the flip flop.
5.   Write Verilog code for 4-bit BCD synchronous counter.
6.   Write Verilog code for counter with given input clock and check whether it works as clock divider performing division of clock by 2, 4, 8 and 16. Verify the functionality of the code.

PART-B

Interfacing and Debugging (EDWinXP, PSpice, MultiSim, Proteus, CircuitLab or any other equivalent tool can be used)

1.   Write a Verilog code to design a clock divider circuit that generates 1/2, 1/3rd and 1/4th clock from a given input clock. Port the design to FPGA and validate the functionality through oscilloscope.
2.   Interface a DC motor to FPGA and write Verilog code to change its speed and direction.
3.   Interface a Stepper motor to FPGA and write Verilog code to control the Stepper motor rotation which in turn may control a Robotic Arm. External switches to be used for different controls like rotate the Stepper motor (i) +N steps if Switch no.1 of a Dip switch is closed   (ii) +N/2 steps if Switch no. 2 of a Dip switch is closed   (iii) –N steps if Switch no. 3 of a Dip switch is closed etc.

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4.　　Interface a DAC to FPGA and write Verilog code to generate Sine wave of frequency F KHz (eg. 200 KHz) frequency. Modify the code to down sample the frequency to F/2 KHz. Display the Original and Down sampled signals by connecting them to an oscilloscope.

5.　　Write Verilog code using FSM to simulate elevator operation.

6.　　Write Verilog code to convert an analog input of a sensor to digital form and to display the same on a suitable display like set of simple LEDs, 7-segment display digits or LCD display.

Course Outcomes: At the end of this course, students will be able to:
1. Write the Verilog/VHDL programs to simulate Combinational circuits in Dataflow, Behavioral and Gate level Abstractions.
2. Describe sequential circuits like flip flops and counters in Behavioral description and obtain simulation waveforms.
3. Use FPGA/CPLD kits for down loading Verilog codes and check output.
4. Synthesize Combinational and Sequential circuits on programmable ICs and test the hardware.
5. Interface the hardware to the programmable chips and obtain the required output

Conduct of Practical Examination:
- All laboratory experiments are to be included for practical examination.
- Students are allowed to pick one experiment from the lot.
- Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.
- Change of experiment is allowed only once and Marks allotted to the procedure part to be made zero.

ENVIRONMENTAL STUDIES

Course Code	: 18CIV59	CIE Marks	: 40
Lecture Hours / Week (L:T:P)	: (1:0:0)	SEE Marks	: 60
Credits	: 01	Exam Hours	: 02

Module - 1

Ecosystems (Structure and Function): Forest, Desert, Wetlands, Riverine, Oceanic and Lake.

Biodiversity: Types, Value; Hot-spots; Threats and Conservation of biodiversity, Forest Wealth, and Deforestation.

Module - 2

Advances in Energy Systems (Merits, Demerits, Global Status and Applications)**:** Hydrogen, Solar, OTEC, Tidal and Wind.

Natural Resource Management (Concept and case-studies): Disaster Management, Sustainable Mining, Cloud Seeding, and Carbon Trading.

Module - 3

Environmental Pollution (Sources, Impacts, Corrective and Preventive measures, Relevant Environmental Acts, Case-studies)**:** Surface and Ground Water Pollution; Noise pollution; Soil Pollution and Air Pollution.
Waste Management & Public Health Aspects: Bio-medical Wastes; Solid waste; Hazardous wastes; E-wastes; Industrial and Municipal Sludge.

Module - 4

Global Environmental Concerns(Concept, policies and case-studies):Ground water depletion/recharging, Climate Change; Acid Rain; Ozone Depletion; Radon and Fluoride problem in drinking water; Resettlement and rehabilitation of people, Environmental Toxicology.

Module - 5

Latest Developments in Environmental Pollution Mitigation Tools (Concept and Applications): G.I.S. & Remote Sensing, Environment Impact Assessment, Environmental Management Systems, ISO14001; Environmental Stewardship- NGOs.
Field work: Visit to an Environmental Engineering Laboratory or Green Building or Water Treatment Plant or Waste water treatment Plant; ought to be Followed by understanding of process and its brief documentation.

Course outcomes: At the end of the course, students will be able to:
1. Understand the principles of ecology and environmental issues that apply to air, land, and water issues on a global scale.
2. Develop critical thinking and/or observation skills, and apply them to the analysis of a problem or question related to the environment.
3. Demonstrate ecology knowledge of a complex relationship between biotic and a biotic components.
4. Apply their ecological knowledge to illustrate and graph a problem and describe the realities that managers face when dealing with complex issues.
5. Relate to the latest Developments in Environmental Pollution Mitigation Tools.

Question paper pattern:
*   The Question paper will have 100 objective questions.
*   Each question will be for 01 marks
*   Student will have to answer all the questions in an OMR Sheet.
*   The Duration of Exam will be 2 hours.

Textbook/s
1. Environmental Studies, Benny Joseph, Tata McGraw – Hill., 2nd Edition, 2012
2. Environmental Studies, S M Prakash, Pristine Publishing House, Mangalore, 3rd Edition, 2018
3. Environmental Studies – From Crisis to Cure, R Rajagopalan, Oxford Publisher, 2005

Reference Books
1. Principles of Environmental Science and Engineering, Raman Sivakumar, Cengage learning, Singapur. 2nd Edition, 2005
2. Environmental Science – working with the Earth, G.Tyler Miller Jr., Thomson Brooks /Cole, 11th Edition, 2006
3. Text Book of Environmental and Ecology, Pratiba Sing, Anoop Singh & Piyush Malaviya, Acme Learning Pvt. Ltd. New Delhi, 1st Edition

B. E. 2018 Scheme Sixth Semester Syllabus (EC / TC)
Choice Based Credit System (CBCS) and Outcome Based Education (OBE)

SEMESTER – VI

DIGITAL COMMUNICATION

Course Code	: 18EC61	CIE Marks : 40
Lecture Hours/Week	: 03 + 2 (Tutorial)	SEE marks : 60
Total Number of Lecture Hours : 50 (10 Hrs / Module)		Exam Hours : 03
CREDITS : 04		

Course Learning Objectives: This course will enable students to:
- Understand the mathematical representation of signal, symbol, and noise.
- Understand the concept of signal processing of digital data and signal conversion to symbols at the transmitter and receiver.
- Compute performance metrics and parameters for symbol processing and recovery in ideal and corrupted channel conditions.
- Compute performance parameters and mitigate channel induced impediments in corrupted channel conditions.

Module-1
Bandpass Signal to Equivalent Low pass: Hilbert Transform, Pre-envelopes, Complex envelopes, Canonical representation of bandpass signals, Complex low pass representation of bandpass systems, Complex representation of band pass signals and systems **(Text 1: 2.8, 2.9, 2.10, 2.11, 2.12, 2.13).**

Line codes: Unipolar, Polar, Bipolar (AMI) and Manchester code and their power spectral densities **(Text 1: Ch 6.10).**
Overview of HDB3, B3ZS, B6ZS **(Ref. 1: 7.2)**

L1,L2,L3

Module-2
Signaling over AWGN Channels- Introduction, Geometric representation of signals, Gram-Schmidt Orthogonalization procedure, Conversion of the continuous AWGN channel into a vector channel, Optimum receivers using coherent detection: ML Decoding, Correlation receiver, matched filter receiver **(Text 1: 7.1, 7.2, 7.3, 7.4).**

L1,L2,L3

Module – 3

Digital Modulation Techniques: Phase shift Keying techniques using coherent detection: generation, detection and error probabilities of BPSK and QPSK, M–ary PSK, M–ary QAM **(Relevant topics in Text 1 of 7.6, 7.7).**

Frequency shift keying techniques using Coherent detection: BFSK generation, detection and error probability **(Relevant topics in Text 1 of 7.8).**
Non coherent orthogonal modulation techniques: BFSK, DPSK Symbol representation, Block diagrams treatment of Transmitter and Receiver, Probability of error (without derivation of probability of error equation) **(Text 1: 7.11, 7.12. 7.13).**

L1,L2,L3

Module-4

Communication through Band Limited Channels: Digital Transmission through Band limited channels: Digital PAM Transmission through Band limited Channels, Signal design for Band limited Channels: Design of band limited signals for zero ISI–The Nyquist Criterion (statement only), Design of band limited signals with controlled ISI-Partial Response signals, Probability of error for detection of Digital PAM: Probability of error for detection of Digital PAM with Zero ISI, Symbol–by–Symbol detection of data with controlled ISI **(Text 2: 9.1, 9.2, 9.3.1, 9.3.2).**
Channel Equalization: Linear Equalizers (ZFE, MMSE), **(Text 2: 9.4.2).**

L1,L2,L3

Module-5

Principles of Spread Spectrum: Spread Spectrum Communication Systems: Model of a Spread Spectrum Digital Communication System, Direct Sequence Spread Spectrum Systems, Effect of De-spreading on a narrowband Interference, Probability of error (statement only), Some applications of DS Spread Spectrum Signals, Generation of PN Sequences, Frequency Hopped Spread Spectrum, CDMA based on IS-95 **(Text 2: 11.3.1, 11.3.2, 11.3.3, 11.3.4, 11.3.5, 11.4.2).**

L1,L2,L3

Course Outcomes: At the end of the course, the students will be able to:
1. Associate and apply the concepts of Bandpass sampling to well speci-fied signals and channels.
2. Analyze and compute performance parameters and transfer rates for low pass and bandpass symbol under ideal and corrupted non band limited channels.

3. Test and validate symbol processing and performance parameters at the receiver under ideal and corrupted bandlimited channels.
4. Demonstrate that bandpass signals subjected to corruption and distortion in a bandlimited channel can be processed at the receiver to meet specified performance criteria.
5. Understand the principles of spread spectrum communications.

Question paper pattern:
- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:
1. Simon Haykin, "Digital Communication Systems", John Wiley & sons, First Edition, 2014, ISBN 978-0-471-64735-5.
2. John G Proakis and Masoud Salehi, "Fundamentals of Communication Systems", 2014 Edition, Pearson Education, ISBN 978-8-131-70573-5.

Reference Books:
1. B.P.Lathi and Zhi Ding, "Modern Digital and Analog communication Systems", Oxford University Press, 4th Edition, 2010, ISBN: 978-0-198-07380-2.
2. Ian A Glover and Peter M Grant, "Digital Communications", Pearson Education, Third Edition, 2010, ISBN 978-0-273-71830-7.
3. Bernard Sklar and Ray, "Digital Communications - Fundamentals and Applications", Pearson Education, Third Edition, 2014, ISBN: 978-81-317-2092-9.

MICROWAVE THEORY and ANTENNAS

Course Code	: 18TE62	CIE Marks : 40
Lecture Hours/Week	: 03 + 2 (Tutorial)	SEE marks : 60
Total Number of Lecture Hours : 50 (10 Hrs / Module)		Exam Hours : 03
CREDITS : 04		

Course Learning Objectives: This course will enable students to:
- Know the Principle of operation of Microwave Tubes.
- Understand the Concept of S-Parameters and various Microwave passive components.
- Understand the Basic Parameters as applied to Antennas
- Analyze Antennas and Arrays of Antennas.

Module 1

Microwave Tubes: Introduction, Reflex Klystron oscillator, Mechanism of oscillations, modes of oscillations, Mode curve (Qualitative Analysis only). (Text-1: 9.1, 9.2.2)
Microwave Transmission Lines: Transmission line equations and solutions, Reflection Coefficient and Transmission Coefficient, Standing wave and Standing wave ratio, Smith chart, Single stub matching. (Text-2: 3.1, 3.2, 3.3, 3.5, 3.6, Except Double stub matching).

L1 – L5

Module 2

Microwave Network theory: Symmetrical Z and Y-Parameters, for reciprocal Networks, S matrix representation of multi-port Networks. (Text-1: 6.1, 6.2, 6.3)
Microwave Passive Devices: Coaxial connectors and adapters, Attenuators, Phase shifters, Waveguide Tees, Magic tees, Circulators (Four port) and isolators (Faraday rotation Isolator). **(**Text-1: 6.4.2, 6.4.14, 6.4.15, 6.4.16, Except Applications of Magic TEE, 6.4.17)
Directional coupler: Two - hole Directional coupler, S- Matrix of a Directional Coupler. (Text-2: 4.5, 4.5.1, 4.5.2)

L1 - L5

Module 3

Strip Lines: Introduction, Micro Strip lines, Parallel strip lines, Coplanar strip lines, Shielded strip Lines. (Text-2: Chapter 11)
Antenna Basics: Introduction, Basic Antenna Parameters, Patterns, Beam Area, Radiation Intensity, Beam Efficiency, Directivity and Gain, Antenna Apertures,

Effective Height, Bandwidth, Radio Communication Link, Antenna Field Zones & Polarization. (Text-3: 2.1- 2.11, 2.13, 2.13, 2.15).

L1 - L4

Module 4

Point Sources and Arrays: Introduction, Point Sources, Power Patterns, Power Theorem, Radiation Intensity, Field Patterns, Phase Patterns, Arrays of Two Isotropic Point Sources, Pattern Multiplication, Linear Arrays of n Isotropic Point Sources of equal Amplitude and Spacing. (Text-3:, 5.1 – 5.10, 13)

Electric Dipoles: Introduction, Short Electric Dipole, Fields of a Short Dipole (General and Far Field Analyses), Radiation Resistance of a Short Dipole, Thin Linear Antenna (Field Analyses), Radiation Resistances of Lambda/2 Antenna. (Text-3: 6.1-6.6).

L1 - L4

Module 5

Loop and Horn Antenna: Introduction, Small loop, Comparison of Far fields of Small Loop and Short Dipole, The Loop Antenna General Case, Far field Patterns of Circular Loop Antenna with Uniform Current , Radiation Resistance of Loops, Directivity of Circular Loop Antennas with Uniform Current, Horn antennas Rectangular Horn Antennas. (Text-3: 7.1-7.8, 7.19, 7.20).

Antenna Types: Helical Antenna, Helical Geometry, Practical Design Considerations of Helical Antenna, Yagi-Uda array, Parabola General Properties, Log Periodic Antenna. (Text-3: 8.3, 8.5, 8.8, 9.5, 11.7).

L1 - L3

Course Outcomes: After studying this course, students will be able to:
1. Describe the characteristic features of Microwave Tubes and the basic parameters of Antennas.
2. Represent the Multiport Network in terms of S-Parameters and analyze their properties.
3. Understand the design concept of Strip lines and Micro strips.
4. Analyze the features of Antennas & Antenna Arrays.
5. Recommend suitable Antennas for various applications.

Question paper pattern:
- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.

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- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. **Microwave Engineering** – Annapurna Das, Sisir K Das, TMH Publication, 2nd Ed., 2010
2. **Microwave Devices and Circuits**- Liao / Pearson Education
3. **Antennas and Wave Propagation** - John D. Krauss, Ronald J Marhefka and Ahmad S Khan, 4th Special Indian Edition , McGraw- Hill Education Pvt. Ltd., 2010

Reference Books:

1. **Microwave Engineering** – David M Pozar, John Wiley India Pvt. Ltd., 3rd Edn, 2008
2. **Microwave Engineering** – Sushrut Das, Oxford Higher Education, 2nd Edn, 2015
3. **Antennas and Wave Propagation** – Harish and Sachidananda: Oxford University Press, 2007.

COMPUTER COMMUNICATION NETWORKS

Course Code	: **18TE63**	CIE Marks : 40
Lecture Hours/Week	: 03 + 2 (Tutorial)	SEE marks : 60
Total Number of Lecture Hours : 50 (10 Hrs / Module)		Exam Hours : 03
CREDITS : 04		

Course Learning Objectives: This course will enable students to:

- Understand the layering architecture of OSI reference model and TCP/IP protocol suite.
- Understand the protocols associated with each layer.
- Learn the different networking architectures and their representations.
- Learn the functions and services associated with each layer.

Module 1

Introduction: Data communication: Components, Data representation, Data flow, Networks: Network criteria, Physical Structures, Network types: LAN, WAN, Switching, The Internet.

Network Models: Protocol Layering: Scenarios, Principles, Logical Connections, TCP/IP Protocol Suite: Layered Architecture, Layers in TCP/IP suite, Description of layers, Encapsulation and Decapsulation, Addressing, Multiplexing and Demultiplexing, The OSI Model: OSI Versus TCP/IP.

Connecting Devices: Hubs, Switches.

L1 - L3

Module 2

Data-Link Layer: Introduction: Nodes and Links, Services, Categories' of link, Sublayers, Link Layer addressing: Types of addresses, ARP. Data Link Control (DLC) services: Framing, Flow and Error Control, Data Link Layer Protocols: Simple Protocol, Stop and Wait protocol, Piggybacking.

Media Access Control: Random Access: ALOHA, CSMA, CSMA/CD, CSMA/CA. Controlled Access: Reservation, Polling, Token Passing.

Wireless LANs: Introduction: Architectural Comparison, Characteristics, IEEE 802.11: Architecture, MAC Sublayer, Addressing Mechanism, Physical Layer, Bluetooth: Architecture, Layers.

L1 - L3

Module 3

Network Layer: Introduction, Network Layer services: Packetizing, Routing and Forwarding, Other services, Packet Switching: Datagram Approach, Virtual Circuit Approach, IPV4 Addresses: Address Space, Classful Addressing, Classless Addressing, DHCP, Network Address Resolution, Forwarding of IP Packets: Based on destination Address and Label.

Network Layer Protocols: Internet Protocol (IP): Datagram Format, Fragmentation, Options, Security of IPv4 Datagrams, ICMPv4: Messages, Debugging Tools, Mobile IP: Addressing, Agents, Three Phases, Inefficiency in Mobile IP.

Unicast Routing: Introduction, Routing Algorithms: Distance Vector Routing, Link State Routing, Path vector routing.

L1 - L3

Module 4

Transport Layer: Introduction: Transport Layer Services, Connectionless and Connection oriented Protocols, Transport Layer Protocols: Simple protocol, Stop and wait protocol, Go-Back-N Protocol, Selective repeat protocol,

Transport-Layer Protocols:
User Datagram Protocol: User Datagram, UDP Services, UDP Applications, Transmission Control Protocol: TCP Services, TCP Features, Segment, Connection, State Transition diagram, Windows in TCP, Flow control, Error control, TCP congestion control.

L1 - L3

Module 5

Quality of Service: Data flow characteristics: Definitions, Flow control to improve QoS: Scheduling, Traffic shaping.

Application Layer: introduction: providing services, Application- layer paradigms, Standard Client –Server Protocols: World wide web, Hyper Text Transfer Protocol, FTP: Two connections, Control Connection, Data Connection, Electronic Mail: Architecture, Wed Based Mail, Telnet: Local versus remote logging. Domain Name system: Name space, DNS in internet, Resolution, DNS Messages, Registrars, DDNS.

L1 - L3

Course outcomes: At the end of the course students will be able to:
1. Understand the concepts of networking thoroughly
2. Identify the protocols and services of different layers.
3. Distinguish the basic network configurations and standards associated with each network.
4. Analyze the performance of the network
5. Apply the knowledge in establishing computer-based networks for real world problems.

Question paper pattern:
- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.

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- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

Behrouz A Forouzan, "Data Communications and Networking", 5th Edition, McGraw Hill, 2013, ISBN: 1-25-906475-3

Reference Books:

1. James J Kurose, Keith W Ross, Computer Networks, Pearson Education.
2. Wayne Tomasi, Introduction to Data Communication and Networking, Pearson Education.
3. Andrew Tannenbaum, "Computer networks", Prentice Hall.
4. William Stallings, "Data and computer communications", Prentice Hall.

OPERATING SYSTEM

Course Code	: 18EC641	CIE Marks	: 40
Lecture Hours/Week	: 03	SEE Marks	: 60
Total Number of Lecture Hours	: 40 (08 Hrs/module)	Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives: This course will enable students to:
- Understand the services provided by an operating system.
- Explain how processes are synchronized and scheduled.
- Understand different approaches of memory management and virtual memory management.
- Describe the structure and organization of the file system
- Understand interprocess communication and deadlock situations.

Module-1
Introduction to Operating Systems
OS, Goals of an OS, Operation of an OS, Computational Structures, Resource allocation techniques, Efficiency, System Performance and User Convenience, Classes operating System, Batch processing, Multi programming, Time Sharing Systems, Real Time and distributed Operating Systems
(Topics from Sections 1.2, 1.3, 2.2 to 2.8 of Text).
                                                                                L1,L2

Module-2
Process Management: OS View of Processes, PCB, Fundamental State Transitions of a process, Threads, Kernel and User level Threads, Non-preemptive scheduling- FCFS and SRN, Preemptive Scheduling- RR and LCN, Scheduling in Unix and Scheduling in Linux
(Topics from Sections 3.3, 3.3.1 to 3.3.4, 3.4, 3.4.1, 3.4.2 , Selected scheduling topics from 4.2 and 4.3 , 4.6, 4.7 of Text).
                                                                             L1,L2,L3

Module – 3
Memory Management: Contiguous Memory allocation, Non-Contiguos Memory Allocation, Paging, Segmentation, Segmentation with paging, Virtual Memory Management, Demand Paging, VM handler, FIFO, LRU page replacement policies, Virtual memory in Unix and Linux
(Topics from Sections 5.5 to 5.9, 6.1 to 6.3 except Optimal policy and 6.3.1, 6.7,6.8 of Text).
                                                                             L1,L2,L3

File Systems: File systems and IOCS, File Operations, File Organizations, Directory structures, File Protection, Interface between File system and IOCS, Allocation of disk space, Implementing file access

(Topics from Sections 7.1 to 7.8 of Text).   **L1,L2**

Module-5

Message Passing and Deadlocks: Overview of Message Passing, Implementing message passing, Mailboxes, Deadlocks, Deadlocks in resource allocation, Handling deadlocks, Deadlock detection algorithm, Deadlock Prevention

(Topics from Sections 10.1 to 10.3, 11.1 to 11.5 of Text).   **L1,L2**

Course Outcomes: At the end of the course, the students will be able to:
1.   Explain the goals, structure, operation and types of operating systems.
2.   Apply scheduling techniques to find performance factors.
3.   Explain organization of file systems and IOCS.
4.   Apply suitable techniques for contiguous and non-contiguous memory allocation.
5.   Describe message passing, deadlock detection and prevention methods.

Question paper pattern:
- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:
Operating Systems – A Concept based Approach, by Dhamdhere, TMH, 2nd edition.

Reference Books:
1.   Operating Systems Concepts, Silberschatz and Galvin, John Wiley India Pvt. Ltd, 5th edition,2001.
2.   Operating System–Internals and Design System, William Stalling, Pearson Education, 4th ed, 2006.
3.   Operating Systems - Design and Implementation, Tanenbaum, TMH, 2001.

ARITIFICAL NEURAL NETWORKS

Course Code	: 18EC642	CIE Marks	: 40
Lecture Hours/Week	: 03	SEE Marks	: 60
Total Number of Lecture Hours	: 40 (08 Hrs/module)	Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives: This course will enable students to:
- Understand the basics of ANN and comparison with Human brain.
- Acquire knowledge on Generalization and function approximation of various ANN architectures.
- Understand reinforcement learning using neural networks
- Acquire knowledge of unsupervised learning using neural networks.

Module-1

Introduction: Biological Neuron – Artificial Neural Model - Types of activation functions – **Architecture**: Feedforward and Feedback, Convex Sets, Convex Hull and Linear Separability, Non-Linear Separable Problem. XOR Problem, Multilayer Networks.

Learning: Learning Algorithms, Error correction and Gradient Descent Rules, Learning objective of TLNs, Perceptron Learning Algorithm, Perceptron Convergence Theorem.

L1, L2

Module-2

Supervised Learning: Perceptron learning and Non Separable sets, α-Least Mean Square Learning, MSE Error surface, Steepest Descent Search, μ-LMS approximate to gradient descent, Application of LMS to Noise Cancelling, Multi-layered Network Architecture, Back propagation Learning Algorithm, Practical consideration of BP algorithm.

L1,L2,L3

Module-3

Support Vector Machines and Radial Basis Function: Learning from Examples, Statistical Learning Theory, Support Vector Machines, SVM application to Image Classification, Radial Basis Function Regularization theory, Generalized RBF Networks, Learning in RBFNs, RBF application to face recognition.

L1,L2, L3

Module-4

Attractor Neural Networks: Associative Learning Attractor Associative Memory, Linear Associative memory, Hopfield Network, application of Hopfield Network, Brain State in a Box neural Network, Simulated Annealing, Boltzmann Machine, Bidirectional Associative Memory.

Module-5
Self-organization Feature Map: Maximal Eigenvector Filtering, Extracting Principal Components, Generalized Learning Laws, Vector Quantization, Self-organization Feature Maps, Application of SOM, Growing Neural Gas.
L1,L2, L3

Course Outcomes: At the end of the course, students will be able to:
1. Understand the role of neural networks in engineering, artificial intelligence, and cognitive modelling.
2. Understand the concepts and techniques of neural networks through the study of important neural network models.
3. Evaluate whether neural networks are appropriate to a particular application.
4. Apply neural networks to particular application.
5. Analyze the steps needed to improve performance of the selected neural network.

Question paper pattern:
- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:
1. **Neural Networks A Classroom Approach**– Satish Kumar, McGraw Hill Education (India) Pvt. Ltd, Second Edition.

Reference Books:
1. **Introduction to Artificial Neural Systems-**J.M. Zurada, Jaico Publications 1994.
2. **Artificial Neural Networks-**B. Yegnanarayana, PHI, New Delhi 1998.

DATA STRUCTURES USING C++

Course Code	: 18EC643	CIE Marks	: 40
Lecture Hours/Week	: 03	SEE Marks	: 60
Total Number of Lecture Hours	: 40 (08 Hrs/module)	Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives: This course will enable students to
- Solve the problems using object oriented approach
- Explain fundamentals of data structures and their applications essential for programming/problem solving
- Analyze Linear Data Structures: Stack, Queues, Lists
- Analyze Non Linear Data Structures: Trees
- Assess appropriate data structure during program development/Problem Solving

Module -1
INTRODUCTION: C++ and its features, Data types, Variables, Operators, Expressions, Control structures, classes and Objects, Functions and parameters, function overloading, Recursion, Constructors, Destructors and Operator overloading, Inheritance, Polymorphism, Programming examples.

L1, L2

Module -2
ARRAYS AND MATRICES: Arrays, Matrices, Special matrices, Sparse matrices.
POINTERS: Pointers, Dynamic memory allocation
LINEAR LISTS: Data objects and structures, Introduction to Linear and Non Linear data structures, Linear list data structures, Array Representation, Vector Representation, Singly Linked lists and chains.

L1, L2

Module -3
STACKS: The abstract data types, Array Representation, Linked Representation, Applications – Parsing and Evaluation of arithmetic expressions, Parenthesis Matching & Towers of Hanoi.

L1, L2, L3

Module -4
QUEUES: The abstract data types, Array Representation, Linked Representation, Applications-Railroad car arrangement, Priority Queues
HASHING: Dictionaries, Linear representation, Hash table representation.

L1, L2, L3

Module -5

TREES: Binary trees, Properties and representation of binary trees, Common binary tree operations, Binary tree traversal the ADT binary tree, ADT binary tree and the class linked binary tree. Binary search trees operations and implementation. Heaps, Applications-Heap Sorting

L1, L2, L3

Course Outcomes: After studying this course, students will be able to:
1. Relate to Dynamic memory allocation, Various types of data structures, operations and algorithms and Sparse matrices and Hashing
2. Apply object-oriented approach to solve problems
3. Understand non-Linear data structures trees and their applications
4. Design appropriate data structures for solving computing problems
5. Analyze the operations of Linear Data structures: Stack, Queue and Linked List and their applications

Text Book:
1. Data structures, Algorithms, and applications in C++, Sartaj Sahni, Universities Press, 2nd Edition, 2005.

Reference Books:
2. Object Oriented Programming with C++, E.Balaguruswamy, TMH, 6th Edition, 2013.

MICROCONTROLLER and EMBEDDED SYSTEMS

Course Code	: 18TE644	CIE Marks	: 40
Lecture Hours/Week	: 03	SEE Marks	: 60
Total Number of Lecture Hours	: 40 (08 Hrs/module)	Exam Hours	: 03
	CREDITS – 03		

Course Learning Objectives: This course will enable students to
- Understand the architectural features and instruction set of 32 bit microcontroller ARM Cortex M3.
- Program ARM Cortex M3 using the various instructions and C language for different applications.
- Understand the basic hardware components and their selection method based on the characteristics and attributes of an embedded system.
- Develop the hardware software co-design and firmware design approaches.
- Explain the need of real time operating system for embedded system applications.

Module -1
ARM-32 bit Microcontroller: Thumb-2 technology and applications of ARM, Architecture of ARM Cortex M3, Various Units in the architecture, Debugging support, General Purpose Registers, Special Registers, exceptions, interrupts, stack operation, reset sequence (Text 1: Ch 1, 2, 3)
L1, L2

Module -2
ARM Cortex M3 Instruction Sets and Programming: Assembly basics, Instruction list and description, Thumb and ARM instructions, Special instructions, Useful instructions, CMSIS, Assembly and C language Programming (Text 1: Ch-4, Ch-10.1 to 10.6)
L1,L2, L3

Module -3
Embedded System Components: Embedded Vs General computing system, Classification of Embedded systems, Major applications and purpose of ES. Elements of an Embedded System (Block diagram and explanation), Differences between RISC and CISC, Harvard and Princeton, Big and Little Endian, Memory (ROM and RAM types), Sensors, Actuators, Optocoupler, Communication Interfaces (I2C, SPI, IrDA, Bluetooth, Wi-Fi, Zigbee only)
(Text 2: All the Topics from Ch-1 and Ch-2 (Fig and explanation before 2.1), 2.1.1.6 to 2.1.1.8, 2.2 to 2.2.2, 2.3 to 2.3.2 to 2.3.3.3, selected topics of 2.4.1 and 2.4.2 only).
L1, L2

Module -4

Embedded System Design Concepts: Characteristics and Quality Attributes of Embedded Systems, Operational and non-operational quality attributes, Embedded Systems-Application and Domain specific, Hardware Software Co-Design and Program Modelling (excluding UML), Embedded firmware design and development (excluding C language).
(Text 2: Ch-3, Ch-4, Ch-7 (Sections 7.1, 7.2 only), Ch-9 (Sections 9.1, 9.2, 9.3.1, 9.3.2 only)

L1,L2, L3

Module -5

RTOS and IDE for Embedded System Design: Operating System basics, Types of operating systems, Task, process and threads (Only POSIX Threads with an example program), Thread preemption, Preemptive Task scheduling techniques, Task Communication, Task synchronization issues – Racing and Deadlock, Concept of Binary and counting semaphores (Mutex example without any program), How to choose an RTOS, Integration and testing of Embedded hardware and firmware, Embedded system Development Environment – Block diagram (excluding Keil), Disassembler/decompiler, simulator, emulator and debugging techniques
(Text 2: Ch-10 (Sections 10.1, 10.2, 10.3, 10.5.2 , 10.7, 10.8.1.1, 10.8.1.2, 10.8.2.2, 10.10 only), Ch 12, Ch-13 (a block diagram before 13.1, 13.3, 13.4, 13.5, 13.6 only)

L1,L2, L3

Course outcomes: After studying this course, students will be able to:
1. Describe the architectural features and instructions of 32 bit microcontroller ARM Cortex M3.
2. Apply the knowledge gained for Programming ARM Cortex M3 for different applications.
3. Understand the basic hardware components and their selection method based on the characteristics and attributes of an embedded system.
4. Develop the hardware /software co-design and firmware design approaches.
5. Explain the need of real time operating system for embedded system applications.

Question paper pattern:
- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.

- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60
.

Text Books:

1. Joseph Yiu, "The Definitive Guide to the ARM Cortex-M3", 2nd Edition, Newnes, (Elsevier), 2010.
2. Shibu K V, "Introduction to Embedded Systems", Tata McGraw Hill Education Private Limited, 2nd Edition.

Reference Books:

1. James K. Peckol, "Embedded systems- A contemporary design tool", John Wiley, 2008, ISBN: 978-0-471-72180-2.
2. Yifeng Zhu, "Embedded Systems with Arm Cortex-M Microcontrollers in Assembly Language and C", 2nd Edn -Man Press LLC ©2015 ISBN:0982692633 9780982692639.
3. Embedded real time systems by K.V. K. K Prasad, Dreamtech publications, 2003.
4. Embedded Systems by Rajkamal, 2nd Edition, McGraw hill Publications, 2010.

RADIO FREQUENCY INTEGRATED CIRCUITS

Course Code	: 18TE645	CIE Marks	: 40
Lecture Hours/Week	: 03	SEE Marks	: 60
Total Number of Lecture Hours	: 40 (08 Hrs/module)	Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives: This course will enable students to:
- Introduce the theory and concept of Radio Frequency Integrated system.
- Understand different types of key wireless/RF circuits including Amplifier, Switch, Mixer, Oscillator, frequency divider, Frequency doublers, Power divider and Transmission lines.
- Analyze the performance parameters of radio frequency circuits, S-parameters, Rise time, Delay, Bandwidth and Amplifiers and identify design trade-off of radiofrequency communication systems.
- Design RLC Networks, High frequency amplifiers, Low Noise amplifiers and RF amplifiers.

Module-1
Overview of Wireless Principles: A brief history of wireless systems, Non cellular wireless applications, Shannon, Modulations & Alphabet Soup, Propagation.
Passive RLC Networks: Introduction, Parallel RLC Tank, Series RLC Networks, Other RLC networks, RLC Networks as Impedance Transformers.
L1, L2

Module-2
Characteristics of passive IC components: Introduction, Interconnect at radio frequencies: Skin effect, Resisters, Capacitors (Parallel plate capacitor, Interconnect capacitance), Inductors (Spiral and Bond wire), Transformers (Monolithic transformer realization), and Interconnect options at high frequency.
A Review of MOS Device Physics: FETs, MOSFET physics, The long –channels approximation (Drain current in linear region, Drain current in saturation, Dynamic elements), Operation in weak inversion (sub threshold), MOS device physics in the short – channel regime, Other effects.
L1, L2

Module-3
Distributed Systems: Introduction, Link between lumped and distributed regimes, Driving-point Impedance of Iterated structures, Transmission lines in more detail, Behavior of Finite – length transmission lines.

The Smith Chart and S-Parameters: Introduction, The smith chart, S parameters, Band Width Estimation Techniques, Introduction, The method of open – circuit time constant (Observation and interpretations, Accuracy of open circuit time constant, Other important considerations), The method of short circuit time constant, Rise time, Delay and Bandwidth (Exclude: Application of the Rise time addition rule, Rise time addition and bandwidth shrinkage).

L1 - L4

Module-4

High Frequency Amplifier Design: Introduction, Zeros as Bandwidth Enhancers, The shunt –series amplifier, Bandwidth Enhancement with fTDoublers, Tuned amplifiers.

Voltage References and Biasing: Introduction, Review of diode behavior, Diodes and bipolar transistors in CMOS technology, Supply –independent bias circuits, Band gap voltage reference, Constant gmbias.

L1, L2, L3

Module-5

Low Noise Amplifier Design: Introduction, Derivation of intrinsic MOSFET two port noise parameters, LNA topologies: Power match versus noise match, Power constrained noise optimization. Mixers: Introduction, Mixer fundamental, Nonlinear systems as linear mixers.

RF Power Amplifiers: Introduction, General considerations, Class A, AB, B and C power amplifier, Class D amplifiers, Class E amplifiers, Class F amplifiers, RF PA design examples.

L1, L2, L3

Course Outcomes: After studying this course, students will be able to:
 1. Describe the theory and concepts of Radio Frequency Integrated system
 2. Understand Wireless systems, RLC networks, Passive Components, MOS devices, Transmission lines, Amplifiers and Mixer.
 3. Analyze characteristics of RLC Networks, Passive IC components, MOS devices, S-parameters, Rise time, Delay, Bandwidth and Amplifiers.
 4. Design RLC Networks, High frequency amplifiers, Low Noise amplifiers and RF amplifiers with general considerations.
 5. Design using Smith chart and S-parameters.

Question paper pattern:
- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:
The Design of CMOS Radio-Frequency Integrated Circuit, Thomas H. Lee, 2nd edition, Cambridge, 2004.

Reference Book:
Design of Analog CMOS Integrated Circuits, Razavi, Behzad, Tata McGraw Hill, 2005.

PYTHON APPLICATION PROGRAMMING

Course Code	: 18EC646	CIE Marks	: 40
Lecture Hours/Week	: 03	SEE Marks	: 60
Total Number of Lecture Hours	: 40(08 Hrs/module)	Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives: This course will enable students to
* Learn Syntax and Semantics and create Functions in Python.
* Handle Strings and Files in Python.
* Understand Lists, Dictionaries and Regular expressions in Python.
* Implement Object Oriented Programming concepts in Python
* Build Web Services, Network and Database Programs in Python.

Module – 1
Why should you learn to write programs, Variables, expressions and statements, Conditional execution, Functions,

L1, L2, L3

Module – 2
Iteration, Strings, Files,

L1, L2, L3

Module – 3
Lists, Dictionaries, Tuples, Regular Expressions,

L1, L2, L3

Module – 4
Classes and objects, Classes and functions, Classes and methods,

L1, L2, L3

Module – 5
Networked programs, Using Web Services, Using databases and SQL,

L1, L2, L3

Course outcomes: The students will be able to:
1. Examine Python syntax and semantics and be fluent in the use of Python flow control and functions.
2. Demonstrate proficiency in handling Strings and File Systems.
3. Create, run and manipulate Python Programs using core data structures like Lists, Dictionaries and use Regular Expressions.
4. Interpret the concepts of Object-Oriented Programming as used in Python.
5. Implement exemplary applications related to Network Programming, Web Services and Databases in Python.

Question paper pattern:
- The question paper will have TEN questions.
- There will be TWO questions from each module.
- Each question will have questions covering all the topics under a module.
- The students will have to answer FIVE full questions, selecting ONE full question from each module.

Text Books:
1. Charles R. Severance, "Python for Everybody: Exploring Data Using Python 3", 1st Edition, Create Space Independent Publishing Platform, 2016 (Chapters 1 – 13, 15).
2. Allen B. Downey, "Think Python: How to Think Like a Computer Scientist", 2nd Edition, Green Tea Press, 2015 (Chapters 15,16,17)

References:
1. Mark Lutz, "Programming Python", 4th Edition, O'Reilly Media, 2011.ISBN-13:978-9350232873.
2. Wesley J Chun, "Core Python Applications Programming", 3rd Edition, Pearson Education India, 2015. ISBN-13: 978-9332555365.
3. Reema Thareja, "Python Programming using problem solving approach", Oxford university press, 2017

SIGNAL PROCESSING

Course Code	: 18EC651	CIE Marks	: 40
Lecture Hours/Week	: 03	SEE Marks	: 60
Total Number of Lecture Hours	: 40 (08 Hrs/module)	Exam Hours	: 03
CREDITS – 03			

Course objective: This course will enable students to:

- Understand, represent and classify continuous time and discrete time signals and systems, together with the representation of LTI systems.
- Ability to represent continuous time signals (both periodic and non-periodic) in the time domain, s-domain and the frequency domain
- Understand the properties of analog filters, and have the ability to design Butterworth filters
- Understand and apply sampling theorem and convert a signal from continuous time to discrete time or from discrete time to continuous time (without loss of information)
- Able to represent the discrete time signal in the frequency domain
- Able to design FIR and IIR filters to meet given specifications

Module-1

Signal Definition, Signal Classification, System definition, System classification, for both continuous time and discrete time. Definition of LTI systems

(Chapter 1)   **L1, L2**

Module-2

Introduction to Fourier Transform, Fourier Series, Relating the Laplace Transform to Fourier Transform, Frequency response of continuous time systems,

(Chapter 3)   **L1, L2**

Module-3

Frequency response of ideal analog filters, Salient features of Butterworth filters Design and implementation of Analog Butterworth filters to meet given specifications

(Chapter 8)   **L1,L2, L3**

Module-4

Sampling Theorem- Statement and proof, converting the analog signal to a digital signal. Practical sampling. The Discrete Fourier Transform, Properties of DFT. Comparing the frequency response of analog and digital systems. (FFT not included)

(Chapter 3, 4)   **L1,L2, L3**

Module-5

Definition of FIR and IIR filters. Frequency response of ideal digital filters Transforming the Analog Butterworth filter to the Digital IIR Filter using suitable mapping techniques, to meet given specifications. Design of FIR Filters using the Window technique, and the frequency sampling technique to meet given specifications Comparing the designed filter with the desired filter frequency response

(Chapter 8)   **L1,L2,L3**

Course Outcomes: After studying this course, students will be able to:

1. Understand and explain continuous time and discrete time signals and systems, in time and frequency domain
2. Apply the concepts of signals and systems to obtain the desired parameter/ representation
3. Analyse the given system and classify the system/arrive at a suitable conclusion
4. Design analog/digital filters to meet given specifications
5. Design and implement *assignment component)*
   a. the analog filter using components/ suitable simulation tools
   b. the digital filter (FIR/IIR) using suitable simulation tools, and
   c. record the input and output of the filter for the given audio signal

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

- 'Signals and Systems', by Simon Haykin and Barry Van Veen, Wiley.

References:

1. 'Theory and Application of Digital Signal Processing', Rabiner and Gold
2. 'Signals and Systems', Schaum's Outline series
3. 'Digital Signal Processing', Schaum's Outline series

SENSORS and SIGNAL CONDITIONING

Course Code	: 18EC652	CIE Marks	: 40
Lecture Hours/Week	: 03	SEE Marks	: 60
Total Number of Lecture Hours : 40 (08 Hrs/module)		Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives: This course will enable students to:
- Understand various technologies associated in manufacturing of sensors
- Acquire knowledge about types of sensors used in modern digital systems
- Get acquainted about material properties required to make sensors

Module 1
Introduction to sensor based measurement systems:
General concepts and terminology, sensor classification, primary sensors, material for sensors, microsensor technology, magnetoresistors, light dependent resistors, resistive hygrometers,resistive gas sensors, liquid conductivity sensors
(Selected topics from ch.1 & 2 of Text)
                                                            L1, L2

Module 2
Reactance Variation and Electromagnetic Sensors: -Capacitive Sensors, Inductive Sensors, Electromagnetic Sensors.
Signal Conditioning for Reactance Variation Sensors-Problems and Alternatives, ac Bridges Carrier Amplifiers, Coherent Detection, Specific Signal Conditioners for Capacitive Sensors, Resolver-to-Digital and Digital-to-Resolver Converters.   **L1, L2**

Module 3
Self-generating Sensors-Thermoelectric sensors, piezoelectric sensors, pyroelectric sensors, photovoltaic sensors, electrochemical sensors.
                                                            L2, L3

Module 4
Digital and intelligent sensors-position encoders, resonant sensors, sensors based on quartz resonators, SAW sensors, Vibrating wire strain gages, vibrating cylinder sensors, Digital flow meters.
                                                            L2, L3

Module 5

Sensors based on semiconductor junctions -Thermometers based on semiconductor junctions, magneto diodes and magneto transistors, photodiodes and phototransistors, sensors based on MOSFET transistors, charge- coupled sensors – types of CCD imaging sensors, ultrasonic-based sensors.

L2, L3

Course Outcomes: After studying this course, students will be able to:
1. Appreciate various types of sensors
2. Describe the manufacturing process of sensors
3. Understand about the material properties required to make sensors
4. Use sensors specific to the end use application
5. Design systems integrated with sensors

Question paper pattern:
- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:
"Sensors and Signal Conditioning", Ramon PallásAreny, John G. Webster, 2nd edition, John Wiley and Sons, 2000

B. E. EC/TE			
Choice Based Credit System (CBCS) and Outcome Based Education (OBE)			
SEMESTER – VI			
VIRTUAL INSTRUMENTATION			
Course Code	18EC653	**CIE Marks**	40
Number of Lecture Hours/Week	03	**SEE Marks**	60
Total Number of Lecture Hours	40(8Hours/Module)	**Exam Hours**	03
CREDITS – 03			

Course objective: This course will enable students to:
- Understand the fundamental principles of virtual instrumentation
- Acquire, analyze and present data using LabVIEW

Module-1	**RBT Level**
Graphical System Design: Introduction, Graphical system design model, Design flow with GSD, Virtual Instrumentation, Virtual instrument and traditional instrument, Hardware and software in virtual instrumentation, Virtual instrumentation for Test, control & design, Graphical system design using LABVIEW, Graphical programming & textual programming.	L1, L2, L3
Module-2	
Introduction to LabVIEW: Introduction, advantages of LABVIEW software environment, palettes, front panel controls & indicators, Block diagram, Data flow program. **Repetition and Loops**: For loops, while loops, structure tunnels, terminals inside or outside loops, shift registers, feed-back nodes, control timing, case structure.	L1, L2, L3
Module-3	
Arrays: Introduction, arrays in LABVIEW, creating one - dimensional array controls, indicators and constants, creating two dimensional arrays, creating multidimensional arrays, initializing array, deleting, inserting, and replacing elements, rows, columns, and pages with in arrays, arrays functions.	L1, L2, L3
Module-4	
Plotting Data: Types of waveforms, waveform graphs, waveform charts, XY graphs, Intensity graphs & charts, Digital waveform graphs, 3D graphs, customizing graphs & charts, configuring a graph or chart, Displaying special planners on the XY graph.	L1,L2, L3
Module-5	
File Input/ Output: File formats, file write &read, generating filenames automatically, **String handling**: string functions, LABVIEW string formats, parsing of strings. **Instrument Control**: Introduction, GPIB communication, Hardware specification, software architecture, Instrument I/O assistant, VISA, Instrument drivers, serial port communications, using other interfaces.	L1, L2, L3

Course Outcomes: After studying this course, students will be able to:
1. Recognize the Graphical system design model and develop programs using the modern tools of Graphical programming & textual programming
2. Develop a virtual instrumentation model using the front panel controls & indicators and loops.
3. Analyze, design the various array and matrix operations using LabVIEW functions.
4. Evaluate the various forms of output representations using graphs & charts
5. Demonstrate Instrument Control, GPIB communication and other interfaces

Students have to conduct the following experiments as a part of CIE marks along with other Activities:

1.   Build a VI code to indicate the change in temperature using LabVIEW
2.   Develop a code in VI to convert 4-bit binary input to gray output using LabVIEW
3.   Generate a VI code to display sinusoidal and triangular waveforms using LabVIEW
4.   Build a code using LabVIEW to compute the sum of N numbers (use FOR loop)
5.   Develop a VI code using LabVIEW to sort the even numbers (use while loop)
6.   Using LabVIEW compute the basic operations of a simple calculator using case structure

Question paper pattern:
- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:
1. "Virtual Instrumentation using LABVIEW", Jovitha Jerome, PHI, 2010
2. "Virtual Instrumentation using LABVIEW", Sanjay Gupta, Joseph John, TMH, McGraw Hill Second Edition, 2011.

Reference:
"Learning with LabView", Robert H Bishop, Prentice Hall, 2009.

B. E. EC/TE Choice Based Credit System (CBCS) and Outcome Based Education (OBE) SEMESTER – VI			
MICROCONTROLLERS			
Course Code	18EC654	CIE Marks	40
Number of Lecture Hours/Week	03	SEE Marks	60
Total Number of Lecture Hours	40(8Hours/Module)	Exam Hours	03
CREDITS – 03			

Course objective: This course will enable students to:
- Learn architecture of 8051.
- Learn programming skills using Assembly language and C
- Design and interface microcontroller based embedded systems.
- Build projects

Module-1	RBT Level
Microprocessors and Microcontroller: Introduction, Microprocessors and Microcontrollers, Microcontroller Survey. (Text 1- Chapter 1) **The 8051 Architecture**: Introduction, Architecture of 8051, Pin diagram of 8051, Memory organization. (Text 1- Chapter 2)	L1, L2
Module-2	
Addressing Modes in 8051 Microcontroller: Introduction, Addressing Modes, External Data Moves, Code Memory Read only Data Moves, PUSH and POP opcodes, Data Exchanges, Example Programs. (Text 1- Chapter 3)	L1, L2
Module-3	
Instruction set: Instruction timings, 8051 instructions: Data transfer instructions, Arithmetic instructions, Logical instructions, Branch instructions, Subroutine instructions, Bit manipulation instruction. (Text 1- Chapter 4, 5 and 6)	L1, L2, L3
Module-4	
8051 Microcontroller Interfacing and Applications: Interfacing 8051 to LCD, Keyboard, parallel and serial ADC, DAC interfacing and programming. (Text 2 – Chapter 12 and 13)	L1,L2, L3
Module-5	
8051 Microcontroller Interrupts and Timers/counters: Basics of interrupts, 8051 interrupt structure, Timers and Counters, 8051 timers/counters, programming 8051 timers in assembly and C . (Text 2 – Chapter 9, Chapter 11 -11.1) **8051 Microcontroller Serial Communication**: Data communication, Basics of Serial Data Communication, 8051 Serial Communication, connections to RS-232, Serial communication Programming in assembly and C. (Text 2 – Chapter 10- 10.1,10.2, 10.3)	L1, L2, L3

Course Outcomes: After studying this course, students will be able to:
1. Explain the basics of Microprocessor and Microcontroller
2. Relate to the 8051 Microcontroller architecture and Pin description
3. Analyze 8051 Addressing modes and use the 8051 instruction set
4. Program the on-chip peripherals in 8051
5. Design and develop applications using 8051 Assembly language and C program

Students have to conduct the following experiments as a part of CIE marks along with other Activities:
1. Write an 8051 ALP to exchange n = 5 bytes of data at location 0027H and at location 0041H.
2. Write an 8051 ALP to sort an array of n = 6 bytes of data in ascending order stored from location 9000H.(use bubble sort algorithm)

3. Write an 8051 ALP to implement (display) an eight bit up/down binary (hex) counters on watch window.
4. Write a program to toggle all the bits of P1 and P2 continuously using CALL and RETURN instructions
5. Write an 8051 ALP to implement ASCII to hexadecimal conversion
6. Write a Program illustrating timer delay Generate a 1second delay continuously using the on-chip timer in interrupt mode.

Question paper pattern:
- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:
1. "The 8051 Microcontroller Architecture, Programming and Applications", Kenneth J Ayala, Thomson learning, 2005.
2. "The 8051 Microcontroller and Embedded Systems-using Assembly and C", Muhammad Ali Mazidi and Janice Gillespie Mazidi and Rollin D McKinaly, Pearson, 2006.

Reference:
"The 8051 Microcontroller: Hardware, Software and Applications" V. Udayashankara and Mallikarjuna Swamy, TMH., 2009.

B. E. EC/TE			
Choice Based Credit System (CBCS) and Outcome Based Education (OBE) SEMESTER – VI			
BASIC VLSI DESIGN			
Course Code	18EC655	CIE Marks	40
Number of Lecture Hours/Week	03	SEE Marks	60
Total Number of Lecture Hours	40(8Hours/Module)	Exam Hours	03
CREDITS – 03			
Course objective: This course will enable students to: • Understand the fundamental aspects of circuits in silicon • Relate to VLSI design processes and design rules			
Module-1			**RBT Level**
Moore's law, speed power performance, nMOS fabrication, CMOS fabrication: n-well, p-well processes, BiCMOS, Comparison of bipolar and CMOS. **Basic Electrical Properties of MOS And BiCMOS Circuits**: Drain to source current versus voltage characteristics, threshold voltage, transconductance.			L1, L2
Module-2			
Basic Electrical Properties of MOS And BiCMOS Circuits: nMOS inverter, Determination of pull up to pull down ratio: nMOS inverter driven through one or more pass transistors, alternative forms of pull up, CMOS inverter, BiCMOS inverters, latch up. **Basic Circuit Concepts**: Sheet resistance, area capacitance calculation, Delay unit, inverter delay, estimation of CMOS inverter delay, super buffers, BiCMOS drivers.			L1, L2
Module-3			
MOS and BiCMOS Circuit Design Processes: MOS layers, stick diagrams, nMOS design style, CMOS design style **Design rules and layout & Scaling of MOS Circuits**: λ - based design rules, scaling factors for device parameters			L1, L2, L3
Module-4			
Subsystem Design and Layout-1: Switch logic pass transistor, Gate logic inverter, NAND gates, NOR gates, pseudo nMOS, Dynamic CMOS **Examples of structured design**: Parity generator, Bus arbitration, multiplexers, logic function block, code converter.			L1,L2, L3
Module-5			
Subsystem Design and Layout-2: Clocked sequential circuits, dynamic shift registers, bus lines, General considerations, 4-bit arithmetic processes, 4-bit shifter, Regularity-Definition & Computation **Practical aspects and testability**: Some thoughts of performance, optimization and CAD tools for design and simulation.			L1, L2, L3
Course Outcomes: After studying this course, students will be able to: 1. Identify the CMOS layout levels, and the design layers used in the process sequence. 2. Describe the general steps required for processing of CMOS integrated circuits. 3. Design static CMOS combinational and sequential logic at the transistor level. 4. Demonstrate different logic styles such as complementary CMOS logic, pass-transistor Logic, dynamic logic, etc. 5. Interpret the need for testability and testing methods in VLSI.			

Question paper pattern:
- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:
"Basic VLSI Design", Douglas A Pucknell, Kamran Eshraghian, 3rd Edition, Prentice Hall of India publication, 2005.

References:
1. "CMOS Digital Integrated Circuits, Analysis And Design", Sung – Mo (Steve) Kang, Yusuf Leblebici, Tata McGraw Hill, 3rd Edition, 2003.
2. "VLSI Technology", S.M. Sze, 2nd edition, Tata McGraw Hill, 2003.

CCN LABORATORY

Course Code : **18TEL66**	CIE Marks : 40	SEE Marks : 60
Lecture Hours/Week: 02 Hours Tutorial (Instructions) + 02 Hours Laboratory		
RBT Level : L1, L2, L3	Exam Hours : 03	
CREDITS– 02		

Course Learning Objectives: This course will enable students to:

- Choose suitable tools to Model a Network and Understand the Protocols at various OSI reference levels.
- Design a suitable Network and Simulate using a Network Simulator Tool.
- Simulate the Networking Concepts and Protocols using C/C++ Programming.
- Model the Networks for different Configurations and Analyze the Results.

Laboratory Experiments

PART A: Simulation Experiments using NS2/NS3/OPNET/NCTUNS/
NetSim/QualNet or any other equivalent tool

1. Simulate a Point to Point Network with Four Nodes and Duplex Links between them. Analyze the Network Performance by Setting the Queue Size and Varying the Bandwidth.

2. Simulate Ethernet LAN using n(6-10) Nodes and Assign Multiple traffic to the Nodes to obtain
   i. Congestion Window for different Sources/ Destinations.
   ii. Compare the Throughput by changing the Error Rate and Data Rate.

3. Simulate the Transmission of Ping Messages over a Network Topology consisting of Six Nodes and Find the Number of Packets dropped due to Congestion.

4. Simulate a Simple BSS with Transmitting Nodes in Wireless LAN and Determine the Performance with respect to Transmission of Packets.

5. Build a Four-node Point to Point Network with links n0-n2, n1-n2 and n2-n3.Connect a TCP link between n0-n3 and UDP link between n1-n3.
   (i) Define BERs for Links. Compare TCP and UDP Protocols when errors occur.
   (ii) Modify to Simulate a Link Failure between the Host and the Target Node. Compare TCP and UDP Protocols when the Target Node is not accessible.

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6. Simulate a Network with a Star Topology (One Router and several Hosts). Declare Applications (TCP or UDP) to send Packets from Hosts and to Receive(on one Host). Test the Bandwidth and the Delay, when Buffers are of infinite Capacities and Buffers are of Limited Capacities.

7. Simulate Link State Routing Algorithm.

PART B: Implement the following experiments in C/C++

1. Write a Program for asynchronous Communication (Example: File Transfer) between PCs using RS232 Cable.

2. Write a Program for a HLDC Frame to perform the following.
   a. Bit Stuffing
   b. Character Stuffing.

3. Write a Program to obtain CRC Code for the given Data, using CRC-CCITT (CRC 16) Polynomial. Verify the Program for the Cases.
   a.   Without Error
   b.   With Error

4. Write Programs for Simulation of Stop and Wait Protocol and Sliding Window Protocol.

5. Write a Program for Dijkstra's Algorithm to Compute the Shortest Routing Path.

6. Write a Program for RSA Algorithm for Encryption and Decryption of Data.

7. Write a Program for Congestion Control using Leaky Bucket Algorithm.

Course outcomes: After studying this course, students will be able to:

1. Use the Network Simulator Tools.
2. Design and Simulate Network elements with various Protocols and Standards.
3. Model the networks for different configurations.
4. Analyze the network performance.
5. Demonstrate the Working of various Protocols and Algorithms using C Programming.

Conduction of Practical Examination:

1. All Laboratory Experiments are to be included for Practical Examination.
2. For examination One Question from PART-A and One question from PART-B to be set.
3. Students are allowed to Pick One Experiment from the Lot.
4. Strictly follow the Instructions as Printed on the Cover Page of Answer Script for breakup of Marks.
5. Change of Experiment is allowed only once and Marks allotted to the Procedure part to be made zero.

ANALOG and DIGITAL COMMUNICATION LABORATORY

Course Code : **18TEL67**	CIE Marks : 40	SEE Marks : 60
Lecture Hours/Week: 02 Hours Tutorial (Instructions) + 02 Hours Laboratory		
RBT Level : L1, L2, L3		Exam Hours : 03
CREDITS – 02		

Course Learning Objectives: This Laboratory course will enable the Students to

• Understand the Analog modulation and demodulation techniques.
• Study the concepts of Time Division Multiplexing.
• Understand the designing of Analog and Digital Modulation schemes.
• Study and analyze the generation of Line Codes.
• Model an Optical Communication System and study its Characteristics.
• Gain hands on experience in Simulating the Digital Communication concepts

Laboratory Experiments
PART-A: Following Expt. 1 to Expt. 5 have to be performed using discrete components.

1. Amplitude Modulation and Demodulation: i) Standard AM, ii)DSBSC (LM741 and LF398 ICs can be used)
2. Frequency modulation and demodulation (IC 8038/2206 can be used)
3. Pulse sampling, flat top sampling and reconstruction
4. Time Division Multiplexing and Demultiplexing of two bandlimited signals.
5. PSK and FSK Generation & Detection.
6.   DPSK & QPSK Generation and Detection.
7. Generation of Line Codes.
8.   Measurement of Propagation Loss, Bending Loss and Numerical Aperture of an Optical Fiber.

PART-B: Simulation Experiments using SCILAB/MATLAB/Simulink or LabVIEW

1. Pulse code Modulation and Demodulation.
2. Delta modulation, Adaptive delta Modulation.
3. Simulate the transmission of baseband signals with raised cosine Transmitter Filter and Plot Eye Diagram.
4.   Computations of the Probability of bit error for coherent binary ASK, FSK and PSK for an AWGN Channel and Compare them with their Performance curves.

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Course Outcomes: At the end of the Course the Students will be able to:
1. Demonstrate Time Division Multiplexing.
2. Design and test Analog and Digital Modulation and demodulation circuits.
3. Design and Generate Line codes for Signal Transmission.
4. Analyze the characteristics of an optical communication system.
5. Simulate the Digital Communication concepts, Compute and Display various parameters along with Plots/Figures.

Conduct of Practical Examination:
- All Laboratory Experiments are to be included for Practical Examination.
- Students are allowed to pick one Experiment from the lot.
- For examination one question from **PART-A** and one question from **PART-B** to be set.
- Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.
- Change of Experiment is allowed only once and the Marks allotted for the Procedure part to be made zero.

B. E. 2018 Scheme Seventh Semester Syllabus (EC / TC)
Choice Based Credit System (CBCS) and Outcome Based Education (OBE)

SEMESTER – VII
OPTICAL COMMUNICATION

Course Code	: 18TE71	CIE Marks	: 40
Lecture Hours/Week	: 3	SEE Marks	: 60
Total Number of Lecture Hours : 40 (08 Hrs/module)		Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives: This course will enable students to:
- Learn the basic principle of optical fiber communication with different modes of light propagation.
- Understand the transmission characteristics and losses in optical fiber.
- Study of optical components and its applications in optical communication networks.
- Learn the network standards in optical fiber and understand the network architectures along with its functionalities.

Module-1
Optical fiber Communications: Historical development, The general system, Advantages of optical fiber communication, Optical fiber waveguides: Ray theory transmission, Modes in planar guide, Phase and group velocity, Cylindrical fiber: Modes, Step index fibers, Graded index fibers, Single mode fibers, Cutoff wavelength, Mode field diameter, effective refractive index. Fiber Materials, Photonic crystal fibers. (Text 2)

L1, L2, L3

Module-2
Transmission characteristics of optical fiber: Attenuation, Material absorption losses, Linear scattering losses, Nonlinear scattering losses, Fiber bend loss, Dispersion, Chromatic dispersion, Intermodal dispersion: Multimode step index fiber.
Optical Fiber Connectors: Fiber alignment and joint loss, Fiber splices, Fiber connectors, Fiber couplers. (Text 2)

L1,L2, L3

Module-3

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Optical sources: Energy Bands, Direct and Indirect Bandgaps, Light Emitting diodes: LED Structures, Light Source Materials, Quantum Efficiency and LED Power, Modulation. Laser Diodes: Modes and Threshold conditions, Rate equation, External Quantum Efficiency, Resonant frequencies, Laser Diode structures and Radiation Patterns: Single mode lasers.

Photodetectors: Physical principles of Photodiodes, Photodetector noise, Detector response time.

Optical Receiver: Optical Receiver Operation: Error sources, Front End Amplifiers, Receiver sensitivity, Quantum Limit. (Text 1)

L1, L2

Module-4

WDM Concepts and Components: Overview of WDM: Operational Principles of WDM, WDM standards, Mach-Zehnder Interferometer Multiplexers, Isolators and Circulators, Fiber grating filters, Dielectric Thin-Film Filters, Diffraction Gratings, Active Optical Components, Tunable light sources.

Optical amplifiers: Basic application and Types, Semiconductor optical amplifiers, Erbium Doped Fiber Amplifiers, Raman Amplifiers, Wideband Optical Amplifiers. (Text 1)

L1,L2, L3

Module-5

Optical Networks: Optical network evolution and concepts: Optical networking terminology, Optical network node and switching elements, Wavelength division multiplexed networks, Public telecommunication network overview. Optical network transmission modes, layers and protocols: Synchronous networks, Asynchronous transfer mode, OSI reference model, Optical transport network, Internet protocol, Wavelength routing networks: Routing and wavelength assignment, Optical switching networks: Optical circuit switched networks, packet switched networks, Multiprotocol Label Switching, Optical burst switching networks, Optical network deployment: Long-haul networks, Metropolitan area networks, Access networks, Local area networks. (Text 2)

L1, L2, L3

Course Outcomes: At the end of the course, the students will be able to:
1. Classification and working of optical fiber with different modes of signal propagation.
2. Describe the transmission characteristics and losses in optical fiber communication.
3. Describe the construction and working principle of optical connectors, multiplexers and amplifiers.

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4. Describe the constructional features and the characteristics of optical sources and detectors.
5. Illustrate the networking aspects of optical fiber and describe various standards associated with it.

Question paper pattern:
- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

TEXT BOOKS:
1. Gerd Keiser, Optical Fiber Communication, 5th Edition, McGraw Hill Education (India) Private Limited, 2015. ISBN: 1-25-900687-5.
2. John M Senior, Optical Fiber Communications, Principles and Practice, 3rd Edition, Pearson Education, 2010, ISBN: 978-81-317-3266-3.

REFERENCE BOOK:
Joseph C Palais, Fiber Optic Communication, Pearson Education, 2005, ISBN:0130085103

WIRELESS   COMMUNICATION

Course Code	: 18TE72	CIE Marks	: 40
Lecture Hours/Week	: 3	SEE Marks	: 60
Total Number of Lecture Hours : 40(08 Hrs / Module)		Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives: The objectives of the course is to enable students to:

• Understand the concepts of propagation mechanisms in wireless channels from a physics standpoint.

• Analyse propagation model for simple channels involving two paths only using concepts studied from physics.

• Develop a statistical model for practical channels involving multiplicity of propagation paths and its application in a cellular scenario.

• Application of Communication theory both Physical and networking to understand GSM and CDMA systems that handle mobile telephony.

Module-1
Mobile Radio Propagation – Large Scale Path Loss

Introduction, Free Space Propagation Model, Relating Power to Electric Field, Three Basic Propagation Mechanisms – Reflection (Ground Reflection), Diffraction, Scattering, Practical Link Budget, Outdoor Propagation Models (Okumura – Hata Model only). (Chapter 4.1 – 4.10, Text 1)

L1, L2, L3, L4

Module-2
Mobile Radio Propagation – Small Scale Fading and Multipath

Small Scale Multipath Propagation, Impulse Response of Multipath Channel, Small Scale Multipath Measurements, Parameters of Mobile Multipath Channels, Types of Small scale Fading, Rayleigh and Rician Distributions, Statistical Models for Multipath Fading Channels. (Chapter 5.1 – 5.7, Text 1)

The Cellular Concept – System Design Fundamentals

Frequency Reuse, Channel Assignment Strategies, Handoff Strategies, Interference and System Capacity. Trunking and Grade of Service. (Chapter 3.2 – 3.6, Text 1)

L1, L2, L3

Module-3
Multiple Access Techniques for Wireless Communications

Introduction to Multi Access, Frequency Division Multi Access, Time Division Multi Access, Spread Spectrum Multi Access, Space Division Multi Access,

Packet Radio, Capacity of Cellular systems.
(Chapter 9.1 – 9.7 , Text 1)
Improving Coverage and Capacity in Cellular Systems (3.7, Text 1)
L1, L2, L3, L4

Module-4

GSM – Global System for Mobile Communications: Historical Overview; System Overview – (Base Station Subsystem, Network and Switching Subsystem, Operating Support System), The Air Interface, Logical and Physical Channels – (Logical Channels, Mapping Between Logical and Physical Channels); Synchronization – (Frequency Synchronization, Time Synchronization, Timing Advance, Summary of Burst Structures); Coding – (Voice Encoding, Channel Encoding, Cryptography, Frequency Hopping); Equalizer, Circuit-Switched Data Transmission – (Establishing a Connection and Handover, Identity Numbers, Identification of a Mobile Subscriber, Examples for Establishment of a Connection, Examples of Different Kinds of Handovers); Services and Billing – (Available Services, Billing). General Packet Radio Service. (Chapter 24, Text 2)
L1, L2, L3

Module-5

IS-95 and CDMA 2000 : System Overview, Air Interface – (Frequency Bands and Duplexing, Spreading and Modulation, Power Control, Pilot Signal), Coding – (Speech Coders, Error Correction Coding), Spreading and Modulation –(Long and Short Spreading Codes and Walsh Codes, Spreading and Modulation in the Uplink, Databurst Randomization and Gating for the Uplink, Spreading and Modulation in the Downlink), Logical and Physical Channels – (Traffic Channels, Access Channel, Pilot Channels, Synchronization Channel, Paging Channel, Power Control Subchannel, Mapping Logical Channels to Physical Channels), Handover. CDMA 2000 –History, 1x Mode, 3x Mode, 1xEV-DO (Chapter 25, Text 2)
L1, L2, L3

Course outcomes: At the end of the course, the students will be able to:
1. Explain concepts of propagation mechanisms like Reflection, Diffraction, Scattering in wireless channels.
2. Analyse signal received levels for simple channels involving two paths only and multipath propagation channels in a specific cellular scenario.
3. Develop a scheme for idle mode, call set up, call progress handling and call tear down in a GSM cellular network.
4. Develop a scheme for idle mode, call set up, call progress handling and call tear down in a CDMA cellular network.
5. Describe multiple access techniques for wireless communications.

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Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

TEXT BOOKS:

1. **"Wireless Communications: Principles and Practice"** Theodore Rappaport, 2nd Edition, Prentice Hall Communications Engineering and Emerging Technologies Series, 2002, ISBN 0-13-042232-0.
2. **"Wireless Communications",** Andreas F Molisch, 2nd Edition, John Wiley and Sons, 2011, ISBN: ISBN: 9780470741870 (H/B), ISBN: 9780470741863 (P/B)

REAL TIME SYSTEM

Course Code	: 18EC731	CIE Marks	: 40
Lecture Hours/Week	: 3	SEE Marks	: 60
Total Number of Lecture Hours : 40 (08 Hrs / Module)		Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives: This Course will enable students to:
- Understand the fundamentals of Real-time systems and its classifications.
- Describe the concepts of computer control and hardware components for Real-Time Application.
- Discuss the languages to develop software for Real-Time Applications.
- Explain the concepts of operating system and RTS development methodologies.

Module-1
Introduction to Real-Time Systems: Historical background, Elements of a Computer Control System, RTS- Definition, Classification of Real-time Systems, Time Constraints, Classification of Programs.
Concepts of Computer Control: Introduction, Sequence Control, Loop Control, Supervisory Control, Centralized Computer Control, Hierarchical Systems.
(Text: 1.1 to 1.6 and 2.1 to 2.6),   **L1, L2**

Module-2
Computer Hardware Requirements for Real-Time Applications: Introduction, General Purpose Computer, Single Chip Microcomputers and Microcontrollers, Specialized Processors, Process-Related Interfaces, Data Transfer Techniques, Communications, Standard Interface.
(Text: 3.1 to 3.8).   **L1, L2**

Module-3
Languages for Real-Time Applications: Introduction, Syntax Layout and Readability, Declaration and Initialization of Variables and Constants, Cutlass, Modularity and Variables, Compilation of Modular Programs, Data types, Control Structures, Exception Handling, Low-level facilities, Co-routines, Interrupts and Device Handling, Concurrency, Real-Time Support, Overview of Real-Time Languages.
(Text: 5.1 to 5.14).,   **L1,L2, L3**

Module-4
Operating Systems: Introduction, Real-Time Multi-Tasking OS, Scheduling

Strategies, Priority Structures, Task Management, Scheduler and Real-Time Clock Interrupt Handler, Memory Management, Code Sharing, Resource Control, Task Co-Operation and Communication, Mutual Exclusion.
(Text: 6.1 to 6.11). **L1, L2**

Module-5

Design of RTS – General Introduction: Introduction, Specification Document, Preliminary Design, Single-Program Approach, Foreground/Background System.
RTS Development Methodologies: Introduction, Yourdon Methodology, Ward and Mellor Method, Hately and Pirbhai Method.
(Text: 7.1 to 7.5 and 8.1, 8.2, 8.4,8.5). **L1, L2, L3**

Course Outcomes: At the end of the course, students should be able to:
1. Explain the fundamentals of Real time systems and its classifications.
2. Understand the concepts of computer control and the suitable computer hardware requirements for real-time applications.
3. Describe the operating system concepts and techniques required for real time systems.
4. Develop the software algorithms using suitable languages to meet Real time applications.
5. Apply suitable methodologies to design and develop Real-Time Systems.

Text Book:
- Real-Time Computer Control, Stuart Bennet, 2nd Edn. Pearson Education. 2008.

Reference Books:
1. "Real –Time Systems", C.M. Krishna, Kang G. Shin, McGraw –Hill International Editions, 1997.
2. Real-Time Systems Design and Analysis, Phillip. A. Laplante, second edition, PHI, 2005.
3. Embedded Systems, Raj Kamal, Tata McGraw Hill, India, third edition, 2005.

SATELLITE COMMUNICATION

Course Code	: 18EC732	CIE Marks	: 40
Lecture Hours/Week	: 3	SEE Marks	: 60
Total Number of Lecture Hours : 40 (08 Hrs / Module)		Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives: This course will enable students to
- Understand the basic principle of satellite orbits and trajectories.
- Study of electronic systems associated with a satellite and the earth station.
- Understand the various technologies associated with the satellite communication.
- Focus on a communication satellite and the national satellite system.
- Study of satellite applications focusing various domains services such as remote sensing, weather forecasting and navigation.

Module-1

Satellite Orbits and Trajectories: Definition, Basic Principles, Orbital parameters, Injection velocity and satellite trajectory, Types of Satellite orbits, Orbital perturbations, Satellite stabilization, Orbital effects on satellite's performance, Eclipses, Look angles: Azimuth angle, Elevation angle. ,
L1, L2

Module-2

Satellite subsystem: Power supply subsystem, Attitude and Orbit control, Tracking, Telemetry and command subsystem, Payload.
Earth Station: Types of earth station, Architecture, Design considerations, Testing, Earth station Hardware, Satellite tracking.,
L1, L2

Module-3

Multiple Access Techniques: Introduction, FDMA (No derivation), SCPC Systems, MCPC Systems, TDMA, CDMA, SDMA.
Satellite Link Design Fundamentals: Transmission Equation, Satellite Link Parameters, Propagation considerations
L1,L2, L3

Module-4

Communication Satellites: Introduction, Related Applications, Frequency Bands, Payloads, Satellite Vs. Terrestrial Networks, Satellite Telephony, Satellite Television, Satellite radio, Regional satellite Systems, National Satellite Systems.

L1, L2

Module-5

Remote Sensing Satellites: Classification of remote sensing systems, orbits, Payloads, Types of images: Image Classification, Interpretation, Applications.
Weather Forecasting Satellites: Fundamentals, Images, Orbits, Payloads, Applications.
Navigation Satellites: Development of Satellite Navigation Systems, GPS system, Applications.,

L1,L2, L3

Course Outcomes: At the end of the course, the students will be able to:
1. Describe the satellite orbits and its trajectories with the definitions of parameters associated with it.
2. Describe the electronic hardware systems associated with the satellite subsystem and earth station.
3. Describe the communication satellites with the focus on national satellite system.
4. Compute the satellite link parameters under various propagation conditions with the illustration of multiple access techniques.
5. Describe the satellites used for applications in remote sensing, weather forecasting and navigation.

Question paper pattern:
- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:
- Anil K. Maini, Varsha Agrawal, Satellite Communications, Wiley India Pvt. Ltd., 2015, ISBN: 978-81-265-2071-8.

Reference Books :
1. Dennis Roddy, Satellite Communications, 4th Edition, McGraw- Hill International edition, 2006
2. Timothy Pratt, Charles Bostian, Jeremy Allnutt, Satellite Communications, 2nd Edition, Wiley India Pvt. Ltd , 2017, ISBN: 978-81-265-0833-4

DIGITAL IMAGE PROCESSING

Course Code	: 18EC733	CIE Marks	: 40
Lecture Hours/Week	: 3	SEE Marks	: 60
Total Number of Lecture Hours : 40 (08 Hrs / Module)		Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives: This course will enable students to
- Understand the fundamentals of digital image processing.
- Understand the image transforms used in digital image processing.
- Understand the image enhancement techniques used in digital image processing.
- Understand the image restoration techniques and methods used in digital image processing.
- Understand the Morphological Operations used in digital image processing.

Module 1
Digital Image Fundamentals: What is Digital Image Processing?, Origins of Digital Image Processing, Examples of fields that use DIP, Fundamental Steps in Digital Image Processing, Components of an Image Processing System, Elements of Visual Perception, Image Sensing and Acquisition.
(Text: Chapter 1 and Chapter 2: Sections 2.1 to 2.2, 2.6.2)   L1,L2

Module-2
Image Enhancement in the Spatial Domain: Image Sampling and Quantization, Some Basic Relationships Between Pixels, Linear and Nonlinear Operations. Some Basic Intensity Transformation Functions, Histogram Processing, Fundamentals of Spatial Filtering, Smoothing Spatial Filters, Sharpening Spatial Filters
(Text:Chapter2: Sections 2.3 to 2.62, Chapter3: Sections3.2 to 3.6), L1,L2

Module-3
Frequency Domain: Preliminary Concepts, The Discrete Fourier Transform (DFT) of Two Variables, Properties of the 2-DDFT, Filtering in the Frequency Domain, Image Smoothing and Image Sharpening Using Frequency Domain Filters, Selective Filtering.
(Text: Chapter4: Sections 4.2, 4.5 to 4.10),   L1,L2

Module-4
Restoration: Noise models, Restoration in the Presence of Noise Only using Spatial Filtering and Frequency Domain Filtering, Linear, Position-Invariant degradations Estimating the Degradation Function, Inverse Filtering, Minimum

Mean Square Error(Wiener) Filtering, Constrained Least Squares Filtering.
(Text: Chapter 5: Sections 5.2, to 5.9) **L1,L2**

Module-5

Morphological Image Processing: Preliminaries, Erosion and Dilation, Opening and Closing.

Image Processing: Color Fundamentals, Color Models, Pseudo color Image Processing.

(Text: Chapter 6: Sections 6.1 to 6.3 Chapter 9: Sections9.1to9.3)
L1,L2

Course Outcomes: At the end of the course, students should be able to:
1. Describe the fundamentals of digital image processing.
2. Understand image formation and the role human visual system plays in perception of gray and color image data.
3. Apply image processing techniques in both the spatial and frequency (Fourier) domains.
4. Design and evaluate image analysis techniques
5. Conduct independent study and analysis of Image Enhancement and restoration techniques.

Question paper pattern:
- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:
- Digital Image Processing- Rafel C Gonzalez and Richard E. Woods, PHI 3rd Edition 2010.

Reference Books:
1. Digital Image Processing- S. Jayaraman, S. Esakkirajan,T. Veerakumar, Tata Mc Graw Hill 2014.
2. Fundamentals of Digital Image Processing- A. K. Jain, Pearson 2004.
3. Image Processing analysis and Machine vision with Mind Tap by Milan Sonka and Roger Boile, Cengage Publications, 2018.

DSP ALGORITHMS and ARCHITECTURE

Course Code	: 18EC734	CIE Marks	: 40
Lecture Hours/Week	: 3	SEE Marks	: 60
Total Number of Lecture Hours : 40 (08 Hrs / Module)		Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives: This course will enable students to:

- Figure out the knowledge and concepts of digital signal processing techniques.
- Understand the computational building blocks of DSP processors and its speed issues.
- Understand the various addressing modes, peripherals, interrupts and pipelining structure of TMS320C54xx processor.
- Learn how to interface the external devices to TMS320C54xx processor in various modes.
- Understand basic DSP algorithms with their implementation.

Module -1

Introduction to Digital Signal Processing:

Introduction, A Digital Signal – Processing System, The Sampling Process, Discrete Time Sequences, Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear Time-Invariant Systems, Digital Filters, Decimation and Interpolation.

Computational Accuracy in DSP Implementations:

Number Formats for Signals and Coefficients in DSP Systems, Dynamic Range and Precision, Sources of Error in DSP Implementation.

L1,L2

Module -2

Architectures for Programmable Digital Signal – Processing Devices:

Introduction, Basic Architectural Features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Speed Issues, Features for External Interfacing.

L1,L2

Module -3

Programmable Digital Signal Processors:

Introduction, Commercial Digital Signal-processing Devices, Data Addressing Modes of TMS32OC54XX, Memory Space of TMS32OC54xx Processors, Program Control. Detail Study of TMS320C54X & 54xx Instructions and

Programming, On – Chip Peripherals, Interrupts of TMS32OC54XX Processors, Pipeline Operation of TMS32OC54xx Processor.

L1,L2

Module -4
Implementation of Basic DSP Algorithms:
Introduction, The Q – notation, FIR Filters, IIR Filters, Interpolation and Decimation Filters (one example in each case).
Implementation of FFT Algorithms:
Introduction, An FFT Algorithm for DFT Computation, Overflow and Scaling, Bit – Reversed Index. Generation & Implementation on the TMS32OC54xx.

L1,L2

Module -5
Interfacing Memory and Parallel I/O Peripherals to Programmable DSP Devices:
Introduction, Memory Space Organization, External Bus Interfacing Signals. Memory Interface, Parallel I/O Interface, Programmed I/O, Interrupts and I/O Direct Memory Access (DMA).
Interfacing and Applications of DSP Processors:
Introduction, Synchronous Serial Interface, A CODEC Interface Circuit, DSP Based Bio-telemetry Receiver, A Speech Processing System, An Image Processing System.

L1,L2

Course Outcomes: At the end of this course, students would be able to:
1. Comprehend the knowledge and concepts of digital signal processing techniques.
2. Apply the knowledge of DSP computational building blocks to achieve speed in DSP architecture or processor.
3. Apply knowledge of various types of addressing modes, interrupts, peripherals and pipelining structure of TMS320C54xx processor.
4. Develop basic DSP algorithms using DSP processors.
5. Discuss about synchronous serial interface and multichannel buffered serial port (McBSP) of DSP device and demonstrate the programming of CODEC interfacing.

Question paper pattern:
• Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
• Each full question can have a maximum of 4 sub questions.
• There will be 2 full questions from each module covering all the topics

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of the module.

- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

- "Digital Signal Processing", Avatar Singh and S. Srinivasan, Thomson Learning, 2004.

Reference Books:

1. "Digital Signal Processing: A practical approach", Ifeachor E. C., Jervis B. W Pearson-Education, PHI, 2002.
2. "Digital Signal Processors", B Venkataramani and M Bhaskar, TMH, 2nd, 2010
3. "Architectures for Digital Signal Processing", Peter Pirsch John Wiley, 2008

CMOS VLSI DESIGN

Course Code	: 18TE735	CIE Marks	: 40
Lecture Hours/Week	: 3	SEE Marks	: 60
Total Number of Lecture Hours : 40 (08 Hrs / Module)		Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives: This course will enable students to:
• Impart knowledge of MOS transistor theory and CMOS technologies
• Learn the operation principles and analysis of inverter circuits.
• Design Combinational, sequential and dynamic logic circuits as per the requirements
• Infer the operation of Semiconductors Memory circuits.
• Demonstrate the concepts of CMOS testing

Module -1
Introduction: A Brief History, MOS Transistors, CMOS Logic (1.1 to 1.4 of TEXT 2)
MOS Transistor Theory: Introduction, Long-channel I-V Characteristics, Non-ideal I-V Effects, DC Transfer Characteristics (2.1, 2.2, 2.4 and 2.5 of TEXT 2).
L1,L2

Module -2
Fabrication: CMOS Fabrication and Layout, VLSI Design Flow, Introduction, CMOS Technologies, Layout Design Rules, (1.5 and 3.1 to 3.3 of TEXT 2).
MOSFET Scaling and Small-Geometry Effects, MOSFET Capacitances (3.5 to 3.6 of TEXT 1)
L1,L2, L3

Module -3
Delay: Introduction, Transient Response, RC Delay Model, Linear Delay Model, Logical Efforts of Paths (4.1 to 4.5 of TEXT2, except sub-sections 4.3.7, 4.4.5, 4.4.6, 4.5.5 and 4.5.6)
Combinational Circuit Design: Introduction, Circuit families (9.1 to 9.2 of TEXT 2, except subsection 9.2.4)
L1,L2

Module -4
Sequential Circuit Design: Introduction, Circuit Design for Latches and Flip-Flops (10.1 and 10.3.1 to 10.3.4 of TEXT 2)

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Dynamic Logic Circuits: Introduction, Basic Principles of Pass Transistor Circuits, Synchronous Dynamic Circuit Techniques, Dynamic CMOS Circuit Techniques (9.1, 9.2, 9.4 to 9.5 of TEXT 1)

L1,L2, L3

Module -5

Semiconductor Memories: Introduction, Dynamic Random Access Memory (DRAM) and Static Random Access Memory (SRAM), (10.1 to 10.3 of Text 1)

Testing and Verification: Introduction, Logic Verification Principles, Manufacturing Test Principles, Design for testability (15.1, 15.3, 15.5 15.6.1 to 15.6.3 of Text 2).

L1, L2, L3

Course Outcomes: At the end of the course, the students will be able to:

1. Demonstrate understanding of MOS transistor theory, CMOS fabrication flow and technology scaling.
2. Draw the basic gates using the stick and layout diagrams with the knowledge of physical design aspects.
3. Demonstrate ability to design Combinational, sequential and dynamic logic circuits as per the requirements.
4. Interpret Memory elements along with timing considerations.
5. Interpret testing and testability issues in VLSI Design.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. "CMOS Digital Integrated Circuits: Analysis and Design" - Sung Mo Kang & Yosuf Leblebici**,** Third Edition, Tata McGraw-Hill.

2. "CMOS VLSI Design- A Circuits and Systems Perspective"**-** Neil H. E. Weste, and David Money Harris, 4th Edition, Pearson Education.

Reference Books:

1. Adel Sedra and K. C. Smith, "Microelectronics Circuits Theory and Applications", 6th or 7th Edition, Oxford University Press, International Version, 2009.
2. Douglas A Pucknell & Kamran Eshraghian, "Basic VLSI Design", PHI 3rd Edition, (original Edition – 1994).
3.Behzad Razavi, "Design of Analog CMOS Integrated Circuits", TMH, 2007.

IoT & WIRELESS SENSOR NETWORKS

Course Code	: 18EC741	CIE Marks	: 40
Lecture Hours/Week	: 3	SEE Marks	: 60
Total Number of Lecture Hours : 40 (08 Hrs / Module)		Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives: This course will enable students to:
- Describe the OSI Model for IoT/M2M Systems.
- Understand the architecture and design principles for device supporting IoT.
- Develop competence in programming for IoT Applications.
- Identify the uplink and downlink communication protocols which best suits the specific application of IOT / WSNs.

Module-1
Overview of Internet of Things: IoT Conceptual Framework, IoT Architectural View, Technology Behind IoT, Sources of IoT, M2M communication, Examples of IoT. Modified OSI Model for the IoT/M2M Systems, data enrichment, data consolidation and device management at IoT/M2M Gateway, web communication protocols used by connected IoT/M2M devices, Message communication protocols (CoAP-SMS, CoAP-MQ, MQTT, XMPP) for IoT/M2M devices. – Refer Chapter 1, 2 and 3 of Text 1.
L1, L2

Module-2
Architecture and Design Principles for IoT: Internet connectivity, Internet-based communication, IPv4, IPv6, 6LoWPAN protocol, IP Addressing in the IoT, Application layer protocols: HTTP, HTTPS, FTP, TELNET and ports.
Data Collection, Storage and Computing using a Cloud Platform: Introduction, Cloud computing paradigm for data collection, storage and computing, Cloud service models, IoT Cloud- based data collection, storage and computing services using Nimbits. - Refer Chapter 4 and 6 of Text 1.
L1, L2

Module-3
Prototyping and Designing Software for IoT Applications: Introduction, Prototyping Embedded device software, Programming Embedded Device Arduino Platform using IDE, Reading data from sensors and devices, Devices, Gateways, Internet and Web/Cloud services software development.
Programming MQTT clients and MQTT server. Introduction to IoT privacy

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and security. Vulnerabilities, security requirements and threat analysis, IoT Security Tomography and layered attacker model. - Refer Chapter 9 and 10 of Text 1. **L1, L2, L3**

Module-4
Overview of Wireless Sensor Networks:
Challenges for Wireless Sensor Networks, Enabling Technologies for Wireless Sensor Networks.
Architectures: Single-Node Architecture - Hardware Components, Energy Consumption of Sensor Nodes, Operating Systems and Execution Environments, Network Architecture-Sensor Network Scenarios, Optimization Goals and Figures of Merit, Design principles for WSNs, Service interfaces of WSNs Gateway Concepts. - Refer Chapter 1, 2, 3 of Text 2.
L1, L2, L3

Module-5
Communication Protocols:
Physical Layer and Transceiver Design Considerations, MAC Protocols for Wireless Sensor Networks, Low Duty Cycle Protocols And Wakeup Concepts - S-MAC , The Mediation Device Protocol, Wakeup Radio Concepts, Contention based protocols(CSMA,PAMAS), Schedule based protocols (LEACH, SMACS, TRAMA) Address and Name Management in WSNs, Assignment of MAC Addresses, Routing Protocols- Energy-Efficient Routing, Geographic Routing, Hierarchical networks by clustering. - Refer Chapter 4, 5, 7 and 11 of Text 2.
L1, L2, L3

Course Outcomes: At the end of the course, students will be able to:
1. Understand choice and application of IoT & M2M communication protocols.
2. Describe Cloud computing and design principles of IoT.
3. Relate to MQTT clients, MQTT server and its programming.
4. Describe the architectures and its communication protocols of WSNs.
5. Identify the uplink and downlink communication protocols associated with specific application of IOT / WSNs

Question paper pattern:
- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.

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- Students will have to answer 5full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:
1. Raj Kamal, "Internet of Things-Architecture and design principles", McGraw Hill Education.
2. Holger Karl & Andreas Willig, "Protocols And Architectures for Wireless Sensor Networks", John Wiley, 2005.

Reference Books:
1. Feng Zhao & Leonidas J. Guibas, "Wireless Sensor Networks- An Information Processing Approach", Elsevier, 2007.
2. Kazem Sohraby, Daniel Minoli, & Taieb Znati, "Wireless Sensor Networks- Technology, Protocols and Applications", John Wiley, 2007.
3. Anna Hac, "Wireless Sensor Network Designs", John Wiley, 2003.

AUTOMOTIVE ELECTRONICS

Course Code	: 18EC742	CIE Marks	: 40
Lecture Hours/Week	: 3	SEE Marks	: 60
Total Number of Lecture Hours : 40 (08 Hrs / Module)		Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives: This course will enable students to:
- Understand the basics of automobile dynamics and design electronics to complement those features.
- Design and implement the electronics that attribute the reliability, safety, and smartness to the automobiles, providing add-on comforts.

Module -1

Automotive Fundamentals Overview – Evolution of Automotive Electronics, Automobile Physical Configuration, Survey of Major Automotive Systems, The Engine – Engine Block, Cylinder Head, Four Stroke Cycle, Engine Control, Ignition System - Spark plug, High voltage circuit and distribution, Spark pulse generation, Ignition Timing, Diesel Engine, Drive Train - Transmission, Drive Shaft, Differential, Suspension, Brakes, Steering System (Text 1: Chapter1), Starter Battery –Operating principle:
(Text 2: Pg. 407-410)
The Basics of Electronic Engine Control – Motivation for Electronic Engine Control – Exhaust Emissions, Fuel Economy, Concept of an Electronic Engine control system, Definition of General terms, Definition of Engine performance terms, Engine mapping, Effect of Air/Fuel ratio, spark timing and EGR on performance, Control Strategy, Electronic Fuel control system, Analysis of intake manifold pressure, Electronic Ignition.
(Text 1: Chapter 5)   **L1, L2**

Module -2

Automotive Sensors – Automotive Control System applications of Sensors and Actuators – Variables to be measured, Airflow rate sensor, Strain Gauge MAP sensor, Engine Crankshaft Angular Position Sensor, Magnetic Reluctance Position Sensor, Hall effect Position Sensor, Shielded Field Sensor, Optical Crankshaft Position Sensor, Throttle Angle Sensor (TAS), Engine Coolant Temperature (ECT) Sensor, Exhaust Gas Oxygen (O2/EGO) Lambda Sensors, Piezoelectric Knock Sensor. **(Text 1: Chapter 6)**
Automotive Engine Control Actuators – Solenoid, Fuel Injector, EGR Actuator, Ignition System
(Text 1: Chapter 6)   **L1, L2**

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Module -3

Digital Engine Control Systems – Digital Engine control features, Control modes for fuel Control (Seven Modes), EGR Control, Electronic Ignition Control - Closed loop Ignition timing, Spark Advance Correction Scheme, Integrated Engine Control System - Secondary Air Management, Evaporative Emissions Canister Purge, Automatic System Adjustment, System Diagnostics. **(Text 1: Chapter 7)**

Control Units – Operating conditions, Design, Data processing, Programming, Digital modules in the Control unit, Control unit software.
(Text 2: Pg. 196-207) **L1, L2**

Module -4

Automotive Networking –Bus Systems – Classification, Applications in the vehicle, Coupling of networks, Examples of networked vehicles
(Text 2: Pg. 85-91),
Buses - CAN Bus, LIN Bus, MOST Bus, Bluetooth, Flex Ray, Diagnostic Interfaces. **(Text 2: Pg. 92-151)**
Vehicle Motion Control – Typical Cruise Control System, Digital Cruise Control System, Digital Speed Sensor, Throttle Actuator, Digital Cruise Control configuration, Cruise Control Electronics (Digital only), Antilock Brake System (ABS)
(Text 1: Chapter 8) **L1,L2**

Module -5

Automotive Diagnostics–Timing Light, Engine Analyzer, On-board diagnostics, Off-board diagnostics, Expert Systems, Occupant Protection Systems – Accelerometer based Air Bag systems. **(Text 1: Chapter 10)**
Future Automotive Electronic Systems – Alternative Fuel Engines, Electric and Hybrid vehicles, Fuel cell powered cars, Collision Avoidance Radar warning Systems, Low tire pressure warning system, Heads Up display, Speech Synthesis, Navigation – Navigation Sensors - Radio Navigation, Signpost navigation, dead reckoning navigation, Voice Recognition Cell Phone dialing, Advanced Cruise Control, Stability Augmentation, Automatic driving Control
(Text 1: Chapter 11) **L1, L2,L3**

Course Outcomes: At the end of the course, students will be able to:
1. Describe the basics of automobile dynamics and design electronics.
2. Acquire an overview of automotive components, subsystems, and basics of Electronic Engine Control in today's automotive industry.
3. Use available automotive sensors and actuators while interfacing with microcontrollers / microprocessors during automotive system design.

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4. Understand the networking of various modules in automotive sys-
tems, communication protocols and diagnostics of the sub systems.
5. Design and implement the electronics that attribute the reliability,
safety, and smartness to the automobiles, providing add-on comforts
and get fair idea on future Automotive Electronic Systems.

Question paper pattern:
- Examination will be conducted for 100 marks with question paper containing
10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the
module.
- Students will have to answer 5 full questions, selecting one full question
from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is
60.

Text Books:
1. William B. Ribbens, "Understanding Automotive Electronics", 6th
Edition, Elsevier Publishing.
2. Robert Bosch GmbH (Ed.) Bosch Automotive Electrics and Automotive
Electronics Systems and Components, Networking and Hybrid Drive,
5th edition, John Wiley & Sons Inc., 2007.

MULTIMEDIA COMMUNICATION

Course Code	: 18EC743	CIE Marks	: 40
Lecture Hours/Week	: 03	SEE Marks	: 60
Total Number of Lecture Hours : 40 (08 Hrs / Module)		Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives: This course will enable students to:
- Understand the importance of multimedia in today's online and offline information sources and repositories.
- Understand the how Text, Audio, Image and Video information can be represented digitally in a computer so that it can be processed, transmitted and stored efficiently.
- Understand the Multimedia Transport in Wireless Networks
- Understand the Real-time multimedia network applications.
- Understand the Different network layer based application.

Module - 1

Multimedia Communications: Introduction, Multimedia information representation, multimedia networks, multimedia applications, Application and networking terminology.
(Chapter 1 of Text 1)   **L1,L2**

Module - 2

Information Representation: Introduction, Digitization principles, Text, Images, Audio and Video.
(Chapter 2 of Text 1)   **L1,L2**

Module - 3

Text and Image Compression: Introduction, Compression principles, text compression, image Compression.**(Chapter 3 of Text 1)**
Distributed Multimedia Systems: Introduction, main Features of a DMS, Resource management of DMS, Networking, Multimedia Operating Systems.
(Chapter 4 - Sections 4.1 to 4.5 of Text 2),   **L1,L2**

Module -4

Audio and video compression: Introduction, Audio compression, video compression, video compression principles, video compression.
(Chapter 4 of Text 1)   **L1,L2**

Multimedia Information Networks: Introduction, LANs, Ethernet, Token ring, Bridges, FDDI High-speed LANs, LAN protocol**(Chap. 8 of Text 1)**.
The Internet: Introduction, IP Datagrams, Fragmentation, IP Address, ARP and RARP, QoS Support, IPv8.
(Chap. 9 of Text 1), L1,L2

Course Outcomes: After studying this course, students will be able to:
1. Understand basics of different multimedia networks and applications.
2. Understand different compression techniques to compress audio and video.
3. Describe multimedia Communication across Networks.
4. Analyse different media types to represent them in digital form.
5. Compress different types of text and images using different compression techniques.

Question paper pattern:
- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:
1. Multimedia Communications- Fred Halsall, Pearson Education, 2001, ISBN -9788131709948.
2. Multimedia Communication Systems- K. R. Rao, Zoran S. Bojkovic, Dragorad A. Milovanovic, Pearson Education, 2004. ISBN - 9788120321458.

Reference Book:
- Multimedia: Computing, Communications and Applications- Raifsteinmetz, Klara Nahrstedt, Pearson Education,2002.ISBN- 978817758

CRYPTOGRAPHY

Course Code	: 18EC744	CIE Marks	: 40
Lecture Hours/Week	: 03	SEE Marks	: 60
Total Number of Lecture Hours : 40 (08 Hrs / Module)		Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives: This course will enable students to:
* Understand the basics of symmetric key and public key cryptography.
* Explain classical cryptography algorithms.
* Acquire knowledge of mathematical concepts required for cryptography.
* Describe pseudo random sequence generation technique.
* Explain symmetric and asymmetric cryptography algorithms.

Module -1
Classical Encryption Techniques: Symmetric cipher model, Substitution techniques, Transposition techniques **(Text 1: Chapter 1)**
Basic Concepts of Number Theory and Finite Fields: Euclidean algorithm, Modular arithmetic
(Text 1: Chapter 3)   **L1,L2**

Module -2
SYMMETRIC CIPHERS: Traditional Block Cipher structure, Data encryption standard (DES), The AES Cipher.
(Text 1: Chapter 2: Section1, 2, Chapter 4:Section 2, 3, 4)   **L1,L2**

Module -3
Basic Concepts of Number Theory and Finite Fields: Groups, Rings and Fields, Finite fields of the form GF(p), Prime Numbers, Fermat's and Euler's theorem, discrete logarithm.
(Text 1: Chapter 3 and Chapter 7: Section 1, 2, 5)   **L1,L2**

Module -4
ASYMMETRIC CIPHERS: Principles of Public-Key Cryptosystems, The RSA algorithm, Diffie - Hellman Key Exchange, Elliptic Curve Arithmetic, Elliptic Curve Cryptography
(Text 1: Chapter 8, Chapter 9: Section 1, 3, 4)   **L1,L2,L3**

Module -5
Pseudo-Random-Sequence Generators and Stream Ciphers:
Linear Congruential Generators, Linear Feedback Shift Registers, Design and analysis of stream ciphers, Stream ciphers using LFSRs, A5, Hughes XPD/

KPD, Nanoteq, Rambutan, Additive generators, Gifford, Algorithm M,PKZIP
(**Text 2: Chapter 16**)   **L1,L2, L3**

Course Outcomes: After studying this course, students will be able to:
1. Explain basic cryptographic algorithms to encrypt and decrypt the data.
2. Use symmetric and asymmetric cryptography algorithms to encrypt and decrypt the information.
3. Describe the mathematics associated with cryptography.
4. Apply concepts of modern algebra in cryptography algorithms.
5. Apply pseudo random sequence in stream cipher algorithms.

Question paper pattern:
- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:
1. William Stallings , "Cryptography and Network Security Principles and Practice", Pearson Education Inc., 6th Edition, 2014, ISBN: 978-93-325-1877-3
2. Bruce Schneier, "Applied Cryptography Protocols, Algorithms, and Source code in C", Wiley Publications, 2nd Edition, ISBN: 9971-51-348-X.

Reference Books:
1. Cryptography and Network Security, Behrouz A. Forouzan, TMH, 2007.
2. Cryptography and Network Security, Atul Kahate, TMH, 2003.

MACHINE LEARNING WITH PYTHON

Course Code	: 18EC745	CIE Marks	: 40
Lecture Hours/Week	: 03	SEE Marks	: 60
Total Number of Lecture Hours : 40 (08 Hrs / Module)		Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives: This course will enable students to
- Define machine learning and problems relevant to machine learning.
- Differentiate supervised, unsupervised and reinforcement learning
- Apply neural networks, Bayes classifier and k nearest neighbor, for problems appear in machine learning.
- Perform statistical analysis of machine learning techniques.

Module – 1
Introduction: Well posed learning problems, Designing a Learning system, Perspective and Issues in Machine Learning.
Concept Learning: Concept learning task, Concept learning as search, Find-S algorithm, Version space, Candidate Elimination algorithm, Inductive Bias.
Python libraries suitable for Machine Learning: Numerical Analysis and Data Exploration with NumPy Arrays, and Data Visualization with Matplotlib
Text Book1, Sections: 1.1 – 1.3, 2.1-2.5, 2.7　　　　　**L1 - L5**

Module – 2
Decision Tree Learning: Decision tree representation, Appropriate problems for decision tree learning, Basic decision tree learning algorithm, hypothesis space search in decision tree learning, Inductive bias in decision tree learning, Issues in decision tree learning. Example program in Python
Text Book1, Sections: 3.1-3.7　　　　　**L1 - L3**

Module – 3
Artificial Neural Networks : Introduction, Neural Network representation, Appropriate problems, Perceptrons, Back propagation algorithm. Example program in Python
Text book 1, Sections: 4.1 – 4.6　　　　　**L1 - L3**

Module – 4
Bayesian Learning: Introduction, Bayes theorem, Bayes theorem and concept learning, ML and LS error hypothesis, ML for predicting probabilities, MDL principle, Naive Bayes classifier, Bayesian belief networks, EM algorithm, Example program in Python.

Text book 1, Sections: 6.1 – 6.6, 6.9, 6.11, 6.12   **L1 - L4**

Module – 5

Evaluating Hypothesis: Motivation, Estimating hypothesis accuracy, Basics of sampling theorem, General approach for deriving confidence intervals, Difference in error of two hypothesis, Comparing learning algorithms.

Instance Based Learning: Introduction, k-nearest neighbor learning, locally weighted regression, radial basis function, cased-based reasoning,

Reinforcement Learning: Introduction, Learning Task, Q Learning Example program in Python.

Text book 1, Sections: 5.1-5.6, 8.1-8.5, 13.1-13.3   **L1 - L3**

Course Outcomes: After studying this course, students will be able to

1.   Identify the problems in machine learning.
2.   Select supervised, unsupervised or reinforcement learning for problem solving.
3.   Apply theory of probability and statistics in machine learning
4.   Apply concept learning, ANN, Bayes classifier, k nearest neighbor
5.   Perform statistical analysis of machine learning techniques.

Question paper pattern:
*   The question paper will have ten questions.
*   There will be 2 questions from each module.
*   Each question will have questions covering all the topics under a module.
*   The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:
1.   Tom M. Mitchell, Machine Learning, India Edition 2013, McGraw Hill Education.

Reference Books:
1.   Trevor Hastie, Robert Tibshirani, Jerome Friedman, The Elements of Statistical Learning, 2nd edition, springer series in statistics.
2.   Ethem Alpaydýn, Introduction to machine learning, second edition, MIT press.
3.   https://www.analyticsvidhya.com/blog/2015/04/comprehensive-guide-data-exploration-sas-using-python-numpy-scipy-matplotlib-pandas/
4.   https://www.oreilly.com/library/view/python-for-data/9781491957653/ch01.html

WIRELESS COMMUNICATION LABORATORY

Course Code : **18TEL76**	CIE Marks : 40	SEE Marks : 60

Lecture Hours/Week: 02 Hours Tutorial (Instructions) + 02 Hours Laboratory

RBT Level : L1 - L4   Exam Hours : 03

CREDITS – 02

Note: Conduct the following experiments to implement the indicated communication processes by simulation using MATLAB or any equivalent tool.

Laboratory Experiments

1. Develop a code to compute the Path loss, Link Budget and sketch relevant plot.

2. Develop a code to represent the different channel models for wireless networks.

3. Analysis of cellular concepts like cell-sectoring, splitting (using Qualnet/ NS3/ any other tool).

4. To consider 2 to 4 message signals, and obtain the Time-Division-Multiplexed waveform and then perform de-multiplexing and get back the original message signals (represent the signal in time domain and frequency domain at various stages).

5. Consider 24 message signals, and obtain the T1 Carrier bit stream. (represent the signal in time domain and frequency domain at various stages).

6. Consider the irreducible polynomial of order N (3 or 4), and obtain the 2^N-1 Codes, for the CDMA system. Build the Spread Spectrum modulation using any one of the valid codes.

7. To verify the correlation properties of the codes developed for the CDMA.

8. To build the BPSK-OFDM modulated waveform for binary input data stream, and recover the message signals from the modulated waveform.

9. To build the QPSK-OFDM modulated waveform for binary input data stream, and recover the message signals from the modulated waveform.

10. To build the GMSK modulated waveform for binary input data stream, and recover the message signals from the modulated waveform.

Course outcomes: On the completion of this laboratory course, the students will be able to:
1. Use simulation tools to demonstrate various aspects of the communication process.
2. Demonstrate the modulation/demodulation based on BPSK/QPSK-OFDM, GMSK, TDM.
3. Analyze the properties/performance of CDMA based codes.
4. Model the T1 Carrier bit stream.
5. Develop codes to characterize and compute the parameters of different channel models of wireless networks.

Conduct of Practical Examination:
- All laboratory experiments are to be included for practical examination.
- Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.
- Change of experiment is allowed only once and Marks allotted to the procedure part to be made zero.

MICROWAVE and ANTENNAS LABORATORY

Course Code : **18TEL77**	CIE Marks : 40	SEE Marks : 60
Lecture Hours/Week: 02 Hours Tutorial (Instructions) + 02 Hours Laboratory		
RBT Level : L1 - L4	Exam Hours : 03	
CREDITS – 02		

Course Learning Objectives: This course will enable students to:
- Understand the Mode Characteristics of Reflex Klystron Oscillator.
- Study the Performance and Extract S-parameters of various Microwave components.
- Study the Radiation Pattern and Find the Field Intensity, Polarization of a given Antenna/ Array.
- Measure Impedance of a given Microwave Component.
- Understand the analyses of Three Point method of obtaining equivalent Circuit Parameters & Dielectric Strength.
- Appraise the proof of Reciprocity Theorem as applied to Antennas.

Laboratory Experiments

1. Study of Reflex Klystron Oscillator Mode Characteristics.

2. Three point method of obtaining equivalent Circuit Parameters.

3. Measurement of Impedance using slotted Line Assembly.

4. Measurement of Dielectric Strength.

5. Study of Circulator/Isolator. Extraction of S-Parameters.

6. Study of Directional coupler. Extraction of S-Parameters.

7. Study of E-plane, H-plane & Magic Tee. Extraction of S-Parameters.

8. Application of Magic Tee as E-H tuner for Impedance matching.

9. Field Intensity Measurement of a Horn Antenna.

10. Field Intensity Measurement of a Parabolic Dish Antenna.

11. Prove Reciprocity Theorem of an Antenna.

12. Measure of Co-Polarization and Cross Polarization of an Antenna.

13. Plot Radiation Pattern of an Antenna Array.

14. Impedance measurement of an Antenna

Course Outcomes: On the completion of this laboratory course, the students will be able to:

1. Explain the Mode Characteristics of Reflex Klystron Oscillator.
2. Demonstrate the performance and extract S-Parameters of various Microwave Components.
3. Plot the Radiation Pattern and find the field Intensity, Polarization of a given Antenna/ Array and Prove Reciprocity Theorem as applied to Antennas.
4. Analyze and Measure Impedance of a given Microwave Component.
5. Explain and Find Three Point method of obtaining equivalent Circuit Parameters & Dielectric Strength.

Conduct of Practical Examination:

- All laboratory experiments are to be included for practical examination.
- Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.
- Change of experiment is allowed only once and Marks allotted to the procedure part to be made zero.

COMMUNICATION THEORY

Course Code	: 18EC751	CIE Marks	: 40
Lecture Hours/Week	: 03	SEE Marks	: 60
Total Number of Lecture Hours : 40 (08 Hrs / Module)		Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives: This course will enable students to:
- Describe essential elements of an electronic communications.
- Understand Amplitude, Frequency & Phase modulations, and Amplitude demodulation.
- Explain the basics of sampling and quantization.
- Understand the various digital modulation schemes.
- The concepts of wireless communication.

Module -1

Introduction to Electronic Communications: Historical perspective, Electromagnetic frequency spectrum, signal and its representation, Elements of electronic communications system, primary communication resources, signal transmission concepts, Analog and digital transmission, Modulation, Concept of frequency translation, Signal radiation and propagation
(Text 1: 1.1 to1.10)

L1, L2

Module -2

Noise: Classification and source of noise **(TEXT1:3.1)**
Amplitude Modulation Techniques: Types of analog modulation, Principle of amplitude modulation, AM power distribution, Limitations of AM,
(TEXT 1: 4.1,4.2, 4.4, 4.6)
Angle Modulation Techniques: Principles of Angle modulation, Theory of FM-basic Concepts, Theory of phase modulation **(TEXT1: 5.1,5.2, 5.5)**
Analog Transmission and Reception: AM Radio transmitters, AM Radio Receivers
(TEXT1:6.1,6.2)

L1, L2

Module -3

Sampling Theorem and pulse Modulation Techniques: Digital Versus analog Transmissions, Sampling Theorem, Classification of pulse modulation techniques, PAM, PWM, PPM, PCM, Quantization of signals
(TEXT 1: 7.1 to 7.8)

L1, L2

Module -4

Digital Modulation Techniques: Types of digital Modulation, ASK,FSK,PSK,QPSK
(TEXT 1: 9.1 to 9.5)
Source and Channel Coding: Objective of source coding, source coding technique, Shannon's source coding theorem, need of channel coding, Channel coding theorem, error control and coding
(TEXT 1: 11.1 to 11.3, 11.8, 11.9,11.12)

L1, L2

Module -5

Evolution of wireless communication systems: Brief History of wireless communications, Advantages of wireless communication, disadvantages of wireless communications, wireless network generations, Comparison of wireless systems, Evolution of next-generation networks, Applications of wireless communication
(TEXT 2: 1.1 to 1.7)
Principles of Cellular Communications: Cellular terminology, Cell structure and Cluster, Frequency reuse concept, Cluster size and system capacity, Method of locating cochannel cells, Frequecy reuse distance
(TEXT 2: 4.1 to 4.7)

L1, L2

Course Outcomes: At the end of the course, students will be able:
1.   Describe operation of communication systems.
2.   Understand the techniques of Amplitude and Angle modulation.
3.   Understand the concept of sampling and quantization.
4.   Understand the concepts of different digital modulation techniques.
5.   Describe the principles of wireless communications system.

Question paper pattern:
•   Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
•   Each full question can have a maximum of 4 sub questions.
•   There will be 2 full questions from each module covering all the topics of the module.
•   Students will have to answer 5 full questions, selecting one full question from each module.
•   The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

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Text Book:

1. Analog and Digital Communications by T L Singal, McGraw Hill Education (India) Private Limited.
2. Wireless Communications by T L Singal, McGraw Hill Education (India) Private Limited.

Reference Books:

1. Modern Digital and Analog Communication Systems B. P. Lathi, Oxford University Press., 4th ed, 2010,
2. Communication Systems: Analog and Digital, R.P.Singh and S.Sapre: TMH 2nd edition, 2007
3. Introduction to Wireless Telecommunications systems and Networks by Gray J Mullett, Cengage learning.

NEURAL NETWORKS

Course Code	: 18EC752	CIE Marks	: 40
Lecture Hours/Week	: 03	SEE Marks	: 60
Total Number of Lecture Hours : 40 (08 Hrs / Module)		Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives: This course will enable students to:
- Understand the basics of ANN and comparison with Human brain.
- Acquire knowledge on Generalization and function approximation of various ANN architectures.
- Understand reinforcement learning using neural networks
- Acquire knowledge of unsupervised learning using neural networks.

Module -1
Introduction: Biological Neuron – Artificial Neural Model -Types of activation functions – **Architecture**: Feedforward and Feedback, Convex Sets, Convex Hull and Linear Separability, Non-Linear Separable Problem. XOR Problem, Multilayer Networks.
Learning: Learning Algorithms, Error correction and Gradient Descent Rules, Learning objective of TLNs, Perceptron Learning Algorithm, Perceptron Convergence Theorem. **L1,L2**

Module -2
Supervised Learning: Perceptron learning and Non Separable sets, α-Least Mean Square Learning, MSE Error surface, Steepest Descent Search, μ-LMS approximate to gradient descent, Application of LMS to Noise Cancelling, Multi-layered Network Architecture, Backpropagation Learning Algorithm, Practical consideration of BP algorithm. **L1,L2,L3**

Module -3
Support Vector Machines and Radial Basis Function:
Learning from Examples, Statistical Learning Theory, Support Vector Machines, SVM application to Image Classification, Radial Basis Function Regularization theory, Generalized RBF Networks, Learning in RBFNs, RBF application to face recognition.

Module -4
Attractor Neural Networks: Associative Learning Attractor Associative Memory, Linear Associative memory, Hopfield Network, application of Hopfield

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Network, Brain State in a Box neural Network, Simulated Annealing, Boltzmann Machine, Bidirectional Associative Memory.

L1,L2,L3

Module -5
Self -organization Feature Map: Maximal Eigenvector Filtering, Extracting Principal Components, Generalized Learning Laws, Vector Quantization, Self -organization Feature Maps, Application of SOM, Growing Neural Gas.

L1,L2,L3

Course Outcomes: At the end of the course, students should be able to:
1. Describe the basics of ANN and comparison with Human brain.
2. Understand the role of neural networks in engineering, artificial intelligence, and cognitive modelling.
3. Understand the concepts and techniques of neural networks through the study of the most important neural network models.
4. Evaluate whether neural networks are appropriate to a particular application.
5. Apply neural networks to particular application, and to know what steps to take to improve performance.

Question paper pattern:
- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:
- **Neural Networks A Classroom Approach** –Satish Kumar, McGraw Hill Education (India) Pvt. Ltd, Second Edition.

Reference Books:
1. **Introduction to Artificial Neural Systems -** J.M. Zurada, Jaico Publications 1994.
2. **Artificial Neural Networks-** B. Yegnanarayana, PHI, New Delhi 1998.

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B. E. EC/TE			
Choice Based Credit System (CBCS) and Outcome Based Education (OBE) SEMESTER – VII			
ARM EMBEDDED SYSTEMS			
Course Code	**18EC753**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**03**	**SEE Marks**	**60**
Total Number of Lecture Hours	**40(8Hours/Module)**	**Exam Hours**	**03**
CREDITS – 03			
Course objective: This course will enable students to: • Understand the importance and applications of ARM Design • Know the architecture of ARM processor • Use instruction sets of ARM processor • Analyze the adaptation of C code, firmware, OS, Interrupts, caches, etc. in ARM embedded systems			
Module-1			**RBT Level**
ARM Embedded Systems Introduction, RISC design philosophy, ARM design philosophy, Embedded system hardware – AMBA bus protocol, ARM bus technology, Memory, Peripherals, Embedded system software – Initialization (BOOT) code, Operating System, Applications. **ARM Processor Fundamentals** ARM core dataflow model, registers, current program status register, Pipeline, Exceptions, Interrupts and Vector Table, Core extensions.			L1, L2
Module-2			
Introduction to the ARM Instruction set Introduction, Data processing instructions, Load - Store instruction, Software interrupt instructions, Program status register instructions, Loading constants, Conditional Execution. ALP programming.			L1, L2, L3
Module-3			
Introduction to the THUMB instruction set Introduction, THUMB register usage, ARM – THUMB interworking, Other branch instructions, Data processing instructions, Stack instructions, Software interrupt instructions. ALP programming			L1, L2, L3
Module-4			
Efficient C Programming: Overview of C Compilers and optimization, Basic C data types, Local Variable Types, Portability issues **Exception and Interrupt Handling:** Exception Handling-ARM Processor Exceptions and Modes, Vector Table, Exception Priorities, Link Register Offset, Interrupts- Interrupt Latency, Basic Interrupt Stack design and implementation, Interrupt Handling Schemes (**general description only** of the schemes)			L1, L2, L3, L4
Module-5			
Firmware: Firmware and Bootloader **Embedded Operating Systems:** Fundamental Components **Caches:** The memory Hierarchy and caches memory-caches and memory management units, Cache architecture basic architecture of caches memory, basic operation of cache controller, the relationship between cache and main memory.			L1, L2

Course Outcomes: After studying this course, students will be able to:
1. Depict the organization, architecture, bus technology, memory and operation of the ARM processors
2. Employ the knowledge of Instruction set of ARM processors to develop basic Assembly Language Programs
3. Recognize the importance of the Thumb mode of operation of ARM processors
4. Describe the techniques involved in writing C code for ARM processors and Exception & Interrupt handling in ARM Processors
5. Describe the importance and use of Firmware, OS and cache in ARM Embedded systems

Students have to conduct the following experiments as a part of CIE marks along with other Activities:

Conduct the following experiments by writing Assembly Language Program (ALP) using ARM Cortex M3 Registers using an evaluation simulator and the required software tool.
1. Write an ALP to find the sum of 10 integer numbers.
2. Write an ALP to multiply two 16-bit binary numbers.
3. Write an ALP to find factorial of a number.
4. Write an ALP to add an array of 16-bit numbers and store the 32-bit result in internal RAM
5. Write an ALP to find the square of a number (1 to 10) using look-up table.
6. Write an ALP to find the largest/smallest number in an array of 32 numbers.

Question paper pattern:
- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:
"ARM System Developers Guide", Andrew N Sloss, Dominic System and Chris Wright, Elsevier, Morgan Kaufmann publisher, 1st Edition, 2008, ISBN:1758608745.

References:
1. "ARM System on chip Architecture", Furber S, Addison Wiley, 2nd Edition, 2008, ISBN:9780201675191
2. "Embedded System", Rajkamal, Tata McGraw-Hill Publishers, 2nd Edition, 2008, ISBN: 0070494703.

B. E. EC/TE			
Choice Based Credit System (CBCS) and Outcome Based Education (OBE)			
SEMESTER – VII			
DIGITAL SYSTEMS DESIGN USING VHDL			
Course Code	18EC754	**CIE Marks**	40
Number of Lecture Hours/Week	03	**SEE Marks**	60
Total Number of Lecture Hours	40(8Hours/Module)	**Exam Hours**	03
CREDITS – 03			
Course objective: This course will enable students to: • Use the industry-standard hardware description language VHDL into the digital design process. • Design VHDL models ranging in complexity from a simple adder to more complex circuits. • Understand the synthesis and testing of the models.			
Module-1			**RBT Level**
Review of Logic Design Fundamentals: Combinational logic, Boolean Algebra and Algebraic Simplification, Karnaugh maps, Designing with NAND and NOR gates, Hazards in combinational Networks, Flipflop and Latches, Mealy Sequential Network Design, Design of Moore Sequential Network, Equivalent states and reduction of state Tables, Synchronous Design, Tristate Logic and Buses (Text 1, Chapter 1- 1.1 to 1.9, 1.12, 1.13)			L1, L2, L3
Module-2			
Introduction to VHDL: VHDL Description of Combinational Networks, Modeling Flip-flops using VHDL Processes, VHDL Models for a Multiplexer, Modeling a sequential Machine, Variables, signals, and constants, Arrays, VHDL operators, VHDL Functions, VHDL Procedures, Packages and Libraries. (Text 1, Chapter 2- 2.1, 2.2, 2.3, 2.5, 2.6, 2.7, 2.8, 2.9, 2.10, 2.11)			L1, L2, L3
Module-3			
Styles of Descriptions: VHDL Data types, VHDL Styles of Description (Text 2, Chapter 1- 1.5, 1.6) **Data flow Description**: Highlights of Data flow Description, Structure of Data flow Description, Data type-vectors, Common VHDL programming Errors (Text 2, Chapter 2- 2.1- to- 2.4)			L1, L2, L3
Module-4			
Designing with programmable Logic Devices: Read only memories, Programmable Logic Arrays, Programmable Array Logic, Other sequential programmable Logic Devices (PLDs), Generics, Generate statements. (Text 1, Chapter 3- 3.1, 3.2, 3.3, 3.4) **Design of Networks for Arithmetic Operations:** Design of serial Adder with Accumulator, Design of Binary Multiplier, Multiplication of signed Binary Numbers, Design of Binary Divider (Text 1, Chapter 4- 4.1, 4.3, 4.4, 4.5)			L1, L2, L3
Module-5			
Synthesis: Highlights of synthesis, synthesis information from entity and module, Mapping process in the hardware domain- Mapping of signal assignment, variable			L1, L2, L3

assignment, if statements, else-if statements, loop statement. (Text 2, Chapter5- 10.1, 10.2, 10.3)

Hardware Testing and Design for Testability: Testing Combinational Logic, Testing Sequential Logic. (Text 1, Chapter 10- 10.1, 10.2))

Course Outcomes: After studying this course, students will be able to:
1. Understand the basic concepts of Digital Design
2. Implement various Combinational and sequential circuits using VHDL descriptions. Write simple VHDL programs in different styles.
3. Design and verify the functionality of digital circuits (PLA, PAL, PLD) and Arithmetic Operations.
4. Identify the suitable Abstraction level for a particular digital design.
5. Write the programs more effectively using Verilog tasks and directives. Perform timing and delay Simulation.

Students have to conduct the following experiments as a part of CIE marks along with other Activities:
Conduct the following experiments using an suitable simulator and the required software tool.
1. Write a VHDL code to implement half and full adder using Data flow style.
2. Write a VHDL code to realize various logic gates.
3. Write a VHDL code to implement four-bit full adder using structural style.
4. Write a VHDL code to implement 2*2 unsigned combinational Array Multiplier.
5. Write a VHDL code to implement D Latch.
6. Implement JK flip flop modeling using VHDL process

Question paper pattern:
- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:
1. "Digital Systems Design using VHDL", Charles H. Roth, Jr., The University of Texas at Austin. 2006 reprint, Thomson Asia Pte Ltd, Singapore
2. "HDL Programming VHDL and Verilog", Nazeih M. Botros, 2009 reprint, Dreamtech press

Reference:
"VHDL for Programmable Logic", Kevin Skahill, Pearson education, 2006

B.E 2018 Eighth Semester Syllabus

B. E. ELECTRONICS AND TELECOMMUNICATION ENGINEERING

Choice Based Credit System (CBCS) and Outcome Based Education (OBE)

SEMESTER – VIII

ADVANCED CELLULAR COMMUNICATION

Course Code	: 18TE81	CIE Marks	: 40
Lecture Hours/Week	: 03	SEE Marks	: 60
Total Number of Lecture Hours : 40 (08 Hrs / Module)		Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives: This course will enable students to:
- Understand the basics of LTE standardization phases and specifications.
- Explain the system architecture of LTE and E-UTRAN, the layer of LTE, based on the use of OFDMA and SC-FDMA principles.
- Analyze the role of LTE radio interface protocols to set up, reconfigure and release the Radio Bearer, for transferring the EPS bearer.
- Analyze the main factors affecting LTE performance including mobile speed and transmission bandwidth.

Module-1
Key Enablers for LTE features: OFDM, Single carrier FDMA, Single carrier FDE, Channel Dependent Multiuser Resource Scheduling, Multi antenna Techniques, IP based Flat network Architecture, LTE Network Architecture. (Sec 1.4- 1.5 of Text).
Wireless Fundamentals: Cellular concept, Broadband wireless channel (BWC), Fading in BWC, Modeling BWC – Empirical and Statistical models, Mitigation of Narrow band and Broadband Fading (Sec 2.2 – 2.7 of Text).
L1, L2, L3

Module-2
Multicarrier Modulation: OFDM basics, OFDM in LTE, Timing and Frequency Synchronization, PAR, SC-FDE (Sec 3.2 – 3.6 of Text).
OFDMA and SC-FDMA: OFDM with FDMA, TDMA, CDMA, OFDMA, SC-FDMA, OFDMA and SC-FDMA in LTE (Sec 4.1 – 4.3, 4.5 of Text).
Multiple Antenna Transmission and Reception: Spatial Diversity overview, Receive Diversity, Transmit Diversity, Interference cancellation and signal

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enhancement, Spatial Multiplexing, Choice between Diversity, Interference suppression and Spatial Multiplexing (Sec 5.1 – 5.6 of Text).

L1,L2,L3

Module-3

Overview and Channel Structure of LTE: Introduction to LTE, Channel Structure of LTE, Downlink OFDMA Radio Resource, Uplink SC-FDMA Radio Resource (Sec 6.1 – 6.4 of Text).

Downlink Transport Channel Processing: Overview, Downlink shared channels, Downlink Control Channels, Broadcast channels, Multicast channels, Downlink physical channels, H-ARQ on Downlink (Sec 7.1 – 7.7 of Text).

L1,L2

Module-4

Uplink Channel Transport Processing: Overview, Uplink shared channels, Uplink Control Information, Uplink Reference signals, Random Access Channels, H-ARQ on uplink (Sec 8.1 – 8.6 of Text).

Physical Layer Procedures: Hybrid – ARQ procedures, Channel Quality Indicator CQI feedback, Precoder for closed loop MIMO Operations, Uplink channel sounding, Buffer status Reporting in uplink, Scheduling and Resource Allocation, Cell Search, Random Access Procedures, Power Control in uplink (Sec 9.1- 9.6, 9.8, 9.9, 9.10 of Text).

L1,L2,L3

Module-5

Radio Resource Management and Mobility Management:
PDCP overview, MAC/RLC overview, RRC overview, Mobility Management (Sec 10.1 – 10.4 of Text).

L1, L2

Course Outcomes: After studying this course, students will be able to:
1. Understand the system architecture and the functional standard specified in LTE4G
2. Analyze the role of LTE radio interface protocols and EPS Data convergence protocols to set up, reconfigure and release data and voice from users.
3. Demonstrate the UTRAN and EPS handling processes from set up to release including mobility management for a variety of data call scenarios.
4. Test and Evaluate the Performance of resource management and packet data processing and transport algorithms.
5. Analyze the main factors affecting LTE performance.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

Arunabha Ghosh, Jan Zhang, Jefferey Andrews, Riaz Mohammed, 'Fundamentals of LTE', Prentice Hall, Communications Engg. and Emerging Technologies.

Reference Books:

1. LTE for UMTS Evolution to LTE-Advanced' HarriHolma and AnttiToskala, Second Edition - 2011, John Wiley & Sons, Ltd. Print ISBN: 9780470660003.
2. 'Evolved Packet System (EPS) ; The LTE and SAE Evolution of 3G UMTS' by Pierre Lescuyer and Thierry Lucidarme, 2008, John Wiley & Sons, Ltd. Print ISBN:978-0-470-05976-0.
3. 'LTE – The UMTS Long Term Evolution ; From Theory to Practice' by Stefania Sesia, Issam Toufik, and Matthew Baker, 2009 John Wiley & Sons Ltd, ISBN 978-0-470-69716-0.

NETWORK SECURITY

Course Code	: 18EC821	CIE Marks	: 40
Lecture Hours/Week	: 3	SEE Marks	: 60
Total Number of Lecture Hours : 40 (08 Hrs / Module)		Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives: This course will enable students to:
- Describe network security services and mechanisms.
- Understand Transport Level Security and Secure Socket Layer
- Know about Security concerns in Internet Protocol security
- Discuss about Intruders, Intrusion detection and Malicious Software
- Discuss about Firewalls, Firewall characteristics, Biasing and Configuration

Module-1

Attacks on Computers and Computer Security: Need for Security, Security Approaches, Principles of Security Types of Attacks.
(Chapter1-Text2)   **L1, L2**

Module-2

Transport Level Security: Web Security Considerations, Secure Sockets Layer, Transport Layer Security, HTTPS, Secure Shell (SSH)
(Chapter15- Text1)   **L1,L2**

Module-3

IP Security: Overview of IP Security (IPSec),IP Security Architecture, Modes of Operation, Security Associations (SA), Authentication Header (AH), Encapsulating Security Payload (ESP), Internet Key Exchange.
(Chapter19-Text1)   **L1,L2**

Module-4

Intruders, Intrusion Detection.**(Chapter20-Text1)**
MALICIOUS SOFTWARE: Viruses and Related Threats, Virus Counter measures,
(Chapter21-Text1)   **L1,L2**

Module-5

Firewalls: The Need for firewalls, Firewall Characteristics, Types of Firewalls, Firewall Biasing, Firewall location and configuration
(Chapter22-Text 1)   **L1, L2**

Course Outcomes: After studying this course, students will be able to:
1. Explain network security services and mechanisms and explain security concepts
2. Understand the concept of Transport Level Security and Secure Socket Layer.
3. Explain Security concerns in Internet Protocol security
4. Explain Intruders, Intrusion detection and Malicious Software
5. Describe Firewalls, Firewall Characteristics, Biasing and Configuration

Question paper pattern:
- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

TEXT BOOKS:
1. Cryptography and Network Security Principles and Practice , Pearson Education Inc., William Stallings, 5th Edition, 2014, ISBN: 978-81-317- 6166-3.
2. Cryptography and Network Security, Atul Kahate, TMH, 2003.

REFERENCE BOOKS:
1. Cryptography and Network Security, Behrouz A. Forouzan, TMH, 2007.

MICRO ELECTRO MECHANICAL SYSTEMS

Course Code	: 18EC822	CIE Marks	: 40
Lecture Hours/Week	: 03	SEE Marks	: 60
Total Number of Lecture Hours	: 40 (8 Hrs /Module)	Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives: This course will enable students to:
- Understand overview of microsystems, their fabrication and application areas.
- Working principles of several MEMS devices.
- Develop mathematical and analytical models of MEMS devices.
- Know methods to fabricate MEMS devices.
- Various application areas where MEMS devices can be used.

Module-1

Overview of MEMS and Microsystems: MEMS and Microsystem, Typical MEMS and Microsystems Products, Evolution of Microfabrication, Microsystems and Microelectronics, Multidisciplinary Nature of Microsystems, Miniaturization. Applications and Markets.

L1, L2

Module-2

Working Principles of Microsystems: Introduction, Microsensors, Microactuation, MEMS with Microactuators, Microaccelerometers, Microfluidics.

Engineering Science for Microsystems Design and Fabrication: Introduction, Molecular Theory of Matter and Inter-molecular Forces, Plasma Physics, Electrochemistry.

L1,L2

Module-3

Engineering Mechanics for Microsystems Design: Introduction, Static Bending of Thin Plates, Mechanical Vibration, Thermo mechanics, Fracture Mechanics, Thin Film Mechanics, Overview on Finite Element Stress Analysis.

L1,L2

Module-4

Scaling Laws in Miniaturization: Introduction, Scaling in Geometry, Scaling in Rigid-Body Dynamics, Scaling in Electrostatic Forces, Scaling in Fluid Mechanics, Scaling in Heat Transfer.

L1,L2

Overview of Micromanufacturing: Introduction, Bulk Micromanufacturing, Surface Micromachining, The LIGA Process, Summary on Micro manufacturing.
L1, L2

Course Outcomes: After studying this course, students will be able to:
1. Appreciate the technologies related to Micro Electro Mechanical Systems.
2. Understand design and fabrication processes involved with MEMS Devices.
3. Analyze the MEMS devices and develop suitable mathematical models.
4. Know various application areas for MEMS device.
5. Describe the Micromanufacturing.

Question paper pattern:
- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:
- Tai-Ran Hsu, MEMS and Micro systems: Design, Manufacture and Nanoscale Engineering, 2nd Ed, Wiley.

Reference Books:
1. Hans H. Gatzen,Volker Saile, JurgLeuthold, Micro and Nano Fabrication: Tools and Processes, Springer, 2015.
2. Dilip Kumar Bhattacharya, Brajesh Kumar Kaushik, Microelectromechanical Systems (MEMS), Cengage Learning.

RADAR ENGINEERING

Course Code	: 18EC823	CIE Marks	: 40
Lecture Hours/Week	: 03	SEE Marks	: 60
Total Number of Lecture Hours : 40 (08 Hrs / Module)		Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives: This course will enable students to:
- Understand the Radar fundamentals and analyze the radar signals.
- Understand various technologies involved inthe designo fradar transmitters and receivers.
- Learn various radars like MTI, Doppler and tracking radars and their comparison

Module-1
Basics of Radar: Introduction, Maximum Unambiguous Range, Radar Waveforms, Definitions with respect to pulse wave form-PRF, PRI, Duty Cycle, Peak Transmitter Power, Average transmitter Power. Simple form of the Radar Equation, Radar Block Diagram and Operation, Radar Frequencies, Applications of Radar, The Origins of Radar, Illustrative Problems.
(Chapter 1 of Text)   **L1, L2,L3**

Module-2
The Radar Equation: Prediction of Range 'Performance, Detection of signal in Noise, Minimum Detectable Signal, Receiver Noise, SNR, Modified Radar Range Equation, Envelope Detector - False Alarm Time and Probability, Probability of Detection, Radar Cross Section of Targets: simple targets – sphere, cone-sphere, Transmitter Power, PRF and Range Ambiguities, System Losses (qualitative treatment), Illustrative Problems.
(Chapter 2 of Text, Except 2.4, 2.6, 2.8 & 2.11)   **L1,L2,L3**

Module-3
MTI and Pulse Doppler Radar: Introduction, Principle, Doppler Frequency Shift, Simple CW Radar, Sweep to Sweep subtraction and Delay Line Canceler, MTI Radar with– Power Amplifier Transmitter, Delay Line Cancelers— Frequency Response of Single Delay- Line Canceler, Blind Speeds, Clutter Attenuation, MTI Improvement Factor, N- Pulse Delay-Line Canceler, Digital MTI Processing–Blind phases, I and Q Channels, Digital MTI Doppler signal processor, Moving Target Detector- Original MTD.
(Chapter 3: 3.1, 3.2, 3.5, 3.6 of Text)   **L1,L2,L3**

Module-4
Tracking Radar: Tracking with Radar- Types of Tracking Radar Systems,

Monopulse Tracking- Amplitude Comparison Monopulse (one-and two-coordinates), Phase Comparison Monopulse.
Sequential Lobing, Conical Scan Tracking, Block Diagram of Conical Scan Tracking Radar, Tracking in Range, Comparison of Trackers.
(Chapter4: 4.1, 4.2, 4.3 of Text), **L1,L2,L3**

Module-5

The Radar Antenna : Functions of The Radar Antenna, Antenna Parameters, Reflector Antennas and Electronically Steered Phase darray Antennas. (Chapter 9:9.1,9.29.4, 9.5 of Text)
Radar Receiver: The Radar Receiver, Receiver Noise Figure, Super Heterodyne Receiver, Duplexers and Receivers Protectors, Radar Displays. **(Chapter 11 of Text)**, **L1, L2,L3**

Course Outcomes: At the end of the course, students will be able to:
1. Describe the radar fundamentals.
2. Analyze the radar signals.
3. Explain the working principle of pulse Doppler radars, their applications and limitations.
4. Describe the working of various radar transmitters and receivers.
5. Analyze the range parameters of pulse radar system which affect the system performance.

Question paper pattern:
- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

TEXT BOOK:
Introduction to Radar Systems- Merrill I Skolink, 3e, TMH, 2001

REFERENCE BOOKS:
1. Radar Principles, Technology, Applications—ByronEdde, Pearson Education, 2004.
2. Radar Principles–Peebles. Jr, P.Z. Wiley. New York, 1998.
3. Principles of Modem Radar: Basic Principles–Mark A. Rkhards, James A. Scheer, William A. HoIm. Yesdee, 2013

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NETWORK MANAGEMENT

Course Code	: 18TE824	CIE Marks	: 40
Lecture Hours/Week	: 03	SEE Marks	: 60
Total Number of Lecture Hours : 40 (08 Hrs / Module)		Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives: This course will enable students to:
• Understand the basic concept of network management
• Analyse the working of SNMP protocol and its functions
• Understand the concepts of telecommunication networks and its applications
• Understand the working of telecom regulatory bodies

Module -1

Introduction: Analogy of Telephone Network Management, Data and Tele-communication Network, Distributed computing Environments,
TCP/IP Based Networks: The Internet and Intranets, Communication Protocols and Standards, Networks, Systems and services, Case Histories of Networking and Management, Challenges of IT Managers,
Network Management: Goals, Organization, and Functions, Network Management Architecture and Organization.
Review of information Network and Technology: Network Topology, Local Area Networks, Network Node Components, Wide Area Networks, Transmission Technology. (refer Text 1)

L1, L2, L3

Module -2

SNMP and Network Management: Basic Foundations: Standards, Models and Language: Network Management standards, Network Management Models, Organization model, information model, Communication model, Abstract syntax Notation One ASN.1, Encoding structure, Macros, Functional Model. (refer Text 1)

L1, L2, L3

Module -3

SNMP Management – RMON: Remote Monitoring, RMON SMI and MIB, RMONI1, RMON2, ATM Remote Monitoring, A Case Study of Internet Traffic Using RMON. (refer Text 1)

L1, L2, L3

Module -4

Telecommunication Management Network (TMN): Why TMN?, operations systems, TMN conceptual model, TMN standards, TMN architecture, TMN Management service architecture, An integrated View of TMN, Implementation issues.

Network Management Applications: Configuration Management, Fault Management, Performance management, Event Correlation Techniques (refer Text 1)

L1, L2, L3

Module -5

Regulatory bodies: Telecom Regulations-Telecom Evolution, Role of regulatory bodies-The Indian Perspective, TRAI Regulation 2002, The telecommunication Interconnection usage charges regulation, Access to Information Regulations on QoS for VOIP based ILD service, Broadcasting and cable services. Interconnection, DTH services, Mobile number regulations. (refer Text 2 & Text 3)

L1, L2, L3

Course Outcomes: At the end of the course, students will be able to:
1. Define, understand and explain concepts related to network Management
2. Relate to the working of SNMP protocol and its functions.
3. Describe the role of regulatory bodies for telecommunication networks
4. Apply the knowledge of computer network and communication   to telecommunication management applications.
5. Analyze the different parameters for management protocol.

Question paper pattern:
- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. Network Management- Principles and Practice, Mani Subramanian, 2nd Edition, Pearson Education, 2010.

2. Telecommunication Regulations by John Buckley, IET.

3. The Telecom Regulatory Authority of India Act, 1997, Georg Thieme Verlag

Reference Books:

1. Network management Concepts and Practices: a Hands- On Approach, J.Richard Burke, PHI, 2008.

2. Advances in Network Management, Jianguo Ding, Auerbach Publication, 2009, ISBN-10: 1420064525, ISBN-13:978-1420064520.

3. Telecommunication: New Signposts to Old Roads, PaulSlaa

4. Telecom Management in Emerging Economies: Evolutionary and Contemporary Perspectives, Murali Krishna Medudula, Mahim Sagar, Ravi Parkash Gandhi.

SUSTAINABLE TELECOMMUNICATION NETWORKS

Course Code	: 18TE825	CIE Marks	: 40
Lecture Hours/Week	: 03	SEE Marks	: 60
Total Number of Lecture Hours	: 40 (8 Hrs /Module)	Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives: This course will enable students to:
• Understand the basic concept of Sustainability
• Analyze the principles of wireless networks
• Understand the concepts of radiation standards
• Understand the working of telecom regulatory bodies
• Identify the different models for telecommunication networks

Module -1
Sustainability: Need for transformation, understanding today's telecommunication industry, business and sustainability, sustainability factors, green products, drivers of sustainability.
L1,L2

Module -2
Energy Efficiency and Management in Wireless Networks: Peer-to-Peer content sharing techniques for Energy Efficiency in Wireless Networks , Foraging-Inspired Radio-Communication Energy Management for Green Multi-Radio Networks, Intelligent Future Wireless Networks for Energy Efficiency, The telecom commercial communication, Internet of Things and data analytics in the cloud-sustainability, communication networks in IOT applications, Digital services and sustainable solutions, bandwidth management, energy management.
L1, L2

Module -3
Regulatory bodies: Telecom Regulations- Telecom Evolution, Role of regulatory bodies-The Indian Perspective, TRAI Regulation 2002, The telecommunication Interconnection usage charges regulation , Access to Information Regulations on QoS for VOIP based ILD service, Broadcasting and cable services Interconnection, DTH services, Mobile number regulations.
L1, L2

Module -4
Radiation standards: Regulation of cellular service and RF radiation safety levels, SAR for cell phones, RFID standards, Wireless devices, ICNIRP, IEEE, CENELEC standards for controlled and occupational and military environments, Myths and Realities.
L1, L2

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Module -5

Revenue models through Telecommunication Networks: Constant Revenue Model for Telecommunication Networks, Business Model Requirements and Challenges in the Mobile Telecommunication Sector, A Novel Dynamic Pricing Model for the Telecommunications Industry.

L1,L2, L3

Course Outcomes: At the end of the course, students will be able to:
1. Analyze the principles of wireless networks
2. Understand and explain the need for sustainability, role of regulatory bodies, radiation hazards and revenue models for telecommunication network.
3. Apply the knowledge of radiation hazards to minimize the effect on human health and environment.
4. Apply the Knowledge of finance management to arrive at effective revenue models for telecommunication networks.
5. Engage in independent learning, submit a report and use ICT for effective presentation on the study on topics related to, Awareness on Mobile Tower Radiation & Its Impacts on Environment, human health and protection from radiation hazards.

Question paper pattern:
- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:
1. The Telecommunications Handbook, Kornel Terplan, Patricia A. Morreale, CRC Press.
2. The Telecom Regulatory Authority of India Act, 1997, Georg Thieme Verlag.
3. Telecommunication: New Signposts to Old Roads, Paul Slaa.
4. Telecom Management in Emerging Economies: Evolutionary and Contemporary Perspectives, Murali Krishna Medudula, Mahim Sagar, Ravi Parkash Gandhi.

Reference Books:
1. Green Networking and Communications: ICT for Sustainability, Shafiullah Khan, Jaime Lloret Mauri.
2. Internet of Things and Data Analytics Handbook, Hwaiyu Geng, John Wiley & Sons.