

**B. E. (Common to all branches)**  
**Choice Based Credit System (CBCS) and Outcome-Based Education (OBE)**  
**SEMESTER - III**

<b>TRANSFORM CALCULUS, FOURIER SERIES AND NUMERICAL TECHNIQUES</b>			
Course Code	<b>21MAT 31</b>	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	2:2:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03
<p><b>Course objectives:</b> The goal of the course Transform Calculus, Fourier series and Numerical techniques 21MAT 31 is</p> <ul style="list-style-type: none"> <li>➤ To have an insight into solving ordinary differential equations by using Laplace transform techniques</li> <li>➤ Learn to use the Fourier series to represent periodical physical phenomena in engineering analysis.</li> <li>➤ To enable the students to study Fourier Transforms and concepts of infinite Fourier Sine and Cosine transforms and to learn the method of solving difference equations by the z-transform method.</li> <li>➤ To develop proficiency in solving ordinary and partial differential equations arising in engineering applications, using numerical methods</li> </ul>			
<p><b>Teaching-Learning Process (General Instructions):</b>            These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.</p> <ol style="list-style-type: none"> <li>In addition to the traditional lecture method, different types of innovative teaching methods may be adopted so that the delivered lessons shall develop students' theoretical and applied mathematical skills.</li> <li>State the need for Mathematics with Engineering Studies and Provide real-life examples.</li> <li>Support and guide the students for self-study.</li> <li>You will also be responsible for assigning homework, grading assignments and quizzes, and documenting students' progress.</li> <li>Encourage the students for group learning to improve their creative and analytical skills.</li> <li>Show short related video lectures in the following ways:               <ul style="list-style-type: none"> <li>● As an introduction to new topics (pre-lecture activity).</li> <li>● As a revision of topics (post-lecture activity).</li> <li>● As additional examples (post-lecture activity).</li> <li>● As an additional material of challenging topics (pre-and post-lecture activity).</li> <li>● As a model solution for some exercises (post-lecture activity).</li> </ul> </li> </ol>			
<b>Module-1: Laplace Transform</b>			
<p>Definition and Laplace transforms of elementary functions (statements only). Problems on Laplace's Transform of <math>e^{at}f(t)</math>, <math>t^n f(t)</math>, <math>\frac{f(t)}{t}</math>. Laplace transforms of Periodic functions (statement only) and unit-step function – problems.</p> <p>Inverse Laplace transforms definition and problems, Convolution theorem to find the inverse Laplace transforms (without Proof) problems. Laplace transforms of derivatives, solution of differential equations.</p> <p style="text-align: right;"><b>(8 Hours)</b></p>			

<b>Self-study:</b> Solution of simultaneous first-order differential equations. (RBT Levels: L1, L2 and L3 )	
<b>Teaching-Learning Process</b>	Chalk and talk method / PowerPoint Presentation
<b>Module-2: Fourier Series</b>	
Introduction to infinite series, convergence and divergence. Periodic functions, Dirichlet's condition. Fourier series of periodic functions with period $2\pi$ and arbitrary period. Half range Fourier series. Practical harmonic analysis. (8 Hours)	
<b>Self-study:</b> Convergence of series by D'Alembert's Ratio test and, Cauchy's root test. (RBT Levels: L1, L2 and L3)	
<b>Teaching-Learning Process</b>	Chalk and talk method / PowerPoint Presentation
<b>Module-3: Infinite Fourier Transforms and Z-Transforms</b>	
Infinite Fourier transforms definition, Fourier sine and cosine transforms. Inverse Fourier transforms, Inverse Fourier cosine and sine transforms. Problems. Difference equations, z-transform-definition, Standard z-transforms, Damping and shifting rules, Problems. Inverse z-transform and applications to solve difference equations. (8 Hours)	
<b>Self Study:</b> Initial value and final value theorems, problems. (RBT Levels: L1, L2 and L3)	
<b>Teaching-Learning Process</b>	Chalk and talk method / PowerPoint Presentation
<b>Module-4: Numerical Solution of Partial Differential Equations</b>	
Classifications of second-order partial differential equations, finite difference approximations to derivatives, Solution of Laplace's equation using standard five-point formula. Solution of heat equation by Schmidt explicit formula and Crank- Nicholson method, Solution of the Wave equation. Problems. (8 Hours)	
<b>Self Study:</b> Solution of Poisson equations using standard five-point formula. (RBT Levels: L1, L2 and L3)	
<b>Teaching-Learning Process</b>	Chalk and talk method / PowerPoint Presentation
<b>Module-5: Numerical Solution of Second-Order ODEs and Calculus of Variations</b>	
Second-order differential equations - Runge-Kutta method and Milne's predictor and corrector method. (No derivations of formulae). Calculus of Variations: Functionals, Euler's equation, Problems on extremals of functional. Geodesics on a plane, Variational problems. (8 Hours)	
<b>Self Study:</b> Hanging chain problem (RBT Levels: L1, L2 and L3)	
<b>Course outcomes:</b> After successfully completing the course, the students will be able : <ul style="list-style-type: none"> <li>➤ To solve ordinary differential equations using Laplace transform.</li> <li>➤ Demonstrate the Fourier series to study the behaviour of periodic functions and their applications in system communications, digital signal processing and field theory.</li> <li>➤ To use Fourier transforms to analyze problems involving continuous-time signals and to apply Z-Transform techniques to solve difference equations</li> <li>➤ To solve mathematical models represented by initial or boundary value problems involving partial differential equations</li> <li>➤ Determine the extremals of functionals using calculus of variations and solve problems arising in dynamics of rigid bodies and vibrational analysis.</li> </ul>	

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% ( 18 Marks out of 50) in the semester-end examination(SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together

**Continuous Internal Evaluation:**

Three Unit Tests each of **20 Marks (duration 01 hour)**

First test at the end of 5<sup>th</sup> week of the semester

Second test at the end of the 10<sup>th</sup> week of the semester

Third test at the end of the 15<sup>th</sup> week of the semester

Two assignments each of **10 Marks**

First assignment at the end of 4<sup>th</sup> week of the semester

Second assignment at the end of 9<sup>th</sup> week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks (duration 01 hours)**

At the end of the 13<sup>th</sup> week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

**CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours**)

The question paper will have ten questions. Each question is set for 20 marks.

There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module

**Suggested Learning Resources:****Text Books:**

1. **B. S. Grewal:** "Higher Engineering Mathematics", Khanna publishers, 44<sup>th</sup> Ed. 2018
2. **E. Kreyszig:** "Advanced Engineering Mathematics", John Wiley & Sons, 10<sup>th</sup> Ed. (Reprint), 2016.

**Reference Books**

1. **V. Ramana:** "Higher Engineering Mathematics" McGraw-Hill Education, 11<sup>th</sup> Ed.
2. **Srimanta Pal & Subodh C. Bhunia:** "Engineering Mathematics" Oxford University Press, 3<sup>rd</sup> Reprint, 2016.
3. **N.P Bali and Manish Goyal:** "A textbook of Engineering Mathematics" Laxmi Publications, Latest edition.
4. **C. Ray Wylie, Louis C. Barrett:** "Advanced Engineering Mathematics" McGraw – Hill Book Co. New York, Latest ed.
5. **Gupta C.B, Sing S.R and Mukesh Kumar:** "Engineering Mathematic for Semester I and II", McGraw Hill Education(India) Pvt. Ltd 2015.
6. **H.K.Dass and Er. Rajnish Verma:** "Higher Engineering Mathematics" S.Chand Publication (2014).
7. **James Stewart:** "Calculus" Cengage publications, 7<sup>th</sup> edition, 4<sup>th</sup> Reprint 2019.

<b>Web links and Video Lectures (e-Resources):</b>
<ul style="list-style-type: none"><li>• <a href="http://.ac.in/courses.php?disciplineID=111">http://.ac.in/courses.php?disciplineID=111</a></li><li>• <a href="http://www.class-central.com/subject/math(MOOCs)">http://www.class-central.com/subject/math(MOOCs)</a></li><li>• <a href="http://academicearth.org/">http://academicearth.org/</a></li><li>• <a href="http://www.bookstreet.in">http://www.bookstreet.in</a>.</li><li>• VTU e-Shikshana Program</li><li>• VTU EDUSAT Program</li></ul>

**Activity-Based Learning (Suggested Activities in Class)/ Practical Based learning**

- Quizzes
- Assignments
- Seminars

**VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI**  
**B.E: Electronics & Communication Engineering / B.E: Electronics & Telecommunication Engineering**  
**NEP, Outcome Based Education (OBE) and Choice Based Credit System (CBCS)**  
**(Effective from the academic year 2021 – 22)**

### III Semester

Digital System Design Using Verilog			
Course Code	21EC32	CIE Marks	50
Teaching Hours/Week (L: T: P: S)	(3:0:2:0)	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory + 13 Lab slots	Total Marks	100
Credits	04	Exam Hours	03
<b>Course objectives: This course will enable students to:</b> <ol style="list-style-type: none"><li>To impart the concepts of simplifying Boolean expression using K-map techniques and Quine-McCluskey minimization techniques.</li><li>To impart the concepts of designing and analyzing combinational logic circuits.</li><li>To impart design methods and analysis of sequential logic circuits.</li><li>To impart the concepts of Verilog HDL-data flow and behavioral models for the design of digital systems.</li></ol>			
<b>Teaching-Learning Process (General Instructions)</b> <p>These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.</p> <ul style="list-style-type: none"><li>Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.</li><li>Show Video/animation films to explain the different concepts of Linear Algebra &amp; Signal Processing.</li><li>Encourage collaborative (Group) Learning in the class .</li><li>Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking.</li><li>Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.</li><li>Topics will be introduced in a multiple representation.</li><li>Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.</li><li>Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.</li><li>Adopt Flipped class technique by sharing the materials / Sample Videos prior to the class and have discussions on the that topic in the succeeding classes.</li><li>Give Programming Assignments.</li></ul>			
<b>Module-1</b>			
<b>Principles of Combinational Logic:</b> Definition of combinational logic, Canonical forms, Generation of switching equations from truth tables, Karnaugh maps- up to 4 variables, Quine-McCluskey Minimization Technique. Quine-McCluskey using Don't Care Terms. (Section 3.1 to 3.5 of Text 1).			
<b>Teaching-Learning Process</b>	Chalk and Talk, YouTube videos <b>RBT Level:</b> L1, L2, L3		
<b>Module-2</b>			
<b>Logic Design with MSI Components and Programmable Logic Devices:</b> Binary Adders and Subtractors, Comparators, Decoders, Encoders, Multiplexers, Programmable Logic Devices (PLDs) (Section 5.1 to 5.7 of Text 2)			
<b>Teaching-Learning Process</b>	Chalk and Talk, YouTube videos <b>RBT Level:</b> L1, L2, L3		

Module-3	
<b>Flip-Flops and its Applications:</b> The Master-Slave Flip-flops (Pulse-Triggered flip-flops): SR flip-flops, JK flip flops, Characteristic equations, Registers, Binary Ripple Counters, Synchronous Binary Counters, Counters based on Shift Registers, Design of Synchronous mod-n Counter using clocked T, JK, D and SR flip-flops. (Section 6.4, 6.6 to 6.9 (Excluding 6.9.3) of Text 2)	
<b>Teaching-Learning Process</b>	Chalk and Talk, YouTube videos <b>RBT Level:</b> L1, L2, L3
Module-4	
<b>Introduction to Verilog:</b> Structure of Verilog module, Operators, Data Types, Styles of Description. (Section 1.1 to 1.6.2, 1.6.4 (only Verilog), 2 of Text 3) <b>Verilog Data flow description:</b> Highlights of Data flow description, Structure of Data flow description. (Section 2.1 to 2.2 (only Verilog) of Text 3)	
<b>Teaching-Learning Process</b>	Chalk and Talk, YouTube videos, Programming assignments <b>RBT Level:</b> L1, L2, L3
Module-5	
<b>Verilog Behavioral description:</b> Structure, Variable Assignment Statement, Sequential Statements, Loop Statements, Verilog Behavioral Description of Multiplexers (2:1, 4:1, 8:1). (Section 3.1 to 3.4 (only Verilog) of Text 3) <b>Verilog Structural description:</b> Highlights of Structural description, Organization of structural description, Structural description of ripple carry adder. (Section 4.1 to 4.2 of Text 3)	
<b>Teaching-Learning Process</b>	Chalk and Talk, YouTube videos, Programming assignments <b>RBT Level:</b> L1, L2, L3
PRACTICAL COMPONENT OF IPCC	
Using suitable simulation software, demonstrate the operation of the following circuits:	
Sl.No	Experiments
1	To simplify the given Boolean expressions and realize using Verilog program.
2	To realize Adder/Subtractor (Full/half) circuits using Verilog data flow description.
3	To realize 4-bit ALU using Verilog program.
4	To realize the following Code converters using Verilog Behavioral description a) Gray to binary and vice versa b) Binary to excess3 and vice versa
5	To realize using Verilog Behavioral description: 8:1 mux, 8:3 encoder, Priority encoder
6	To realize using Verilog Behavioral description: 1:8 Demux, 3:8 decoder, 2-bit Comparator
7	To realize using Verilog Behavioral description: Flip-flops: a) JK type b) SR type c) T type and d) D type
8	To realize Counters - up/down (BCD and binary) using Verilog Behavioral description.
Demonstration Experiments (For CIE only – not to be included for SEE)	
Use FPGA/CPLD kits for downloading Verilog codes and check the output for interfacing experiments.	
9	Verilog Program to interface a Stepper motor to the FPGA/CPLD and rotate the motor in the specified direction (by N steps).
10	Verilog programs to interface a Relay or ADC to the FPGA/CPLD and demonstrate its working.
11	Verilog programs to interface DAC to the FPGA/CPLD for Waveform generation.
12	Verilog programs to interface Switches and LEDs to the FPGA/CPLD and demonstrate its working.

### Course Outcomes

At the end of the course the student will be able to:

1. Simplify Boolean functions using K-map and Quine-McCluskey minimization technique.
2. Analyze and design for combinational logic circuits.
3. Analyze the concepts of Flip Flops (SR, D, T and JK) and to design the synchronous sequential circuits using Flip Flops.
4. Model Combinational circuits (adders, subtractors, multiplexers) and sequential circuits using Verilog descriptions.

### Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together

#### CIE for the theory component of IPCC

Two Tests each of **20 Marks (duration 01 hour)**

- First test at the end of 5<sup>th</sup> week of the semester
- Second test at the end of the 10<sup>th</sup> week of the semester

Two assignments each of **10 Marks**

- First assignment at the end of 4<sup>th</sup> week of the semester
- Second assignment at the end of 9<sup>th</sup> week of the semester

Scaled-down marks of two tests and two assignments added will be CIE marks for the theory component of IPCC for **30 marks**.

#### CIE for the practical component of IPCC

- On completion of every experiment/program in the laboratory, the students shall be evaluated and marks shall be awarded on the same day. The **15 marks** are for conducting the experiment and preparation of the laboratory record, the other **05 marks shall be for the test** conducted at the end of the semester.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to 15 marks.
- The laboratory test (**duration 03 hours**) at the end of the 15<sup>th</sup> week of the semester /after completion of all the experiments (whichever is early) shall be conducted for 50 marks and scaled down to 05 marks.

Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **20 marks**.

#### SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (duration 03 hours)

- The question paper will have ten questions. Each question is set for 20 marks.
- There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
- The students have to answer 5 full questions, selecting one full question from each module.



**The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper shall include questions from the practical component.**

- The minimum marks to be secured in CIE to appear for SEE shall be the 12 (40% of maximum marks-30) in the theory component and 08 (40% of maximum marks -20) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included. The maximum of 04/05 questions to be set from the practical component of IPCC, the total marks of all questions should not be more than the 20 marks.

SEE will be conducted for 100 marks and students shall secure 35% of the maximum marks to qualify in the SEE. Marks secured will be scaled down to 50.

**Suggested Learning Resources:**

**Text Books**

1. Digital Logic Applications and Design by John M Yarbrough, Thomson Learning, 2001.
2. Digital Principles and Design by Donald D Givone, McGraw Hill, 2002.
3. HDL Programming VHDL and Verilog by Nazeih M Botros, 2009 reprint, Dreamtech press.

**Reference Books:**

1. Fundamentals of logic design, by Charles H Roth Jr., Cengage Learning
2. Logic Design, by Sudhakar Samuel, Pearson/ Sanguine, 2007
3. Fundamentals of HDL, by Cyril P R, Pearson/Sanguine 2010

**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

Programming Assignments / Mini Projects can be given to improve programming skills.

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**(Effective from the academic year 2021 – 22)**

### III Semester

Basic Signal Processing			
Course Code	21EC33	CIE Marks	50
Teaching Hours/Week (L: T: P: S)	(3:0:2:0)	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory + 13 Lab slots	Total Marks	100
Credits	04	Exam Hours	03
<p><b>Course objectives: This course will enable students to:</b></p> <p><b>Preparation:</b> To prepare students with fundamental knowledge/ overview in the field of Signal Processing with Familiarization with the concept of Vector spaces and orthogonality with a qualitative insight into applications in communications.</p> <p><b>Core Competence:</b> To equip students with a basic foundation of Signal Processing by delivering the basics of quantitative parameters for Matrices &amp; Linear Transformations, the mathematical description of discrete time signals and systems, analyzing the signals in time domain using convolution sum, classifying signals into different categories based on their properties, analyzing Linear Time Invariant (LTI) systems in time and transform domains</p>			
<p><b>Teaching-Learning Process (General Instructions)</b></p> <p>These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.</p> <ul style="list-style-type: none"> <li>Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.</li> <li>Show Video/animation films to explain the different concepts of Linear Algebra &amp; Signal Processing.</li> <li>Encourage collaborative (Group) Learning in the class.</li> <li>Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking.</li> <li>Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.</li> <li>Topics will be introduced in a multiple representation.</li> <li>Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.</li> <li>Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.</li> <li>Adopt Flipped class technique by sharing the materials / Sample Videos prior to the class and have discussions on the that topic in the succeeding classes.</li> <li>Give Programming Assignments.</li> </ul>			
Module-1			
<p><b>Vector Spaces:</b> Vector spaces and Null subspaces, Rank and Row reduced form, Independence, Basis and dimension, Dimensions of the four subspaces, Rank-Nullity Theorem, Linear Transformations</p> <p><b>Orthogonality:</b> Orthogonal Vectors and Subspaces, Projections and Least squares, Orthogonal Bases and Gram-Schmidt Orthogonalization procedure</p> <p><b>(Refer Chapters 2 and 3 of Text 1)</b></p>			
<b>Teaching-Learning Process</b>	<p>Chalk and Talk, YouTube videos, Flipped Class Technique, Programming assignments</p> <p><b>RBT Level:</b> L1, L2, L3</p>		

Module-2	
<b>Eigen values and Eigen vectors:</b> Review of Eigen values and Diagonalization of a Matrix, Special Matrices (Positive Definite, Symmetric) and their properties, Singular Value Decomposition. <b>(Refer Chapter 5, Text 1)</b>	
<b>Teaching-Learning Process</b>	Chalk and Talk, YouTube videos, Flipped Class Technique, Programming assignments <b>RBT Level:</b> L1, L2, L3
Module-3	
<b>Introduction and Classification of signals:</b> Definition of signal and systems with examples, Elementary signals/Functions: Exponential, sinusoidal, step, impulse and ramp functions <b>Basic Operations on signals:</b> Amplitude scaling, addition, multiplication, time scaling, time shift and time reversal. Expression of triangular, rectangular and other waveforms in terms of elementary signals <b>System Classification and properties:</b> Linear-nonlinear, Time variant -invariant, causal-noncausal, static-dynamic, stable-unstable, invertible. <b>(Text 2) [Only for Discrete Signals &amp; Systems]</b>	
<b>Teaching-Learning Process</b>	Chalk and Talk, YouTube videos, Flipped Class Technique, Programming assignments <b>RBT Level:</b> L1, L2, L3
Module-4	
<b>Time domain representation of LTI System:</b> Impulse response, convolution sum. Computation of convolution sum using graphical method for unit step and unit step, unit step and exponential, exponential and exponential, unit step and rectangular, and rectangular and rectangular. <b>LTI system Properties in terms of impulse response:</b> System interconnection, Memory less, Causal, Stable, Invertible and Deconvolution and step response <b>(Text 2) [Only for Discrete Signals &amp; Systems]</b>	
<b>Teaching-Learning Process</b>	Chalk and Talk, YouTube videos, Flipped Class Technique, Programming assignments <b>RBT Level:</b> L1, L2, L3
Module-5	
<b>The Z-Transforms:</b> Z transform, properties of the region of convergence, properties of the Z-transform, Inverse Z-transform by partial fraction, Causality and stability, Transform analysis of LTI systems. <b>(Text 2)</b>	
<b>Teaching-Learning Process</b>	Chalk and Talk, YouTube videos, Flipped Class Technique, Programming assignments <b>RBT Level:</b> L1, L2, L3

PRACTICAL COMPONENT OF IPCC	
Sl.No	Experiments
1	a. Program to create and modify a vector (array). b. Program to create and modify a matrix.
2	Programs on basic operations on matrix.
3	Program to solve system of linear equations.
4	Program for Gram-Schmidt orthogonalization.
5	Program to find Eigen value and Eigen vector.
6	Program to find Singular value decomposition.

7	Program to generate discrete waveforms.
8	Program to perform basic operation on signals.
9	Program to perform convolution of two given sequences.
10	a. Program to perform verification of commutative property of convolution. b. Program to perform verification of distributive property of convolution. c. Program to perform verification of associative property of convolution.
11	Program to compute step response from the given impulse response.
12	Programs to find Z-transform and inverse Z-transform of a sequence.

### Course outcomes (Course Skill Set)

At the end of the course the student will be able to :

1. Understand the basics of Linear Algebra
2. Analyse different types of signals and systems
3. Analyse the properties of discrete time signals & systems
4. Analyse discrete time signals & systems using Z transforms

### Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together

### CIE for the theory component of IPCC

Two Tests each of **20 Marks (duration 01 hour)**

- First test at the end of 5<sup>th</sup> week of the semester
- Second test at the end of the 10<sup>th</sup> week of the semester

Two assignments each of **10 Marks**

- First assignment at the end of 4<sup>th</sup> week of the semester
- Programming assignment at the end of 9<sup>th</sup> week of the semester, which can be implemented using programming languages like C++/Python/Java/Scilab

Scaled-down marks of two tests and two assignments added will be CIE marks for the theory component of IPCC for **30 marks**.

### CIE for the practical component of IPCC

- On completion of every experiment/program in the laboratory, the students shall be evaluated and marks shall be awarded on the same day. The **15 marks** are for conducting the experiment and preparation of the laboratory record, the other **05 marks shall be for the test** conducted at the end of the semester.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to 15 marks.
- The laboratory test (**duration 03 hours**) at the end of the 15<sup>th</sup> week of the semester /after completion of all the experiments (whichever is early) shall be conducted for 50 marks and scaled down to 05 marks.

Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **20 marks**.

**SEE for IPCC**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (duration 03 hours)

- The question paper will have ten questions. Each question is set for 20 marks.
- There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
- The students have to answer 5 full questions, selecting one full question from each module.

**The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper shall include questions from the practical component.**

- The minimum marks to be secured in CIE to appear for SEE shall be the 12 (40% of maximum marks-30) in the theory component and 08 (40% of maximum marks -20) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included. The maximum of 04/05 questions to be set from the practical component of IPCC, the total marks of all questions should not be more than the 20 marks.

SEE will be conducted for 100 marks and students shall secure 35% of the maximum marks to qualify in the SEE. Marks secured will be scaled down to 50.

**Suggested Learning Resources:****Text Books**

1. Gilbert Strang, "Linear Algebra and its Applications", Cengage Learning, 4<sup>th</sup> Edition, 2006, ISBN 97809802327
2. Simon Haykin and Barry Van Veen, "Signals and Systems", 2<sup>nd</sup> Edition, 2008, Wiley India. ISBN9971-51-239-4.

**Reference Books:**

1. **Michael Roberts**, "Fundamentals of Signals & Systems", 2<sup>nd</sup> edition, Tata McGraw-Hill, 2010, ISBN978-0-07-070221-9.
2. **Alan V Oppenheim, Alan S Willsky and S Hamid Nawab**, "Signals and Systems" Pearson Education Asia / PHI, 2<sup>nd</sup> edition, 1997. Indian Reprint 2002.
3. **H P Hsu, R Ranjan**, "Signals and Systems", Schaum's outlines, TMH, 2006.
4. **B P Lathi**, "Linear Systems and Signals", Oxford University Press, 2005.
5. **Ganesh Rao and Satish Tunga**, "Signals and Systems", Pearson/Sanguine.
6. **Seymour Lipschutz, Marc Lipson**, "Schaums Easy Outline of Linear Algebra", 2020.

**Web links and Video Lectures (e-Resources):**

Video lectures on Signals and Systems by Alan V Oppenheim

[Lecture 1, Introduction | MIT RES.6.007 Signals and Systems, Spring 2011 - YouTube](#)

[Lecture 2, Signals and Systems: Part 1 | MIT RES.6.007 Signals and Systems, Spring 2011 - YouTube](#)

NPTEL video lectures signals and system:

[https://www.youtube.com/watch?v=7Z3LE5uM-6Y&list=PLbMVogVj5nJQQZbah2uRZIRZ\\_9kfoqZyx](https://www.youtube.com/watch?v=7Z3LE5uM-6Y&list=PLbMVogVj5nJQQZbah2uRZIRZ_9kfoqZyx)

Video lectures on Linear Algebra by Gilbert Strang

<https://www.youtube.com/watch?v=ZK3O402wf1c&list=PL49CF3715CB9EF31D&index=1>

**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

Programming Assignments / Mini Projects can be given to improve programming skills

**VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI**  
**B.E: Electronics & Communication Engineering / B.E: Electronics & Telecommunication Engineering**  
**NEP, Outcome Based Education (OBE) and Choice Based Credit System (CBCS)**  
**(Effective from the academic year 2021 – 22)**

**III Semester**

Analog Electronic Circuits			
Course Code	21EC34	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:1	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3
<b>Course objectives:</b> This course will enable students to <ul style="list-style-type: none"><li>• Explain various BJT parameters, connections and configurations.</li><li>• Design and demonstrate the diode circuits and transistor amplifiers.</li><li>• Explain various types of FET biasing and demonstrate the use of FET amplifiers.</li><li>• Analyze Power amplifier circuits in different modes of operation.</li><li>• Construct Feedback and Oscillator circuits using FET.</li></ul>			
<b>Teaching-Learning Process (General Instructions)</b> These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes. <ol style="list-style-type: none"><li>1.Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.</li><li>2.Show Video/animation films to explain evolution of communication technologies.</li><li>3. Encourage collaborative (Group) Learning in the class</li><li>4.Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking</li><li>5.Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.</li><li>6.Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.</li><li>7.Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.</li></ol>			
Module-1			
<b>BJT Biasing:</b> Biasing in BJT amplifier circuits: The Classical Discrete circuit bias (Voltage-divider bias), Biasing using a collector to base feedback resistor. <b>Small signal operation and Models:</b> Collector current and transconductance, Base current and input resistance, Emitter current and input resistance, voltage gain, Separating the signal and the DC quantities, The hybrid $\Pi$ model, The T model. <b>MOSFETs:</b> Biasing in MOS amplifier circuits: Fixing $V_{GS}$ , Fixing $V_G$ , Drain to Gate feedback resistor. Small signal operation and modeling: The DC bias point, signal current in drain, voltage gain, small signal equivalent circuit models, transconductance, The T equivalent circuit model. [Text 1: 3.5(3.5.1, 3.5.3), 3.6(3.6.1 to 3.6.7), 4.5(4.5.1, 4.5.2, 4.5.3), 4.6(4.6.1 to 4.6.7) ]			
Teaching-Learning Process	Chalk and talk method, Power Point Presentation. <b>Self-study topics:</b> Basic BJT Amplifier Configurations- Design of Common Emitter and Common collector amplifier circuits. <b>RBT Level:</b> L1, L2, L3		
Module-2			
<b>MOSFET Amplifier configuration:</b> Basic configurations, characterizing amplifiers, CS amplifier with and without source resistance $R_S$ , Source follower. <b>MOSFET internal capacitances and High frequency model:</b> The gate capacitive effect, Junction capacitances, High frequency model. <b>Frequency response of the CS amplifier:</b> The three frequency bands, high frequency response, Low			

frequency response. <b>Oscillators:</b> FET based Phase shift oscillator, LC and Crystal Oscillators (no derivation) [Text 1: 4.7(4.7.1 to 4.7.4, 4.7.6) 4.8(4.8.1, 4.8.2, 4.8.3), 4.9, 12.2.2, 12.3.1, 12,3,2]	
<b>Teaching-Learning Process</b>	Chalk and talk method, Power Point Presentation. <b>Self-study topics:</b> Discrete Circuit MOS Amplifier – The common source amplifier and the source follower. <b>RBT Level:</b> L1, L2, L3
<b>Module-3</b>	
<b>Feedback Amplifier:</b> General feedback structure, Properties of negative feedback, The Four Basic Feedback Topologies, The series-shunt, series-series, shunt-shunt and shunt-series amplifiers (Qualitative Analysis). <b>Output Stages and Power Amplifiers:</b> Introduction, Classification of output stages, Class A output stage, Class B output stage: Transfer Characteristics, Power Dissipation, Power Conversion efficiency, Class AB output stage, Class C tuned Amplifier. [Text 1: 7.1, 7.2, 7.3, 7.4.1, 7.5.1, 7.6 (7.6.1 to 7.6.3), 13.1, 13.2, 13.3(13.3.1, 13.3.2, 13.3.3, 13.4, 13.7)]	
<b>Teaching-Learning Process</b>	Chalk and talk method, Power Point Presentation. <b>Self-study topics:</b> Class D power amplifier. <b>RBT Level:</b> L1, L2, L3
<b>Module-4</b>	
<b>Op-Amp Circuits:</b> Op-amp DC and AC Amplifiers, DAC - Weighted resistor and R-2R ladder, ADC- Successive approximation type, Small Signal half wave rectifier, Absolute value output circuit, Active Filters, First and second order low-pass and high-pass Butterworth filters, Band-pass filters, Band reject filters. <b>555 Timer and its applications:</b> Monostable and Astable Multivibrators. [Text 2: 6.2, 8.11(8.11.1a, 8.11.1b), 8.11.2a, 8.12.2,8.13 7.2, 7.3, 7.4, 7.5, 7.6, 7.8, 7.9, 9.4.1, 9.4.1(a), 9.4.3, 9.4.3(a)]	
<b>Teaching-Learning Process</b>	Chalk and talk method, Power Point Presentation. <b>Self-study topics:</b> Clippers and Clampers, Peak detector, Sample and hold circuit. <b>RBT Level:</b> L1, L2, L3
<b>Module-5</b>	
<b>Overview of Power Electronic Systems:</b> Power Electronic Systems, Power Electronic Converters and Applications. <b>Thyristors:</b> Static Anode-Cathode characteristics and Gate characteristics of SCR, Turn-ON methods, Turn-off Mechanism, Turn-OFF Methods: Natural and Forced Commutation – Class A without design consideration. <b>Gate Trigger Circuit:</b> Resistance Firing Circuit, Resistance capacitance firing circuit, Unijunction Transistor: Basic operation and UJT Firing Circuit. [Text 3: 1.3, 1.5,1.6, 2.2, 2.3, 2.4,2.6, 2.7,2.9, 2.10, 3.2, 3.5.1, 3.5.2, 3.6.1, 3.6.3,3.6.4]	
<b>Teaching-Learning Process</b>	Chalk and talk method, Power Point Presentation. <b>Self-study topics:</b> Basic Construction, working and applications of DIAC, TRIAC, IGBT, GTO. <b>RBT Level:</b> L1, L2, L3
<b>Course Outcomes (Course Skill Set)</b> At the end of the course the student will be able to : <ol style="list-style-type: none"> <li>1. Understand the characteristics of BJTs and FETs for switching and amplifier circuits.</li> <li>2. Design and analyze FET amplifiers and oscillators with different circuit configurations and biasing conditions.</li> <li>3. Understand the feedback topologies and approximations in the design of amplifiers and oscillators.</li> <li>4. Design of circuits using linear ICs for wide range applications such as ADC, DAC, filters and timers.</li> <li>5. Understand the power electronic device components and its functions for basic power electronic circuits.</li> </ol>	

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous Internal Evaluation:**

Three Unit Tests each of **20 Marks (duration 01 hour)**

1. First test at the end of 5<sup>th</sup> week of the semester
2. Second test at the end of the 10<sup>th</sup> week of the semester
3. Third test at the end of the 15<sup>th</sup> week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4<sup>th</sup> week of the semester
5. Second assignment at the end of 9<sup>th</sup> week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks (duration 01 hours)**

6. At the end of the 13<sup>th</sup> week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

**CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours**)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module.

**Suggested Learning Resources:****Books**

1. Microelectronic Circuits, Theory and Applications, Adel S Sedra, Kenneth C Smith, 6<sup>th</sup> Edition, Oxford, 2015. ISBN:978-0-19-808913-1
2. Op-Amps and Linear Integrated Circuits, Ramakant A Gayakwad, 4<sup>th</sup> Edition, Pearson Education, 2018. ISBN: 978-93-325-4991-3
3. Electronic Principles, Albert Malvino, David J Bates, 7<sup>th</sup> Edition, McGraw Hill Education (India) Private Limited, 2017, ISBN:978-0-07-063424-4

**Web links and Video Lectures (e-Resources):**

- Integrated Electronics: Analog and Digital Circuits and Systems, Jacob Millman, Christos C. Halkias, McGraw-Hill, 2015.
- Electronic Devices and Circuit, Boylestad & Nashelsky, Eleventh Edition, Pearson, January 2015.



### III Semester

Analog and Digital Electronics Lab			
Course Code	21ECL35	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:0:2:0	SEE Marks	50
Credits	1	Exam Hours	3
<b>Course objectives:</b> This laboratory course enables students to <ul style="list-style-type: none"> <li>• Understand the electronic circuit schematic and its working</li> <li>• Realize and test amplifier and oscillator circuits for the given specifications</li> <li>• Realize the opamp circuits for the applications such as DAC, implement mathematical functions and precision rectifiers.</li> <li>• Study the static characteristics of SCR and test the RC triggering circuit.</li> <li>• Design and test the combinational and sequential logic circuits for their functionalities.</li> <li>• Use the suitable ICs based on the specifications and functions.</li> </ul>			
Sl.No.	Experiments		
1	Design and set up the BJT common emitter voltage amplifier with and without feedback and determine the gain- bandwidth product, input and output impedances.		
2	Design and set-up BJT/FET i) Colpitts Oscillator, ii) Crystal Oscillator and iii) RC Phase shift oscillator		
3	Design and set up the circuits using opamp: i) Adder, ii) Integrator, iii) Differentiator and iv) Comparator		
4	Obtain the static characteristics of SCR and test SCR Controlled HWR and FWR using RC triggering circuit.		
5	Design and implement (a) Half Adder & Full Adder using basic gates and NAND gates, (b) Half subtractor & Full subtractor using NAND gates, (c) 4-variable function using IC74151(8:1MUX).		
6	Realize (i) Binary to Gray code conversion & vice-versa (IC74139), (ii) BCD to Excess-3 code conversion and vice versa		
7	a) Realize using NAND Gates: i) Master-Slave JK Flip-Flop, ii) D Flip-Flop and iii) T Flip-Flop b) Realize the shift registers using IC7474/7495: (i) SISO (ii) SIPO (iii) PISO (iv) PIPO (v) Ring counter and (vi) Johnson counter.		
8	Realize a) Design Mod – N Synchronous Up Counter & Down Counter using 7476 JK Flip-flop b) Mod-N Counter using IC7490 / 7476 c) Synchronous counter using IC74192		

9	Design 4-bit R – 2R Op-Amp Digital to Analog Converter (i) for a 4-bit binary input using toggle switches (ii) by generating digital inputs using mod-16
10	Pseudorandom sequence generator using IC7495
11	Test the precision rectifiers using opamp: i) Half wave rectifier ii) Full wave rectifier
12	Design and test Monostable and Astable Multivibrator using 555 Timer
<b>Course outcomes (Course Skill Set):</b> At the end of the course the student will be able to: <ol style="list-style-type: none"> <li>Design and analyze the BJT/FET amplifier and oscillator circuits.</li> <li>Design and test Opamp circuits to realize the mathematical computations, DAC and precision rectifiers.</li> <li>Design and test the combinational logic circuits for the given specifications.</li> <li>Test the sequential logic circuits for the given functionality.</li> <li>Demonstrate the basic electronic circuit experiments using SCR and 555 timer.</li> </ol>	
<b>Assessment Details (both CIE and SEE)</b> <p>The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).</p> <p><b>Continuous Internal Evaluation (CIE):</b>  CIE marks for the practical course is <b>50 Marks</b>.  The split-up of CIE marks for record/ journal and test are in the ratio <b>60:40</b>.</p> <ul style="list-style-type: none"> <li>Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.</li> <li>Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.</li> <li>Total marks scored by the students are scaled down to 30 marks (60% of maximum marks).</li> <li>Weightage to be given for neatness and submission of record/write-up on time.</li> <li>Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8<sup>th</sup> week of the semester and the second test shall be conducted after the 14<sup>th</sup> week of the semester.</li> <li>In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.</li> <li>The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book</li> <li>The average of 02 tests is scaled down to <b>20 marks</b> (40% of the maximum marks).</li> </ul> <p>The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.</p>	
<b>Semester End Evaluation (SEE):</b> SEE marks for the practical course is 50 Marks. SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University All laboratory experiments are to be included for practical examination.	

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours

Rubrics suggested in Annexure-II of Regulation book

**Suggested Learning Resources:**

1. Fundamentals of Electronic Devices and Circuits Lab Manual, David A Bell, 5<sup>th</sup> Edition, 2009, Oxford University Press.
2. Op-Amps and Linear Integrated Circuits, Ramakant A Gayakwad, 4<sup>th</sup> Edition, Pearson Education, 2018. ISBN: 978-93-325-4991-3.
3. Fundamentals of Logic Design, Charles H Roth Jr., Larry L Kinney, Cengage Learning, 7<sup>th</sup> Edition.

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**III Semester**

LD (Logic Design) Lab using Pspice / MultiSIM			
Course Code	21EC381	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	0:0:2:0	SEE Marks	50
Credits	1	Exam Hours	100
<b>Course objectives:</b> <ul style="list-style-type: none"><li>• Impart the concepts of De Morgan’s Theorem, SOP, POS forms.</li><li>• Impart the concepts of designing and analyzing combinational logic circuits.</li><li>• Impart the concepts of analysis of sequential logic circuits.</li><li>• Analyze and design any given synchronous sequential circuits.</li></ul>			
<b>Sl.No</b>	<b>Experiments</b>		
1	Implementation of De Morgan’s theorem and SOP/POS expressions using Pspice/Multisim.		
2	Implementation of Half Adder, Full Adder, Half Subtractor and Full Subtractor using Pspice/ Multisim.		
3	Design and implementation of 4-bit Parallel Adder/ Subtractor using IC 7483 and BCD to Excess-3 code conversion and vice-versa using Pspice/Multisim.		
4	Design and implement of IC 7485 5-bit magnitude comparator using Pspice/Multisim.		
5	To Realize Adder & Subtractor using IC 74153 (4:1 MUX) and 4-variable function using IC74151 (8:1MUX) using Pspice/Multisim.		
6	To realize Adder and Subtractor using IC 74139/ 74155N (Demux/Decoder) and Binary to Gray code conversion & vice versa using 74139/ 74155N using Pspice/Multisim.		
7	SR, Master-Slave JK, D & T flip-flops using NAND Gates using Pspice/Multisim.		
8	Design and realize the Synchronous counters (up/down decade/binary) using Pspice/Multisim.		
9	Realize the shift registers and their modes (SISO, PISO, PIPO, SIPO) using 7474/7495 using Pspice/Multisim.		
10	Design Pseudo Random Sequence generator using 7495 using Pspice/Multisim.		
11	Design Serial Adder with Accumulator and simulate using Pspice/Multisim.		
12	Design using Pspice/Multisim Mod-N Counters.		
<b>Course outcomes (Course Skill Set):</b> <p>At the end of the course the student will be able to:</p> <ol style="list-style-type: none"><li>1. Demonstrate the truth table of various expressions and combinational circuits using logic gates.</li><li>2. Design various combinational circuits such as adders, subtractors, comparators, multiplexers and code converters.</li><li>3. Construct flips-flops, counters and shift registers.</li><li>4. Design and implement synchronous counters.</li></ol>			
<b>Assessment Details (both CIE and SEE)</b> <p>The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student</p>			

shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

**Continuous Internal Evaluation (CIE):**

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled down to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8<sup>th</sup> week of the semester and the second test shall be conducted after the 14<sup>th</sup> week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

**Semester End Evaluation (SEE):**

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours

Rubrics suggested in Annexure-II of Regulation book

**Suggested Learning Resources:**

- Digital Logic Applications and Design by John M Yarbrough, Thomson Learning, 2001
- Digital Principles and Design by Donald D Givone, McGraw Hill, 2002.

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**III Semester**

AEC (Analog Electronic Circuits) Lab			
Course Code	21EC382	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	0:0:2:0	SEE Marks	50
Credits	1	Exam Hours	2
<b>Course objectives:</b> <ul style="list-style-type: none"><li>To provide practical exposure to the students on designing, setting up, executing and debugging various electronic circuits using simulation software.</li><li>To give the knowledge and practical exposure on simple applications of analog electronic circuits.</li></ul>			
<b>Sl.No</b>	<b>Experiments using Pspice/MultiSIM software</b>		
1	Experiments to realize diode clipping (single, double ended) circuits.		
2	Experiments to realize diode clamping (positive, negative) circuits.		
3	Experiments to realize Full wave rectifier without filter (and set-up to measure the ripple factor, $V_p$ -p, $V_{rms}$ , etc.).		
4	Design and conduct an experiment on Series Voltage Regulator using Zener diode to determine line/load regulation characteristics.		
5	Realize BJT Darlington Emitter follower without bootstrapping and determine the gain, input and output impedances (other configurations of emitter follower can also be considered).		
6	Set-up and study the working of complementary symmetry class B push pull power amplifier (other power amplifiers can also be suitably considered) and calculate the efficiency.		
7	Design and set-up the oscillator circuits (Hartley, Colpitts, etc. using BJT/FET) and determine the frequency of oscillation.		
8	Design and set-up the crystal oscillator and determine the frequency of oscillation.		
9	Experiment to realize Input and Output characteristics of BJT Common emitter configuration and evaluation of parameters.		
10	Experiments to realize Transfer and drain characteristics of a MOSFET.		
11	Experiments to realize UJT triggering circuit for Controlled Full wave Rectifier.		
12	Design and simulation of Regulated power supply.		
<b>Course outcomes (Course Skill Set):</b> <p>At the end of the course the student will be able to:</p> <ol style="list-style-type: none"><li>Understand the circuit schematic and its working.</li><li>Study the characteristics of different electronic devices.</li><li>Design and test simple electronic circuits as per the specifications using discrete electronic components.</li><li>Compute the parameters from the characteristics of active devices.</li><li>Familiarize with EDA software which can be used for electronic circuit simulation.</li></ol>			

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

**Continuous Internal Evaluation (CIE):**

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled down to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8<sup>th</sup> week of the semester and the second test shall be conducted after the 14<sup>th</sup> week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

**Semester End Evaluation (SEE):**

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University.

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners).

Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours.

Rubrics suggested in Annexure-II of Regulation book.

**Suggested Learning Resources:**

1. David A Bell, "Fundamentals of Electronic Devices and Circuits Lab Manual, 5th Edition, 2009, Oxford University Press.
2. Muhammed H Rashid, "Introduction to PSpice using OrCAD for circuits and electronics", 3<sup>rd</sup> Edition, Prentice Hall, 2003.

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**III Semester**

LIC (Linear Integrated Circuits) Lab using Pspice / MultiSIM			
Course Code	21EC383	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:0:2:0	SEE Marks	50
Credits	1	Exam Hours	100
<b>Course objectives:</b> <ul style="list-style-type: none"><li>To apply operational amplifiers in linear and nonlinear applications.</li><li>To acquire the basic knowledge of special function ICs.</li><li>To use Multisim/Pspice software for circuit design and simulation</li></ul>			
<b>Sl.No</b>	<b>Experiments using Pspice / MultiSIM</b> Every experiment has to be designed, circuit to be drawn / constructed and executed in the specified software. Results are also to be noted and inferred.		
	Note: Standard design procedure to be adopted.		
1	To realize using op-amp an Inverting Amplifier and Non-Inverting Amplifier		
2	To realize using op-amps i) Summing Amplifier ii)Difference amplifier		
3	To realize using op-amps an Instrumentation Amplifier		
4	To realize using op-amps i) Differentiator ii)Integrator		
5	To realize using op-amps a Full wave Precision Rectifier		
6	To realize using op-amps <ul style="list-style-type: none"><li>Inverting and Non-Inverting Zero Crossing Detectors</li><li>Positive and Negative Voltage level detectors</li></ul>		
7	To realize using op-amp an Inverting Schmitt Trigger		
8	To realize using op-amp an Astable Multivibrator		
9	To design and implement using op-amps <ul style="list-style-type: none"><li>Butterworth I &amp; II order Low Pass Filter</li><li>Butterworth I &amp; II order High Pass Filter</li></ul>		
10	To design and implement using op-amp a RC Phase Shift Oscillator		
11	To design and implement Mono-stable Multivibrator using 555 timer		
12	To design and implement 4 - bit R-2R Digital to Analog Converter		
<b>Course outcomes (Course Skill Set):</b> After studying this course, students will be able to; <ul style="list-style-type: none"><li>Sketch/draw circuit schematics, construct circuits, analyze and troubleshoot circuits containing op-amps, resistors, diodes, capacitors and independent sources.</li><li>Relate to the manufacturer's data sheets of IC 555 timer and IC <math>\mu</math>a741 op-amp.</li><li>Realize and verify the operation of analog integrated circuits like Amplifiers, Precision Rectifiers, Comparators and Waveform generators.</li><li>Design and implement analog integrated circuits like Oscillators, Active filters, Timer circuits, Data converters and compare the experimental results with theoretical values.</li></ul>			



**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

**Continuous Internal Evaluation (CIE):**

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled down to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8<sup>th</sup> week of the semester and the second test shall be conducted after the 14<sup>th</sup> week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

**Semester End Evaluation (SEE):**

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours

Rubrics suggested in Annexure-II of Regulation book

**Suggested Learning Resources:**

Op-Amps and Linear Integrated Circuits, Ramakant A Gayakwad, 4<sup>th</sup> Edition, Pearson Education, 2018.

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**III Semester**

LabVIEW Programming Basics			
Course Code	21EC384	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	0:0:2:0	SEE Marks	50
Credits	1	Exam Hours	100
<b>Course objectives:</b> <ul style="list-style-type: none"><li>• Aware of various front panel controls and indicators.</li><li>• Connect and manipulate nodes and wires in the block diagram.</li><li>• Locate various toolbars and pull-down menus for the purpose of implementing specific functions.</li><li>• Locate and utilize the context help window.</li><li>• Familiar with LabVIEW and different applications using it.</li><li>• Run a Virtual Instrument (VI).</li></ul>			
<b>Sl.No</b>	<b>VI Programs (using LabVIEW software) to realize the following:</b>		
1	Basic arithmetic operations: addition, subtraction, multiplication and division		
2	Boolean operations: AND, OR, XOR, NOT and NAND		
3	Sum of ‘n’ numbers using ‘for’ loop		
4	Factorial of a given number using ‘for’ loop		
5	Determine square of a given number		
6	Factorial of a given number using ‘while’ loop		
7	Sorting even numbers using ‘while’ loop in an array		
8	Finding the array maximum and array minimum		
	Demonstration Experiments (For CIE)		
9	Build a Virtual Instrument that simulates a heating and cooling system. The system must be able to be controlled manually or automatically.		
10	Build a Virtual Instrument that simulates a Basic Calculator (using formula node).		
11	Build a Virtual Instrument that simulates a Water Level Detector.		
12	Demonstrate how to create a basic VI which calculates the area and perimeter of a circle.		
<b>Course outcomes (Course Skill Set):</b> <p>At the end of the course the student will be able to:</p> <ol style="list-style-type: none"><li>1. Use Lab VIEW to create data acquisition, analysis and display operations</li><li>2. Create user interfaces with charts, graph and buttons</li><li>3. Use the programming structures and data types that exist in Lab VIEW</li><li>4. Use various editing and debugging techniques</li></ol>			
<b>Assessment Details (both CIE and SEE)</b> <p>The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course.</p>			

The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

**Continuous Internal Evaluation (CIE):**

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled down to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8<sup>th</sup> week of the semester and the second test shall be conducted after the 14<sup>th</sup> week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

**Semester End Evaluation (SEE):**

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours

Rubrics suggested in Annexure-II of Regulation book

**Suggested Learning Resources:**

1. Virtual Instrumentation using LABVIEW, Jovitha Jerome, PHI, 2011
2. Virtual Instrumentation using LABVIEW, Sanjay Gupta, Joseph John, TMH, McGraw Hill, Second Edition, 2011.

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**IV Semester**

Maths for Communication Engineers			
Course Code	21EC41	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	3:0:0:1	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3
<b>Course objectives:</b> <ul style="list-style-type: none"><li>To facilitate the students in understanding the Concepts of Electric and Magnetic Fields through Mathematical representations.</li><li>To enable the students in using the concepts of Field theory to arrive at important Mathematical relations associated with Electromagnetic waves.</li><li>To provide a foundation in Random variables and Random Processes which find application in Communication.</li></ul>			
<b>Teaching-Learning Process (General Instructions)</b> <p>The sample strategies, which the teacher can use to accelerate the attainment of the various course outcomes are listed in the following:</p> <ol style="list-style-type: none"><li><b>1. Explain the importance of Mathematics in Communication links and Prerequisites of the course.</b></li><li><b>2. Prepare handouts of related problems and encourage the doubts.</b></li><li><b>3. Prepare assignment questions related to theory and problems.</b></li><li><b>4. Prepare concept-based quiz questions.</b></li><li><b>5. Encourage short videos available on web related to important topics of Digital Signal Processing.</b></li><li><b>6. Encourage Students to create a forum wherein they can discuss theoretical concepts and problems.</b></li></ol>			
<b>Prerequisites:</b> <p><b>[i] Vector Analysis</b> – Scalars and Vectors, Vector Algebra, Rectangular, Cylindrical and Spherical Coordinate system, Vector components and Unit vectors, Scalar and Vector fields, Dot product, cross product, Vector differentiation, Vector integration <b>[Revise Module-2 of 21MAT21 course]</b></p> <p><b>[ii] Probability Basics-</b> Why Probability? Axioms and Properties of Probability, Finding Probability Values, Conditional Probabilities and Independence, Independence among n events, Partitions</p>			
<b>Module-1: Static Electric Field and Flux Density</b>			
<b>Coulomb's Law and Electric Field Intensity:</b> The Experimental law of Coulomb, Electric Field Intensity, Field of a line charge			
<b>Electric Flux Density and Gauss-Divergence Theorem:</b> Electric Flux Density, Gauss' Law, Application of Gauss' Law for a Differential Volume Element, Divergence, Maxwell's First Equation, Divergence Theorem (From Text-1)			
<b>Teaching-Learning Process</b>	Chalk and talk method/Power point presentation <b>Self-Study:</b> Electric Field of a Sheet of Charge <b>RBT Level:</b> L1, L2, L3		
<b>Module-2: Electric Potential, Current Density and Steady Magnetic Field</b>			
<b>Electric Potential:</b> Energy Expended in moving a point charge in an Electric field, The Line Integral, Definition of Potential Difference and Potential, Potential field of a point charge, Potential Gradient			
<b>Current Density:</b> Current and Current Density, Current Continuity Equation			
<b>Steady Magnetic field:</b> Biot-Savart's Law, Ampere's Circuital Law (Statement, Illustration and Mathematical representation), Curl, Stokes' Theorem, Magnetic Flux and Flux density (From Text-1)			

<b>Teaching-Learning Process</b>	Chalk and talk method/Power point presentation <b>Self-Study:</b> Conductor Properties and Boundary Conditions, Scalar and Vector Magnetic Potential <b>RBT Level:</b> L1, L2, L3
<b>Module-3: Time Varying Fields, Maxwell's Equations and Uniform Plane Wave</b>	
<b>Time Varying Fields and Maxwell's Equations:</b> Faraday's Law, Displacement Current, Maxwell's Equations in Point Form, Maxwell's Equations in Integral Form <b>Uniform Plane Wave:</b> Wave Propagation in Free Space, Wave Propagation in Dielectrics, Poynting's Theorem and Wave Power, Propagation in Good Conductors: Skin Depth (From Text-1)	
<b>Teaching-Learning Process</b>	Chalk and talk method/Power point presentation <b>Self-Study:</b> Reflection of Uniform Plane Waves at Normal Incidence, Standing Wave Ratio <b>RBT Level:</b> L1, L2, L3
<b>Module-4: Single Random Variables</b>	
<b>Single Random Variables:</b> Definition of Random Variables, Cumulative Distribution Function, Continuous and Discrete Random Variables, Expectations, Characteristic Functions, Functions of Single Random Variables, Conditioned Random Variables (From Text-2)	
<b>Teaching-Learning Process</b>	Chalk and talk method/Power point presentation <b>Self-Study:</b> Multiple Random Variables <b>RBT Level:</b> L1, L2, L3
<b>Module-5: Random Processes</b>	
<b>Random Processes:</b> Ensemble, PDF, Independence, Expectations, Stationarity, Correlation Functions (ACF, CCF, Addition and Multiplication), Ergodic Random Processes, Power Spectral Densities (Wiener Khinchin, Addition and Multiplication of RPs, Cross Spectral Densities), Linear Systems (Output Mean, Cross-Correlation and Autocorrelation of Input and Output), Noise (From Text-2)	
<b>Teaching-Learning Process</b>	Chalk and talk method/Power point presentation <b>Self-Study:</b> Matched Filters <b>RBT Level:</b> L1, L2, L3
<b>Course outcome (Course Skill Set)</b> At the end of the course the student will be able to: <ol style="list-style-type: none"> <li>1. Recall the basic laws and definitions (with mathematical representations) in Electric and Magnetic fields.</li> <li>2. Apply the basic laws of Electric and Magnetic fields to arrive at Divergence Theorem, Current continuity Equation, Curl, Stokes' theorem.</li> <li>3. Apply Electric and Magnetic field concepts to arrive at Maxwell's equations, Electromagnetic wave equations and Poynting's theorem (Important concepts related to Communication link).</li> <li>4. Recall the definitions related to Random variables and Random Processes.</li> <li>5. Model the Random events in the Communication set-up and determine useful statistical parameters.</li> </ol>	
<b>Assessment Details (both CIE and SEE)</b> The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together. <b>Continuous Internal Evaluation:</b> Three Unit Tests each of <b>20 Marks (duration 01 hour)</b> <ol style="list-style-type: none"> <li>1. First test at the end of 5<sup>th</sup> week of the semester</li> </ol>	

2. Second test at the end of the 10<sup>th</sup> week of the semester
3. Third test at the end of the 15<sup>th</sup> week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4<sup>th</sup> week of the semester
5. Second assignment at the end of 9<sup>th</sup> week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks (duration 01 hours)**

6. At the end of the 13<sup>th</sup> week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

**CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours**)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module.

**Suggested Learning Resources:**

**Text Books:**

1. W H Hayt and J A Buck, "Engineering Electromagnetics", Mc Graw Education, 8<sup>th</sup> Edition, 2014.
2. Richard H Williams, "Probability, Statistics, and Random Processes for Engineers", Cengage Learning, Second Indian Reprint, 2019.

**Reference Books:**

1. Mathew N O Sadiku, "Elements of Electromagnetics", Oxford University Press, 4<sup>th</sup> edition, 2007.
2. Joseph A Edminister, "Electromagnetics", Schaum's Outlines, Revised 2<sup>nd</sup> Edition, 2017.
3. E C Jordan and K G Balmain, "Electromagnetic Waves and Radiating Systems ", Pearson, 2<sup>nd</sup> Edition, 2015.
4. Hwei P Hsu, "Theory and Problems of Probability, Random Variables and Random Processes", Schaum's Outlines, Mc Graw Hill, 2017.
5. K N Hari Bhat, K Anitha Sheela and Jayant Ganguly, "Probability Theory and Stochastic Processes for Engineers", Cengage Learning, 2019.

**Web links and Video Lectures (e-Resources)**

- <https://nptel.ac.in/courses/108106073>
- <https://archive.nptel.ac.in/courses/117/105/117105085>

**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

- Form multiple teams in the class and suggest them to prepare charts/models/animations or conduct an interactive quiz based on concepts of the course.

#### IV Semester

Digital Signal Processing			
Course Code	21EC42	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:2:0	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory + 8-10 Lab slots	Total Marks	100
Credits	04	Exam Hours	03
<b>Course objectives:</b> <ul style="list-style-type: none"><li>1. <b>Preparation:</b> To prepare students with fundamental knowledge/ overview in the field of Digital Signal Processing</li><li>2. <b>Core Competence:</b> To equip students with a basic foundation of Signal Processing by delivering the basics of Discrete Fourier Transforms &amp; their properties, design of filters and overview of digital signal processors</li></ul>			
<b>Teaching-Learning Process (General Instructions)</b> <p>These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.</p> <ul style="list-style-type: none"><li>1. Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.</li><li>2. Show Video/animation films to explain the different concepts of Digital Signal Processing</li><li>3. Encourage collaborative (Group) Learning in the class</li><li>4. Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking</li><li>5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.</li><li>6. Topics will be introduced in a multiple representation.</li><li>7. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.</li><li>8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.</li><li>9. Adopt Flipped class technique by sharing the materials / Sample Videos prior to the class and have discussions on the that topic in the succeeding classes</li><li>10. Give Programming Assignments</li></ul>			
<b>Module-1</b>			
<b>Discrete Fourier Transforms (DFT):</b> Frequency domain sampling and Reconstruction of Discrete Time Signals, The Discrete Fourier Transform, DFT as a linear transformation, Properties of the DFT: Periodicity, Linearity and Symmetry properties, Multiplication of two DFTs and Circular Convolution [Text 1]			
<b>Teaching-Learning Process</b>	Chalk and Talk, YouTube videos, Programming assignments <b>RBT Level:</b> L1, L2, L3		
<b>Module-2</b>			
<b>Additional DFT Properties, Linear filtering methods based on the DFT:</b> Use of DFT in Linear Filtering, Filtering of Long data Sequences. Fast-Fourier-Transform (FFT) algorithms: Efficient Computation of the DFT: Radix-2 FFT algorithms for the computation of DFT and IDFT decimation in-time [Text 1]			

<b>Teaching-Learning Process</b>	Chalk and Talk, YouTube videos, Programming assignments <b>RBT Level:</b> L1, L2, L3
<b>Module-3</b>	
<b>Design of FIR Filters:</b> Characteristics of practical frequency-selective filters, Symmetric and Anti-symmetric FIR filters, Design of Linear-phase FIR (low pass and High pass) filters using windows - Rectangular, Hamming, Hanning, Bartlett windows. Structure for FIR Systems: Direct form, Cascade form and Lattice structures <b>[Text1]</b>	
<b>Teaching-Learning Process</b>	Chalk and Talk, YouTube videos, Programming assignments <b>RBT Level:</b> L1, L2, L3
<b>Module-4</b>	
<b>IIR Filter Design:</b> Infinite Impulse response Filter Format, Bilinear Transformation Design Method, Analog Filters using Low pass prototype transformation, Normalized Butterworth Functions, Bilinear Transformation and Frequency Warping, Bilinear Transformation Design Procedure, Digital Butterworth (Lowpass and Highpass) Filter Design using BLT. Realization of IIR Filters in Direct form I and II <b>[Text 2]</b>	
<b>Teaching-Learning Process</b>	Chalk and Talk, YouTube videos, Programming assignments <b>RBT Level:</b> L1, L2, L3
<b>Module-5</b>	
<b>Digital Signal Processors:</b> DSP Architecture, DSP Hardware Units, Fixed point format, Floating point Format, IEEE Floating point formats, Fixed point digital signal processors, FIR and IIR filter implementations in Fixed point systems. <b>[Text 2]</b>	
<b>Teaching-Learning Process</b>	Chalk and Talk, YouTube videos, Programming assignments <b>RBT Level:</b> L1, L2, L3
<b>PRACTICAL COMPONENT OF IPCC</b>	
<b>List of Programs to be implemented &amp; executed using any programming languages like C++/Python/Java/Scilab / MATLAB/CC Studio (but not limited to)</b> <ol style="list-style-type: none"> <li>1. Computation of N point DFT of a given sequence and to plot magnitude and phase spectrum.</li> <li>2. Computation of circular convolution of two given sequences and verification of commutative, distributive and associative property of convolution.</li> <li>3. Computation of linear convolution of two sequences using DFT and IDFT.</li> <li>4. Computation of circular convolution of two given sequences using DFT and IDFT</li> <li>5. Verification of Linearity property, circular time shift property &amp; circular frequency shift property of DFT.</li> <li>6. Verification of Parseval's theorem</li> <li>7. Design and implementation of IIR (Butterworth) low pass filter to meet given specifications.</li> <li>8. Design and implementation of IIR (Butterworth) high pass filter to meet given specifications.</li> <li>9. Design and implementation of low pass FIR filter to meet given specifications.</li> <li>10. Design and implementation of high pass FIR filter to meet given specifications.</li> <li>11. To compute N- Point DFT of a given sequence using DSK 6713 simulator</li> <li>12. To compute linear convolution of two given sequences using DSK 6713 simulator</li> <li>13. To compute circular convolution of two given sequences using DSK 6713 simulator</li> </ol>	
<b>Course outcomes (Course Skill Set)</b> At the end of the course the student will be able to: <ol style="list-style-type: none"> <li>1. Determine response of LTI systems using time domain and DFT techniques</li> <li>2. Compute DFT of real and complex discrete time signals</li> <li>3. Compute DFT using FFT algorithms</li> <li>4. Design FIR and IIR Digital Filters</li> <li>5. Design of Digital Filters using DSP processor</li> </ol>	



**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together

**CIE for the theory component of IPCC**

Two Tests each of **20 Marks (duration 01 hour)**

- First test at the end of 5<sup>th</sup> week of the semester
- Second test at the end of the 10<sup>th</sup> week of the semester

Two assignments each of **10 Marks**

- First assignment at the end of 4<sup>th</sup> week of the semester
- Programming assignment at the end of 9<sup>th</sup> week of the semester, which can be implemented using programming languages like C++/Python/Java/Scilab

Scaled-down marks of two tests and two assignments added will be CIE marks for the theory component of IPCC for **30 marks**.

**CIE for the practical component of IPCC**

- On completion of every experiment/program in the laboratory, the students shall be evaluated and marks shall be awarded on the same day. The **15 marks** are for conducting the experiment and preparation of the laboratory record, the other **05 marks shall be for the test** conducted at the end of the semester.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to 15 marks.
- The laboratory test (**duration 03 hours**) at the end of the 15<sup>th</sup> week of the semester /after completion of all the experiments (whichever is early) shall be conducted for 50 marks and scaled down to 05 marks.

Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **20 marks**.

**SEE for IPCC**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (duration 03 hours)

- The question paper will have ten questions. Each question is set for 20 marks.
- There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
- The students have to answer 5 full questions, selecting one full question from each module.

**The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper shall include questions from the practical component.**

- The minimum marks to be secured in CIE to appear for SEE shall be the 12 (40% of maximum marks-30) in the theory component and 08 (40% of maximum marks -20) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included. The maximum of 04/05 questions to be set from the practical component of IPCC, the total marks of all questions should not be more than the 20 marks.

SEE will be conducted for 100 marks and students shall secure 35% of the maximum marks to qualify in the SEE. Marks secured will be scaled down to 50.

**Suggested Learning Resources:****Text Books:**

1. Proakis & Manolakis, "Digital Signal Processing - Principles Algorithms & Applications", 4<sup>th</sup> Edition, Pearson education, New Delhi, 2007. ISBN: 81-317-1000-9.
2. Li Tan, Jean Jiang, "Digital Signal processing - Fundamentals and Applications", Academic Press, 2013, ISBN: 978-0-12-415893.

**Reference Books:**

1. Sanjit K Mitra, "Digital Signal Processing, A Computer Based Approach", 4<sup>th</sup> Edition, McGraw Hill Education, 2013,
2. Oppenheim & Schaffer, "Discrete Time Signal Processing", PHI, 2003.
3. D Ganesh Rao and Vineeth P Gejji, "Digital Signal Processing" Cengage India Private Limited, 2017, ISBN: 9386858231

**Web links and Video Lectures (e-Resources):**

By Prof. S. C. Dutta Roy, IIT Delhi

<https://nptel.ac.in/courses/117102060>

**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

Programming Assignments / Mini Projects can be given to improve programming skills

**VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI**  
**B.E: Electronics & Communication Engineering / B.E: Electronics & Telecommunication Engineering**  
**NEP, Outcome Based Education (OBE) and Choice Based Credit System (CBCS)**  
**(Effective from the academic year 2021 – 22)**

**IV Semester**

<b>Circuits &amp; Controls</b>			
Course Code	<b>21EC43</b>	CIE Marks	50
Teaching Hours/Week (L: T: P: S)	(3:0:2:0)	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory + 12 Lab slots	Total Marks	100
Credits	04	Exam Hours	03
<b>Course objectives: This course will enable students to:</b> <ol style="list-style-type: none"> <li>1. Apply mesh and nodal techniques to solve an electrical network.</li> <li>2. Solve different problems related to Electrical circuits using Network Theorems and Two port network.</li> <li>3. Familiarize with the use of Laplace transforms to solve network problems.</li> <li>4. Understand basics of control systems and design mathematical models using block diagram reduction, SFG, etc.</li> <li>5. Understand Time domain and Frequency domain analysis.</li> <li>6. Familiarize with the State Space Model of the system.</li> </ol>			
<b>Teaching-Learning Process (General Instructions)</b> These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes. <ul style="list-style-type: none"> <li>• Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.</li> <li>• Show Video/animation films to explain the different concepts of Linear Algebra &amp; Signal Processing.</li> <li>• Encourage collaborative (Group) Learning in the class .</li> <li>• Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking.</li> <li>• Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.</li> <li>• Topics will be introduced in a multiple representation.</li> <li>• Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.</li> <li>• Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.</li> <li>• Adopt Flipped class technique by sharing the materials / Sample Videos prior to the class and have discussions on the that topic in the succeeding classes.</li> <li>• Give Programming Assignments.</li> </ul>			
<b>Module-1</b>			
<b>Basic concepts and network theorems</b> Types of Sources, Loop analysis, Nodal analysis with independent DC and AC Excitations. (Textbook 1: 2.3, 4.1, 4.2, 4.3, 4.4, 10.6) Super position theorem, Thevenin's theorem, Norton's Theorem, Maximum Power transfer Theorem. (Textbook 2: 9.2, 9.4, 9.5, 9.7)			
<b>Teaching-Learning Process</b>	Chalk and Talk, YouTube videos, Demonstrate the concepts using circuits <b>RBT Level:</b> L1, L2, L3		

<b>Module-2</b>	
<b>Two port networks:</b> Short- circuit Admittance parameters, Open- circuit Impedance parameters, Transmission parameters, Hybrid parameters (Textbook 3: 11.1, 11.2, 11.3, 11.4, 11.5) <b>Laplace transform and its Applications:</b> Step Ramp, Impulse, Solution of networks using Laplace transform, Initial value and final value theorem (Textbook 3: 7.1, 7.2, 7.4, 7.7, 8.4)	
<b>Teaching-Learning Process</b>	Chalk and Talk <b>RBT Level:</b> L1, L2, L3
<b>Module-3</b>	
<b>Basic Concepts and representation:</b> Types of control systems, effect of feedback systems, differential equation of physical systems (only electrical systems), Introduction to block diagrams, transfer functions, Signal Flow Graphs (Textbook 4: Chapter 1.1, 2.2, 2.4, 2.5, 2.6)	
<b>Teaching-Learning Process</b>	Chalk and Talk, YouTube videos <b>RBT Level:</b> L1, L2, L3
<b>Module-4</b>	
<b>Time Response analysis:</b> Time response of first order systems. Time response of second order systems, time response specifications of second order systems (Textbook 4: Chapter 5.3, 5.4) <b>Stability Analysis:</b> Concepts of stability necessary condition for stability, Routh stability criterion, relative stability Analysis (Textbook 4: Chapter 5.3, 5.4, 6.1, 6.2, 6.4, 6.5)	
<b>Teaching-Learning Process</b>	Chalk and Talk, Any software tool to show time response <b>RBT Level:</b> L1, L2, L3
<b>Module-5</b>	
<b>Root locus:</b> Introduction the root locus concepts, construction of root loci (Textbook 4: 7.1, 7.2, 7.3) <b>Frequency Domain analysis and stability:</b> Correlation between time and frequency response and Bode plots (Textbook 4: 8.1, 8.2, 8.4) <b>State Variable Analysis:</b> Introduction to state variable analysis: Concepts of state, state variable and state models. State model for Linear continuous –Time systems, solution of state equations. (Textbook 4: 12.2, 12.3, 12.6)	
<b>Teaching-Learning Process</b>	Chalk and Talk, Any software tool to plot Root locus, Bode plot <b>RBT Level:</b> L1, L2, L3

<b>PRACTICAL COMPONENT OF IPCC</b>	
Using suitable hardware and simulation software, demonstrate the operation of the following circuits:	
<b>Sl.No</b>	<b>Experiments</b>
1	Verification of Superposition theorem
2	Verification of Thevenin's theorem
3	Speed torque characteristics of i)AC Servomotor ii) DC Servomotors
4	Determination of time response specification of a second order Under damped System, for different damping factors.
5	Determination of frequency response of a second order System
6	Determination of frequency response of a lead lag compensator
7	Using Suitable simulation package study of speed control of DC motor using i) Armature control ii) Field control

8	Using suitable simulation package, draw Root locus & Bode plot of the given transfer function.
<b>Demonstration Experiments (For CIE only, not for SEE)</b>	
9	Using suitable simulation package, obtain the time response from state model of a system.
10	Implementation of PI, PD Controllers.
11	Implement a PID Controller and hence realize an Error Detector.
12	Demonstrate the effect of PI, PD and PID controller on the system response.

### Course Outcomes

At the end of the course the student will be able to:

1. Analyse and solve Electric circuit, by applying, loop analysis, Nodal analysis and by applying network Theorems.
2. Evaluate two port parameters of a network and Apply Laplace transforms to solve electric networks.
3. Deduce transfer function of a given physical system, from differential equation representation or Block Diagram representation and SFG representation.
4. Calculate time response specifications and analyse the stability of the system.
5. Draw and analyse the effect of gain on system behaviour using root loci.
6. Perform frequency response Analysis and find the stability of the system.
7. Represent State model of the system and find the time response of the system.

### Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together

### CIE for the theory component of IPCC

Two Tests each of **20 Marks (duration 01 hour)**

- First test at the end of 5<sup>th</sup> week of the semester
- Second test at the end of the 10<sup>th</sup> week of the semester

Two assignments each of **10 Marks**

- First assignment at the end of 4<sup>th</sup> week of the semester
- Second assignment at the end of 9<sup>th</sup> week of the semester

Scaled-down marks of two tests and two assignments added will be CIE marks for the theory component of IPCC for **30 marks**.

### CIE for the practical component of IPCC

- On completion of every experiment/program in the laboratory, the students shall be evaluated and marks shall be awarded on the same day. The **15 marks** are for conducting the experiment and preparation of the laboratory record, the other **05 marks shall be for the test** conducted at the end of the semester.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to 15 marks.
- The laboratory test (**duration 03 hours**) at the end of the 15<sup>th</sup> week of the semester /after completion of all the experiments (whichever is early) shall be conducted for 50 marks and

scaled down to 05 marks.

Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **20 marks**.

#### **SEE for IPCC**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (duration 03 hours)

- The question paper will have ten questions. Each question is set for 20 marks.
- There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
- The students have to answer 5 full questions, selecting one full question from each module.

**The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper shall include questions from the practical component.**

- The minimum marks to be secured in CIE to appear for SEE shall be the 12 (40% of maximum marks-30) in the theory component and 08 (40% of maximum marks -20) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included. The maximum of 04/05 questions to be set from the practical component of IPCC, the total marks of all questions should not be more than the 20 marks.

SEE will be conducted for 100 marks and students shall secure 35% of the maximum marks to qualify in the SEE. Marks secured will be scaled down to 50.

#### **Suggested Learning Resources:**

##### **Text Books**

1. Engineering circuit analysis, William H Hayt, Jr, Jack E Kemmerly, Steven M Durbin, Mc Graw Hill Education, Indian Edition 8e.
2. Networks and Systems, D Roy Choudhury, New age international Publishers, second edition.
3. Network Analysis, M E Van Valkenburg, Pearson, 3e.
4. Control Systems Engineering, I J Nagrath, M. Gopal, New age international Publishers, Fifth edition.

##### **Web links and Video Lectures (e-Resources):**

- <https://nptel.ac.in/courses/108106098>
- <https://nptel.ac.in/courses/108102042>

##### **Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

*Programming Assignments / Mini Projects can be given to improve programming skills*

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**IV Semester**

Communication Theory			
Course Code	21EC44	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:1	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3
<b>Course objectives:</b> This course will enable students to <ul style="list-style-type: none"><li>Understand and analyse concepts of Analog Modulation schemes viz; AM, FM., Low pass sampling and Quantization as a random process.</li><li>Understand and analyse concepts digitization of signals viz; sampling, quantizing and encoding.</li><li>Evolve the concept of SNR in the presence of channel induced noise and study Demodulation of analog modulated signals.</li><li>Evolve the concept of quantization noise for sampled and encoded signals and study the concepts of reconstruction from these samples at a receiver.</li></ul>			
<b>Teaching-Learning Process (General Instructions)</b> These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes. <ol style="list-style-type: none"><li>Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.</li><li>Show Video/animation films to explain evolution of communication technologies.</li><li>Encourage collaborative (Group) Learning in the class.</li><li>Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking.</li><li>Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.</li><li>Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.</li><li>Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.</li></ol>			
Module-1			
<b>AMPLITUDE MODULATION:</b> Introduction, Amplitude Modulation: Time & Frequency Domain description, Switching modulator, Envelop detector. <b>DOUBLE SIDE BAND-SUPPRESSED CARRIER MODULATION:</b> Time and Frequency Domain description, Ring modulator, Coherent detection, Costas Receiver, Quadrature Carrier Multiplexing. <b>SINGLE SIDE-BAND AND VESTIGIAL SIDEBAND METHODS OF MODULATION:</b> SSB Modulation, VSB Modulation, Frequency Translation, Frequency Division Multiplexing, Theme Example: VSB Transmission of Analog and Digital Television. [Text1: 3.1 to 3.8]			
Teaching-Learning Process	Chalk and talk method, Power Point Presentation. <b>Self-study topics:</b> Properties of the Fourier Transform, Dirac Delta Function. <b>RBT Level:</b> L1, L2, L3		
Module-2			
<b>ANGLE MODULATION:</b> Basic definitions, Frequency Modulation: Narrow Band FM, Wide Band FM, Transmission bandwidth of FM Signals. Generation of FM Signals. Demodulation of FM Signals. FM			

Stereo Multiplexing, Phase-Locked Loop: Nonlinear model of PLL, Linear model of PLL, Nonlinear Effects in FM Systems. The Superheterodyne Receiver [Text1: 4.1 to 4.6]	
<b>Teaching-Learning Process</b>	Chalk and talk method, Power Point Presentation, YouTube videos. <b>Self-study topics:</b> FM Broadcasting System [Ref1] <b>RBT Level:</b> L1, L2, L3
<b>Module-3</b>	
<b>NOISE:</b> Shot Noise, Thermal noise, White Noise, Noise Equivalent Bandwidth. <b>NOISE IN ANALOG MODULATION:</b> Introduction, Receiver Model, Noise in DSB-SC receivers. Noise in AM receivers, Threshold effect, Noise in FM receivers, Capture effect, FM threshold effect, FM threshold reduction, Preemphasis and De-emphasis in FM (Text1: 5.10, 6.1 to 6.6)	
<b>Teaching-Learning Process</b>	Chalk and talk method, Power Point Presentation, YouTube videos. <b>Self-study topics:</b> Mean, Correlation and Covariance functions of Random Processes <b>RBT Level:</b> L1, L2, L3
<b>Module-4</b>	
<b>SAMPLING AND QUANTIZATION:</b> Introduction, Why Digitize Analog Sources? The Low pass Sampling process Pulse Amplitude Modulation. Time Division Multiplexing, Pulse-Position Modulation, Generation of PPM Waves, Detection of PPM Waves. (Text1: 7.1 to 7.7 )	
<b>Teaching-Learning Process</b>	Chalk and talk method, Power Point Presentation, YouTube videos. <b>Self-study topics:</b> T1 carrier systems [Ref1] <b>RBT Level:</b> L1, L2, L3
<b>Module-5</b>	
<b>SAMPLING AND QUANTIZATION (Contd):</b> The Quantization Random Process, Quantization Noise, Pulse-Code Modulation: Sampling, Quantization, Encoding, Regeneration, Decoding, Filtering, Multiplexing; Delta Modulation (Text1: 7.8 to 7.10), Application examples - (a) Video + MPEG (Text1:7.11) and (b) Vocoder (refer Section 6.8 of Reference Book 1)	
<b>Teaching-Learning Process</b>	Chalk and talk method, Power Point Presentation, YouTube videos. <b>Self-study topics:</b> Digital Multiplexing. [Ref1] <b>RBT Level:</b> L1, L2, L3
<b>Course Outcomes (Course Skill Set)</b> At the end of the course the student will be able to: <ol style="list-style-type: none"> <li>1. Understand the amplitude and frequency modulation techniques and perform time and frequency domain transformations.</li> <li>2. Identify the schemes for amplitude and frequency modulation and demodulation of analog signals and compare the performance.</li> <li>3. Characterize the influence of channel noise on analog modulated signals.</li> <li>4. Understand the characteristics of pulse amplitude modulation, pulse position modulation and pulse code modulation systems.</li> <li>5. Illustration of digital formatting representations used for Multiplexers, Vocoder and Video transmission.</li> </ol>	
<b>Assessment Details (both CIE and SEE)</b> The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.	



**Continuous Internal Evaluation:**

Three Unit Tests each of **20 Marks (duration 01 hour)**

1. First test at the end of 5<sup>th</sup> week of the semester
2. Second test at the end of the 10<sup>th</sup> week of the semester
3. Third test at the end of the 15<sup>th</sup> week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4<sup>th</sup> week of the semester
5. Second assignment at the end of 9<sup>th</sup> week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks (duration 01 hours)**

6. At the end of the 13<sup>th</sup> week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

**CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours**)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module.

**Suggested Learning Resources:****Books**

1. Simon Haykins & Moher, Communication Systems, 5<sup>th</sup> Edition, John Wiley, India Pvt. Ltd, 2010, ISBN 978 - 81 - 265 - 2151 - 7.

**Reference Books**

1. B P Lathi and Zhi Ding, Modern Digital and Analog Communication Systems, Oxford University Press., 4<sup>th</sup> edition, 2010, ISBN: 97801980738002.
2. Simon Haykins, An Introduction to Analog and Digital Communication, John Wiley India Pvt. Ltd., 2008, ISBN 978-81-265-3653-5.
3. H Taub & D L Schilling, Principles of Communication Systems, TMH, 2011.

#### IV Semester

Communication Laboratory I			
Course Code	21ECL46	CIE Marks	50
Teaching Hours/Week (L: T: P: S)	0:0:2:0	SEE Marks	50
Credits	1	Exam Hours	3
<b>Course objectives:</b> This laboratory course enables students to <ul style="list-style-type: none"> <li>• Model an analog communication system signal transmission and reception.</li> <li>• Realize the electronic circuits to perform analog and pulse modulations and demodulations.</li> <li>• Verify the sampling theorem and relate the signal and its spectrum before and after sampling.</li> <li>• Understand the process of PCM and delta modulations.</li> <li>• Understand the PLL operation.</li> </ul>			
Sl.No.	Experiments		
1	Design of active second order Butterworth low pass and high pass filters.		
2	Amplitude Modulation and Demodulation of (a) Standard AM and (b) DSBSC (LM741 and LF398 ICs can be used)		
3	Frequency modulation and demodulation		
4	Design and test Time Division Multiplexing and Demultiplexing of two bandlimited signals.		
5	Design and test i) Pulse sampling, flat top sampling and reconstruction. ii) Pulse amplitude modulation and demodulation.		
6	Design and test BJT/FET Mixer		
7	Pulse Code Modulation and demodulation		
8	Phase locked loop Synthesis		
9	Illustration of (a) AM modulation and demodulation and display the signal and its spectrum. (b) DSB-SC modulation and demodulation and display the signal and its spectrum. (Use MATLAB/SCILAB)		
10	Illustration of FM modulation and demodulation and display the signal and its spectrum. (Use MATLAB/SCILAB)		
11	Illustrate the process of sampling and reconstruction of low pass signals. Display the signals and its spectrums of both analog and sampled signals. (Use MATLAB/SCILAB).		
12	Illustration of Delta Modulation and the effects of step size selection in the design of DM encoder. (Use MATLAB/SCILAB)		

**Course outcomes (Course Skill Set):**

At the end of the course the student will be able to:

1. Demonstrate the AM and FM modulation and demodulation by representing the signals in time and frequency domain.
2. Design and test the sampling, Multiplexing and PAM with relevant circuits.
3. Demonstrate the basic circuitry and operations used in AM and FM receivers.
4. Illustrate the operation of PCM and delta modulations for different input conditions.

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

**Continuous Internal Evaluation (CIE):**

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled down to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8<sup>th</sup> week of the semester and the second test shall be conducted after the 14<sup>th</sup> week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

**Semester End Evaluation (SEE):**

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners).

Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours.

Rubrics suggested in Annexure-II of Regulation book

**Suggested Learning Resources:**

1. Louis E Frenzel, Principles of Electronic Communication Systems, McGraw Hill Education (India) Private Limited, 2016.
2. B P Lathi, Zhi Ding, Modern Digital and Analog Communication Systems, Oxford University Press, 2015.

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**B.E: Electronics & Communication Engineering / B.E: Electronics & Telecommunication Engineering**  
**NEP, Outcome Based Education (OBE) and Choice Based Credit System (CBCS)**  
**(Effective from the academic year 2021 – 22)**

**IV Semester**

Embedded C Basics			
Course Code	21EC481	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	0:0:2:0	SEE Marks	50
Credits	1	Exam Hours	100
<b>Course objectives:</b> <ul style="list-style-type: none"><li>Understand the basic programming of Microprocessor and microcontroller.</li><li>To develop the microcontroller-based programs for various applications.</li></ul>			
<b>Sl.No</b>	<b>Experiments</b>		
	Conduct the following experiments by writing C Program using Keil microvision simulator (any 8051 microcontroller can be chosen as the target).		
1	Write a 8051 C program to multiply two 16 bit binary numbers.		
2	Write a 8051 C program to find the sum of first 10 integer numbers.		
3	Write a 8051 C program to find factorial of a given number.		
4	Write a 8051 C program to add an array of 16 bit numbers and store the 32 bit result in internal RAM		
5	Write a 8051 C program to find the square of a number (1 to 10) using look-up table.		
6	Write a 8051 C program to find the largest/smallest number in an array of 32 numbers		
7	Write a 8051 C program to arrange a series of 32 bit numbers in ascending/descending order		
8	Write a 8051 C program to count the number of ones and zeros in two consecutive memory locations.		
9	Write a 8051 C program to scan a series of 32 bit numbers to find how many are negative.		
10	Write a 8051 C program to display “Hello World” message (either in simulation mode or interface an LCD display).		
11	Write a 8051 C program to convert the hexadecimal data 0xCFh to decimal and display the digits on ports P0, P1 and P2 (port window in simulator).		
<b>Course outcomes (Course Skill Set):</b> <p>At the end of the course the student will be able to:</p> <ol style="list-style-type: none"><li>Write C programs in 8051 for solving simple problems that manipulate input data using different instructions of 8051 C.</li><li>Develop testing and experimental procedures on 8051 Microcontroller, analyze their operation under different cases.</li><li>Develop programs for 8051 Microcontroller to implement real world problems.</li><li>Design and Develop Mini projects</li></ol>			
<b>Assessment Details (both CIE and SEE)</b> <p>The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).</p>			

**Continuous Internal Evaluation (CIE):**

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.

Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.

Total marks scored by the students are scaled down to 30 marks (60% of maximum marks).

Weightage to be given for neatness and submission of record/write-up on time.

Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8<sup>th</sup> week of the semester and the second test shall be conducted after the 14<sup>th</sup> week of the semester.

In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.

The suitable rubrics can be designed to evaluate each student's performance and learning ability.

Rubrics suggested in Annexure-II of Regulation book

The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

**Semester End Evaluation (SEE):**

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours

Rubrics suggested in Annexure-II of Regulation book

**Suggested Learning Resources:**

"The 8051 Microcontroller: Hardware, Software and Applications", V Udayashankara and M S Mallikarjuna Swamy, McGraw Hill Education, 1<sup>st</sup> edition, 2017.

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**IV Semester**

<b>C++ Basics</b>			
Course Code	<b>21EC482</b>	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	0:0:2:0	SEE Marks	50
Credits	1	Exam Hours	100
<b>Course objectives:</b> <ul style="list-style-type: none"> <li>Understand object-oriented programming concepts, and apply them in solving problems.</li> <li>To create, debug and run simple C++ programs.</li> <li>Introduce the concepts of functions, friend functions, inheritance, polymorphism and function overloading.</li> <li>Introduce the concepts of exception handling and multithreading.</li> </ul>			
<b>Sl.No</b>	<b>Experiments</b>		
1	Write a C++ program to find largest, smallest & second largest of three numbers using inline functions MAX & Min.		
2	Write a C++ program to calculate the volume of different geometric shapes like cube, cylinder and sphere using function overloading concept.		
3	Define a STUDENT class with USN, Name & Marks in 3 tests of a subject. Declare an array of 10 STUDENT objects. Using appropriate functions, find the average of the two better marks for each student. Print the USN, Name & the average marks of all the students.		
4	Write a C++ program to create class called MATRIX using two-dimensional array of integers, by overloading the operator == which checks the compatibility of two matrices to be added and subtracted. Perform the addition and subtraction by overloading + and - operators respectively. Display the results by overloading the operator <<. If (m1 == m2) then m3 = m1 + m2 and m4 = m1 - m2 else display error		
5	Demonstrate simple inheritance concept by creating a base class FATHER with data members: <i>First Name, Surname, DOB &amp; bank Balance</i> and creating a derived class SON, which inherits: Surname & Bank Balance feature from base class but provides its own feature: First Name & DOB. Create & initialize F1 & S1 objects with appropriate constructors & display the FATHER & SON details.		
6	Write a C++ program to define class name FATHER & SON that holds the income respectively. Calculate & display total income of a family using Friend function.		
7	Write a C++ program to accept the student detail such as name & 3 different marks by get_data() method & display the name & average of marks using display() method. Define a friend function for calculating the average marks using the method mark_avg().		
8	Write a C++ program to explain virtual function (Polymorphism) by creating a base class polygon which has virtual function areas two classes rectangle & triangle derived from polygon & they have area to calculate & return the area of rectangle & triangle respectively.		
9	Design, develop and execute a program in C++ based on the following requirements: An EMPLOYEE class containing data members & members functions: i) Data members: employee number (an integer), Employee_Name (a string of characters), Basic_Salary (in integer), All_Allowances (an integer), Net_Salary (an integer). (ii) Member functions: To read the data of an employee, to calculate Net_Salary & to print the values of all the data members. (All_Allowances = 123% of Basic, Income Tax (IT) = 30% of gross salary (=basic_Salary_All_Allowances_IT).		
10	Write a C++ program with different class related through multiple inheritance & demonstrate the use of different access specified by means of members variables & members functions.		

11	Write a C++ program to create three objects for a class named count object with data members such as roll_no & Name. Create a members function set_data ( ) for setting the data values & display ( ) member function to display which object has invoked it using „this" pointer.
12	Write a C++ program to implement exception handling with minimum 5 exceptions classes including two built in exceptions.
<b>Course outcomes (Course Skill Set):</b> At the end of the course the student will be able to: <ol style="list-style-type: none"> <li>1. Write C++ program to solve simple and complex problems</li> <li>2. Apply and implement major object-oriented concepts like message passing, function overloading, operator overloading and inheritance to solve real-world problems.</li> <li>3. Use major C++ features such as Templates for data type independent designs and File I/O to deal with large data set.</li> <li>4. Analyze, design and develop solutions to real-world problems applying OOP concepts of C++</li> </ol>	
<b>Assessment Details (both CIE and SEE)</b> The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE). <b>Continuous Internal Evaluation (CIE):</b> CIE marks for the practical course is <b>50 Marks</b> . The split-up of CIE marks for record/ journal and test are in the ratio <b>60:40</b> . <ul style="list-style-type: none"> <li>• Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.</li> <li>• Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.</li> <li>• Total marks scored by the students are scaled down to 30 marks (60% of maximum marks).</li> <li>• Weightage to be given for neatness and submission of record/write-up on time.</li> <li>• Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8<sup>th</sup> week of the semester and the second test shall be conducted after the 14<sup>th</sup> week of the semester.</li> <li>• In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.</li> <li>• The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book</li> <li>• The average of 02 tests is scaled down to <b>20 marks</b> (40% of the maximum marks).</li> </ul> The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.	
<b>Semester End Evaluation (SEE):</b> SEE marks for the practical course is 50 Marks. SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University All laboratory experiments are to be included for practical examination. (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. <b>OR</b> based on the course requirement evaluation rubrics shall be decided jointly by examiners. Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly. Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.	



General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours

Rubrics suggested in Annexure-II of Regulation book

**Suggested Learning Resources:**

1. Object oriented programming in TURBO C++, Robert Lafore, Galgotia Publications, 2002
2. The Complete Reference C++, Herbert Schildt, 4<sup>th</sup> Edition, Tata McGraw Hill, 2003.
3. Object Oriented Programming with C++, E Balaguruswamy, 4<sup>th</sup> Edition, Tata McGraw Hill, 2006.

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**IV Semester**

Octave / Scilab for Signals			
Course Code	21EC483	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	0:0:2:0	SEE Marks	50
Credits	1	Exam Hours	100
<b>Course objectives:</b> <div><div>1. <b>Preparation:</b> To prepare students with fundamental knowledge/ overview in the field of signals and processing.</div><div>2. <b>Core Competence:</b> To equip students with a basic foundation in electronic engineering and mathematics fundamentals required for comprehending the operation and application of signal processing.</div><div>3. <b>Professionalism &amp; Learning Environment:</b> To inculcate in students an ethical and professional attitude by providing an academic environment inclusive of effective communication, teamwork, ability to relate engineering issues to a broader social context, and life-long learning needed for a successful professional career.</div></div>			
Sl.No	Experiments		
1	Verify the Sampling theorem.		
2	Determine linear convolution, Circular convolution and Correlation of two given sequences. Verify the result using theoretical computations.		
3	Determine the linear convolution of two given point sequences using FFT algorithm. Verify the result using theoretical computations.		
4	Determine the correlation using FFT algorithm. Verify the result using theoretical computations.		
5	Determine the spectrum of the given sequence using FFT. Verify the result using theoretical computations.		
6	Design and test FIR filter using Windowing method (Hamming, Hanning and Rectangular window) for the given order and cut-off frequency.		
7	Design and test IIR Butterworth 1 <sup>st</sup> and 2 <sup>nd</sup> order low & high pass filter.		
8	Design and test IIR Chebyshev 1 <sup>st</sup> and 2 <sup>nd</sup> order low & high pass filter.		
9	Generation of an AM – Suppressed Carrier Wave & visualization of the time domain and frequency domain plots.		
10	Generation and visualization of standard test signals (both continuous and discrete time).		
11	Generation and visualization of audio signal (pre-recorded) and generation of echo.		
12	Generation and visualization of the STFT of a chirp (and other related) signal.		
<b>Course outcomes (Course Skill Set):</b> At the end of the course the student will be able to: <div><div>• Demonstrate the DSP concepts on signal generation and sampling using Scilab/Octave</div><div>• Design and verify the computation of discrete signals using Scilab/Octave.</div><div>• Demonstrate and verify the application of FFT/DFT algorithm for a given signal using Scilab/Octave.</div><div>• Design and demonstrate programs to evaluate different types of low and high pass FIR filters using Scilab/Octave.</div><div>• Design, demonstrate and visualize different real world signals using Scilab/Octave programs.</div></div>			

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

**Continuous Internal Evaluation (CIE):**

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.

Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.

Total marks scored by the students are scaled down to 30 marks (60% of maximum marks).

Weightage to be given for neatness and submission of record/write-up on time.

Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8<sup>th</sup> week of the semester and the second test shall be conducted after the 14<sup>th</sup> week of the semester.

In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.

The suitable rubrics can be designed to evaluate each student's performance and learning ability.

Rubrics suggested in Annexure-II of Regulation book

The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

**Semester End Evaluation (SEE):**

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours

Rubrics suggested in Annexure-II of Regulation book

**Suggested Learning Resources:**

Digital Signal Processing Using MATLAB, John G Proakis and Vinay K Ingle, Cengage Learning, 2011

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**IV Semester**

DAQ using LabVIEW			
Course Code	21EC484	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	0:0:2:0	SEE Marks	50
Credits	1	Exam Hours	100
<b>Course objectives:</b> <ul style="list-style-type: none"><li>• Process the knowledge of loop constructs.</li><li>• Fundamentals of graphical programming and use LabVIEW modules</li><li>• Implement ‘Timing’ functions.</li><li>• Input algebraic formulas via ‘Formula Nodes’ and ‘Expression Nodes’.</li></ul>			
<b>Sl.No</b>	<b>Experiments</b>		
1	Data acquisition using LabVIEW for temperature measurement with thermocouple.		
2	Data acquisition using LabVIEW for temperature measurement with AD590.		
3	Data acquisition using LabVIEW for temperature measurement with RTD.		
4	Data acquisition using LabVIEW for temperature measurement with Thermistor.		
5	Creation of a CRO using LabVIEW and measurement of frequency and amplitude from external source.		
6	Create function generator using LabVIEW and display the amplitude and frequency on CRO (externally connected)		
7	Demonstrate amplitude modulation considering modulating and carrier wave from external source.		
8	Interface LEDs to DAQ output and implement counter.		
9	Data acquisition using LabVIEW for load / strain measurement using suitable transducers.		
10	Demonstrate binary to grey code converter (& vice versa) using DAQ card.		
11	Data acquisition using LabVIEW for distance/humidity measurement using suitable transducers.		
12	Reading audio input with Microphones and output using DAQ card.		
<b>Course outcomes (Course Skill Set):</b> <p>At the end of the course the student will be able to:</p> <ol style="list-style-type: none"><li>1. Build temperature indicating instruments using LabVIEW (NI DAQ)</li><li>2. Interface peripheral devices/instruments to LabVIEW</li><li>3. Build LabVIEW modules to sense and process audio inputs</li><li>4. Apply programming structures, data types, and the analysis and signal processing algorithms in LabVIEW</li><li>5. Debug and troubleshoot applications</li></ol>			
<b>Assessment Details (both CIE and SEE)</b> <p>The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course.</p>			

The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

**Continuous Internal Evaluation (CIE):**

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled down to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8<sup>th</sup> week of the semester and the second test shall be conducted after the 14<sup>th</sup> week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

**Semester End Evaluation (SEE):**

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours

Rubrics suggested in Annexure-II of Regulation book

**Suggested Learning Resources:**

1. Virtual Instrumentation using LABVIEW, Jovitha Jerome, PHI, 2011
2. Virtual Instrumentation using LABVIEW, Sanjay Gupta, Joseph John, TMH, McGraw Hill, Second Edition, 2011.

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**V Semester**

<b>Digital Communication</b>			
Course Code	<b>21EC51</b>	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	3:0:0:1	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3
<b>Course objectives:</b> <ul style="list-style-type: none"> <li>• Understand the concept of signal processing of digital data and signal conversion to symbols at the transmitter and receiver.</li> <li>• Compute performance metrics and parameters for symbol processing and recovery in ideal and corrupted channel conditions.</li> <li>• Understand the principles of spread spectrum communications.</li> <li>• Understand the basic principles of information theory and various source coding techniques.</li> <li>• Build a comprehensive knowledge about various Source and Channel Coding techniques.</li> <li>• Discuss the different types of errors and error detection and controlling codes used in the communication channel.</li> <li>• Understand the concepts of convolution codes and analyze the code words using time domain and transform domain approach.</li> </ul>			
<b>Teaching-Learning Process (General Instructions)</b> The sample strategies, which the teacher can use to accelerate the attainment of the various course outcomes are listed in the following: <ol style="list-style-type: none"> <li>1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.</li> <li>2. Arrange visits to nearby PSUs such as BHEL, BEL, ISRO, etc., and small-scale communication industries.</li> <li>3. Show Video/animation films to explain the functioning of various modulation techniques, Channel, and source coding.</li> <li>4. Encourage collaborative (Group) Learning in the class</li> <li>5. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking</li> <li>6. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize &amp; analyze information rather than simply recall it.</li> <li>7. Topics will be introduced in multiple representations.</li> <li>8. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.</li> <li>9. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.</li> </ol>			
<b>Module-1</b>			
<b>Digital Modulation Techniques:</b> Phase shift Keying techniques using coherent detection: generation, detection and error probabilities of BPSK and QPSK, M-ary PSK, M-ary QAM. Frequency shift keying techniques using Coherent detection: BFSK generation, detection and error probability. Non coherent orthogonal modulation techniques: BFSK, DPSK Symbol representation, Block diagrams treatment of Transmitter and Receiver, Probability of error (without derivation of probability of error equation).			
<b>Teaching-Learning Process</b>	Chalk and talk method, Simulation of modulation techniques, Power Point Presentation, YouTube videos Animation of BPSK, QPSK, BFSK and DPSK. Problems on Generation and detection of DPSK, QPSK. <b>Self-study topic:</b> Minimum shift keying and Non-coherent BFSK <b>RBT Level:</b> L1, L2, L3		

Module-2	
<b>Signalling Communication through Band Limited AWGN Channels:</b> <b>Signalling over AWGN Channels-</b> Introduction, Geometric representation of signals, Gram- Schmidt Orthogonalization procedure, Conversion of the continuous AWGN channel into a vector channel (without statistical characterization), Optimum receivers using coherent detection: ML Decoding, Correlation receiver, matched filter receiver. <b>Signal design for Band limited Channels:</b> Design of band limited signals for zero ISI-The Nyquist Criterion (statement only), Design of band limited signals with controlled ISI-Partial Response signals, Probability of error for detection of Digital PAM: Symbol-by-Symbol detection of data with controlled ISI.	
<b>Teaching-Learning Process</b>	Chalk & talk method, PowerPoint Presentation, YouTube videos <b>Self-study topics:</b> Maximum Likelihood detection, Channel equalization <b>RBT Level:</b> L1, L2, L3
Module-3	
<b>Principles of Spread Spectrum:</b> Spread Spectrum Communication Systems: Model of a Spread Spectrum Digital Communication System, Direct Sequence Spread Spectrum Systems, Effect of De-spreading on a narrowband Interference, Probability of error (statement only), Some applications of DS Spread Spectrum Signals, Generation of PN Sequences, Frequency Hopped Spread Spectrum, CDMA based on IS-95.	
<b>Teaching-Learning Process</b>	Chalk & talk method, Seminar about security issues in communication systems <b>RBT Level:</b> L1, L2, L3
Module-4	
<b>Introduction to Information Theory:</b> Measure of information, Average information content of symbols in long independent sequences. <b>Source Coding:</b> Encoding of the Source Output, Shannon's Encoding Algorithm, Shannon-Fano Encoding Algorithm, Huffman coding. <b>Error Control Coding:</b> Introduction, Examples of Error control coding, methods of Controlling Errors, Types of Errors, types of Codes.	
<b>Teaching-Learning Process</b>	Chalk and talk method, Problems on source coding, error control codes <b>RBT Level:</b> L1, L2, L3
Module-5	
<b>Linear Block Codes:</b> Matrix description of Linear Block Codes, Error Detection & Correction capabilities of Linear Block Codes, Single error correction Hamming code, Table lookup Decoding using Standard Array. <b>Convolution codes:</b> Convolution Encoder, Time domain approach, Transform domain approach, Code Tree, Trellis and State Diagram.	
<b>Teaching-Learning Process</b>	Chalk and talk method, Animation of convolution encoders <b>RBT Level:</b> L1, L2, L3
<b>Course outcomes (Course Skill Set)</b> At the end of the course the student will be able to: <ol style="list-style-type: none"> <li>1. Analyze different digital modulation techniques and choose the appropriate modulation technique for the given specifications.</li> <li>2. Test and validate symbol processing and performance parameters at the receiver under ideal and corrupted bandlimited channels.</li> <li>3. Differentiate various spread spectrum schemes and compute the performance parameters of communication system.</li> <li>4. Apply the fundamentals of information theory and perform source coding for given message</li> <li>5. Apply different encoding and decoding techniques with error Detection and Correction.</li> </ol>	

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous Internal Evaluation:**

Three Unit Tests each of **20 Marks (duration 01 hour)**

1. First test at the end of 5<sup>th</sup> week of the semester
2. Second test at the end of the 10<sup>th</sup> week of the semester
3. Third test at the end of the 15<sup>th</sup> week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4<sup>th</sup> week of the semester
5. Second assignment at the end of 9<sup>th</sup> week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks (duration 01 hours)**

6. At the end of the 13<sup>th</sup> week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

**CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours**)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module.

**Suggested Learning Resources:****Text Books:**

1. Simon Haykin, "Digital Communication Systems", John Wiley & sons, First Edition, 2014, ISBN 978-0-471-64735-5.
2. John G Proakis and Masoud Salehi, "Fundamentals of Communication Systems", 2014 Edition, Pearson Education, ISBN 978-8-131-70573-5.
3. K Sam Shanmugam, "Digital and analog communication systems", John Wiley India Pvt. Ltd, 1996.
4. Hari Bhat, Ganesh Rao, "Information Theory and Coding", Cengage, 2017.
5. Todd K Moon, "Error Correction Coding", Wiley Std. Edition, 2006.

**Reference Books:**

1. Bernard Sklar, "Digital Communications – Fundamentals and Applications", Second Edition, Pearson Education, 2016, ISBN: 9780134724058.
2. K Sam Shanmugam, "Digital and analog communication systems", John Wiley India Pvt. Ltd, 1996.

**Web links and Video Lectures (e-Resources)**

- <https://nptel.ac.in/courses/108102096>



**VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI**  
**B.E: Electronics & Communication Engineering / B.E: Electronics & Telecommunication Engineering**  
**NEP, Outcome Based Education (OBE) and Choice Based Credit System (CBCS)**  
**(Effective from the academic year 2021 – 22)**

**V Semester**

Object Oriented Programming with Java & Data Structures			
Course Code	21EC52	CIE Marks	50
Teaching Hours/Week (L: T: P: S)	(3:0:2:0)	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory + 13 Lab slots	Total Marks	100
Credits	04	Exam Hours	03
<b>Course objectives:</b> <b>The goal of the course ‘Object Oriented Programming with Java &amp; Data Structures’ is</b> <ol style="list-style-type: none"><li>1. To make students learn fundamentals features of object oriented language and JAVA</li><li>2. To set up a Java JDK environment to create, debug and run simple Java programs.</li><li>3. To Illustrate linear representation of data structures: Stack, Queues, Lists.</li></ol>			
<b>Teaching-Learning Process (General Instructions)</b> These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes. <ol style="list-style-type: none"><li>1. In addition to the traditional lecture method, different types of innovative teaching methods may be adopted so that the delivered lessons shall develop student’s theoretical and programming skills.</li><li>2. State the need for learning Programming with real-life examples.</li><li>3. Support and guide the students for self-study.</li><li>4. You will also be responsible for assigning homework, grading assignments and quizzes, and documenting students' progress.</li><li>5. Encourage the students for group learning to improve their creative and analytical skills.</li><li>6. Show short related video lectures in the following ways:<ul style="list-style-type: none"><li>• As an introduction to new topics (pre-lecture activity).</li><li>• As a revision of topics (post-lecture activity).</li><li>• As additional examples (post-lecture activity).</li><li>• As an additional material of challenging topics (pre-and post-lecture activity).</li><li>• As a model solution of some exercises (post-lecture activity).</li></ul></li></ol>			
<b>Module-1: Introduction to JAVA</b>			
An Overview of Java: Object-Oriented Programming, A First Simple program, Data types, Variables and arrays: Primitive types, Booleans, A Closer Look at Literals, Variables, Type conversion and casting, Arrays, Introducing Classes: Class fundamentals, Declaring objects, Assigning Object Reference Variables, Introducing Methods, Constructors, The this keyword, Garbage collection, The finalize() method, A stack class. TextBook 1: Ch: 2, Ch: 3, Ch: 6			
<b>Teaching-Learning Process</b>	Chalk and Talk, PowerPoint Presentation <b>RBT Level:</b> L1, L2, L3		
<b>Module-2: OOP in JAVA</b>			
A Closer Look at Methods and classes: Overloading methods, Using objects as parameters, Returning objects, Access control, static members, final members, Command Line Arguments, String Class. Inheritance Basics: Member access and Inheritance, A Superclass Variable can reference a subclass object, Using Super, Creating a Multilevel Hierarchy, When Constructors are called. Text Book 1: Ch: 7			

<b>Teaching-Learning Process</b>	Chalk and Talk, PowerPoint Presentation <b>RBT Level:</b> L1, L2, L3
<b>Module-3: Inheritance and Exception Handling</b>	
Java Collection Framework: Inheritance Hierarchy, Collection interface, The HashSet Class, Generic Collections, Generic methods, Generic Wildcards. Iterators, TreeSet class, LinkedHashSet Class, EnumSet Class, List Interface, ArrayList and Vector classes, Linked class, ListIterator interface. Text Book 2: Ch: 4	
<b>Teaching-Learning Process</b>	Chalk and Talk, PowerPoint Presentation <b>RBT Level:</b> L1, L2, L3
<b>Module-4: Stack, Queues, Linked data structures</b>	
Stacks: Stack operations, JCF Stack class, A stack interface, An indexed implementation, A linked implementation, Abstracting the common code, Queues: Queue operations, JCF Queue Interface, A simple queue interface, An indexed implementation, Application: A Client-Server system. Text Book 2: Ch: 5, Ch: 6	
<b>Teaching-Learning Process</b>	Chalk and Talk, PowerPoint Presentation <b>RBT Level:</b> L1, L2, L3
<b>Module-5: Lists, Trees, Binary Tree</b>	
Lists: JCF list interface, Range-view operation sublist( ), List iterators, Other List types. Tree: Tree definitions, Decision trees, Ordered trees, Traversal algorithms Binary Tree: Definitions, Full binary trees, Complete Binary trees, Binary tree traversal algorithms, Expression tree. Text Book 2: Ch: 7, Ch: 10, Ch: 11	
<b>Teaching-Learning Process</b>	Chalk and Talk, PowerPoint Presentation <b>RBT Level:</b> L1, L2, L3

<b>PRACTICAL COMPONENT OF IPCC</b>	
<b>Sl.No</b>	<b>Experiments</b>
1	Use Eclipse or NetBeans IDE and acquaint with the various menus. Create a test project, add a test class, and run it. Try debug step by step with a small program of about 10 to 15 lines which contains at least one if else condition and a for loop. To include suitable Small Java programs.
2	Design a class to represent a Student (details include the Student ID, Name of the Student, Branch, year, location and college). Assign initial values using constructor. Design a sub-class with methods to accept the marks & attendance and hence calculate average of marks of 6 subjects and attendance percentage.
3	Write a recursive and non recursive Java program to implement i) Linear search ii) Binary search
4	Write a Java program to implement i) Bubble sort ii) Selection sort iii) quick sort iv) insertion sort
5	Write a Java program to generate 'N' Fibonacci numbers using recursive and non-recursive methods.
6	Write a menu-driven Java program to implement the following data structures using an array: a)Stack ADT (b) Queue ADT
7	Write a menu-driven Java program to implement the following operations on Singly Linked List (SLL): a) Create a SLL of integers. b) Insert a given integer from SLL. c) Delete a given integer into SLL. d) Display the contents of SLL.

8	Write a Java program to perform the following operations: a) Insert an element into a Binary Search Tree (BST). b) Delete an element from a BST. c) Search for a key element in a BST d) Traverse the BST in pre-order, in-order & post-order.
9	Write a java program to demonstrate method overloading and constructors overloading.
10	Write a Java programs to implement the following using a singly linked list and perform the given operations. a) Stack ADT i) push an element into stack ii) pop an element from the stack iii) display the contents of the stack
11	Write a Java programs to implement the following using a singly linked list and perform the given operations. b) Queue ADT i) insert an element into queue ii) delete an element from the queue iii) display the contents of the queue
12	Write a java program that works as a simple calculator. Use a Grid Layout to arrange Buttons for digits and for the + - * % operations. Add a text field to display the result. Handle any possible exceptions like divide by zero.

#### **Course Outcomes**

At the end of the course the student will be able to:

1. Use OOP concepts effectively to build simple application programs.
2. Set up a Java JDK environment to create, debug and run simple java programs
3. Explain and implement the object oriented core-concepts such as class, object, inheritance and exception handling using JAVA.
4. Implement the data structures such as Arrays, Lists, Stack, Queue and Trees using Java
5. Make a decision on choosing a suitable data structure for a specific application program.

#### **Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together

#### **CIE for the theory component of IPCC**

Two Tests each of **20 Marks (duration 01 hour)**

- First test at the end of 5<sup>th</sup> week of the semester
- Second test at the end of the 10<sup>th</sup> week of the semester

Two assignments each of **10 Marks**

- First assignment at the end of 4<sup>th</sup> week of the semester
- Second assignment at the end of 9<sup>th</sup> week of the semester

Scaled-down marks of two tests and two assignments added will be CIE marks for the theory component of IPCC for **30 marks**.

#### **CIE for the practical component of IPCC**

- On completion of every experiment/program in the laboratory, the students shall be evaluated and marks shall be awarded on the same day. The **15 marks** are for conducting the experiment and preparation of the laboratory record, the other **05 marks shall be for the test** conducted at the end of the semester.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous

evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to 15 marks.

- The laboratory test (**duration 03 hours**) at the end of the 15<sup>th</sup> week of the semester /after completion of all the experiments (whichever is early) shall be conducted for 50 marks and scaled down to 05 marks.

Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **20 marks**.

#### **SEE for IPCC**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (duration 03 hours)

- The question paper will have ten questions. Each question is set for 20 marks.
- There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
- The students have to answer 5 full questions, selecting one full question from each module.

**The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper shall include questions from the practical component.**

- The minimum marks to be secured in CIE to appear for SEE shall be the 12 (40% of maximum marks-30) in the theory component and 08 (40% of maximum marks -20) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included. The maximum of 04/05 questions to be set from the practical component of IPCC, the total marks of all questions should not be more than the 20 marks.

SEE will be conducted for 100 marks and students shall secure 35% of the maximum marks to qualify in the SEE. Marks secured will be scaled down to 50.

#### **Suggested Learning Resources:**

##### **Text Books**

1. "JAVA The Complete Reference", Herbert Schildt, 7<sup>th</sup> Edition, Tata McGraw Hill, 2007.
2. "Data Structures with Java", John R Hubbard, 2<sup>nd</sup> edition, Schaum's Outlines.

##### **Reference Books**

1. "Fundamentals of OOP and Data Structures in Java", Richard Wiener, Lewis J Pinson, Cambridge University Press, 2000.
2. "Object Oriented Programming and Java", Danny Poo, Derek Kion, Swarnalatha Ashok, Springer, 2<sup>nd</sup> edition, 2007.
3. "Java Fundamentals", Herbert Schildt, Dale Skrien, McGraw Hill Education, 2017.
4. "Data Structures and Algorithms Made Easy in JAVA: Data Structure and Algorithmic Puzzles", Narasimha Karumanchi, CareerMonk Publications, Second edition, 2011.
5. "Data Structures & Algorithms in Java", Goodrich, Tamassia, Goldwasser, Universities Press; Second edition, 2005.

##### **Web links and Video Lectures (e-Resources):**

- VTU e-Shikshana Program
- VTU EDUSAT Program
- <https://www.youtube.com/watch?v=CFD9EFcNZTQ>
- <https://www.youtube.com/watch?v=grEKMHGyYns>

##### **Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

Quizzes, Assignments, Seminars

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**V Semester**

Computer Communication Networks			
Course Code	21EC53	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	3:0:0:1	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3
<b>Course objectives:</b> This course will enable students to: <div><div>1.</div><div>Understand the layering architecture of OSI reference model and TCP/IP protocol suite.</div></div> <div><div>2.</div><div>Understand the protocols associated with each layer.</div></div> <div><div>3.</div><div>Learn the different networking architectures and their representations.</div></div> <div><div>4.</div><div>Learn the functions and services associated with each layer.</div></div>			
<b>Teaching-Learning Process (General Instructions)</b> These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes. <div><div>1.</div><div>Lecture method (L): the traditional lecture method, or a different type of teaching method may be adopted to develop the outcomes.</div></div> <div><div>2.</div><div>Show Video/animation films to explain the functioning of various concepts in networking.</div></div> <div><div>3.</div><div>Encourage collaborative (Group) Learning in the class.</div></div> <div><div>4.</div><div>Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking .</div></div> <div><div>5.</div><div>Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyse information rather than simply recall it.</div></div> <div><div>6.</div><div>Demonstrate implementation of various protocols to help better understand the functioning of various concepts in networking.</div></div> <div><div>7.</div><div>Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.</div></div> <div><div>8.</div><div>Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.</div></div>			
Module-1			
<b>Introduction:</b> Data communication: Components, Data representation, Data flow, Networks: Network criteria, Physical Structures, Network types: LAN, WAN, Switching, The Internet. (1.1,1.2, 1.3 (1.3.1to 1.3.4 of Text)). <b>Network Models:</b> TCP/IP Protocol Suite: Layered Architecture, Layers in TCP/IP suite, Description of layers, Encapsulation and Decapsulation, Addressing, Multiplexing and Demultiplexing, The OSI Model: OSI Versus TCP/IP. (2.2, 2.3 of Text) <b>Data-Link Layer:</b> Introduction: Nodes and Links, Services, Two Categories' of link, Sublayers, Link Layer addressing: Types of addresses, ARP (9.1, 9.2 (9.2.1, 9.2.2))			
Teaching-Learning Process	Chalk and talk method, PowerPoint Presentation, YouTube videos, Animation of OSI and TCP-IP protocol suites, Example of ARP and RARP.		
	<b>Self-Study:</b> Internet standards and administration, <b>RBT Level:</b> L1, L2, L3		
Module-2			
Data Link Control (DLC) services: Framing, Flow and Error Control. (11.1 of Text) Media Access Control: Random Access: ALOHA, CSMA, CSMA/CD, CSMA/CA. (12.1 of Text). <b>Connecting Devices:</b> Hubs, Switches, Virtual LANs: Membership, Configuration, Communication between Switches, Advantages. (17.1,17.2 of text) <b>Wired and Wireless LANs:</b> Ethernet Protocol, Standard Ethernet. (13.1, 13.2 (13.2.1 to 13.2.5 of Text)			

Introduction to wireless LAN: Architectural Comparison, Characteristics, Access Control. (15.1 of Text)	
<b>Teaching-Learning Process</b>	Chalk and talk method, PowerPoint Presentation, YouTube videos, Animations showing Framing, CSMA, Connecting devices, Problems on ALOHA, CSMA, Framing and Standard ethernet. <b>Self-Study:</b> Fast Ethernet, Gigabit ethernet & IEEE802.11 wireless LANs <b>RBT Level:</b> L1, L2, L3
<b>Module-3</b>	
<p><b>Network Layer:</b> Introduction, Network Layer services: Packetizing, Routing and Forwarding, Other services, Packet Switching: Datagram Approach, Virtual Circuit Approach, IPV4 Addresses: Address Space, Classful Addressing, Classless Addressing, DHCP, Network Address Resolution (18.1(excluding 18.1.3), 18.2, 18.4 of Text)</p> <p><b>Network Layer Protocols:</b> Internet Protocol (IP): Datagram Format, Fragmentation, Options, Security of IPv4 Datagrams. (19.1of Text), IPv6 addressing and Protocol (22.1 and 22.2).</p> <p><b>Unicast Routing:</b> Introduction, Routing Algorithms: Distance Vector Routing, Link State Routing, Path vector routing. (20.1, 20.2 of Text)</p>	
<b>Teaching-Learning Process</b>	Chalk and talk method, PowerPoint Presentation, YouTube videos, Animation of DHCP, routing protocols, Numericals on Addressing, <b>Self-Study:</b> Network Layer performance, RIP, OSPF <b>RBT Level:</b> L1, L2, L3
<b>Module-4</b>	
<p><b>Transport Layer:</b> Introduction: Transport Layer Services, Connectionless and Connection oriented Protocols, Transport Layer Protocols: Simple protocol, Stop and wait protocol, Go-BackN Protocol, Selective repeat protocol, Piggybacking (23.1, 23.2.1, 23.2.2, 23.2.3, 23.2.4, 23.2.5 of Text)</p> <p><b>Transport-Layer Protocols in the Internet:</b> User Datagram Protocol: User Datagram, UDP Services, UDP Applications, Transmission Control L1, L2, L3 Protocol: TCP Services, TCP Features, Segment, Connection, State Transition diagram, Windows in TCP, Error control, TCP congestion control. (24.2, 24.3.1, 24.3.2, 24.3.3, 24.3.4, 24.3.6, 24.3.8, 24.3.9 of Text)</p> <p><b>*Note: Exclude FSMs for CIE and SEE</b></p>	
<b>Teaching-Learning Process</b>	Chalk and talk method, PowerPoint Presentation, YouTube videos, Animation/Implementation of Flow control protocols and TCP using simulators, <b>Self-Study:</b> Flow Control in TCP <b>RBT Level:</b> L1, L2, L3
<b>Module-5</b>	
<p><b>Application Layer:</b> Introduction: providing services, Application- layer paradigms, Standard Client – Server Protocols: Hyper Text Transfer Protocol, FTP: Two connections, Control Connection, Data Connection, Electronic Mail: Architecture, Domain Name system: Name space, DNS in internet, Resolution, DNS Messages, Registrars, DDNS, security of DNS. (25.1, 26.1.2, 26.2, 26.3, 26.6 of Text) Quality of Service (30.1, 30.2.) Network Security (31.1)</p>	
<b>Teaching-Learning Process</b>	Chalk and talk method, PowerPoint Presentation, YouTube videos, Animation/Implementation of HTTP, FTP, DNS using network simulators, <b>Self Study:</b> WWW , TELNET <b>RBT Level:</b> L1, L2, L3
<p><b>Course outcomes (Course Skill Set)</b></p> <p>At the end of the course the student will be able to:</p> <ol style="list-style-type: none"> <li>1. Understand the concepts of networking thoroughly.</li> <li>2. Identify the protocols and services of different layers.</li> <li>3. Distinguish the basic network configurations and standards associated with each network.</li> <li>4. Discuss and analyse the various applications that can be implemented on networks.</li> </ol>	
<p><b>Assessment Details (both CIE and SEE)</b></p> <p>The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each</p>	

subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous Internal Evaluation:**

Three Unit Tests each of **20 Marks (duration 01 hour)**

1. First test at the end of 5<sup>th</sup> week of the semester
2. Second test at the end of the 10<sup>th</sup> week of the semester
3. Third test at the end of the 15<sup>th</sup> week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4<sup>th</sup> week of the semester
5. Second assignment at the end of 9<sup>th</sup> week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks (duration 01 hours)**

6. At the end of the 13<sup>th</sup> week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

**CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours**)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module.

**Suggested Learning Resources:**

**Text Books:**

Forouzan, "Data Communications and Networking", 5<sup>th</sup> Edition, McGraw Hill, 2013, ISBN: 1-25-906475-3.

**Reference Books:**

1. James J Kurose, Keith W Ross, "Computer Networks", Pearson Education.
2. Wayne Tomasi, "Introduction to Data Communication and Networking", Pearson India, 1<sup>st</sup> edition.
3. Andrew Tannenbaum, "Computer Networks", Prentice Hall.
4. William Stallings, "Data and Computer Communications", Prentice Hall.

**Web links and Video Lectures (e-Resources)**

- <https://nptel.ac.in/courses/106105183>.
- TCP/IP Tutorial and Technical Overview, (IBM Redbook) - Download From <http://www.redbooks.ibm.com/abstracts/gg243376.html>
- TCP/IP Guide, Charles M Kozierok, Available Online - <http://www.tcpipguide.com/>
- Request for Comments (RFC) - IETF - <http://www.ietf.org/rfc.html>
- <https://cosmolearning.org/courses/computer-networks-524/video-lectures/>
- [https://www.eecis.udel.edu/~bohacek/videoLectures/ComputerNetworking/ComputerNetworking\\_v2.html](https://www.eecis.udel.edu/~bohacek/videoLectures/ComputerNetworking/ComputerNetworking_v2.html)

**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

- Implementation of simple networks and various networking protocols and algorithms using simulators like NCTUns / CISCO packet tracer and measurement of various parameters using WireShark
- Implementation of simple networks and various networking protocols and algorithms in C/C++/Python

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**V Semester**

Microwave Theory and Antennas			
Course Code	21EC54	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	3:0:0:1	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3
<b>Course objectives:</b> This course will enable students to : <ul style="list-style-type: none"><li>Describe the microwave properties and its transmission media.</li><li>Describe the microwave devices for several applications.</li><li>Understand the basic concepts of antenna theory.</li><li>Identify antenna types for specific applications.</li></ul>			
<b>Teaching-Learning Process (General Instructions)</b> <p>These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.</p> <ol style="list-style-type: none"><li>Using videos for demonstration of the fundamental principles to students for better understanding of concepts.</li><li>Demonstration of microwave devices and Antennas in the lab environment where students can study them in real time.</li></ol>			
Module-1			
<b>Microwave Sources:</b> Introduction, Gunn Diode (Text 2: 7.1,7.1.1,7.1.2) <b>Microwave transmission lines:</b> Microwave frequencies, Microwave devices, Microwave systems. Transmission line equations and solutions, Reflection Coefficient and Transmission Coefficient. Standing wave and standing wave ratio. Smith chart, Single stub matching. Text 2: 0.1, 0.2, 0.3, 3.1, 3.2, 3.3, 3.5, 3.6 (except double stub matching)			
<b>Teaching-Learning Process</b>	Chalk and Talk would be helpful for the quantitative analysis. Videos of the Basic principles of the devices would help students to grasp better. <b>RBT Level:</b> L1, L2, L3		
Module-2			
<b>Microwave Network Theory:</b> Introduction, S matrix representation of multi-port networks (Text 1: 6.1, 6.3, 6.3.1, 6.3.2) <b>Microwave passive devices:</b> Coaxial connectors and Adapters, Attenuators, Phase shifters, waveguide Tees, Magic Tee, Circulator, Isolator. (Text 1: 6.4.2, 6.4.14, 6.4.15, 6.4.16, 6.4.17 A, B)			
<b>Teaching-Learning Process</b>	Chalk and talk method, Power point presentation <b>RBT Level:</b> L1, L2, L3		
Module-3			
<b>Strip Lines:</b> Introduction, Microstrip lines, Parallel Strip lines (Text 2: 11.1,11.2) <b>Antenna Basics:</b> Introduction, Basic Antenna Parameters, Patterns, Beam Area, Radiation Intensity, Beam efficiency, Directivity and Gain, Antenna Aperture Effective height, Bandwidth, Radio communication Link, Antenna Field Zones (Text 3: 2.1-2.7, 2.9-2.11, 2.13).			
<b>Teaching-Learning Process</b>	Chalk and talk method, Power point presentation and videos. <b>RBT Level:</b> L1, L2, L3		



<b>Module-4</b>	
<p><b>Point sources and arrays:</b> Introduction, Point Sources, Power patterns, Power theorem, Radiation Intensity, Arrays of 2 isotropic point sources, Pattern multiplication, Linear arrays of n Isotropic sources of equal amplitude and Spacing. (Text 3: 5.1-5.6, 5.9, 5.13)</p> <p><b>Electric Dipole:</b> Introduction, Short Electric dipole, Fields of a short dipole. Radiation resistance of a short dipole. Thin linear antenna (field analysis). (Text 3: 6.1-6.5)</p>	
<b>Teaching-Learning Process</b>	Chalk and talk method, Power point presentation <b>RBT Level:</b> L1, L2, L3
<b>Module-5</b>	
<p><b>Loop and Horn antenna:</b> Introduction: Small loop, Comparison of far fields of small loop and Short dipole. Radiation resistance of small loop, Horn Antennas, Rectangular antennas. (Text 3: 7.1,7.2, 7.4, 7.6, 7.7, 7.8, 7.19, 7.20)</p> <p><b>Antenna Types:</b> The Helix geometry, Helix modes, Practical design consideration for mono-filar axial mode Helical Antenna, Yagi Uda array, Parabolic Reflector (Text 3: 8.3, 8.4, 8.5, 8.8, 9.5)</p>	
<b>Teaching-Learning Process</b>	Chalk and talk method, Power point presentation <b>RBT Level:</b> L1, L2, L3
<p><b>Course outcome (Course Skill Set)</b></p> <p>At the end of the course the student will be able to:</p> <ol style="list-style-type: none"> <li>1. Describe the use and advantages of microwave transmission</li> <li>2. Analyze various parameters related to transmission lines.</li> <li>3. Identify microwave devices for several applications.</li> <li>4. Analyze various antenna parameters and their significance in building the RF system.</li> <li>5. Identify various antenna configurations for suitable applications.</li> </ol>	
<p><b>Assessment Details (both CIE and SEE)</b></p> <p>The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.</p> <p><b>Continuous Internal Evaluation:</b></p> <p>Three Unit Tests each of <b>20 Marks (duration 01 hour)</b></p> <ol style="list-style-type: none"> <li>1. First test at the end of 5<sup>th</sup> week of the semester</li> <li>2. Second test at the end of the 10<sup>th</sup> week of the semester</li> <li>3. Third test at the end of the 15<sup>th</sup> week of the semester</li> </ol> <p>Two assignments each of <b>10 Marks</b></p> <ol style="list-style-type: none"> <li>4. First assignment at the end of 4<sup>th</sup> week of the semester</li> <li>5. Second assignment at the end of 9<sup>th</sup> week of the semester</li> </ol> <p>Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for <b>20 Marks (duration 01 hours)</b></p> <ol style="list-style-type: none"> <li>6. At the end of the 13<sup>th</sup> week of the semester</li> </ol> <p>The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be <b>scaled down to 50 marks</b></p> <p>(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).</p>	

**CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours**)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module.

**Suggested Learning Resources:**

**Text Books:**

1. Microwave Engineering -Annapurna Das, Sisir K Das, TMH Publication, 2<sup>nd</sup> Edition, 2010.
2. Microwave Devices and Circuits – Samuel Y Liao, Pearson Education.
3. Antennas and Wave Propagation -John D Krauss, Ronald J Marhefka, Ahmad S Khan, 4<sup>th</sup> Edition, McGraw Hill Education, 2013.

**Reference Books:**

1. Microwave Engineering -David M Pozar, John Wiley India Pvt Ltd., Pvt Ltd., 3<sup>rd</sup> edition, 2008.
2. Microwave Engineering-Sushrut Das, Oxford Higher Education, 2<sup>nd</sup> Edn, 2015.
3. Antennas and Wave Propagation- Harish and Sachidananda, Oxford University Press, 2007.

**Web links and Video Lectures (e-Resources)**

- Nptel Videos and Lectures
- [https://www.tutorialspoint.com/antenna\\_theory/antenna\\_theory\\_horn.html](https://www.tutorialspoint.com/antenna_theory/antenna_theory_horn.html)
- <http://www.antenna-theory.com/antennas/smallLoop.php>

**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

- Lab based demos for the devices can be done in the form of experiments.
- Mini Projects can be given to students involving design of microwave devices and Antennas.

**V Semester**

Communication Lab II			
Course Code	21ECL55	CIE Marks	50
Teaching Hours/Week (L: T: P: S)	0:0:2:0	SEE Marks	50
Credits	1	Exam Hours	3
<b>Course objectives:</b> This laboratory course enables students to <ul style="list-style-type: none"><li>• Design and demonstrate communication circuits for different digital modulation techniques.</li><li>• To simulate Source coding Algorithms using C/C++/ MATLAB code.</li><li>• To simulate Error correcting and detecting codes using C/C++/ MATLAB code.</li><li>• Simulate the networking concepts and protocols using C/C++/ Network simulation tool.</li><li>• Understand entropies and mutual information of different communication channels.</li></ul>			
Sl.No.	Experiments		
Implement the following using discrete components			
1	FSK generation and detection		
2	PSK generation and detection		
3	DPSK Transmitter and receiver		
4	QPSK Transmitter and Receiver		
Implement the following in C/C++/MATLAB/Scilab/Python or any other Suitable software			
5	Write a program to encode binary data using Huffman code and decode it.		
6	Write a program to encode binary data using a (7,4) Hamming code and decode it.		
7	Write a program to encode binary data using a ((3,1,2)/suitably designed) Convolution code and decode it.		
8	For a given data, use CRC-CCITT polynomial to obtain the CRC code. Verify the program for the cases    a) Without error    b) With error		
Implement the following algorithms in C/C++/MATLAB/Network simulator			
9	Write a program for congestion control using leaky bucket algorithm.		
10	Write a program for distance vector algorithm to find suitable path for transmission.		
11	Write a program for flow control using sliding window protocols.		
12	Configure a simple network (Bus/star) topology using simulation software <b>OR</b> Configure a simple network (Ring/Mesh) topology using simulation software.		
Demonstration Experiments (For CIE)			
13	Configure and simulate simple Wireless Local Area network.		
14	Simulate the BER performance of (2, 1, 3) binary convolutional code with generator sequences $g(1) = (1\ 0\ 1\ 1)$ and $g(2) = (1\ 1\ 1\ 1)$ on AWGN channel. Use QPSK modulation scheme. Channel decoding is to be performed through Viterbi decoding. Plot the bit error rate versus SNR (dB), i.e. $P_{e,b}$ versus $E_b/N_0$ . Consider binary input vector of size 3 lakh bits. Also find the coding gain.		

15	<p>Simulate the BER performance of (7, 4) Hamming code on AWGN channel. Use QPSK modulation scheme. Channel decoding is to be performed through maximum-likelihood decoding. Plot the bit error rate versus SNR (dB), i.e. <math>P_{e,b}</math> versus <math>E_b/N_0</math>. Consider binary input vector of size 5 lakh bits. Use the following parity check matrix for the (7, 4) Hamming code. Also find the coding gain.</p> $H = \begin{bmatrix} 1 & 0 & 0 & 1 & 1 & 1 & 0 \\ 0 & 1 & 0 & 0 & 1 & 1 & 1 \\ 0 & 0 & 1 & 1 & 1 & 0 & 1 \end{bmatrix}$
16	<p>Simulate the BER performance of 1/3 Turbo code. Turbo encoder uses two recursive systematic encoders with <math>G(D) = \left[ 1, \frac{1+D^4}{1+D+D^2+D^3+D^4} \right]</math> and pseudo-random interleaver. Use QPSK modulation scheme. Channel decoding is to be performed through maximum a-posteriori (MAP) decoding algorithm. Plot the bit error rate versus SNR (dB), i.e. <math>P_{e,b}</math> versus <math>E_b/N_0</math>. Consider binary input vector of size of around 3 lakh bits and the block length as 10384 bits. Also find the coding gain.</p>

### Course outcomes (Course Skill Set):

On the completion of this laboratory course, the students will be able to:

1. Design and test the digital modulation circuits and display the waveforms.
2. To Implement the source coding algorithm using C/C++/ MATLAB code.
3. To Implement the Error Control coding algorithms using C/C++/ MATLAB code.
4. Illustrate the operations of networking concepts and protocols using C programming and network simulators.

### Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

### Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled down to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8<sup>th</sup> week of the semester and the second test shall be conducted after the 14<sup>th</sup> week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

### Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners).

Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours.

Rubrics suggested in Annexure-II of Regulation book

**Suggested Learning Resources:**

1. Simon Haykin, "Digital Communication Systems", John Wiley & sons, First Edition, 2014, ISBN 978-0-471-64735-5.
2. K Sam Shanmugam, "Digital and analog communication systems", John Wiley India Pvt. Ltd, 1996.
3. Forouzan, "Data Communications and Networking", 5<sup>th</sup> Edition, McGraw Hill, 2013, ISBN: 1-25-906475-3.

**VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI**  
**B.E: Electronics & Communication Engineering / B.E: Electronics & Telecommunication Engineering**  
**NEP, Outcome Based Education (OBE) and Choice Based Credit System (CBCS)**  
**(Effective from the academic year 2021 – 22)**

**V Semester**

IoT (Internet of Things) Lab			
Course Code	21EC581	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	0:0:2:0	SEE Marks	50
Credits	1	Exam Hours	100
<b>Course objectives:</b> <ul style="list-style-type: none"><li>To impart necessary and practical knowledge of components of Internet of Things</li><li>To develop skills required to build real-life IoT based projects.</li></ul>			
<b>Sl.No</b>	<b>Experiments</b>		
1	i) To interface LED/Buzzer with Arduino/Raspberry Pi and write a program to 'turn ON' LED for 1 sec after every 2 seconds. ii) To interface Push button/Digital sensor (IR/LDR) with Arduino/Raspberry Pi and write a program to 'turn ON' LED when push button is pressed or at sensor detection.		
2	i) To interface DHT11 sensor with Arduino/Raspberry Pi and write a program to print temperature and humidity readings. ii) To interface OLED with Arduino/Raspberry Pi and write a program to print temperature and humidity readings on it.		
3	To interface motor using relay with Arduino/Raspberry Pi and write a program to 'turn ON' motor when push button is pressed.		
4	To interface Bluetooth with Arduino/Raspberry Pi and write a program to send sensor data to smartphone using Bluetooth.		
5	To interface Bluetooth with Arduino/Raspberry Pi and write a program to turn LED ON/OFF when '1'/'0' is received from smartphone using Bluetooth.		
6	Write a program on Arduino/Raspberry Pi to upload temperature and humidity data to thingspeak cloud.		
7	Write a program on Arduino/Raspberry Pi to retrieve temperature and humidity data from thingspeak cloud.		
8	To install MySQL database on Raspberry Pi and perform basic SQL queries.		
9	Write a program on Arduino/Raspberry Pi to publish temperature data to MQTT broker.		
10	Write a program to create UDP server on Arduino/Raspberry Pi and respond with humidity data to UDP client when requested.		
11	Write a program to create TCP server on Arduino/Raspberry Pi and respond with humidity data to TCP client when requested.		
12	Write a program on Arduino/Raspberry Pi to subscribe to MQTT broker for temperature data and print it.		
<b>Course outcomes (Course Skill Set):</b> At the end of the course the student will be able to: <ol style="list-style-type: none"><li>Understand internet of Things and its hardware and software components</li><li>Interface I/O devices, sensors &amp; communication modules</li><li>Remotely monitor data and control devices</li><li>Develop real life IoT based projects</li></ol>			
<b>Assessment Details (both CIE and SEE)</b> The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).			

**Continuous Internal Evaluation (CIE):**

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled down to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8<sup>th</sup> week of the semester and the second test shall be conducted after the 14<sup>th</sup> week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

**Semester End Evaluation (SEE):**

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours

Rubrics suggested in Annexure-II of Regulation book

**Suggested Learning Resources:**

1. Vijay Madiseti, Arshdeep Bahga, Internet of Things. "A Hands on Approach", University Press
2. Dr. SRN Reddy, Rachit Thukral and Manasi Mishra, "Introduction to Internet of Things: A practical Approach", ETI Labs
3. Pethuru Raj and Anupama C Raman, "The Internet of Things: Enabling Technologies, Platforms, and Use Cases", CRC Press
4. Jeeva Jose, "Internet of Things", Khanna Publishing House, Delhi
5. Adrian McEwen, "Designing the Internet of Things", Wiley
6. Raj Kamal, "Internet of Things: Architecture and Design", McGraw Hill

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(Effective from the academic year 2021 – 22)

## V Semester

Communication Simulink Toolbox			
Course Code	21EC582	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	0:0:2:0	SEE Marks	50
Credits	1	Exam Hours	100
<b>Course objectives:</b> <ul style="list-style-type: none"><li>To impart knowledge of simulation software in digital communications</li><li>To develop skills required to build and analyze the performance of various simulated communication systems under different conditions</li></ul>			
<b>Sl. No.</b>	<b>Experiments</b>		
1	Modulation & demodulation of a random binary data stream using 16 – QAM.		
2	Bit error rate (BER) improvement using Pulse Shaping on 16 – QAM signal. (Use forward error correction (FEC) coding.)		
3	Perform OFDM modulation and obtain time domain and frequency domain plots to show a low-rate signal, a high-rate signal, and a frequency selective multipath channel response.		
4	(a) Simulate basic OFDM with no cyclic prefix. (b) Perform Equalization, Convolution, and Cyclic Prefix Addition on basic OFDM.		
5	OFDM with FFT Based Oversampling - Modify an OFDM+ Cyclic Prefix signal to efficiently output an oversampled waveform from the OFDM modulator.		
6	Simulate a basic communication system in which the signal is first QPSK modulated and then subjected to Orthogonal Frequency Division Multiplexing (OFDM).		
7	Obtain the scatter plots & eye diagrams of a QPSK signal to visualize the signal behaviour in presence of AWGN.		
8	(a) Generate a multiband signal using the Communications Toolbox. (b) Random noise generation using Simulink & display histogram plots of Gaussian, Rayleigh, Rician, and Uniform noise.		
9	QPSK Transmitter and Receiver in Simulink.		
10	Multipath Fading Channel in Simulink – For example: Simulate QPSK transmission over a <ul style="list-style-type: none"><li>• multipath Rayleigh fading channel and</li><li>• a multipath Rician fading channel.</li></ul>		
11	Adjacent and Co-Channel Interference using Simulink. <ul style="list-style-type: none"><li>• Use PSK-modulated signals to show the effects of adjacent and co-channel interference on a transmitted signal.</li></ul>		
12	Modulation Classification with Deep Learning <ul style="list-style-type: none"><li>• Predict Modulation Type Using CNN</li></ul>		
<b>Course outcomes (Course Skill Set):</b> <p>At the end of the course the student will be able to:</p> <ol style="list-style-type: none"><li>1. Perform sampling, aliasing, filtering, and quadrature modulation through simulation.</li><li>2. Plot signal space representation of digital modulation techniques.</li><li>3. Design and implement a pulse shape and matched filter to avoid inter-symbol interference and maximize receiver SNR.</li><li>4. Demonstrate advanced wireless communication techniques like Multipath fading, CCI etc. and model the same using MATLAB / Simulink.</li></ol>			
<b>Assessment Details (both CIE and SEE)</b> <p>The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each</p>			



course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

**Continuous Internal Evaluation (CIE):**

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled down to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8<sup>th</sup> week of the semester and the second test shall be conducted after the 14<sup>th</sup> week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

**Semester End Evaluation (SEE):**

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours

Rubrics suggested in Annexure-II of Regulation book

**Suggested Learning Resources:**

1. Communication Toolbox – Examples (<https://in.mathworks.com/>)
2. "Digital Communication Laboratory" Courseware by Professor Lee C Potter, Dr. Yang Yang, Electrical and Computer Engineering, The Ohio State University.

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**V Semester**

Antenna Design & Testing			
Course Code	21EC583	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	0:0: 2 :0	SEE Marks	50
Credits	1	Exam Hours	100
<b>Course objectives:</b> <ul style="list-style-type: none"><li>To understand the various antenna parameters.</li><li>Conduct experiments to study the Radiation pattern of Antennas.</li><li>Design different types of antenna arrays and study the pattern characteristics (MATLAB)</li><li>Design of MMIC antennas like Patch Antenna and study the characteristics.</li></ul>			
<b>Sl.No</b>	<b>Experiments</b>		
1	To obtain the radiation pattern of a Yagi-Uda Antenna array and calculate its directivity.		
2	To obtain the radiation pattern of a Dipole Antenna array and calculate its directivity.		
3	To calculate the aperture of a Dipole Antenna.		
4	To obtain the near and far fields of a given antenna and compare the fields.		
5	To obtain the Radiation pattern of a microstrip antenna.		
6	To obtain the resonant frequency of a Yagi-Uda /Dipole antenna.		
7	To obtain the bandwidth of a given Antenna.		
8	Plot 2-D and 3-D radiation pattern of omnidirectional antenna using MATLAB.		
9	Design and implementation of a broadside array using MATLAB.		
10	Design and implementation of an endfire array using MATLAB.		
<b>Demonstration Experiments ( For CIE )</b>			
11	Design of a Patch Antenna using HFSS Software.		
12	Design of a dipole Antenna using HFSS Software.		
<b>Course outcomes (Course Skill Set):</b> At the end of the course the student will be able to: <ul style="list-style-type: none"><li>Analyze the radiation pattern and characteristics of antenna</li><li>Ability to design various antenna</li><li>Ability to use different software tools to study antenna characteristics</li><li>Analyze radiation pattern of linear array antennas</li></ul>			
<b>Assessment Details (both CIE and SEE)</b>  The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).  <b>Continuous Internal Evaluation (CIE):</b> CIE marks for the practical course is <b>50 Marks</b> . The split-up of CIE marks for record/ journal and test are in the ratio <b>60:40</b> . <ul style="list-style-type: none"><li>Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed</li></ul>			

by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.

- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled down to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8<sup>th</sup> week of the semester and the second test shall be conducted after the 14<sup>th</sup> week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

#### **Semester End Evaluation (SEE):**

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours

Rubrics suggested in Annexure-II of Regulation book

#### **Suggested Learning Resources:**

1. Antennas and Wave Propagation -John D Krauss, Ronald J Marhefka, Ahmad S Khan, 4<sup>th</sup> Edition, McGraw Hill Education, 2013.
2. <https://www.mathworks.com/help/antenna/>
3. Help and demo files of the HFSS and MATLAB software

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**(Effective from the academic year 2021 – 22)**

**V Semester**

Microwaves Toolbox			
Course Code	21EC584	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	0:0:2:0	SEE Marks	50
Credits	1	Exam Hours	100
<b>Course objectives:</b> <ul style="list-style-type: none"><li>• Identification of microwave components/devices.</li><li>• Study basic principles of operation of microwave devices/ components</li></ul>			
<b>Sl.No</b>	<b>Experiments</b>		
1	V- I Characteristics of Gunn-diode.		
2	Study of characteristics of Magic Tee.		
3	Coupling and Isolation characteristics of microstrip directional coupler.		
4	Determination of power division of microstrip power divider.		
5	Determination of resonance characteristics of microstrip ring resonator and computation of dielectric constant of the substrate.		
6	Measurement of frequency, guide wavelength, power and attenuation in a microwave Test bench.		
7	Study of characteristics of E plane Tee / H plane Tee.		
8	To measure unknown impedance using Smith chart through test bench setup.		
9	Measurement of VSWR and reflection coefficient and attenuation in a microwave test bench setup.		
10	Study propagation of wave using rectangular waveguide using MATLAB.		
11	Study of impedance matching using MATLAB.		
12	To calculate phase and group velocity using MATLAB.		
<b>Course outcomes (Course Skill Set):</b> At the end of the course the student will be able to: <ul style="list-style-type: none"><li>1. Demonstrate the characteristics of microwave sources.</li><li>2. Demonstrate the characteristics of directional coupler</li><li>3. Study of microwave measurement procedure.</li><li>4. Apply MATLAB toolbox for study of microwaves phenomena.</li></ul>			
<b>Assessment Details (both CIE and SEE)</b>  The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE). <b>Continuous Internal Evaluation (CIE):</b> CIE marks for the practical course is <b>50 Marks</b> . The split-up of CIE marks for record/ journal and test are in the ratio <b>60:40</b> . <ul style="list-style-type: none"><li>• Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.</li></ul>			

- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled down to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8<sup>th</sup> week of the semester and the second test shall be conducted after the 14<sup>th</sup> week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

#### **Semester End Evaluation (SEE):**

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours

Rubrics suggested in Annexure-II of Regulation book

#### **Suggested Learning Resources:**

##### **MATLAB**

1. Microwave Engineering -Annapurna Das, Sisir K Das, TMH Publication, 2<sup>nd</sup> Edition, 2010.
2. Antennas and Wave Propagation -John D Krauss, Ronald J Marhefka, Ahmad S Khan, 4<sup>th</sup> Edition, McGraw Hill Education, 2013.
3. <https://www.mathworks.com/help/antenna>
4. <https://www.mathworks.com/help/antenna/ref/waveguide.html>

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**VI Semester**

Computer Organization & ARM Microcontrollers			
Course Code	21EC62	CIE Marks	50
Teaching Hours/Week (L: T: P: S)	(3:0:2:0)	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory + 12 Lab slots	Total Marks	100
Credits	04	Exam Hours	03
<b>Course objectives: This course will enable students to:</b> <div>1. Explain the basic organization of a computer system.</div> <div>2. Demonstrate functioning of different sub systems, such as processor, Input/output, and memory.</div> <div>3. Describe the architectural features and instructions of 32-bit microcontroller ARM Cortex M3.</div> <div>4. Apply the knowledge gained for Programming ARM Cortex M3 for different applications.</div> <div>5. Understand the basic hardware components and their selection method based on the characteristics and attributes of an embedded system.</div>			
<b>Teaching-Learning Process (General Instructions)</b> These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes. <div><div>Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.</div><div>Encourage collaborative (Group) Learning in the class.</div><div>Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking.</div><div>Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.</div><div>Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.</div><div>Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.</div><div>Give Programming Assignments.</div></div>			
<b>Module-1</b>			
<b>Basic Structure of Computers:</b> Basic Operational Concepts, Bus Structures, Performance – Processor Clock, Basic Performance Equation, Clock Rate, Performance Measurement. Text Book 1: Chapter 1 – 1.3, 1.4, 1.6 (1.6.1-1.6.4, 1.6.7), Chapter 2 – 2.2 to 2.10 <b>Input/Output Organization:</b> Accessing I/O Devices, Interrupts – Interrupt Hardware, Direct Memory Access, Buses, Interface Circuits, Standard I/O Interfaces – PCI Bus, SCSI Bus, USB. Text Book 1: Chapter 4 – 4.1, 4.2, 4.4, 4.5, 4.6, 4.7			
<b>Teaching-Learning Process</b>	Chalk and Talk, YouTube videos <b>RBT Level:</b> L1, L2, L3		
<b>Module-2</b>			
<b>Memory System:</b> Basic Concepts, Semiconductor RAM Memories, Read Only Memories, Speed, Size, and Cost, Cache Memories – Mapping Functions, Replacement Algorithms, Performance Considerations. Text book 1: Chapter 5 – 5.1 to 5.4, 5.5 (5.5.1, 5.5.2), 5.6 <b>Basic Processing Unit:</b> Some Fundamental Concepts, Execution of a Complete Instruction, Multiple Bus Organization, Hard-wired Control, Micro programmed Control. Basic concepts of pipelining, Text book 1: Chapter7, Chapter 8 – 8.1			

<b>Teaching-Learning Process</b>	Chalk and Talk, YouTube videos <b>RBT Level:</b> L1, L2, L3
<b>Module-3</b>	
<b>ARM Embedded Systems:</b> Introduction, RISC design philosophy, ARM design philosophy, Embedded system hardware – AMBA bus protocol, ARM bus technology, Memory, Peripherals, Embedded system software – Initialization (BOOT) code, Operating System, Applications. ARM Processor Fundamentals, ARM core dataflow model, registers, current program status register, Pipeline, Exceptions, Interrupts and Vector Table, Core extensions. Text book 2: Chapter 1, 2	
<b>Teaching-Learning Process</b>	Chalk and Talk, YouTube videos <b>RBT Level:</b> L1, L2, L3
<b>Module-4</b>	
<b>Introduction to the ARM Instruction set:</b> Introduction, Data processing instructions, Load - Store instruction, Software interrupt instructions, Program status register instructions, Loading constants, ARMv5E extensions, Conditional Execution. Text book 2: Chapter 3	
<b>Teaching-Learning Process</b>	Chalk and Talk, Power point presentations, Programming assignments <b>RBT Level:</b> L1, L2, L3
<b>Module-5</b>	
<b>Introduction to the THUMB instruction set:</b> Introduction, THUMB register usage, ARM – THUMB interworking, Other branch instructions, Data processing instructions, Stack instructions, Software interrupt instructions. <b>Efficient C Programming:</b> Overview of C Compilers and optimization, Basic C Data types, C looping structures. Text book 2: Chapter 4, 5	
<b>Teaching-Learning Process</b>	Chalk and Talk, Power point presentations, Programming assignments <b>RBT Level:</b> L1, L2, L3

<b>PRACTICAL COMPONENT OF IPCC</b>	
Conduct the following experiments by writing Assembly Language Program (ALP) using ARM Cortex M3 Registers using an evaluation board/simulator and the required software tool.	
Sl.No	Experiments
1	Write an ALP to i) multiply two 16-bit binary numbers. ii) add two 64-bit numbers.
2	Write an ALP to find the sum of first 10 integer numbers.
3	Write an ALP to find factorial of a number.
4	Write an ALP to add an array of 16-bit numbers and store the 32-bit result in internal RAM.
5	Write an ALP to find the square of a number (1 to 10) using look-up table.
6	Write an ALP to find the largest/smallest number in an array of 32 numbers.
7	Write an ALP to arrange a series of 32-bit numbers in ascending/descending order.
8	i) Write an ALP to count the number of ones and zeros in two consecutive memory locations. ii) Write an ALP to Scan a series of 32-bit numbers to find how many are negative.

### Demonstration Experiments (For CIE only not for SEE)

Conduct the following experiments on an ARM CORTEX M3 evaluation board using evaluation version of Embedded 'C' & Keil  $\mu$ vision-4 tool/compiler.

9	Interface a Stepper motor and rotate it in clockwise and anti-clockwise direction.
10	Interface a DAC and generate Triangular and Square waveforms.
11	Display the Hex digits 0 to F on a 7-segment LED interface, with a suitable delay in between.
12	Interface a simple Switch and display its status through Relay, Buzzer and LED.

### Course Outcomes

At the end of the course the student will be able to:

1. Explain the basic organization of a computer system.
2. Demonstrate functioning of different sub systems, such as processor, Input/output, and memory.
3. Describe the architectural features and instructions of 32-bit microcontroller ARM Cortex M3.
4. Apply the knowledge gained for Programming ARM Cortex M3 for different applications.

### Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together

### CIE for the theory component of IPCC

Two Tests each of **20 Marks (duration 01 hour)**

- First test at the end of 5<sup>th</sup> week of the semester
- Second test at the end of the 10<sup>th</sup> week of the semester

Two assignments each of **10 Marks**

- First assignment at the end of 4<sup>th</sup> week of the semester
- Second assignment at the end of 9<sup>th</sup> week of the semester

Scaled-down marks of two tests and two assignments added will be CIE marks for the theory component of IPCC for **30 marks**.

### CIE for the practical component of IPCC

- On completion of every experiment/program in the laboratory, the students shall be evaluated and marks shall be awarded on the same day. The **15 marks** are for conducting the experiment and preparation of the laboratory record, the other **05 marks shall be for the test** conducted at the end of the semester.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to 15 marks.
- The laboratory test (**duration 03 hours**) at the end of the 15<sup>th</sup> week of the semester /after completion of all the experiments (whichever is early) shall be conducted for 50 marks and scaled down to 05 marks.

Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **20 marks**.



**SEE for IPCC**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (duration 03 hours)

- The question paper will have ten questions. Each question is set for 20 marks.
- There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
- The students have to answer 5 full questions, selecting one full question from each module.

**The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper shall include questions from the practical component.**

- The minimum marks to be secured in CIE to appear for SEE shall be the 12 (40% of maximum marks-30) in the theory component and 08 (40% of maximum marks -20) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included. The maximum of 04/05 questions to be set from the practical component of IPCC, the total marks of all questions should not be more than the 20 marks.

SEE will be conducted for 100 marks and students shall secure 35% of the maximum marks to qualify in the SEE. Marks secured will be scaled down to 50.

**Suggested Learning Resources:****Textbooks**

1. Carl Hamacher, Zvonko Vranesic, Safwat Zaky, Computer Organization, 5<sup>th</sup> Edition, Tata McGraw Hill, 2002. (Listed topics only from Chapters 1, 2, 4, 5, 8).
2. Andrew N Sloss, Dominic System and Chris Wright, "ARM System Developers Guide", Elsevier, Morgan Kaufman publisher, 1<sup>st</sup> Edition, 2008.

**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

Programming Assignments / Mini Projects can be given to improve programming skills

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**VI Semester**

Wireless and Cellular Communication			
Course Code	21TC63	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	3:0:0:1	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3
<b>Course objectives:</b> This course aims to develop: <ul style="list-style-type: none"><li>• An understanding on functioning of wireless communication system and evolution of different wireless communication systems and standards.</li><li>• An ability to compare recent technologies used for wireless communication.</li><li>• An ability to explain the architecture, functioning, protocols, capabilities and application of various wireless communication networks.</li><li>• An ability to explain multiple access techniques for Wireless Communication.</li><li>• An ability to evaluate design challenges, constraints and security issues associated with wireless systems.</li></ul>			
<b>Teaching-Learning Process (General Instructions)</b> The sample strategies, which the teacher can use to accelerate the attainment of the various course outcomes are listed in the following: <ol style="list-style-type: none"><li>1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.</li><li>2. Arrange visits to nearby PSUs and industries.</li><li>3. Show Video/animation films to explain the functioning of various fabrication &amp; testing techniques.</li><li>4. Encourage collaborative (Group) Learning in the class</li><li>5. Topics will be introduced in multiple representations.</li><li>6. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.</li></ol>			
Module-1			
<b>Overview of Wireless Communications:</b> History & Current Wireless Systems, The wireless spectrum & Standards. [Text Book 1 – Chapter 1 – 1.1, 1.4, 1.5, 1.6] <b>Cellular Systems and Infrastructure-Based Wireless Networks:</b> Cellular System Design, Frequency Reuse in Cellular Systems, Dynamic Resource Allocation in Cellular Systems, Area Spectral Efficiency, Interference Model, Power Control Impact on Interference, Interference Mitigation. [Text Book 1 – Chapter 15]			
Teaching-Learning Process	Chalk and talk method, PowerPoint Presentation, YouTube videos <b>RBT Level:</b> L1, L2, L3		
Module-2			
<b>Introduction to 3G/4G Wireless Communications:</b> Introduction, 2G, 3G, 4G Wireless Standards, Overview of Cellular Service Progression. <b>Principles of Wireless Communications:</b> The Wireless Communication Environment, Modelling of Wireless Systems, System Model for Narrowband Signals, Rayleigh Fading Wireless Channel, BER Performance of Wireless Systems, Intuition for BER in a Fading Channel, Channel Estimation in Wireless Systems, Diversity in wireless systems, Multiple Receive Antenna System Model, Symbol Detection in Multiple Antenna Systems. BER in Multi-Antenna Wireless Systems. Diversity Order.			

[Text Book 2 – Chapter 1 & Chapter 3]	
<b>Teaching-Learning Process</b>	Chalk and talk method, Power point presentation <b>RBT Level:</b> L1, L2, L3
<b>Module-3</b>	
<b>The Wireless Channel:</b> Basics of Wireless Channel Modelling, Average Delay Spread in Outdoor Cellular Channels, Coherence BW in Wireless Communications, Relation between ISI & Coherence BW, Doppler Fading in Wireless Systems, Doppler impact on a Wireless Channel, Coherence Time of the Wireless Channel, Jakes Model for Wireless Channel Correlation, Implications of Coherence Time. [Text Book 2 – Chapter 4]	
<b>Teaching-Learning Process</b>	Chalk and talk method, PowerPoint Presentation <b>RBT Level:</b> L1, L2, L3
<b>Module-4</b>	
<b>MIMO Wireless Communications:</b> Introduction, MIMO System Model, MIMO ZF Receiver, MIMO MMSE Receiver, SVD of the MIMO Channel, SVD & MIMO Capacity, Asymptotic MIMO Capacity, Alamouti and Space-Time Codes, Another OSTBC Example, Nonlinear MIMO Receiver: V – BLAST, MIMO Beamforming. [Text Book 2 – Chapter 6]	
<b>Teaching-Learning Process</b>	Chalk and talk method, PowerPoint Presentation, YouTube videos <b>RBT Level:</b> L1, L2, L3
<b>Module-5</b>	
<b>Orthogonal Frequency Division Multiplexing (OFDM):</b> Introduction, Motivation & Multicarrier Basics, OFDM Example, BER for OFDM, MIMO – OFDM, Effect of Frequency Offset in OFDM, OFDM – Peak-to-Average Ratio (PAPR), SC-FDMA.  <b>Wireless – System Planning:</b> Introduction, Free Space Propagation Model, Ground – Reflection Scenario, Okumura Model, Hata Model, Log-Normal Shadowing, Receiver – Noise Computation, Link – Budget Analysis, Tele traffic Theory, Tele traffic System Model, Steady – State Analysis. [Text Book 2 – Chapter 7 & Chapter 8]	
<b>Teaching-Learning Process</b>	Chalk and talk method, Power point presentation, YouTube videos <b>RBT Level:</b> L1, L2, L3
<b>Course outcomes (Course Skill Set)</b> At the end of the course the student will be able to: <ol style="list-style-type: none"> <li>1. Apply cellular concepts to evaluate the signal reception performance in a cellular network and traffic analysis to design cellular network with given quality of service constraints.</li> <li>2. Determine the type and appropriate model of wireless fading channel based on the system parameters and the property of the wireless medium.</li> <li>3. Analyse and design receiver and transmitter diversity techniques.</li> <li>4. Determine the appropriate transceiver design of multi-antenna systems and evaluate the data rate performance.</li> <li>5. Design wireless communication systems with key 3G (e.g., CDMA) and 4G (OFDM) technologies.</li> </ol>	
<b>Assessment Details (both CIE and SEE)</b> The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.	
<b>Continuous Internal Evaluation:</b> Three Unit Tests each of <b>20 Marks (duration 01 hour)</b>	

1. First test at the end of 5<sup>th</sup> week of the semester
2. Second test at the end of the 10<sup>th</sup> week of the semester
3. Third test at the end of the 15<sup>th</sup> week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4<sup>th</sup> week of the semester
5. Second assignment at the end of 9<sup>th</sup> week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks (duration 01 hours)**

6. At the end of the 13<sup>th</sup> week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

**CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours**)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module.

**Suggested Learning Resources:**

**Text Books:**

1. Wireless Communications, Andreas Goldsmith, Stanford University, Cambridge University Press.
2. Principles of Modern Wireless Communication Systems: Theory and Practice, Aditya K Jagannatham, McGraw Hill Education (India) Pvt. Ltd., 2018. Print Edition: ISBN: 978-1-25-902957-8; E-Book Edition: ISBN: 978-93-392-2003-7.

**Reference Books:**

1. Fundamentals of Wireless Communications, David Tse and Pramod Viswanath, Publisher: Cambridge University Press.
2. Wireless Communications: Principles and Practice, Theodore Rappaport, Prentice Hall.

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**VI Semester**

Wireless and Cellular Communication Laboratory			
Course Code	21TCL66	CIE Marks	50
Teaching Hours/Week (L: T: P: S)	0:0:2:0	SEE Marks	50
Credits	1	Exam Hours	3
<b>Course objectives:</b> This laboratory course enables students to <ul style="list-style-type: none"><li>• Design, model, simulate and verify the various components of wireless communications.</li><li>• Use various simulation tools to demonstrate the various aspects of the communication process.</li></ul>			
Sl.No	Experiments		
1	Develop a code to understand: <ul style="list-style-type: none"><li>a) the pathloss prediction formula (Calculation of received signal strength as a function of distance of separation, antenna height and carrier frequency).</li><li>b) the effect of shadowing on pathloss formula (Calculation of pathloss exponent and variance of shadow fading from measurements and hence finding the large-scale propagation's statistical characteristics).</li></ul>		
2	Develop a MATLAB code to compare three different channel models (Okumura Model, Hata Model, Log-Normal Shadowing, COST-Hata) for wireless system.		
3	Analysis of Cellular concepts like cell-sectoring, splitting (using Qualnet /NS3/ any other tool).		
4	Consider a 2 to 4 message signal and obtain the Time Division Multiplexed Waveform and then perform De-Multiplexed wave and get back the original message (Represent the signal in time domain and frequency domain at various stages).		
5	Consider a multiplexed 24 message signal and obtain the T1 Carrier bit stream (represent the signal in time domain and frequency domain at various stages).		
6	To build BPSK-OFDM system in MATLAB and verify through necessary Waveforms.		
7	To build QPSK-OFDM system in MATLAB and verify through necessary Waveforms.		
8	To build GMSK system in MATLAB and verify through necessary waveforms.		
9	(a) Simulate basic OFDM with no cyclic prefix. (b) Perform Equalization, Convolution, and Cyclic Prefix Addition on basic OFDM.		
10	OFDM with FFT Based Oversampling - Modify an OFDM+ Cyclic Prefix signal to efficiently output an oversampled waveform from the OFDM modulator.		
11	Flat Fading: To study the outage probability, LCR & ADF in SISO for Selection Combining and MRC.		
12	For an irreducible polynomial of order N (3 or 4), obtain the $2^N-1$ Codes. For the resulting CDMA system, Build and Analyse the Spread Spectrum Modulation using any one of the Valid Codes.		
<b>Course outcomes (Course Skill Set):</b> On the completion of this laboratory course, the students will be able to: <ul style="list-style-type: none"><li>1. Use simulation tools to demonstrate various aspects of the communication process.</li><li>2. Demonstrate the modulation/demodulation based on BPSK/ QPSK-OFDM, GMSK, TDM.</li><li>3. Analyse the properties/ performance of CDMA based codes.</li><li>4. Model the T1 carrier bit stream.</li></ul>			

5. Develop codes to characterize and compute the parameters of different channel models of wireless networks.

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

**Continuous Internal Evaluation (CIE):**

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled down to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8<sup>th</sup> week of the semester and the second test shall be conducted after the 14<sup>th</sup> week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

**Semester End Evaluation (SEE):**

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners).

Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours. Rubrics suggested in Annexure-II of Regulation book.

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**VI Semester**

Communication Engineering			
Course Code	21EC651	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	3:0:0: 1	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3
<b>Course objectives:</b> This course will enable students to: <ul style="list-style-type: none"><li>• Describe essential elements of an electronic communication system.</li><li>• Understand Amplitude, Frequency &amp; Phase modulations, and Amplitude demodulation.</li><li>• Define the sampling theorem and methods to generate pulse modulations.</li><li>• Learn the various methods of digital modulation techniques and compare the different schemes.</li><li>• Introduce the basic concepts of information theory and coding.</li><li>• Understand the basic concepts of wireless and cellular communications.</li></ul>			
<b>Teaching-Learning Process (General Instructions)</b> The sample strategies, which the teacher can use to accelerate the attainment of the various course outcomes are listed in the following: <ol style="list-style-type: none"><li>1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.</li><li>2. Show Video/animation films to explain the evolution of communication technologies.</li><li>3. Encourage collaborative (Group) Learning in the class</li><li>4. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking</li><li>5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.</li><li>6. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.</li><li>7. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.</li></ol>			
<b>Module-1</b>			
<b>Introduction to Electronic Communications:</b> Historical perspective, Electromagnetic frequency spectrum, Signal and its representation, Elements of electronic communications system, primary communication resources, signal transmission concepts, Analog and digital transmission, Modulation, Concept of frequency translation, Signal radiation and propagation (Text 1: 1.1 to 1.10)			
<b>Teaching-Learning Process</b>	Chalk and talk method, Power Point Presentation <b>Self-study topics:</b> Classification of Signals and systems <b>RBT Level:</b> L1, L2, L3		
<b>Module-2</b>			
<b>Amplitude Modulation Techniques:</b> Types of analog modulation, Principle of amplitude modulation, AM power distribution, Limitations of AM, (TEXT 1: 4.1, 4.2, 4.4, 4.6) <b>Angle Modulation Techniques:</b> Principles of Angle modulation, Theory of FM-basic Concepts, Theory of phase modulation (TEXT1: 5.1, 5.2, 5.5)			
<b>Teaching-Learning Process</b>	Chalk and talk method/Power point presentation <b>Self-study topics:</b> DSBSC, SSB and VSB modulation techniques and comparison. <b>RBT Level:</b> L1, L2, L3		

<b>Module-3</b>	
<b>Sampling Theorem and Pulse Modulation Techniques:</b> Digital Versus Analog Transmissions, Sampling Theorem, Classification of pulse modulation techniques, PAM, PWM, PPM, PCM, Quantization of signals (TEXT 1: 7.2 to 7.8)	
<b>Teaching-Learning Process</b>	Chalk and talk method <b>Self-study topics:</b> Differential PCM and Delta Modulation <b>RBT Level:</b> L1, L2, L3
<b>Module-4</b>	
<b>Digital Modulation Techniques:</b> Types of digital Modulation, ASK, FSK, PSK, QPSK. (TEXT 1: 9.1 to 9.5) <b>Information Theory, Source and Channel Coding:</b> Information, Entropy and its properties, Shannon, Hartley Theorem, Objectives of source coding, Source coding technique, Shannon source coding theorem, Channel coding theorem, Error Control and Coding. [Text1: 10.1,10.2, 10.11.2, 11.1 to 11.3, 11.8, 11.9, 11.12]	
<b>Teaching-Learning Process</b>	Chalk and talk method, Power Point Presentation. <b>Self-study topics:</b> Quadrature Amplitude Modulation, Comparison of Digital Modulation techniques. <b>RBT Level:</b> L1, L2, L3
<b>Module-5</b>	
<b>Evolution of wireless communication systems:</b> Brief History of wireless communications, Advantages of wireless communication, disadvantages of wireless communications, wireless network generations, Comparison of wireless systems, Evolution of next generation networks, Applications of wireless communication (TEXT 2: 1.1 to 1.7) <b>Principles of Cellular Communications:</b> Cellular terminology, Cell structure and Cluster, Frequency reuse concept, Cluster size and system capacity, Method of locating cochannel cells, Frequency reuse distance (TEXT 2: 4.1 to 4.7)	
<b>Teaching-Learning Process</b>	Chalk and talk method/Power point presentation <b>Self-study topics:</b> Basic propagation mechanisms, Multipath fading. <b>RBT Level:</b> L1, L2, L3
<b>Course outcomes (Course Skill Set)</b> At the end of the course the student will be able to: <ol style="list-style-type: none"> <li>1. Describe the scheme and concepts of radiation and propagation of communication signals through air.</li> <li>2. Understand the AM and FM modulation techniques and represent the signal in time and frequency domain relations.</li> <li>3. Understand the process of sampling and quantization of signals and describe different methods to generate digital signals.</li> <li>4. Describe the basic digital modulation techniques, channel capacity, source coding technique and the channel coding.</li> <li>5. Compare the different wireless communication systems and describe the structure of cellular communication.</li> </ol>	
<b>Assessment Details (both CIE and SEE)</b> The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.	



**Continuous Internal Evaluation:**

Three Unit Tests each of **20 Marks (duration 01 hour)**

1. First test at the end of 5<sup>th</sup> week of the semester
2. Second test at the end of the 10<sup>th</sup> week of the semester
3. Third test at the end of the 15<sup>th</sup> week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4<sup>th</sup> week of the semester
5. Second assignment at the end of 9<sup>th</sup> week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks (duration 01 hours)**

6. At the end of the 13<sup>th</sup> week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

**CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours**)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module.

**Suggested Learning Resources:****Books:**

1. T L Singal, Analog and Digital Communications, McGraw Hill Education (India) Private Limited, 2012, 0-07-107269-1
2. T L Singal, Wireless Communications, McGraw Hill Education (India) Private Limited, 2016, ISBN:0-07-068178-3.

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**VI Semester**

Microcontrollers			
Course Code	21EC652	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	3:0:0:1	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3
<b>Course objectives:</b> This course will enable students to: <ul style="list-style-type: none"><li>• Understand the difference between a Microprocessor and a Microcontroller and embedded microcontrollers.</li><li>• Familiarize the basic architecture of 8051 microcontroller.</li><li>• Program 8051microprocessor using Assembly Level Language and C.</li><li>• Understand the interrupt system of 8051 and the use of interrupts.</li><li>• Understand the operation and use of inbuilt Timers/Counters and Serial port of 8051.</li><li>• Interface 8051 to external memory and I/O devices using its I/O ports.</li></ul>			
<b>Teaching-Learning Process (General Instructions)</b> The sample strategies, which the teacher can use to accelerate the attainment of the various course outcomes are listed in the following: <ol style="list-style-type: none"><li>1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.</li><li>2. Show Video/animation films to explain the functioning of various techniques.</li><li>3. Encourage collaborative (Group) Learning in the class</li><li>4. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking</li><li>5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.</li><li>6. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.</li><li>7. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.</li><li>8. Give Programming Assignments.</li></ol>			
<b>Module-1</b>			
<b>8051 Microcontroller:</b> Microprocessor Vs Microcontroller, Embedded Systems, Embedded Microcontrollers, 8051 Architecture- Registers, Pin diagram, I/O ports functions, Internal Memory organization. External Memory (ROM & RAM) interfacing. Text2 : Chapter 1 section 1.1 to 1.3, chapter 3 sections 3.1 to 3.3			
<b>Teaching-Learning Process</b>	Chalk and talk method, Simulation of modulation techniques <b>RBT Level:</b> L1, L2, L3		
<b>Module-2</b>			
<b>8051 Instruction Set:</b> Addressing Modes, Data Transfer instructions, Arithmetic instructions, Logical instructions, Bit manipulation instructions. Simple Assembly language program examples (without loops) to use these instructions. Text2 : Chapter 5 , chapter 6, chapter 7, chapter 8			
<b>Teaching-Learning Process</b>	Chalk and talk method/Power point presentation <b>RBT Level:</b> L1, L2, L3		

<b>Module-3</b>	
<b>8051 Jump and Call instructions &amp; Embedded C</b> Jump and Call Instructions, Calls & Subroutine instructions. Assembly language program examples on subroutine and involving loops. Text2 : chapter 8 section 8.1 to 8.4 <b>8051 Programming in C:</b> Data Types and Time delay in 8051 C, I/O programming in 8051 C, Logical Operations in C. Text1 : chapter 7 section 7.1 to 7.3	
<b>Teaching-Learning Process</b>	Chalk and talk method <b>RBT Level:</b> L1, L2, L3
<b>Module-4</b>	
<b>8051 Timers and Serial Port</b> <b>8051 Timers and Counters</b> – Operation and Assembly language programming to generate a pulse using Mode-1 and a square wave using Mode- 2 on a port pin. <b>8051 Serial Communication-</b> Basics of Serial Data Communication, RS- 232 standard, 9 pin RS232 signals, Simple Serial Port programming in Assembly and C to transmit a message and to receive data serially. Text1 : Chapter 9 section 9.1 Chapter 10 section 10.1 to 10.5	
<b>Teaching-Learning Process</b>	Chalk and talk method <b>RBT Level:</b> L1, L2, L3
<b>Module-5</b>	
<b>8051 Interrupts and Interfacing Applications</b> 8051 Interrupts. 8051 Assembly language programming to generate an external interrupt using a switch, 8051 C programming to generate a square waveform on a port pin using a Timer interrupt. <b>Interfacing</b> 8051 to ADC-0804, DAC, LCD and Stepper motor and their 8051 Assembly and C language interfacing programming. Text 1: Chapter 11 section 11.1 and 11.2 Chapter 13 section 13.1 to 13.2, chapter 12 section 12.1, chapter 17 section 17.2	
<b>Teaching-Learning Process</b>	Chalk and talk method/Power point presentation <b>RBT Level:</b> L1, L2, L3
<b>Course outcome (Course Skill Set)</b> At the end of the course the student will be able to: <ol style="list-style-type: none"> <li>1. Explain the difference between Microprocessors &amp; Microcontrollers, Architecture of 8051 Microcontroller, Interfacing of 8051 to external memory and Instruction set of 8051.</li> <li>2. Develop 8051 Assembly level programs using 8051 instruction set.</li> <li>3. Develop 8051 Assembly / C language program to generate timings and waveforms using 8051 timers, to send &amp; receive serial data using 8051 serial port.</li> <li>4. Develop 8051 Assembly / C language programs to generate square wave on 8051 I/O port pin using interrupt and C Programme to send &amp; receive serial data using 8051 serial port.</li> <li>5. Interface various peripheral devices to 8051 using I/O ports.</li> </ol>	
<b>Assessment Details (both CIE and SEE)</b> The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together. <b>Continuous Internal Evaluation:</b> Three Unit Tests each of <b>20 Marks (duration 01 hour)</b> <ol style="list-style-type: none"> <li>1. First test at the end of 5<sup>th</sup> week of the semester</li> <li>2. Second test at the end of the 10<sup>th</sup> week of the semester</li> </ol>	

3. Third test at the end of the 15<sup>th</sup> week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4<sup>th</sup> week of the semester
5. Second assignment at the end of 9<sup>th</sup> week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks (duration 01 hours)**

6. At the end of the 13<sup>th</sup> week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

**CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours**)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module.

**Suggested Learning Resources:**

**Text Books:**

1. "The 8051 Microcontroller and Embedded Systems – using assembly and C", Muhammad Ali Mazidi, Janice Gillespie Mazidi and Rollin D McKinlay; PHI, 2006 / Pearson, 2006.
2. "The 8051 Microcontroller", Kenneth J Ayala, 3<sup>rd</sup> Edition, Thomson/Cengage Learning.

**Reference Books:**

1. "The 8051 Microcontroller Based Embedded Systems", Manish K Patel, McGraw Hill, 2014, ISBN: 978-93-329-0125-4.
2. "Microcontrollers: Architecture, Programming, Interfacing and System Design", Raj Kamal, Pearson Education, 2005.

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**VI Semester**

Basic VLSI Design			
Course Code	21EC653	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	3:0:0:1	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3
<b>Course objectives:</b> <ul style="list-style-type: none"><li>• Impart knowledge of MOS transistor theory and CMOS technologies</li><li>• Impart knowledge on architectural choices and performance trade-offs involved in designing and realizing the circuits in CMOS technology</li><li>• Cultivate the concepts of subsystem design processes</li><li>• Demonstrate the concepts of CMOS testing</li></ul>			
<b>Teaching-Learning Process (General Instructions)</b> <p>The sample strategies, which the teacher can use to accelerate the attainment of the various course outcomes are listed in the following:</p> <ol style="list-style-type: none"><li>1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.</li><li>2. Show Video/animation films to explain the functioning of various techniques.</li><li>3. Encourage collaborative (Group) Learning in the class</li><li>4. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking</li><li>5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.</li><li>6. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.</li><li>7. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.</li><li>8. Incorporate programming examples given under Activity based learning.</li></ol>			
<b>Module-1</b>			
<b>Introduction:</b> A Brief History, MOS Transistors, MOS Transistor Theory, Ideal I-V Characteristics, Non-ideal I-V Effects, DC Transfer Characteristics (1.1, 1.3, 2.1, 2.2, 2.4, 2.5 of TEXT2). <b>Fabrication:</b> nMOS Fabrication, CMOS Fabrication [P-well process, N-well process, Twin tub process], BiCMOS Technology (1.7, 1.8, 1.10 of TEXT1).			
<b>Teaching-Learning Process</b>	Chalk and talk method, YouTube videos, Power point presentation <b>RBT Level:</b> L1, L2		
<b>Module-2</b>			
<b>MOS and BiCMOS Circuit Design Processes:</b> MOS Layers, Stick Diagrams, Design Rules and Layout. <b>Basic Circuit Concepts:</b> Sheet Resistance, Area Capacitances of Layers, Standard Unit of Capacitance, Some Area Capacitance Calculations, Delay Unit, Inverter Delays, Driving Large Capacitive Loads (3.1 to 3.3, 4.1, 4.3 to 4.8 of TEXT1).			
<b>Teaching-Learning Process</b>	Chalk and talk method/Power point presentation <b>RBT Level:</b> L1, L2, L3		

<b>Module-3</b>	
<b>Scaling of MOS Circuits:</b> Scaling Models & Scaling Factors for Device Parameters <b>Subsystem Design Processes:</b> Some General considerations, An illustration of Design Processes, <b>Illustration of the Design Processes:</b> Regularity, Design of an ALU Subsystem, The Manchester Carry-chain and Adder Enhancement Techniques (5.1, 5.2, 7.1, 7.2, 8.2, 8.3, 8.4.1, 8.4.2 of TEXT1).	
<b>Teaching-Learning Process</b>	Chalk and talk method, YouTube videos, Power point presentation <b>RBT Level:</b> L1, L2, L3
<b>Module-4</b>	
<b>Subsystem Design:</b> Some Architectural Issues, Switch Logic, Gate (restoring) Logic, Parity Generators, Multiplexers, The Programmable Logic Array (PLA) (6.1 to 6.3, 6.4.1, 6.4.3, 6.4.6 of TEXT1). <b>FPGA Based Systems:</b> Introduction, Basic concepts, Digital design and FPGAs, FPGA based System design, FPGA architecture, Physical design for FPGAs (1.1 to 1.4, 3.2, 4.8 of TEXT3).	
<b>Teaching-Learning Process</b>	Chalk and talk method, YouTube videos, Power point presentation <b>RBT Level:</b> L1, L2, L3
<b>Module-5</b>	
<b>Memory, Registers and Aspects of system Timing:</b> System Timing Considerations, Some commonly used Storage/Memory elements (9.1, 9.2 of TEXT1). <b>Testing and Verification:</b> Introduction, Logic Verification, Logic Verification Principles, Manufacturing Test Principles, Design for testability (12.1, 12.1.1, 12.3, 12.5, 12.6 of TEXT 2).	
<b>Teaching-Learning Process</b>	Chalk and talk method/Power point presentation <b>RBT Level:</b> L1, L2, L3
<b>Course outcome (Course Skill Set)</b> At the end of the course the student will be able to: <ol style="list-style-type: none"> <li>1. Demonstrate understanding of MOS transistor theory, CMOS fabrication flow and technology scaling.</li> <li>2. Draw the basic gates using the stick and layout diagrams with the knowledge of physical design aspects.</li> <li>3. Interpret Memory elements along with timing considerations</li> <li>4. Demonstrate knowledge of FPGA based system design</li> <li>5. Interpret testing and testability issues in VLSI Design</li> <li>6. Analyze CMOS subsystems and architectural issues with the design constraints.</li> </ol>	
<b>Assessment Details (both CIE and SEE)</b> The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together. <b>Continuous Internal Evaluation:</b> Three Unit Tests each of <b>20 Marks (duration 01 hour)</b> <ol style="list-style-type: none"> <li>1. First test at the end of 5<sup>th</sup> week of the semester</li> <li>2. Second test at the end of the 10<sup>th</sup> week of the semester</li> <li>3. Third test at the end of the 15<sup>th</sup> week of the semester</li> </ol> Two assignments each of <b>10 Marks</b> <ol style="list-style-type: none"> <li>4. First assignment at the end of 4<sup>th</sup> week of the semester</li> <li>5. Second assignment at the end of 9<sup>th</sup> week of the semester</li> </ol>	

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks (duration 01 hours)**

6. At the end of the 13<sup>th</sup> week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

**CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject **(duration 03 hours)**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module.

**Suggested Learning Resources:**

**Text Books:**

1. "Basic VLSI Design"- Douglas A Pucknell & Kamran Eshraghian, PHI, 3<sup>rd</sup> Edition.
2. "CMOS VLSI Design- A Circuits and Systems Perspective", Neil H E Weste, David Harris, Ayan Banerjee, 3<sup>rd</sup> Edition, Pearson Education.
3. "FPGA Based System Design", Wayne Wolf, Pearson Education, 2004, Technology and Engineering.

**Web links and Video Lectures (e-Resources)**

- <https://nptel.ac.in/courses/117101058>
- <https://nptel.ac.in/courses/117106093>
- <https://youtu.be/9SnR3M3CI4>
- <https://nptel.ac.in/courses/108/107/108107129/>

**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

Wherever necessary **Cadence/Synopsis/Menta Graphics tools** must be used.

1. Write Verilog Code for the following circuits and their Test Bench for verification, observe the waveform and synthesize the code with technological library with given Constraints\*. Do the initial timing verification with gate level simulation.
  - i. An inverter
  - ii. A Buffer
  - iii. Transmission Gate
  - iv. Basic/universal gates
  - v. Flip flop -RS, D, JK, MS, T
  - vi. Serial & Parallel adder
  - vii. 4-bit counter [Synchronous and Asynchronous counter]
2. Design an op-amp with given specification\* using given differential amplifier Common source and Common Drain amplifier in library\*\* and completing the design flow mentioned below:
  - a. Draw the schematic and verify the following
    - i) DC Analysis
    - ii) AC Analysis
    - iii) Transient Analysis
  - b. Draw the Layout and verify the DRC, ERC
  - c. Check for LVS
  - d. Extract RC and back annotate the same and verify the Design.

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**VI Semester**

Electronic Circuits with Verilog			
Course Code	21EC654	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	2:0:2:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3
<b>Course objectives:</b> <ul style="list-style-type: none"><li>• To understand the basic Verilog HDL design flow.</li><li>• To understand the basic Verilog programming concepts.</li><li>• To describe the simple logic circuits using dataflow, gate-level, and behavioural level modelling.</li><li>• To model digital systems using advanced concepts of Verilog HDL.</li></ul>			
<b>Teaching-Learning Process (General Instructions)</b> <p>The sample strategies, which the teacher can use to accelerate the attainment of the various course outcomes are listed in the following:</p> <ol style="list-style-type: none"><li>1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.</li><li>2. Show Video/animation films to explain the functioning of various techniques.</li><li>3. Encourage collaborative (Group) Learning in the class</li><li>4. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking</li><li>5. Adopt Problem Based Learning (PBL), which fosters students’ Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.</li><li>6. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.</li><li>7. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.</li><li>8. Give programming assignments.</li></ol>			
<b>Module-1</b>			
<b>Overview of Digital Design with Verilog HDL:</b> Evolution of CAD, emergence of HDLs, typical HDL-flow, why Verilog HDL?, trends in HDLs. (Text 1) <b>Hierarchical Modeling Concepts:</b> Top-down and bottom-up design methodology, differences between modules and module instances, parts of a simulation, design block, stimulus block. (Text 1)			
<b>Teaching-Learning Process</b>	Chalk and talk method, Power point presentation <b>RBT Level:</b> L1, L2, L3		
<b>Module-2</b>			
<b>Basic Concepts:</b> Lexical conventions, datatypes, system tasks, compiler directives. (Text 1) <b>Modules and Ports:</b> Module definition, port declaration, connecting ports, hierarchical name referencing. (Text 1)			
<b>Teaching-Learning Process</b>	Chalk and talk method, Power point presentation <b>RBT Level:</b> L1, L2, L3		
<b>Module-3</b>			
<b>Gate-Level Modeling:</b> Modeling using basic Verilog gate primitives, description of and/or and buf/not type gates, rise, fall and turn-off delays, min, max, and typical delays. (Text1) <b>Dataflow Modeling:</b> Continuous assignments, delay specification, expressions, operators, operands, operator types. (Text 1)			



<b>Teaching-Learning Process</b>	Chalk and talk method, Power point presentation <b>RBT Level:</b> L1, L2, L3
<b>Module-4</b>	
<b>Behavioral Description:</b> Behavioral Description Highlights, Structure of the HDL Behavioral Description, Sequential Statements, IF Statement, The case Statement, Verilog casex and casez The wait-for Statement. The Loop Statement, For-Loop, While-Loop, Verilog repeat, Verilog forever (content with respect to Verilog only) (Text 2)	
<b>Teaching-Learning Process</b>	Chalk and talk method, Power point presentation <b>RBT Level:</b> L1, L2, L3
<b>Module-5</b>	
<b>Structural Description:</b> Highlights of Structural Description, Organization of Structural Description Binding (4.1, 4.2, 4.3 till example 4.9) (Text 2) <b>Tasks and Functions:</b> Differences between tasks and functions, declaration, invocation, automatic tasks and functions. (Text 1)	
<b>Teaching-Learning Process</b>	Chalk and talk method, Power point presentation <b>RBT Level:</b> L1, L2, L3
<b>Course outcomes (Course Skill Set)</b> At the end of the course the student will be able to: <ol style="list-style-type: none"> <li>1. Under the Verilog HDL design flow.</li> <li>2. Describe the basic concepts of Verilog HDL programming.</li> <li>3. Design of digital electronics circuits using dataflow, behavioural, gate-level, and structural modelling.</li> <li>4. Design complex digital circuits using advanced Verilog concepts.</li> </ol>	
<b>Assessment Details (both CIE and SEE)</b> The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.	
<b>Continuous Internal Evaluation:</b> Three Unit Tests each of <b>20 Marks (duration 01 hour)</b> <ol style="list-style-type: none"> <li>1. First test at the end of 5<sup>th</sup> week of the semester</li> <li>2. Second test at the end of the 10<sup>th</sup> week of the semester</li> <li>3. Third test at the end of the 15<sup>th</sup> week of the semester</li> </ol> Two assignments each of <b>10 Marks</b> <ol style="list-style-type: none"> <li>4. First assignment at the end of 4<sup>th</sup> week of the semester</li> <li>5. Second assignment at the end of 9<sup>th</sup> week of the semester</li> </ol> Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for <b>20 Marks (duration 01 hours)</b> <ol style="list-style-type: none"> <li>6. At the end of the 13<sup>th</sup> week of the semester</li> </ol> The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be <b>scaled down to 50 marks</b> (to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course). <b>CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.</b> <b>Semester End Examination:</b>	

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours**)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module.

**Suggested Learning Resources:**

**Text Books:**

1. "Verilog HDL: A Guide to Digital Design and Synthesis", Samir Palnitkar, Pearson education, Second edition.
2. "HDL programming (VHDL and Verilog)", Nazeih M Botros, John Wiley India Pvt. Ltd., 2008.

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**VI Semester**

Sensors & Actuators			
Course Code	21EC655	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3
<b>Course objectives:</b> <ul style="list-style-type: none"><li>• To provide the fundamental knowledge about sensors and measurement system.</li><li>• To impart the knowledge of static and dynamic characteristics of instruments and understand the factors in selection of instruments for measurement.</li><li>• To discuss the principle, design and working of transducers for the measurement of physical time varying quantities.</li><li>• Understand the working of various actuators suitable in industrial process control systems.</li><li>• Understand the principle and application of smart sensors.</li></ul>			
<b>Teaching-Learning Process (General Instructions)</b> <p>These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.</p> <ol style="list-style-type: none"><li>1. Explain the fundamental concepts required for the module in the introduction phase for the module.</li><li>2. Conducting quiz after completion of every module in class and evaluate.</li><li>3. Asking questions about completed previous topic, will aid to assess the student understanding.</li><li>4. Evaluate the internals answer booklet by correcting the mistakes if any.</li><li>5. Modules revision at the end as well use practical lab sessions and demonstrate the concepts if applicable and feasible.</li></ol>			
Module-1			
<b>Sensors and measurement system:</b> Sensors and transducers, Classifications of transducers-primary & secondary, active & passive, analog and digital transducers. Smart sensors.			
<b>Measurement:</b> Definition, significance of measurement, instruments and measurement systems. mechanical, electrical and electronic instruments. Elements of generalized measurement system with example. Input-output configuration of measuring instruments and measurement systems, methods of correction for interfering and modifying inputs.			
Teaching-Learning Process	Chalk and talk method, PowerPoint Presentation, More examples relating to applications <b>RBT Level:</b> L1, L2, L3		
Module-2			
<b>Static and Dynamic Characteristics:</b> Static calibration and error calibration curve, accuracy and precision, indications of precision, static error, scale range and scale span, reproducibility and drift, repeatability, signal to noise ratio, sensitivity, linearity, hysteresis, threshold, dead zone and dead time, resolution, signal to noise ratio, factors influencing the choice of transducers/instruments.			
Dynamic response – Dynamic characteristics, Transfer function of generalized first order system, time constant. Transfer function of generalized second order system, natural frequency and Damping ratio.			
Teaching-Learning Process	Chalk and talk method, Power point presentation, VI Lab to demonstrate the characteristics of sensors, More examples relating to applications <b>RBT Level:</b> L1, L2, L3		

<b>Module-3</b>	
<p><b>Measurement of Temperature:</b> RTD, Thermistor, Thermocouple, laws of thermocouple, Thermopile, AD590.</p> <p><b>Measurement of Displacement:</b> Introduction, Principles of Transduction, Variable resistance devices, variable Inductance Transducer, Variable Capacitance Transducer, Hall Effect Devices, Proximity Devices, Digital Transducer.</p>	
<b>Teaching-Learning Process</b>	<p>Chalk and talk method, PowerPoint Presentation, Virtual instrumentation Lab to demonstrate the characteristics of sensors</p> <p><b>RBT Level:</b> L1, L2, L3</p>
<b>Module-4</b>	
<p><b>Measurement of Strain:</b> Introduction, Types of Strain Gauges, Theory of operation of resistance strain gauges, Types of Electrical Strain Gauges –Wire gauges, unbounded strain gauges, foil gauges, semiconductor strain gauges (principle, types &amp; list of characteristics only), Strain gauge Circuits – Wheatstone bridge circuit, Applications.</p> <p><b>Measurement of Force &amp; Torque:</b> Introduction, Force measuring sensor –Load cells – column types devices, proving rings, cantilever beam, pressductor. Hydraulic load cell, electronic weighing system. Torque measurement: Absorption type, transmission type, stress type &amp; deflection type.</p>	
<b>Teaching-Learning Process</b>	<p>Chalk and talk method, PowerPoint Presentation, More examples relating to applications</p> <p><b>RBT Level:</b> L1, L2, L3</p>
<b>Module-5</b>	
<p><b>Actuators and process control system:</b> Introduction. Block diagram and description of process control system with an example. Introduction, Block diagram of Final control operation, Signal conversions analog, digital, pneumatic signal. Actuators, Control elements.</p> <p><b>Electrical actuating systems:</b> Solid-state switches, Solenoids, Electric Motors- Principle of operation and its application: D.C motors, AC motors, Synchronous Motor, Stepper motors.</p> <p><b>Pneumatic Actuators:</b> Principle and working of pneumatic actuators. (Numerical problems on the topic).</p> <p><b>Hydraulic Actuators:</b> Principle and working of Hydraulic actuators. (Numerical problems on the topic).</p>	
<b>Teaching-Learning Process</b>	<p>Chalk and talk method, Power point presentation</p> <p>More examples relating to applications</p> <p><b>RBT Level:</b> L1, L2, L3</p>
<p><b>Course outcome (Course Skill Set)</b></p> <p>At the end of the course the student will be able to:</p> <ol style="list-style-type: none"> <li>1. Discuss the fundamental concepts related to sensors and measurement, functional elements of measurement system, I/O Characteristics of measurement system.</li> <li>2. Interpret and analyse the static and dynamic characteristics of instruments.</li> <li>3. Elucidate the working principle and usage of different transducers for temperature, displacement and level measurement.</li> <li>4. Discuss the principle and working of different types of actuators used in industrial application.</li> <li>5. Discuss the principle and working of strain, force and torque measurement.</li> </ol>	
<p><b>Assessment Details (both CIE and SEE)</b></p> <p>The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.</p>	

**Continuous Internal Evaluation:**

Three Unit Tests each of **20 Marks (duration 01 hour)**

1. First test at the end of 5<sup>th</sup> week of the semester
2. Second test at the end of the 10<sup>th</sup> week of the semester
3. Third test at the end of the 15<sup>th</sup> week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4<sup>th</sup> week of the semester
5. Second assignment at the end of 9<sup>th</sup> week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks (duration 01 hours)**

6. At the end of the 13<sup>th</sup> week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

**CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject **(duration 03 hours)**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module.

**Suggested Learning Resources:****Text Books:**

1. Electrical and Electronic Measurements and Instrumentation, A K Sawhney, 17<sup>th</sup> Edition, (Reprint 2004), Dhanpat Rai & Co. Pvt. Ltd., 2004.
2. Instrumentation: Devices and Systems, C S Rangan, G R Sarma, V S V Mani, 2<sup>nd</sup> Edition (32 Reprint), McGraw Hill Education (India), 2014.
3. Process Control Instrumentation Technology by C D Johnson, 7<sup>th</sup> Edition, Pearson Education Private Limited, New Delhi 2002.

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**VI Semester**

<b>Artificial Neural Networks</b>			
Course Code	<b>21EC641</b>	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	2:2:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3
<b>Course objectives:</b> <ul style="list-style-type: none"> <li>• Preparation: To prepare students with fundamental knowledge and comprehensive understanding of artificial neural networks.</li> <li>• Core Competence: To equip students to develop and configure ANNs with different types of learning algorithms for real world problems.</li> <li>• Professionalism &amp; Learning Environment: To inculcate an engineering student an ethical and professional attitude by providing an academic environment inclusive of effective communication, teamwork, ability to relate engineering issues to a broader social context, and life-long learning needed for a successful professional career.</li> </ul>			
<b>Teaching-Learning Process (General Instructions)</b> The sample strategies, which the teacher can use to accelerate the attainment of the various course outcomes are listed in the following: <ol style="list-style-type: none"> <li>1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.</li> <li>2. Show Video/animation films to explain the functioning of various learning algorithms.</li> <li>3. Encourage collaborative (Group) Learning in the class.</li> <li>4. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking.</li> <li>5. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.</li> <li>6. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.</li> </ol>			

<b>Module-1</b>	
<b>Introduction:</b> Neural Networks, Application Scope of Neural Networks. <b>Artificial Neural Network: An Introduction.</b> - Fundamental Concept, Evolution of Neural Networks, Basic models of Artificial Neural Networks (ANN), Important Technologies of ANNs, McCulloch-Pitts Neuron, Linear Separability. <b>Text 1:</b> 1,1.1,1.2,2.1,2.2,2.3,2.4,2.5,2.6.	
<b>Teaching-Learning Process</b>	Chalk and talk method, PowerPoint Presentation, YouTube videos, Animation of basic model of a neuron in comparison of biological neuron. <b>RBT Level:</b> L1, L2, L3
<b>Module-2</b>	
Hebb Network and simple problems <b>Supervised Learning Network – Introduction</b> –Perceptron Networks-Theory, Perceptron learning rule, architecture, flowchart for training Process, Perceptron training algorithm for single output classes, Perceptron training algorithm for Multiple output classes, Perceptron Network Testing Algorithm, Adaptive Linear Neuron- Theory, Delta rule, Architecture, flowchart, Training, Testing algorithm (Adaline), Multiple Adaptive Linear Neurons -Theory, Architecture, Flowchart, Training algorithm.	

<b>Teaching-Learning Process</b>	Chalk and talk method, PowerPoint Presentation, YouTube videos, Animation of supervised learning algorithms. Problems on Hebb network <b>RBT Level:</b> L1, L2, L3
<b>Module-3</b>	
<b>Back-Propagation Network</b> - Theory, Architecture, Flowchart for training process, Training Algorithm, Learning Factors of Back-Propagation Network, Testing Algorithm of Back-Propagation Network. Radial Basis Function Network, Time Delay Neural Network, Functional Link Networks. <b>Text 1:</b> 3.5,3.6,3.7,3.8.	
<b>Teaching-Learning Process</b>	Chalk and talk method, Power Point Presentation, YouTube videos Self-study topics: Architecture, Flowchart, Training and Testing algorithm. <b>RBT Level:</b> L1, L2, L3
<b>Module-4</b>	
<b>Associative Memory Network</b> – Introduction, Training algorithm for Pattern association- Hebb Rule. Associative Memory Network - Theory, Architecture, Flowchart, Training algorithm, Testing Algorithm, Heteroassociative Memory Network- Theory, architecture, Testing algorithm, Hopfield Networks – Discrete Hopfield Network – architecture, Training algorithm, Testing algorithm of Discrete Hopfield Network. <b>Text 1:</b> 4.1,4.2,4.3,4.4,4.6.	
<b>Teaching-Learning Process</b>	Chalk and talk method, Power Point Presentation, YouTube videos Self-study topics: Architecture, Flowchart, Training and Testing algorithm. <b>RBT Level:</b> L1, L2, L3
<b>Module-5</b>	
<b>Unsupervised Learning Networks</b> – Introduction, Fixed weight competitive nets – Maxnets, Architecture, Testing/application algorithm of Maxnet. Mexican Hat Net- Architecture, Flowchart, algorithm, Kohonen Self organizing Feature Maps – Theory, architecture. Learning Vector quantization – Theory, Architecture. <b>Text 1:</b> 5.1,5.2-5.2.1,5.2.2,5.3- 5.3.1,5.3.2,5.4- 5.4.1,5.4.2.	
<b>Teaching-Learning Process</b>	Chalk and talk method, Power Point Presentation, YouTube videos Self-study topics: Architecture, Flowchart, Training and Testing algorithm. <b>RBT Level:</b> L1, L2, L3
<b>Course outcome (Course Skill Set)</b>  At the end of the course the student will be able to: <ol style="list-style-type: none"> <li>1. Compare and contrast the biological neural network and ANN.</li> <li>2. Discuss the ANN for pattern classification.</li> <li>3. Develop and configure ANN's with different types of functions and learning algorithms.</li> <li>4. Apply ANN for real world problems.</li> </ol>	
<b>Assessment Details (both CIE and SEE)</b>  The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.  <b>Continuous Internal Evaluation:</b> Three Unit Tests each of <b>20 Marks (duration 01 hour)</b> <ol style="list-style-type: none"> <li>1. First test at the end of 5<sup>th</sup> week of the semester</li> <li>2. Second test at the end of the 10<sup>th</sup> week of the semester</li> <li>3. Third test at the end of the 15<sup>th</sup> week of the semester</li> </ol> Two assignments each of <b>10 Marks</b>	

4. First assignment at the end of 4<sup>th</sup> week of the semester
5. Second assignment at the end of 9<sup>th</sup> week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks (duration 01 hours)**

6. At the end of the 13<sup>th</sup> week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

**CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject **(duration 03 hours)**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module.

**Suggested Learning Resources:**

**Text Book:**

S N Sivanandam and S N Deepa, "Principles of Soft Computing", 2<sup>nd</sup> Edition, Wiley India Pvt. Ltd., 2014.

**Reference Book:**

Simon Haykin, "Neural Networks: A comprehensive foundation", 2<sup>nd</sup> Edition, PHI, 1998.



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**VI Semester**

Cryptography			
Course Code	21EC642	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	2:2:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3
<b>Course objectives:</b> This course will enable students to: <ul style="list-style-type: none"><li>• Preparation: To prepare students with fundamental knowledge/ overview in the field of Information Security with knowledge of mathematical concepts required for cryptography.</li><li>• Core Competence: To equip students with a basic foundation of Cryptography by delivering the basics of symmetric key and public key cryptography and design of pseudo random sequence generation technique</li></ul>			
<b>Teaching-Learning Process (General Instructions)</b> The sample strategies, which the teacher can use to accelerate the attainment of the various course outcomes are listed in the following: <ol style="list-style-type: none"><li>1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.</li><li>2. Show Video/animation films to explain the different Cryptographic Techniques / Algorithms</li><li>3. Encourage collaborative (Group) Learning in the class</li><li>4. Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking</li><li>5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.</li><li>6. Topics will be introduced in a multiple representation.</li><li>7. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.</li><li>8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.</li><li>9. Adopt Flipped class technique by sharing the materials / Sample Videos prior to the class and have discussions on the that topic in the succeeding classes</li><li>10. Give Programming Assignments</li></ol>			
<b>Module-1</b>			
<b>Basic Concepts of Number Theory and Finite Fields:</b> Divisibility and The Division Algorithm Euclidean algorithm, Modular arithmetic, Groups, Rings and Fields, Finite fields of the form GF(p), Polynomial Arithmetic, Finite Fields of the Form GF(2 <sup>m</sup> ) (Text 1: Chapter 3)			
<b>Teaching-Learning Process</b>	Chalk and Talk, YouTube videos, Flipped Class Technique Programming on implementation of Euclidean algorithm, multiplicative inverse, Finite fields of the form GF(p), construction of finite field over GF(2 <sup>m</sup> ). <b>RBT Level:</b> L1, L2, L3		
<b>Module-2</b>			
<b>Introduction:</b> Computer Security Concepts, A Model for Network Security (Text 1: Chapter 1) <b>Classical Encryption Techniques:</b> Symmetric cipher model, Substitution techniques, Transposition techniques (Text 1: Chapter 1)			
<b>Teaching-Learning Process</b>	Chalk and Talk, YouTube videos, Flipped Class Technique and PPTs. Programming on Substitution and Transposition techniques. Self-study topics: Security Mechanisms, Services and Attacks. <b>RBT Level:</b> L1, L2, L3		

<b>Module-3</b>	
<b>Block Ciphers:</b> Traditional Block Cipher structure, Data encryption standard (DES) (Text 1: Chapter 2: Section 1, 2) The AES Cipher. (Text 1: Chapter 4: Section 2, 3, 4) <b>More on Number Theory:</b> Prime Numbers, Fermat's and Euler's theorem, discrete logarithm. (Text 1: Chapter 7: Section 1, 2, 5)	
<b>Teaching-Learning Process</b>	Chalk and Talk, YouTube videos, Flipped Class Technique and PPTs. Implementation of SDES using programming languages like C++/Python/Java/Scilab. Self-study topics: DES S-Box- Linear and differential attacks <b>RBT Level:</b> L1, L2, L3
<b>Module-4</b>	
<b>ASYMMETRIC CIPHERS:</b> Principles of Public-Key Cryptosystems, The RSA algorithm, Diffie - Hellman Key Exchange, Elliptic Curve Arithmetic, Elliptic Curve Cryptography (Text 1: Chapter 8, Chapter 9: Section 1, 3, 4)	
<b>Teaching-Learning Process</b>	Chalk and Talk, YouTube videos, Flipped Class Technique and PPTs. Implementation of Asymmetric key algorithms using programming languages like C++/Python/Java/Scilab Numerical examples on Elliptic Curve Cryptography <b>RBT Level:</b> L1, L2, L3
<b>Module-5</b>	
<b>Pseudo-Random-Sequence Generators and Stream Ciphers:</b> Linear Congruential Generators, Linear Feedback Shift Registers, Design and analysis of stream ciphers, Stream ciphers using LFSRs, A5, Hughes XPD/KPD, Nanoteq, Rambutan, Additive generators, Gifford, Algorithm M, PKZIP (Text 2: Chapter 16)	
<b>Teaching-Learning Process</b>	Chalk and Talk, YouTube videos, Flipped Class Technique and PPTs. Implementation of simple stream ciphers using programming languages like C++/Python/Java/Scilab. <b>RBT Level:</b> L1, L2, L3
<b>Course outcomes (Course Skill Set)</b> At the end of the course the student will be able to: <ol style="list-style-type: none"> <li>1. Explain traditional cryptographic algorithms of encryption and decryption process.</li> <li>2. Use symmetric and asymmetric cryptography algorithms to encrypt and decrypt the data.</li> <li>3. Apply concepts of modern algebra in cryptography algorithms.</li> <li>4. Design pseudo random sequence generation algorithms for stream cipher systems.</li> </ol>	
<b>Assessment Details (both CIE and SEE)</b> The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.	
<b>Continuous Internal Evaluation:</b> Three Unit Tests each of <b>20 Marks (duration 01 hour)</b> <ol style="list-style-type: none"> <li>1. First test at the end of 5<sup>th</sup> week of the semester</li> <li>2. Second test at the end of the 10<sup>th</sup> week of the semester</li> <li>3. Third test at the end of the 15<sup>th</sup> week of the semester</li> </ol> Two assignments each of <b>10 Marks</b> <ol style="list-style-type: none"> <li>4. First assignment at the end of 4<sup>th</sup> week of the semester</li> <li>5. Second assignment at the end of 9<sup>th</sup> week of the semester</li> </ol> Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for <b>20 Marks (duration 01 hours)</b>	

6. At the end of the 13<sup>th</sup> week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

**CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours**)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module.

**Suggested Learning Resources:**

**Text Books:**

1. William Stallings, "Cryptography and Network Security Principles and Practice", Pearson Education Inc., 6<sup>th</sup> Edition, 2014, ISBN: 978-93-325-1877-3
2. Bruce Schneier, "Applied Cryptography Protocols, Algorithms, and Source code in C", Wiley Publications, 2<sup>nd</sup> Edition, ISBN: 9971-51-348-X.

**Reference Books:**

1. Cryptography and Network Security, Behrouz A Forouzan, TMH, 2007.
2. Cryptography and Network Security, Atul Kahate, TMH, 2003.

**Web links and Video Lectures (e-Resources)**

- <https://nptel.ac.in/courses/106105031>

**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

- Programming Assignments / Mini Projects can be given to improve programming skills

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**VI Semester**

Python Programming			
Course Code	21EC643	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	2:0:2:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3
<b>Course objectives:</b> <ul style="list-style-type: none"><li>To learn programming using Python</li><li>Develop application using Python</li></ul>			
<b>Teaching-Learning Process (General Instructions)</b> <p>The sample strategies, which the teacher can use to accelerate the attainment of the various course outcomes are listed in the following:</p> <ol style="list-style-type: none"><li>In addition to the traditional lecture method, different types of innovative teaching methods may be adopted so that the delivered lessons shall develop student's theoretical and programming skills.</li><li>State the need for learning Programming with real-life examples.</li><li>Support and guide the students for self-study.</li><li>You will also be responsible for assigning homework, grading assignments and quizzes, and documenting students' progress</li><li>Encourage the students for group learning to improve their creative and analytical skills.</li><li>Show short, related video lectures in the following ways:<ul style="list-style-type: none"><li>As an introduction to new topics (pre-lecture activity).</li><li>As a revision of topics (post-lecture activity).</li><li>As additional examples (post-lecture activity).</li><li>As an additional material of challenging topics (pre-and post-lecture activity).</li><li>As a model solution of some exercises (post-lecture activity).</li></ul></li></ol>			
<b>Module-1</b>			
Python Basics, Python language features, History , Entering Expressions into the Interactive Shell, The Integer, Floating-Point, and String Data Types, String Concatenation and Replication, Storing Values in Variables, Your First Program, Dissecting Your Program, Flow control, Boolean Values, Comparison Operators, Boolean Operators, Mixing Boolean and Comparison Operators, Elements of Flow Control, Program Execution, Flow Control Statements, Importing Modules, Ending a Program Early with sys.exit(), Functions, def Statements with Parameters, Return Values and return Statements, The None Value, Keyword Arguments and print(), Local and Global Scope, The global Statement, Exception Handling, A Short Program: Guess the Number Textbook 1: Chapters 1 – 3			
<b>Teaching-Learning Process</b>	Chalk and talk method, Simulation of modulation techniques <b>RBT Level:</b> L1, L2, L3		
<b>Module-2</b>			
Data Structures: Lists: The List Data Type, Working with Lists Strings: Manipulating Strings, Working with Strings, Useful String Methods Tuples and Dictionaries, basics Using Data Structures to Model Real-World Things, Manipulating Strings. Textbook 1: Chapters 4 – 6			
<b>Teaching-Learning Process</b>	Chalk and talk method/Power point presentation <b>RBT Level:</b> L1, L2, L3		

<b>Module-3</b>	
<p>Pattern Matching with Regular Expressions, Finding Patterns of Text Without Regular Expressions, Finding Patterns of Text with Regular Expressions, More Pattern Matching with Regular Expressions,, The findall() Method, Character Classes, Making Your Own Character Classes, The Caret and Dollar Sign Characters, The Wildcard Character, Review of Regex Symbols.</p> <p>Reading and Writing Files, Files and File Paths, The os.path Module, The File Reading/Writing Process, Saving Variables with the shelve Module, Saving Variables with the pprint. pformat() Function Textbook 1: Chapters 7, 8</p>	
<b>Teaching-Learning Process</b>	Chalk and talk method / PowerPoint Presentation <b>RBT Level:</b> L1, L2, L3
<b>Module-4</b>	
<p>Classes and objects: Programmer-defined types, Attributes, Rectangles, Instances as return values, Objects are mutable, Copying, Classes and functions: Time, Pure functions, Modifiers, Prototyping versus planning, Classes and methods: Object-oriented features, Printing objects, Another example, The init method, The __str__ method, Operator overloading, Type-based dispatch, Polymorphism. Textbook 2: Textbook 2: Chapters 15 – 18</p>	
<b>Teaching-Learning Process</b>	Chalk and talk method / PowerPoint Presentation <b>RBT Level:</b> L1, L2, L3
<b>Module-5</b>	
<p>HTTP, The World's simplest Web Browser, Retrieving an image over HTTP, Retrieving web pages with urllib, Parsing html and scraping the web, Parsing HTML using RE, BeautifulSoup, Reading binary files using urllib, XML, Parsing XML, Looping through nodes, JSON, Parsing JSON, API, geocoding Web Service, Security &amp; API usage, What is database?, Database Concepts, Database Browser, Creating a database table, SQL, Spidering Twitter, Basic data modeling, Programming with multiple tables, Three kinds of Keys, JOIN Text book : Chapter 2, 13, 15</p>	
<b>Teaching-Learning Process</b>	Chalk and talk method/Power point presentation <b>RBT Level:</b> L1, L2, L3
<p><b>Course outcomes (Course Skill Set)</b> At the end of the course the student will be able to:</p> <ol style="list-style-type: none"> <li>1. To acquire programming skills in Python</li> <li>2. To demonstrate data structure representation using Python</li> <li>3. To develop the skill of pattern matching and files in Python</li> <li>4. To acquire Object Oriented Skills in Python</li> <li>5. To develop the ability to write database applications in Python</li> </ol>	
<p><b>Assessment Details (both CIE and SEE)</b> The weightage of Continuous 5 End Examination) taken together.</p> <p><b>Continuous Internal Evaluation:</b> Three Unit Tests each of <b>20 Marks (duration 01 hour)</b></p> <ol style="list-style-type: none"> <li>1. First test at the end of 5<sup>th</sup> week of the semester</li> <li>2. Second test at the end of the 10<sup>th</sup> week of the semester</li> <li>3. Third test at the end of the 15<sup>th</sup> week of the semester</li> </ol> <p>Two assignments each of <b>10 Marks</b></p> <ol style="list-style-type: none"> <li>4. First assignment at the end of 4<sup>th</sup> week of the semester</li> <li>5. Second assignment at the end of 9<sup>th</sup> week of the semester</li> </ol> <p>Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for <b>20 Marks (duration 01 hours)</b></p>	

6. At the end of the 13<sup>th</sup> week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

**CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours**)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module.

**Suggested Learning Resources:**

**Text Books:**

1. Al Sweigart, "Automate the Boring Stuff with Python", 1<sup>st</sup> Edition, No Starch Press, 2015. (Available under CC-BY-NC-SA license at <https://automatetheboringstuff.com/>) (Chapters 1 to 8)
2. Allen B Downey, "Think Python: How to Think Like a Computer Scientist", 2<sup>nd</sup> Edition, Green Tea Press, 2015. (Available under CC-BY-NC license at <http://greenteapress.com/thinkpython2/thinkpython2.pdf>) (Chapters 15 - 18) (Download pdf/html files from the above links)
3. Charles R. Severance, "Python for Everybody: Exploring Data Using Python 3", 1<sup>st</sup>, Create Space Independent Publishing Platform, 2016

**Web links and Video Lectures (e-Resources)**

- <https://www.youtube.com/watch?v=xQNe0TRyig>
- <https://www.youtube.com/watch?v=kqtD5dpm9C8>

**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

- Write a program to generate Fibonacci series
- Write a program to find factorial of a number using function.
- Write a menu driven program to implement stack using Lists
- Create a DB using dictionaries containing key as USN and related fields containing Name, gender, Marks1, Marks2 & Marks3 of students. Implement the following functions to perform  
i) Update Name/gender/marks ii) search for usn and display the relevant fields iii) delete based on search for name iv) generate the report with avg marks more than 70%
- Write a program to implement search and replace multiple occurrences of a given substring in the main string in a list.
- Write a function called most\_frequent that takes a string and prints the letters in decreasing order of frequency.
- Write a program that reads a file, display the contents, builds a histogram of the words in the file and print most common words in the file.
- Write a program that searches a directory and all of its subdirectories, recursively, and returns a list of complete paths for all files with a given suffix.

- Write python code to extract From: and To: Email Addresses from the given text file using regular expressions. <https://www.py4e.com/code3/mbox.txt>.
- Consider the sentence *"From rjlowe@iupui.edu Fri Jan 4 14:50:18 2008"*, Write python code to extract email address and time of the day from the given sentence
- Write a program to read, display and count number of sentences of the given file.
- Write a program that gets the current date and prints the day of the week.
- Write a function called print\_time that takes two Time objects and prints total time it in the form hour:minute:second.
- Write a program that takes a birthday as input and prints the user's age and the number of days, hours, minutes and seconds until their next birthday.

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**VI Semester**

Micro Electro Mechanical Systems			
Course Code	21EC644	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	3: 0 :0 : 1	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3
<b>Course objectives:</b> <ul style="list-style-type: none"><li>• <b>Preparation:</b> To prepare students with fundamental knowledge/ overview in the field of Micro Electro Mechanical Systems.</li><li>• <b>Core Competence:</b> To equip students with a basic foundation in electronic engineering, mechanical engineering, electrical engineering, chemistry, physics and mathematics fundamentals required for comprehending the operation and application of MEMS circuits, design.</li><li>• <b>Professionalism &amp; Learning Environment:</b> To inculcate in students an ethical and professional attitude by providing an academic environment inclusive of effective communication, teamwork, ability to relate engineering issues to a broader social context, and life-long learning needed for a successful professional career.</li></ul>			
<b>Teaching-Learning Process (General Instructions)</b> <p>These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.</p> <ol style="list-style-type: none"><li>1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes</li><li>2. Show Video/animation films to explain the functioning of various</li><li>3. Encourage collaborative (Group) Learning in the class to promote critical thinking</li><li>4. Topics for seminars on several MEMS related topics and their applications</li><li>5. Encourage the students to take up mini projects and main projects</li><li>6. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.</li></ol>			
<b>Module-1</b>			
<b>Overview of MEMS and Microsystems:</b> MEMS and Microsystem, Typical MEMS and Microsystems Products, Evolution of Microfabrication, Microsystems and Microelectronics, Multidisciplinary Nature of Microsystems, Miniaturization. Applications and Markets. <b>Text1: 1.1, 1.2, 1.3, 1.4, 1.5, 1.6, 1.7, 1.8, 1.9</b>			
<b>Teaching-Learning Process</b>	Chalk and talk method, Animation of MEMS products and applications <b>RBT Level: L1, L2, L3</b>		
<b>Module-2</b>			
<b>Working Principles of Microsystems:</b> Introduction, Microsensors, Micro actuation, MEMS with Micro actuators, Micro accelerometers, Microfluidics. <b>Text1: 2.1,2.2, 2.3, 2.4, 2.5, 2.6</b> <b>Engineering Science for Microsystems Design and Fabrication:</b> Introduction, Atomic Structure of Matter, Ions and Ionization Molecular Theory of Matter and Intermolecular Forces, Plasma Physics, Electrochemistry. <b>Text1: 3.1, 3.2, 3.3, 3.4, 3.7, 3.8</b>			
<b>Teaching-Learning Process</b>	PowerPoint Presentation, YouTube videos, Animations of MEMS Micro sensors, Micro actuators, Micro accelerometers and Microfluidics, molecules, Ions and matter <b>RBT Level: L1, L2, L3</b>		



<b>Module-3</b>	
<b>Engineering Mechanics for Microsystems Design:</b> Introduction, Static Bending of Thin Plates, Mechanical Vibration, Thermo mechanics, Fracture Mechanics, Thin Film Mechanics, Overview on Finite Element Stress Analysis. <b>Text1: 4.1,4.2,4.3,4.4,4.5,4.6,4.7</b>	
<b>Teaching-Learning Process</b>	Chalk and talk method, Power Point Presentations and supporting YouTube Videos Solve numericals related to Thin Plates, and Vibration. Self study topics: solve numericals related to other topics <b>RBT Level:</b> L1, L2, L3
<b>Module-4</b>	
<b>Scaling Laws in Miniaturization:</b> Introduction, Scaling in Geometry, Scaling in Rigid-Body Dynamics, Scaling in Electrostatic Forces, Scaling in Electromagnetic Forces, Scaling in Electricity, Scaling in Fluid Mechanics, Scaling in Heat Transfer. <b>Text1: 6.1, 6.2,6.3,6.4,6.5,6.6,6.7,6.8</b>	
<b>Teaching-Learning Process</b>	Chalk and Talk Method, You Tube Videos, Solve numericals related to scaling in Geometry Self study topics: solve numericals of other topics <b>RBT Level:</b> L1, L2, L3
<b>Module-5</b>	
<b>Overview of Micromanufacturing:</b> Introduction, Bulk Micromanufacturing, Surface Micromachining, The LIGA Process, Summary on Micromanufacturing. <b>Text1: 9.1,9.2,9.3,9.4,9.5</b> <b>Microsystem Packaging:</b> Introduction, Overview of Mechanical Packaging of Microelectronics, Microsystem Packaging. <b>Text1: 11.1,11.2, 11.3</b>	
<b>Teaching-Learning Process</b>	Power Point Presentation, YouTube videos, Animation of MEMS micromanufacturing Supporting animation videos on packaging <b>RBT Level:</b> L1, L2, L3
<b>Course outcomes (Course Skill Set)</b> At the end of the course the student will be able to: <ol style="list-style-type: none"> <li>1. Appreciate the technologies related to Micro Electro Mechanical Systems.</li> <li>2. Understand design and fabrication processes involved with MEMS devices.</li> <li>3. Analyse the MEMS devices and develop suitable mathematical models</li> <li>4. Know various application areas for MEMS device.</li> </ol>	
<b>Assessment Details (both CIE and SEE)</b> The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together. <b>Continuous Internal Evaluation:</b> Three Unit Tests each of <b>20 Marks (duration 01 hour)</b> <ol style="list-style-type: none"> <li>1. First test at the end of 5<sup>th</sup> week of the semester</li> <li>2. Second test at the end of the 10<sup>th</sup> week of the semester</li> <li>3. Third test at the end of the 15<sup>th</sup> week of the semester</li> </ol> Two assignments each of <b>10 Marks</b> <ol style="list-style-type: none"> <li>4. First assignment at the end of 4<sup>th</sup> week of the semester</li> <li>5. Second assignment at the end of 9<sup>th</sup> week of the semester</li> </ol> Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for <b>20 Marks (duration 01 hours)</b> <ol style="list-style-type: none"> <li>6. At the end of the 13<sup>th</sup> week of the semester</li> </ol> The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be <b>scaled down to 50 marks</b>	

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

**CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours**)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module.

**Suggested Learning Resources:**

**Text Book:**

**Tai-Ran Hsu**, MEMS and Micro systems: Design and Manufacture, 1<sup>st</sup> Ed, Tata Mc Graw Hill.

**Reference Books:**

1. **Hans H Gatzen, Volker Saile, JurgLeuthold**, Micro and Nano Fabrication: Tools and Processes, Springer, 2015.
2. **Dilip Kumar Bhattacharya, Brajesh Kumar Kaushik**, Microelectromechanical Systems (MEMS), Cengage Learning.
3. **Chang Liu**, Foundations of MEMS, Pearson Ed.

**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

- Develop mini projects and Final year projects using MEMS components to address the real world problems

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**VII Semester**

VLSI Circuits & Systems			
Course Code	21TC71	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	3:0:0:1	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3
<b>Course objectives:</b> <ul style="list-style-type: none"><li>• Impart knowledge of MOS transistor theory and CMOS processing technology.</li><li>• Impart knowledge on designing Combinational and sequential circuits.</li><li>• Cultivate the concepts of subsystem design processes.</li><li>• Learn the tools and methods for CMOS testing and verification.</li></ul>			
<b>Teaching-Learning Process (General Instructions)</b> <p>The sample strategies, which the teacher can use to accelerate the attainment of the various course outcomes are listed in the following:</p> <ol style="list-style-type: none"><li>1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.</li><li>2. Show Video/animation films to explain about the VLSI circuits &amp; systems design and fabrication.</li><li>3. Encourage collaborative (Group) Learning in the class</li><li>4. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking</li><li>5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.</li><li>6. Topics will be introduced in multiple representations.</li><li>7. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.</li><li>8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.</li></ol>			
<b>Module-1</b>			
<b>Introduction:</b> A brief history, MOS Transistors, CMOS Logic (Up to Pass Transistors and Transmission Gates), CMOS Fabrication and Layout (1.1 to 1.4.6 and 1.5 of TEXT1)			
<b>Teaching-Learning Process</b>	Chalk and talk method, PowerPoint Presentation, YouTube videos of CMOS Fabrication Practical Topics: Simulation of Simple CMOS circuits using a suitable tool. Self-study topics: VLSI Fabrication steps. <b>RBT Level:</b> L1, L2, L3		
<b>Module-2</b>			
<b>MOS Transistor Theory:</b> Introduction, Long-channel I-V Characteristics, DC Transfer Characteristics. <b>CMOS Processing Technology:</b> Introduction, CMOS Technologies, Layout Design Rules (2.1, 2.2, 2.3, 2.5 and 3.1 to 3.3 of TEXT1)			
<b>Teaching-Learning Process</b>	Chalk and talk method, PowerPoint Presentation, YouTube videos of Layout Design rules and Stick diagram Self-study topics: Stick diagrams & Layouts of CMOS Circuits, VLSI technology Flow <b>RBT Level:</b> L1, L2, L3		
<b>Module-3</b>			
<b>Combinational Circuit Design:</b> Introduction, Circuit families (Static CMOS & Dynamic Circuits)			

<b>Sequential Circuit Design:</b> Introduction, Circuit Design for Latches and Flip-flops (Conventional CMOS Latches, Conventional CMOS Flip-Flops, Pulsed Latches, Resettable Latches and Flip-Flops, Enabled Latches and Flip-Flops, Differential Flip-Flops Dual Edge-Triggered Flip-Flops ) (9.1, 9.2.1, 9.2.4, 10.1, 10.3.1, 10.3.2, 10.3.3, 10.3.4, 10.3.5, 10.3.8 and 10.3.9 of TEXT1).	
<b>Teaching-Learning Process</b>	Chalk and talk method, PowerPoint Presentation, YouTube videos of CMOS circuit design Self-study topics: VLSI Design and Fabrication challenges <b>RBT Level:</b> L1, L2, L3
<b>Module-4</b>	
<b>Data path Subsystem:</b> Introduction, Addition/Subtraction, (Single-Bit Addition, Carry-Propagate Addition, Subtraction), One/Zero Detectors. (11.1, 11.2.1, 11.2.2, 11.2.3, 11.3 of TEXT1). <b>Array Subsystems:</b> Introduction, SRAM (SRAM Cells, Row Circuitry, Column Circuitry) DRAM, Read only memory (12.1, 12.2.1, 12.2.2, 12.2.3, 12.3 and 12.4 of TEXT 1).	
<b>Teaching-Learning Process</b>	Chalk and talk method, PowerPoint Presentation, YouTube videos of Subsystem Design Self-study topics: Full Custom & ASIC Design <b>RBT Level:</b> L1, L2, L3
<b>Module-5</b>	
<b>Design Methodology and Tools:</b> Introduction, Structured design strategies. <b>Testing, Debugging and Verification:</b> Introduction, Logic Verification, Logic Verification Principles, Manufacturing Test Principles, Design for testability (14.1, 14.2, 15.1 and 15.6 of TEXT 1).	
<b>Teaching-Learning Process</b>	Chalk and talk method, PowerPoint Presentation, YouTube videos of VLSI tools & testing Self-study topics: Survey on different VLSI Design tools. <b>RBT Level:</b> L1, L2, L3
<b>Course outcomes (Course Skill Set)</b> At the end of the course the student will be able to: <ol style="list-style-type: none"> <li>1. Explain the background of CMOS VLSI and basic logic circuits.</li> <li>2. Apply knowledge of MOS transistor theory and CMOS design rules in designing VLSI Circuits.</li> <li>3. Demonstrate the Combinational and sequential logic design.</li> <li>4. Analyze the performance of CMOS subsystems.</li> <li>5. Identify suitable tools and methods for CMOS testing and verification.</li> </ol>	
<b>Assessment Details (both CIE and SEE)</b> The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together. <b>Continuous Internal Evaluation:</b> Three Unit Tests each of <b>20 Marks (duration 01 hour)</b> <ol style="list-style-type: none"> <li>1. First test at the end of 5<sup>th</sup> week of the semester</li> <li>2. Second test at the end of the 10<sup>th</sup> week of the semester</li> <li>3. Third test at the end of the 15<sup>th</sup> week of the semester</li> </ol> Two assignments each of <b>10 Marks</b> <ol style="list-style-type: none"> <li>4. First assignment at the end of 4<sup>th</sup> week of the semester</li> <li>5. Second assignment at the end of 9<sup>th</sup> week of the semester</li> </ol> Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for <b>20 Marks (duration 01 hours)</b> <ol style="list-style-type: none"> <li>6. At the end of the 13<sup>th</sup> week of the semester</li> </ol> The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be <b>scaled down to 50 marks</b>	

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

**CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours**)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module.

**Suggested Learning Resources:**

**Text Book:**

"CMOS VLSI Design- A Circuits and Systems Perspective", Neil H E Weste, David Harris, Ayan Banerjee, 3<sup>rd</sup> Edition, Pearson Education.

**Reference Book:**

"Introduction to VLSI Circuits and Systems", John P Uyemura, Wiley Student Edition

**Web links and Video Lectures (e-Resources):**

- <https://www.youtube.com/watch?v=9SnR3M3CIm4>
- <https://nptel.ac.in/courses/117106093>
- <https://www.youtube.com/watch?v=fwNkg1fsqBY>
- <https://nptel.ac.in/courses/108/107/108107129/>

**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Wherever necessary Cadence/Synopsis/Mentor Graphics tools may be used.

1. Design an Inverter with given specifications\*, completing the design flow mentioned below:

- a. Draw the schematic and verify the following:
  - i) DC Analysis
  - ii) Transient Analysis
- b. Draw the Layout and verify the DRC, ERC
- c. Check for LVS
- d. Extract RC and back annotate the same and verify the Design
- e. Verify & Optimize for Time, Power and Area to the given constraint\*

2. Design the following circuits with the given specifications\*, completing the design flow mentioned below:

- a. Draw the schematic and verify the following:
  - i) DC Analysis ii) AC Analysis iii) Transient Analysis
- b. Draw the Layout and verify the DRC, ERC
- c. Check for LVS
- d. Extract RC and back annotate the same and verify the Design.

\* Appropriate specification should be given.

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**VII Semester**

Optical Communication and Optical networks			
Course Code	21TC72	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	2:0:0:1	SEE Marks	50
Total Hours of Pedagogy	30	Total Marks	100
Credits	2	Exam Hours	3
Non-MCQ pattern of CIE and SEE			
<b>Course objectives:</b> This course will enable students to: <ul style="list-style-type: none"><li>• Learn the basic principle of optical fiber communication with different modes of light propagation.</li><li>• Understand the transmission characteristics and losses in optical fiber.</li><li>• Study of optical components and its applications in optical communication networks.</li><li>• To study the transmission characteristics for overall design considerations.</li><li>• Identify the client layers of the optical network.</li><li>• Attain knowledge of different network elements and optical layer services.</li></ul>			
<b>Teaching-Learning Process (General Instructions)</b> The sample strategies, which the teacher can use to accelerate the attainment of the various course outcomes are listed in the following: <ol style="list-style-type: none"><li>1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.</li><li>2. Show Video/animation films to explain the functioning of various techniques.</li><li>3. Encourage collaborative (Group) Learning in the class</li><li>4. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking</li><li>5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.</li><li>6. Topics will be introduced in multiple representations.</li><li>7. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.</li><li>8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.</li></ol>			
Module-1			
<b>Optical Fiber Structures:</b> Optical Fiber Modes and Configurations, Mode theory for circular waveguides, Single mode fibers, Fiber materials. <b>Attenuation and Dispersion:</b> Attenuation, Absorption, Scattering Losses, Bending loss, Signal Dispersion: Modal delay, Group delay, Material dispersion. [Text 1: 3.1, 3.2, 2.3 [2.3.1 to 2.3.4], 2.4 [2.4.1, 2.4.2], 2.5, 2.7].			
Teaching-Learning Process	Chalk and talk method, Power point presentation RBT Level: L1, L2, L3		
Module-2			
<b>Optical Sources and detectors:</b> Light Emitting Diode: LED Structures, Light source materials, Quantum efficiency and LED power, Laser Diodes: Modes and threshold conditions, Rate equations, External quantum efficiency, Resonant frequencies, Photodetectors: The pin Photodetector, Avalanche Photodiodes. <b>WDM Concepts:</b> Overview of WDM, Isolators and Circulators, Fiber grating filters, Dielectric thin-film filters, Diffraction Gratings.			

[Text1: 4.2 ,4.3, 6.1, 10.1, 10.3, 10.4, 10.5, 10.7]	
<b>Teaching-Learning Process</b>	Chalk and talk method, Power point presentation <b>RBT Level:</b> L1, L2, L3
<b>Module-3</b>	
<b>Introduction to Optical Networks:</b> Telecommunication network Architecture, services, circuit switching and packet switching, optical Networks, optical layer, transparency and all optical networks, optical packet switching, transmission basics, network evolution. (Text 2: 1.1,1.2,1.3,1.4,1.5,1.6,1.7,1.8)	
<b>Teaching-Learning Process</b>	Chalk and talk method, Power point presentation <b>RBT Level:</b> L1, L2, L3
<b>Module-4</b>	
<b>Transmission System Engineering:</b> System model, Power penalty, Transmitter, receiver, optical amplifiers, Crosstalk, Dispersion, Fiber nonlinearities, overall design considerations. (Text 2: 5.1,5.2,5.3,5.4,5.5,5.6,5.7,5.8,5.12) <b>Client layers of optical network:</b> SONET/SDH, optical transport network, generic framing procedure, Ethernet, IP, Multiprotocol label switching. (Text 2: 6.1, 6.2,6.3,6.4,6.5,6.6)	
<b>Teaching-Learning Process</b>	Chalk and talk method, Power point presentation <b>RBT Level:</b> L1, L2, L3
<b>Module-5</b>	
<b>WDM Network Elements:</b> Optical line terminals, optical line amplifiers, optical add/drop multiplexers, optical cross connects. (Text 2: 7.1,7.2,7.3,7.4) <b>Control and Management:</b> Network Management Functions, optical layer services and interfacing, Layers within the optical layer. (Text 2: 8.1,8.2,8.3)	
<b>Teaching-Learning Process</b>	Chalk and talk method, Power point presentation <b>RBT Level:</b> L1, L2, L3
<b>Course outcomes (Course Skill Set)</b> At the end of the course the student will be able to: <ol style="list-style-type: none"> <li>1. Classification and characterization of optical fibers with different modes of signal propagation.</li> <li>2. Describe the constructional features and the characteristics of optical fiber and optical devices used for signal transmission and reception.</li> <li>3. Identify the transmission characteristics for overall design considerations.</li> <li>4. Describe the client layers of the optical network.</li> <li>5. Attain knowledge of different network elements and optical layer services.</li> </ol>	
<b>Assessment Details (both CIE and SEE)</b> The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together  <b>Continuous Internal Evaluation (CIE):</b> CIE will be the same as other core theory courses. <b>CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.</b>  <b>Semester End Examination (SEE):</b>	

***For non-MCQ pattern of CIE and SEE***

**Continuous Internal Evaluation (CIE):**

At the beginning of the semester, the instructor/faculty teaching the course has to announce the methods of CIE for the course.

Three Unit Tests each of **20 Marks (duration 01 hour)**

1. First test at the end of 5<sup>th</sup> week of the semester
2. Second test at the end of the 10<sup>th</sup> week of the semester
3. Third test at the end of the 15<sup>th</sup> week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4<sup>th</sup> week of the semester
5. Second assignment at the end of 9<sup>th</sup> week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks (duration 01 hours)**

6. At the end of the 13<sup>th</sup> week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

**CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours**)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module.

**Suggested Learning Resources:**

**Text Books**

1. Gerd Keiser, 'Optical Fiber Communication', 5<sup>th</sup> Edition, McGraw Hill Education (India) Private Limited, 2016. ISBN:1-25-900687-5.
2. Kumar Sivarajan and Rajiv Ramaswamy, Galen Sasaki, 'Optical networks : A practical perspective', 3<sup>rd</sup> edition, Morgan Kauffman Publishing, 2010.

**Reference Books**

1. John M Senior, 'Optical Fiber Communications, Principles and Practice', 3<sup>rd</sup> Edition, Pearson Education, 2010. ISBN:978-81-317-3266-3
2. Biswajit Mukherjee, 'Optical Communication Networks', TMH, 1998.



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**VII Semester**

Optical & Satellite Communication			
Course Code	21EC741	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	3:0:0:1	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3
<b>Course objectives:</b> This course will enable students to: <ul style="list-style-type: none"><li>• Learn the basic principle of optical fiber communication with different modes of light propagation.</li><li>• Understand the transmission characteristics and losses in optical fiber.</li><li>• Study of optical components and its applications in optical communication networks.</li><li>• Understand the basic principle of satellite orbits and trajectories.</li><li>• Study of electronic systems associated with a satellite and the earth station.</li><li>• Study satellite applications focusing various domains services such as remote sensing, weather forecasting and navigation.</li></ul>			
<b>Teaching-Learning Process (General Instructions)</b> <p>The sample strategies, which the teacher can use to accelerate the attainment of the various course outcomes are listed in the following:</p> <ol style="list-style-type: none"><li>1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.</li><li>2. Show Video/animation films to explain the functioning of various techniques.</li><li>3. Encourage collaborative (Group) Learning in the class</li><li>4. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking</li><li>5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.</li><li>6. Topics will be introduced in multiple representations.</li><li>7. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.</li><li>8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.</li></ol>			
<b>Module-1</b>			
<b>Optical Fiber Structures:</b> Optical Fiber Modes and Configurations, Mode theory for circular waveguides, Single mode fibers, Fiber materials, Photonic Crystal Fibers, Fiber Optic Cables. <b>Attenuation and Dispersion:</b> Attenuation: Absorption, Scattering Losses, Bending loss, Signal Dispersion: Modal delay, Group delay, Material dispersion. [Text1 : 2.3[2.3.1 to 2.3.4], 2.4[2.4.1, 2.4.2],2.5, 2.7,2.8, 2.11, 3.1, 3.2].			
<b>Teaching-Learning Process</b>	Chalk and talk method, Power Point Presentation. Self-study topics: Optical Spectral bands, Basic optical laws and definitions. <b>RBT Level:</b> L1, L2, L3		
<b>Module-2</b>			
<b>Optical Sources and detectors:</b> Light Emitting Diode: LED Structures, Light source materials, Quantum efficiency and LED power, Laser Diodes: Modes and threshold conditions, Rate equations, External quantum efficiency, Resonant frequencies, Photodetectors: The pin Photodetector, Avalanche Photodiodes. <b>WDM Concepts:</b> Overview of WDM, Isolators and Circulators, Fiber grating filters, Dielectric thin-film filters, Diffraction Gratings.			

<b>Optical Amplifiers:</b> Basic Applications and types, Erbium doped fiber amplifiers. [Text1: 4.2 ,4.3, 6.1, 10.1, 10.3, 10.4, 10.5, 10.7, 11.1, 11.3.1,11.3.2]	
<b>Teaching-Learning Process</b>	Chalk and talk method, Power point presentation Self-study topics: Raman Amplifiers. <b>RBT Level:</b> L1, L2, L3
<b>Module-3</b>	
<b>Satellite Orbit and Trajectories:</b> Definition, Basic Principles, Orbital parameters, Injection velocity and satellite trajectory, Types of Satellite orbits. [Text2: 2.1, 2.2, 2.3,2.4,2.5] <b>Satellite In-orbit Operations:</b> Orbital perturbations, Satellite stabilization, Orbital effects on satellite's performance, Eclipses, Look angles: Azimuth angle, Elevation angle. [Text2: 3.3, 3.4, 3.5, 3.6, 3.7]	
<b>Teaching-Learning Process</b>	Chalk and talk method, Power Point Presentation. Self-study topics: Satellite launch sequence. <b>RBT Level:</b> L1, L2, L3
<b>Module-4</b>	
<b>Satellite Hardware:</b> Satellite Subsystems, Power supply subsystem, Attitude and Orbit control, Tracking, Telemetry and command subsystem, Payload. [Text2: 4.1, 4.5, 4.6, 4.7,4.8] <b>Earth Station:</b> Types of earth station, Architecture, Design considerations, Testing, Earth station Hardware, Satellite tracking. [Text2: 8.1, 8.2, 8.3,8.4,8.5,8.6]	
<b>Teaching-Learning Process</b>	Chalk and talk method, Power Point Presentation. Self-study topics: Mechanical structure and propulsion subsystem <b>RBT Level:</b> L1, L2, L3
<b>Module-5</b>	
<b>Communication Satellites:</b> Introduction, Related Applications, Frequency Bands, Payloads, Satellite Vs. Terrestrial Networks, Satellite Television, Satellite Data Communication Services. <b>Applications:</b> Remote Sensing Satellites: Classification, Orbits, payloads. Weather Forecasting Satellites: Overview, Fundamentals, orbits and payload. Global Positioning Satellite System.	
<b>Teaching-Learning Process</b>	Chalk and talk method, Power point presentation Self-study topics: Regional, National and International Satellite systems <b>RBT Level:</b> L1, L2, L3
<b>Course outcomes (Course Skill Set)</b> At the end of the course the student will be able to: <ol style="list-style-type: none"> <li>1. Classification and characterization of optical fibers and devices used for optical communication.</li> <li>2. Understand the principle of operation of optical devices used for multiplexing and amplification of light.</li> <li>3. Describe the satellite orbits and its trajectories with the definitions of parameters associated with it.</li> <li>4. Describe the electronic hardware systems associated with the satellite subsystem and earth station.</li> <li>5. Understand the functioning of satellites for communication, remote sensing, and weather and navigation applications.</li> </ol>	
<b>Assessment Details (both CIE and SEE)</b> The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together. <b>Continuous Internal Evaluation:</b> Three Unit Tests each of <b>20 Marks (duration 01 hour)</b>	

1. First test at the end of 5<sup>th</sup> week of the semester
2. Second test at the end of the 10<sup>th</sup> week of the semester
3. Third test at the end of the 15<sup>th</sup> week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4<sup>th</sup> week of the semester
5. Second assignment at the end of 9<sup>th</sup> week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks (duration 01 hours)**

6. At the end of the 13<sup>th</sup> week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

**CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours**)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module.

**Suggested Learning Resources:**

**Text Books:**

1. Gerd Keiser, Optical Fiber Communication, 5<sup>th</sup> Edition, McGraw Hill Education (India) Private Limited, 2016. ISBN:1-25-900687-5.
2. Anil K Maini, Varsha Agrawal, Satellite Communication, Wiley India Pvt. Ltd., 2015, ISBN: 978-81-265-2071-8.

**Reference Books:**

1. John M Senior, Optical Fiber Communications, Principles and Practice, 3<sup>rd</sup> Edition, Pearson Education, 2010, ISBN:978-81-317-3266-3
2. Timothy Pratt, Charles Bostian, Jeremy Allnutt, Satellite Communications, 2<sup>nd</sup> Edition, Wiley India Pvt. Ltd , 2017, ISBN: 978-81-265-0833-4
3. Dennis Roddy, Satellite Communications, 4<sup>th</sup> Edition, McGraw- Hill International edition, 2006.

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**VII Semester**

ARM Embedded Systems			
Course Code	21EC742	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	3:0:0:1	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3
<b>Course objectives:</b> This course will enable students to: <ul style="list-style-type: none"><li>• Explain the architectural features and instructions of 32 bit ARM microcontroller</li><li>• Develop Programs using the various instructions of ARM for different Applications.</li><li>• Understand the basic hardware components and their selection method based on the characteristics and</li><li>• Attributes of an embedded system.</li><li>• Develop the hardware software co-design and firmware design approaches.</li><li>• Explain the need of real time operating system for embedded system applications.</li></ul>			
<b>Teaching-Learning Process (General Instructions)</b> The sample strategies, which the teacher can use to accelerate the attainment of the various course outcomes are listed in the following: <ol style="list-style-type: none"><li>1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.</li><li>2. Show Video/animation films to explain the functioning of various techniques.</li><li>3. Encourage collaborative (Group) Learning in the class</li><li>4. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking</li><li>5. Adopt Problem Based Learning (PBL), which fosters students’ Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.</li><li>6. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.</li><li>7. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.</li><li>8. Give programming assignments.</li></ol>			
<b>Module-1</b>			
<b>ARM Embedded System:</b> RISC Design Philosophy, ARM design Philosophy, Embedded System hardware and Embedded System software. <b>ARM Processor Fundamentals:</b> Registers, Current Program Status Registers, Pipeline, Exceptions, Interrupts and the Vector table, Core Extensions, Architecture Revisions, ARM processor families (Text1 : Chapter 1 and Chapter 2 )			
<b>Teaching-Learning Process</b>	Chalk and talk method, Power point presentation <b>RBT Level:</b> L1, L2, L3		
<b>Module-2</b>			
<b>ARM Instructions:</b> Introduction, Data Processing Instructions, Branch Instructions, Load – Store Instructions Software Instructions, Program Status Register Instructions, Conditional Execution. <b>Thumb Instructions:</b> Thumb register usage, ARM – Thumb Interworking, Other branch Instructions, Data Processing instructions, Single and Multiple Register Load Store Instructions, Stack Instructions, Software Interrupt Instructions. (Text1: Chapter 3 and chapter 4,)			

<b>Teaching-Learning Process</b>	Chalk and talk method, Power point presentation <b>RBT Level:</b> L1, L2, L3
<b>Module-3</b>	
<p><b>Embedded System Components:</b> Embedded Vs General computing system, Classification of Embedded systems, Major applications and purpose of ES. Elements of an Embedded System (Block diagram and explanation), Differences between RISC and CISC, Harvard and Princeton, Big and Little Endian formats, Memory (ROM and RAM types), Sensors, Actuators, Optocoupler, Communication Interfaces (I2C, SPI, IrDA, Bluetooth, Wi-Fi, Zigbee only)</p> <p>(Text 2: All the Topics from Ch-1 and Ch-2 (Fig and explanation before 2.1) 2.1.1.6 to 2.1.1.8, 2.2 to 2.2.2.3, 2.3 to 2.3.2, 2.3.3.3, selected topics of 2.4.1 and 2.4.2 only).</p>	
<b>Teaching-Learning Process</b>	Chalk and talk method, Power point presentation <b>RBT Level:</b> L1, L2, L3
<b>Module-4</b>	
<p><b>Embedded System Design Concepts:</b> Characteristics and Quality Attributes of Embedded Systems, Operational and non-operational quality attributes, Embedded Systems-Application and Domain specific, Hardware Software Co-Design and Program Modeling (excluding UML), Embedded firmware design and development (excluding C language).</p> <p>Text 2: Ch-3, Ch-4 (4.1, 4.2.1 and 4.2.2 only), Ch-7 (Sections 7.1, 7.2 only), Ch-9 (Sections 9.1, 9.2, 9.3.1, 9.3.2 only)</p>	
<b>Teaching-Learning Process</b>	Chalk and talk method, Power point presentation <b>RBT Level:</b> L1, L2, L3
<b>Module-5</b>	
<p><b>RTOS and IDE for Embedded System Design:</b> Operating System basics, Types of operating systems, Task, process and threads (Only POSIX Threads with an example program), Thread preemption, Preemptive Task scheduling techniques, Task Communication, Task synchronization issues – Racing and Deadlock, Concept of Binary and counting semaphores (Mutex example without any program), How to choose an RTOS, Integration and testing of Embedded hardware and firmware, Embedded system Development Environment – Block diagram (excluding Keil), Disassembler/decompiler, simulator, emulator and debugging techniques</p> <p>(Text 2: Ch-10 (Sections 10.1, 10.2, 10.3, 10.5.2, 10.7, 10.8.1.1, 10.8.1.2, 10.8.2.2, 10.10 only), Ch-12, Ch-13 (a block diagram before 13.1, 13.3, 13.4, 13.5, 13.6 only)</p>	
<b>Teaching-Learning Process</b>	Chalk and talk method, Power point presentation <b>RBT Level:</b> L1, L2, L3
<p><b>Course outcomes (Course Skill Set)</b></p> <p>At the end of the course the student will be able to:</p> <ol style="list-style-type: none"> <li>1. Describe the architectural features and instructions of 32 bit microcontroller ARM Cortex M3.</li> <li>2. Apply the knowledge gained for Programming ARM Cortex M3 for different applications.</li> <li>3. Understand the basic hardware components and their selection method based on the characteristics and attributes of an embedded system.</li> <li>4. Develop the hardware software co-design and firmware design approaches.</li> <li>5. Explain the need of real time operating system for embedded system applications.</li> </ol>	
<p><b>Assessment Details (both CIE and SEE)</b></p> <p>The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.</p>	

**Continuous Internal Evaluation:**

Three Unit Tests each of **20 Marks (duration 01 hour)**

1. First test at the end of 5<sup>th</sup> week of the semester
2. Second test at the end of the 10<sup>th</sup> week of the semester
3. Third test at the end of the 15<sup>th</sup> week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4<sup>th</sup> week of the semester
5. Second assignment at the end of 9<sup>th</sup> week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks (duration 01 hours)**

6. At the end of the 13<sup>th</sup> week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

**CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours**)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module.

**Suggested Learning Resources:****Text Books:**

1. Andrew N Sloss, "ARM System Developer's guide", Elsevier Publications, 2016
2. Shibu K V, "Introduction to Embedded Systems", Tata McGraw Hill Education Private Limited, 2<sup>nd</sup> Edition.

**Reference Books:**

1. James K Peckol, "Embedded systems- A contemporary design tool", John Wiley, 2008.
2. Yifeng Zhu, "Embedded Systems with Arm Cortex-M Microcontrollers in Assembly Language and C", 2<sup>nd</sup> Ed., Man Press LLC ©, 2015.
3. K V K K Prasad, "Embedded real time systems", Dreamtech publications, 2003.
4. Rajkamal, "Embedded Systems", 2<sup>nd</sup> Edition, McGraw hill Publications, 2010.

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**VII Semester**

Basic Digital Image Processing			
Course Code	21EC743	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	2:0:2:1	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3
<b>Course objectives:</b> <ul style="list-style-type: none"><li>• Understand the fundamentals of digital image processing</li><li>• Understand the image enhancement techniques in spatial domain used in digital image processing</li><li>• Understand the frequency domain enhancement techniques in digital image processing</li><li>• Understand the Color Image Processing in digital image processing</li><li>• Understand the image restoration techniques and methods used in digital image processing</li></ul>			
<b>Teaching-Learning Process (General Instructions)</b> <p>These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.</p> <ol style="list-style-type: none"><li>1. Show Video/animation films to explain the functioning of various image processing concepts.</li><li>2. Encourage cooperative (Group) Learning through puzzles, diagrams, coding etc., in the class.</li><li>3. Encourage students to ask questions and investigate their own ideas helps improve their problem-solving skills as well as gain a deeper understanding of academic concepts.</li><li>4. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking</li><li>5. Students are encouraged to do coding based projects to gain knowledge in image processing.</li><li>6. Adopt Problem Based Learning (PBL), which fosters students’ Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.</li><li>7. Topics will be introduced in multiple representations.</li><li>8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.</li><li>9. Arrange visits to nearby PSUs such as CAIR(DRDO), NAL, BEL, ISRO, etc., and small-scale software industries to give industry exposure.</li></ol>			
<b>Module-1</b>			
<b>Digital Image Fundamentals:</b> What is Digital Image Processing?, Origins of Digital Image Processing, Examples of fields that use DIP, Fundamental Steps in Digital Image Processing, Components of an Image Processing System, Elements of Visual Perception, Image Sensing and Acquisition, Image Sampling and Quantization, Some Basic Relationships Between Pixels. [Text 1: Chapter 1, Chapter 2: Sections 2.1 to 2.5]			
<b>Teaching-Learning Process</b>	Chalk and talk method, PowerPoint Presentation, YouTube videos, Videos on Image processing applications Self-study topics: Arithmetic and Logical operations Practical topics: Problems on Basic Relationships Between Pixels. <b>RBT Level:</b> L1, L2, L3		
<b>Module-2</b>			
<b>Spatial Domain:</b> Some Basic Intensity Transformation Functions, Histogram Processing, Fundamentals of Spatial Filtering, Smoothing Spatial Filters, Sharpening Spatial Filters [Text 1: Chapter 3: Sections 3.2 to 3.6]			

<b>Teaching-Learning Process</b>	Chalk and talk method, PowerPoint Presentation, YouTube videos and animations of Intensity Transformation Functions, Histogram Processing, Spatial domain filters. Self-study topics: Point, line and edge detection. Practical topics: Problems on Intensity Transformation Functions, Histogram, Spatial domain filters <b>RBT Level:</b> L1, L2, L3
<b>Module-3</b>	
<b>Frequency Domain:</b> Basics of Filtering in the Frequency Domain, Image Smoothing and Image Sharpening Using Frequency Domain Filters. [Text 1: Chapter 4: Sections 4.7 to 4.9]	
<b>Teaching-Learning Process</b>	Chalk and talk method, PowerPoint Presentation, YouTube videos on frequency domain filtering, Color image processing. Self-study topics: Basic concept of segmentation. Practical topics: Problems on Image smoothing and sharpening <b>RBT Level:</b> L1, L2, L3
<b>Module-4</b>	
<b>Color Image Processing:</b> Color Fundamentals, Color Models, Pseudo-color Image Processing. [Text 1: Chapter 6: Sections 6.1 to 6.3]	
<b>Teaching-Learning Process</b>	Chalk and talk method, PowerPoint Presentation, YouTube videos on Color image processing. Practical topics: Problems on Pseudo-color Image Processing <b>RBT Level:</b> L1, L2, L3
<b>Module-5</b>	
<b>Restoration:</b> A model of the Image Degradation/Restoration Process, Noise models, Restoration in the Presence of Noise Only using Spatial Filtering and Frequency Domain Filtering, Inverse Filtering, Minimum Mean Square Error (Wiener) Filtering. [Text 1: Chapter 5: Sections 5.1, to 5.4.3, 5.7, 5.8]	
<b>Teaching-Learning Process</b>	Chalk and talk method, PowerPoint Presentation, YouTube videos on Noise models, filters and its applications. Self-study topics: Linear position invariant degradation, Estimation of degradation function. <b>RBT Level:</b> L1, L2, L3
<b>Course outcome (Course Skill Set)</b> At the end of the course the student will be able to: <ol style="list-style-type: none"> <li>1. Understand image formation and the role of human visual system plays in perception of gray and color image data.</li> <li>2. Apply image processing techniques in spatial domains.</li> <li>3. Apply image processing techniques in frequency (Fourier) domains.</li> <li>4. Conduct independent study and analysis of Image Enhancement techniques.</li> </ol>	
<b>Assessment Details (both CIE and SEE)</b> The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.	
<b>Continuous Internal Evaluation:</b> Three Unit Tests each of <b>20 Marks (duration 01 hour)</b> <ol style="list-style-type: none"> <li>1. First test at the end of 5<sup>th</sup> week of the semester</li> <li>2. Second test at the end of the 10<sup>th</sup> week of the semester</li> </ol>	



<p>3. Third test at the end of the 15<sup>th</sup> week of the semester</p> <p>Two assignments each of <b>10 Marks</b></p> <p>4. First assignment at the end of 4<sup>th</sup> week of the semester</p> <p>5. Second assignment at the end of 9<sup>th</sup> week of the semester</p> <p>Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for <b>20 Marks (duration 01 hours)</b></p> <p>6. At the end of the 13<sup>th</sup> week of the semester</p> <p>The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be <b>scaled down to 50 marks</b></p> <p>(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).</p> <p><b>CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.</b></p> <p><b>Semester End Examination:</b></p> <p>Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (<b>duration 03 hours</b>)</p> <ol style="list-style-type: none"> <li>1. The question paper will have ten questions. Each question is set for 20 marks.</li> <li>2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), <b>should have a mix of topics</b> under that module.</li> </ol> <p>The students have to answer 5 full questions, selecting one full question from each module.</p>
<p><b>Suggested Learning Resources:</b></p> <p><b>Text Book:</b></p> <p>Digital Image Processing- Rafael C Gonzalez and Richard E Woods, PHI, 3<sup>rd</sup> Edition, 2010.</p> <p><b>Reference Books:</b></p> <ol style="list-style-type: none"> <li>1. Digital Image Processing- S Jayaraman, S Esakkirajan, T Veerakumar, Tata McGraw Hill, 2014.</li> <li>2. Fundamentals of Digital Image Processing- A K Jain, PHI Learning Private Limited 2014.</li> </ol>
<p><b>Web links and Video Lectures (e-Resources)</b></p> <ul style="list-style-type: none"> <li>• Image databases, <a href="https://imageprocessingplace.com/root_files_V3/image_databases.htm">https://imageprocessingplace.com/root_files_V3/image_databases.htm</a></li> <li>• Student support materials, <a href="https://imageprocessingplace.com/root_files_V3/students/students.htm">https://imageprocessingplace.com/root_files_V3/students/students.htm</a></li> <li>• NPTEL Course, Introduction to Digital Image Processing, <a href="https://nptel.ac.in/courses/117105079">https://nptel.ac.in/courses/117105079</a></li> <li>• Computer Vision and Image Processing, <a href="https://nptel.ac.in/courses/108103174">https://nptel.ac.in/courses/108103174</a></li> <li>• Image Processing and Computer Vision – Matlab and Simulink, <a href="https://in.mathworks.com/solutions/image-video-processing.html">https://in.mathworks.com/solutions/image-video-processing.html</a></li> </ul>
<p><b>Activity Based Learning (Suggested Activities in Class)/ Practical Based learning</b></p> <ul style="list-style-type: none"> <li>• Simulink models for Image processing</li> </ul>

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**VII Semester**

Basic Digital Signal Processing			
Course Code	21EC744	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	3:0:0:1	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3
<b>Course objectives:</b> This course will enable students to: <ul style="list-style-type: none"><li>• <b>Preparation:</b> To prepare students with fundamental knowledge/ overview in the field of Signal Processing</li><li>• <b>Core Competence:</b> To equip students with a basic foundation of Signal Processing by delivering the mathematical description of discrete time signals and systems, classifying signals into different categories based on their properties, analyzing Linear Time Invariant (LTI)systems in time and transform domains, basics of FIR &amp; IIR Filter Design</li></ul>			
<b>Teaching-Learning Process (General Instructions)</b> These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes. <ol style="list-style-type: none"><li>1. Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.</li><li>2. Show Video/animation films to explain the different concepts Digital Signal Processing.</li><li>3. Encourage collaborative (Group) Learning in the class.</li><li>4. Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking.</li><li>5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.</li><li>6. Topics will be introduced in a multiple representation.</li><li>7. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.</li><li>8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.</li><li>9. Adopt Flipped class technique by sharing the materials / Sample Videos prior to the class and have discussions on the that topic in the succeeding classes</li><li>10. Give Programming Assignments.</li></ol>			
<b>Module-1</b>			
Signal Definition, Signal Classification, System definition, System classification, for both continuous time and discrete time, Definition of LTI systems (Chapter1)			
<b>Teaching-Learning Process</b>	Chalk and talk method, YouTube videos, Flipped Class Technique, Programming assignments <b>RBT Level:</b> L1, L2, L3		
<b>Module-2</b>			
Introduction to Fourier Transform, Fourier Series, Relating the Laplace Transform to Fourier Transform, Frequency response of continuous time systems (Chapter3)			
<b>Teaching-Learning Process</b>	Chalk and talk method, YouTube videos, Flipped Class Technique, Programming assignments <b>RBT Level:</b> L1, L2, L3		

<b>Module-3</b>	
Frequency response of ideal analog filters, Salient features of Butterworth filters Design and implementation of Analog Butterworth filters to meet given specifications (Chapter8)	
<b>Teaching-Learning Process</b>	Chalk and talk method, YouTube videos, Flipped Class Technique, Programming assignments <b>RBT Level:</b> L1, L2, L3
<b>Module-4</b>	
Sampling Theorem- Statement and proof, converting the analog signal to a digital signal, Practical sampling, The Discrete Fourier Transform, Properties of DFT, Comparing the frequency response of analog and digital systems (FFT not included) (Chapter 3,4)	
<b>Teaching-Learning Process</b>	Chalk and talk method, YouTube videos, Flipped Class Technique, Programming assignments <b>RBT Level:</b> L1, L2, L3
<b>Module-5</b>	
Definition of FIR and IIR filters, Frequency response of ideal digital filters. Transforming the Analog Butterworth filter to the Digital IIR Filter using BLT to meet given specifications. Design of Low pass / High pass FIR Filters using the Window technique, to meet given specifications, Comparing the designed filter with the desired filter frequency response (Chapter8)	
<b>Teaching-Learning Process</b>	Chalk and talk method, Power point presentation, YouTube videos, Flipped Class Technique, Programming assignments <b>RBT Level:</b> L1, L2, L3
<b>Course outcome (Course Skill Set)</b> At the end of the course the student will be able to: <ol style="list-style-type: none"> <li>1. Understand the continuous time and discrete time signals and systems, in time and frequency domain</li> <li>2. Apply the concepts of signals and systems to obtain the desired parameter/representation</li> <li>3. Design analog/digital filters to meet given specifications</li> <li>4. Design and implement the analog filter using components/suitable simulation tools</li> <li>5. Design and implement the digital filter (FIR/IIR) using suitable simulation tools, and record the input and output of the filter for the given audio signal</li> </ol>	
<b>Assessment Details (both CIE and SEE)</b> The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.	
<b>Continuous Internal Evaluation:</b> Three Unit Tests each of <b>20 Marks (duration 01 hour)</b> <ol style="list-style-type: none"> <li>1. First test at the end of 5<sup>th</sup> week of the semester</li> <li>2. Second test at the end of the 10<sup>th</sup> week of the semester</li> <li>3. Third test at the end of the 15<sup>th</sup> week of the semester</li> </ol> Two assignments each of <b>10 Marks</b> <ol style="list-style-type: none"> <li>4. First assignment at the end of 4<sup>th</sup> week of the semester</li> <li>5. Second assignment at the end of 9<sup>th</sup> week of the semester</li> </ol> Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for <b>20 Marks (duration 01 hours)</b> <ol style="list-style-type: none"> <li>6. At the end of the 13<sup>th</sup> week of the semester</li> </ol> The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be <b>scaled down to 50 marks</b>	

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

**CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours**)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module.

**Suggested Learning Resources:**

**Text Books:**

1. 'Signals and Systems', Simon Haykin and Barry Van Veen, Wiley.
2. "Fundamentals of Digital Signal Processing", Lonnie C Ludeman, John Wiley and Sons, 1986.

**Reference Books:**

3. 'Theory and Application of Digital Signal Processing', Rabiner and Gold
4. 'Signals and Systems', Schaum's Outline series
5. 'Digital Signal Processing', Schaum's Outline series

**Web links and Video Lectures (e-Resources)**

By Prof. S C Dutta Roy, IIT Delhi  
<https://nptel.ac.in/courses/117102060>

**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

- Programming Assignments / Mini Projects can be given to improve programming skills

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**VII Semester**

E-waste Management			
Course Code	21EC745	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	3:0:0:1	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3
<b>Course objectives:</b> <ul style="list-style-type: none"><li>• <b>Current Status:</b> According to a report on e-waste presented by the United Nations (UN) in World Economic Forum on January 24, 2019, the waste stream reached 48.5 MT in 2018. With such a large quantity of e-waste being generated each year, the future of e-waste recycling in India looks pretty bright. The E-waste (Management) Rules, 2016, enacted on October 1, 2017, added over 21 products (Schedule-I) under the purview of the rule.</li><li>• <b>Purview:</b> This course covers an extensive review of e-waste management in India. With a focus on the evolution of legal frameworks in India and the world, it presents impacts and outcomes; challenges and opportunities; and management strategies and practices to deal with e-waste. It also includes a survey of pan-India initiatives and trajectories of law-driven initiatives for effective e-waste management along with responses from industries and producers.</li><li>• <b>Scope:</b> There is a considerable scope for e-waste recycling in India. It is not only a solution to help mitigate e-waste management issues, but it also helps to generate employment. With the rise in e-waste recycling plants, the demand for employees with all levels of qualification and skills also increases.</li></ul>			
<b>Teaching-Learning Process (General Instructions)</b> <p>These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.</p> <ol style="list-style-type: none"><li>1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.</li><li>2. Show Video/animation films to explain the functioning of various techniques.</li><li>3. Encourage collaborative (Group) Learning in the class</li><li>4. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking</li><li>5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.</li><li>6. Topics will be introduced in multiple representations.</li><li>7. Discuss how every concept can be applied to the real world - and when that's possible, it helps to improve the students' understanding.</li><li>8. Arrange visits to nearby industries to give industry exposure.</li></ol>			
<b>Module-1</b>			
<b>Sustainable development and e-waste management:</b> Importance of electrical and electronic equipment in a nation's development, and e-waste as toxic companion of digital era, I: Let's understand e-waste, II: E-waste statistics: quantities, collection and recycling, E-waste categories and harmonising statistics, III: An overview on status of e-waste related legislation across the globe; IV: UN initiatives for e-waste management: creating partnerships and achieving Agenda 2030; V: Indian scenario: e-waste generation, collection and recycling.			
<b>Teaching-Learning Process</b>	Chalk and talk method, YouTube videos. <b>RBT Level:</b> L1, L2		
<b>Module-2</b>			
<b>Extended producer responsibility: a mainstay for e-waste management:</b> Evolution of concept of 'extended producer responsibility', EPR applied for waste management and extended for e-waste			

<p>management, EPR: goals, implementation, and challenges for e-waste management, EPR implemented for e-waste management under the existing regulatory frameworks in different countries, Role of a PRO prescribed in regulatory framework, Considerations for successful implementation of EPR, Challenges in implementation of EPR for e-waste management, Impact of EPR, EPR and e-waste management in India.</p> <p><b>Toxicity and impacts on environment and human health:</b> Toxicity, recycling, and regulations, I: Environmental concerns, II: Human health concerns.</p>	
<b>Teaching-Learning Process</b>	Chalk and talk method, PowerPoint Presentation, More examples relating to applications. <b>RBT Level:</b> L1, L2, L3
<b>Module-3</b>	
<p><b>Treating e-waste, resource efficiency, and circular economy:</b> Safe environment, resource use, and circular economy, Circular economy: recycling, resource recovery, and resource efficiency, Potentials of urban mining in circular economy, Recycling and resource efficiency related challenges to the circular economy, Urban mining, recycling, resource use, resource efficiency, and circular economy in India.</p> <p><b>E-waste management through legislations in India:</b> I: Historical backdrop of regulatory regime for e-waste in India, II: E-waste (management) Rules, 2016 and E-waste (management) Amendment Rules, 2018, III: Analysing performance of EPR and CPCB as regulatory mechanisms, IV: Legal cases and judicial directives.</p>	
<b>Teaching-Learning Process</b>	Chalk and talk method, PowerPoint Presentation <b>RBT Level:</b> L1, L2, L3
<b>Module-4</b>	
<p><b>Strategies and initiatives for dealing with e-waste in India:</b> I: Overview of pan-India initiatives for dealing with e-waste during 2000 and 2012, II: Law-driven e-waste management – initiatives by the government, non-government agencies, and judiciary.</p>	
<b>Teaching-Learning Process</b>	Chalk and talk method, PowerPoint Presentation. <b>RBT Level:</b> L1, L2, L3
<b>Module-5</b>	
<p><b>Moving towards horizons:</b> I: Legal and judicial domain, II: Economic concerns, III: Environment concerns, IV: Recycling culture/recycling society.</p>	
<b>Teaching-Learning Process</b>	Chalk and talk method, PowerPoint Presentation, More examples relating to applications. <b>RBT Level:</b> L1, L2, L3
<p><b>Course outcome (Course Skill Set)</b></p> <p>At the end of the course the student will be able to:</p> <ol style="list-style-type: none"> <li>1. Understand the existing discourse on e-waste and its management, statistics across the world, opportunities, and challenges w.r.t. regulatory framework, SDGs, CE, and LCIA (Life Cycle Impact Assessment) and MFA (Material Flow Analysis), Indian scenario.</li> <li>2. Describe EPR, a regulatory framework for achieving specified goals across different countries and impacts on environment and human health.</li> <li>3. Explain themes in the context of resource use and sustainable development. Urban mining, informal sector operations and need for resource use policy, financial support for recycling infrastructure building, etc. in Indian context and also explain to what extent – different aspects of e-waste management have been incorporated in the existing regulatory framework in comparison with international legislatures.</li> <li>4. Identify and infer pan-Indian initiatives dealing with e-waste management, ranging from building knowledge base through research and social action by different stakeholders to technological and legal advancements, and industrial initiatives. Analyse roadmap for the Agenda 2030.</li> <li>5. Use opportunities and challenges around four domains: legal and judicial domain; economic concerns; recycling culture/society; and environment concerns.</li> </ol>	

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous Internal Evaluation:**

Three Unit Tests each of **20 Marks (duration 01 hour)**

1. First test at the end of 5<sup>th</sup> week of the semester
2. Second test at the end of the 10<sup>th</sup> week of the semester
3. Third test at the end of the 15<sup>th</sup> week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4<sup>th</sup> week of the semester
5. Second assignment at the end of 9<sup>th</sup> week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks (duration 01 hours)**

6. At the end of the 13<sup>th</sup> week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

**CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours**)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module.

**Suggested Learning Resources:****Text Book:**

Varsha Bhagat Gangulay, 'E-Waste Management', Taylor and Francis, 2022.

**Web links and Video Lectures (e-Resources)**

- <https://link.springer.com/book/10.1007/978-3-030-14184-4>
- [https://rajyasabha.nic.in/rsnew/publication\\_electronic/E-Waste\\_in\\_india.pdf](https://rajyasabha.nic.in/rsnew/publication_electronic/E-Waste_in_india.pdf)
- <https://greene.gov.in/wp-content/uploads/2018/01/E-waste-Vol-II-E-waste-Management-Manual.pdf>
- <https://nptel.ac.in/courses/105105169>

**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

- Groups can be made to conduct a survey on the present scenario of India and top 5 countries facing ewaste management challenges.
- Industry visits to give an exposure of the e waste management process and also business.
- Case studies to develop e-waste management models.
- Survey of few e-waste management companies can be carried out and submit report.

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**VII Semester**

Advanced Design Tools for VLSI			
Course Code	21EC721	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	3:0:0:1	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3
<b>Course objectives:</b> <ul style="list-style-type: none"><li>• Impart knowledge of EDA tools and methodology for FPGA</li><li>• Learn principles of IP core for FPGA and embedded systems</li><li>• Infer the concept of machine learning in fabrication and physical design</li></ul>			
<b>Teaching-Learning Process (General Instructions)</b> <p>The sample strategies, which the teacher can use to accelerate the attainment of the various course outcomes are listed in the following:</p> <ol style="list-style-type: none"><li>1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.</li><li>2. Arrange visits to nearby PSUs and small-scale communication industries.</li><li>3. Show Video/animation films to explain the functioning of various techniques.</li><li>4. Encourage collaborative (Group) Learning in the class</li><li>5. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking</li><li>6. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.</li><li>7. Topics will be introduced in multiple representations.</li><li>8. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.</li><li>9. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.</li></ol>			
<b>Module-1</b>			
<b>Introduction:</b> Introduction, Prologue, EDA: From Methodologies, Algorithms, Tools to Integrated Circuits and Systems, EDA from Halcyon's Days to the Blooming Paradigm of Chip Industry, Categories of the EDA Tools, Quo Vadis, EDA? The Challenges and Opportunities, Designing the System as SoC Using the Soft IP Cores, Types of IP Cores, Design Issues Pertaining to the Soft IP Cores Text Book1: 1.1 to 1.5, 1.7 to 1.10			
<b>Development of FPGA Based Network on Chip for Circumventing Spam:</b> Introduction, Conception of the Spam Mail, FPGA Based Network on Chip for Circumventing Spam, Tools Infrastructure and Design Flow, Introducing Hardware-Software Co-design, Hardware Software Co-design, Framework Proposed in the Present Case Study, Description of System at Higher Level, Resolving the System a Step Down, System Design, Development of Soft IP Core of Bloom Filter, Presenting System Design of Purely Software Modules, Integrating of the Hardware-Software Modules Using EDK Text Book1: 2.1 to 2.13			
<b>Teaching-Learning Process</b>	Chalk and talk method, , PowerPoint Presentation, YouTube videos <b>RBT Level:</b> L1, L2, L3		
<b>Module-2</b>			
<b>Analog Front End and FPGA Based Soft IP Core for ECG Logger:</b> Prior Art, The Very Rationale of the System, Analog Front End of the Setup, VHDL Implementation of the ECG Soft IP Core, ModelSim Simulation Results, Synthesis Results Using Mentor Graphics Tool, Monitoring the ECG Using MODEM			



Based Setup, ECG Signal Reconstruction Mechanism at the Hospital End, VHDL Listing for Driving the Analog Demultiplexer and Serial DAC from Spartan-3E FPGA, Discussion Regarding the VHDL Implementation, ModelSim Simulation Results, Synthesis Results Using Mentor Graphics Tool: Leonardo Spectrum. Text Book1: 3.1 to 3.12	
<b>Teaching-Learning Process</b>	Chalk and talk method/Power point presentation <b>RBT Level:</b> L1, L2, L3
<b>Module-3</b>	
<b>FPGA Based Multifunction Interface for Embedded Applications:</b> Introduction, Universal FPGA Based Interface for High End Embedded Applications, Soft IP Core for the LCD Interface, Soft IP Core for the DAC Interface, Handel C Listing of the Soft IP Core for the DAC Interface, Soft IP Core for the Linear Tech LTC6912-1 Dual Amp, Soft IP Core for the ADC Interface, Soft IP Core for the VGA Interface, Soft IP Core for the Keyboard Interface, Triangular Wave Generator Using DAC Text Book1: 4.1 - 4.10	
<b>Teaching-Learning Process</b>	Chalk and talk method, Power point presentation <b>RBT Level:</b> L1, L2, L3
<b>Module-4</b>	
<b>Machine Learning for Compact Lithographic Process Models:</b> Introduction, The Lithographic Patterning Process, Machine Learning of Compact Process Models, Neural Network Compact Patterning Models. Text Book2: 2.1 to 2.4  <b>Machine Learning for Mask Synthesis:</b> Introduction, Machine Learning-Guided OPC, Machine Learning-Guided EPC. Text Book2: 3.1 to 3.4	
<b>Teaching-Learning Process</b>	Chalk and talk method, Power point presentation <b>RBT Level:</b> L1, L2, L3
<b>Module-5</b>	
<b>Machine Learning in Physical Verification, Mask Synthesis, and Physical Design:</b> Introduction, Machine Learning in Physical Verification, Machine Learning in Mask Synthesis, Machine Learning in Physical Design. Text Book2: 4.1 to 4.4	
<b>Teaching-Learning Process</b>	Chalk and talk method, Power point presentation <b>RBT Level:</b> L1, L2, L3
<b>Course outcome (Course Skill Set)</b> At the end of the course the student will be able to: <ol style="list-style-type: none"> <li>1. Demonstrate the EDA methodologies and Tools for FPGA based NoC</li> <li>2. Interpretation of soft core for ECG logger</li> <li>3. Interfacing of DAC for embedded Application</li> <li>4. Interpretation of Machine Learning for fabrication</li> <li>5. Interpretation of ML in physical design</li> </ol>	
<b>Assessment Details (both CIE and SEE)</b> The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.	
<b>Continuous Internal Evaluation:</b> Three Unit Tests each of <b>20 Marks (duration 01 hour)</b> <ol style="list-style-type: none"> <li>1. First test at the end of 5<sup>th</sup> week of the semester</li> </ol>	

2. Second test at the end of the 10<sup>th</sup> week of the semester
3. Third test at the end of the 15<sup>th</sup> week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4<sup>th</sup> week of the semester
5. Second assignment at the end of 9<sup>th</sup> week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks (duration 01 hours)**

6. At the end of the 13<sup>th</sup> week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

**CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours**)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module.

**Suggested Learning Resources:**

**Text Books:**

1. Rajanish K Kamat, Santosh A Shinde, Pawan K Gaikwad, Hansraj Guhilot, 'Harnessing VLSI System Design with EDA Tools', Springer, 2012.
2. Ibrahim (Abe) M Elfadel, Duane S Boning, Xin Li, 'Machine Learning in VLSI Computer-Aided Design', Springer, 2011.

**Web links and Video Lectures (e-Resources)**

- <https://www.digimat.in/nptel/courses/video/117101004/L01.html>
- [https://www.youtube.com/watch?v=zC5b5\\_7oRKK](https://www.youtube.com/watch?v=zC5b5_7oRKK)

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**VII Semester**

<b>Digital Image Processing</b>			
Course Code	<b>21EC722</b>	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	3:0:0:1	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3
<b>Course objectives:</b> <ul style="list-style-type: none"> <li>• Understand the fundamentals of digital image processing.</li> <li>• Understand the image transform used in digital image processing.</li> <li>• Understand the image enhancement techniques in spatial domain used in digital image processing.</li> <li>• Understand the Color Image Processing and frequency domain enhancement techniques in digital image processing.</li> <li>• Understand the image restoration techniques and methods used in digital image processing.</li> </ul>			
<b>Teaching-Learning Process (General Instructions)</b> These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes. <ol style="list-style-type: none"> <li>1. Show Video/animation films to explain the functioning of various image processing concepts.</li> <li>2. Encourage cooperative (Group) Learning through puzzles, diagrams, coding etc., in the class.</li> <li>3. Encourage students to ask questions and investigate their own ideas helps improve their problem-solving skills as well as gain a deeper understanding of academic concepts.</li> <li>4. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking</li> <li>5. Students are encouraged to do coding based projects to gain knowledge in image processing.</li> <li>6. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.</li> <li>7. Topics will be introduced in multiple representations.</li> <li>8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding</li> <li>9. Arrange visits to nearby PSUs such as CAIR (DRDO), NAL, BEL, ISRO, etc., and small-scale software industries to give industry exposure.</li> </ol>			
<b>Module-1</b>			
<b>Digital Image Fundamentals:</b> What is Digital Image Processing?, Origins of Digital Image Processing, Examples of fields that use DIP, Fundamental Steps in Digital Image Processing, Components of an Image Processing System, Elements of Visual Perception, Image Sensing and Acquisition, Image Sampling and Quantization, Some Basic Relationships Between Pixels. [Text 1: Chapter 1, Chapter 2: Sections 2.1 to 2.5]			
<b>Teaching-Learning Process</b>	Chalk and talk method, PowerPoint Presentation, YouTube videos, Videos on Image processing applications Self-study topics: Arithmetic and Logical operations Practical topics: Problems on Basic Relationships Between Pixels. <b>RBT Level:</b> L1, L2, L3		

<b>Module-2</b>	
<b>Image Transforms:</b> Introduction, Two-Dimensional Orthogonal and Unitary Transforms, Properties of Unitary Transforms, Two-Dimensional DFT, cosine Transform, Haar Transform. Text 2: Chapter 5: Sections 5.1 to 5.3, 5.5, 5.6, 5.9]	
<b>Teaching-Learning Process</b>	Chalk and talk method, PowerPoint Presentation, YouTube videos of various transformation techniques and related applications. Self-study topics: Sine transforms, Hadamard transforms, KL transform, Slant transform. Practical topics: Problems on DFT and DCT <b>RBT Level:</b> L1, L2, L3
<b>Module-3</b>	
<b>Spatial Domain:</b> Some Basic Intensity Transformation Functions, Histogram Processing, Fundamentals of Spatial Filtering, Smoothing Spatial Filters, Sharpening Spatial Filters [Text: Chapter 3: Sections 3.2 to 3.6]	
<b>Teaching-Learning Process</b>	Chalk and talk method, PowerPoint Presentation, YouTube videos and animations of Intensity Transformation Functions, Histogram Processing, Spatial domain filters. Self-study topics: Point, line and edge detection. Practical topics: Problems on Intensity Transformation Functions, Histogram, Spatial domain filters <b>RBT Level:</b> L1, L2, L3
<b>Module-4</b>	
<b>Frequency Domain:</b> Basics of Filtering in the Frequency Domain, Image Smoothing and Image Sharpening Using Frequency Domain Filters. <b>Color Image Processing:</b> Color Fundamentals, Color Models, Pseudo-color Image Processing. [Text 1: Chapter 4: Sections 4.7 to 4.9 and Chapter 6: Sections 6.1 to 6.3]	
<b>Teaching-Learning Process</b>	Chalk and talk method, PowerPoint Presentation, YouTube videos on frequency domain filtering, Color image processing. Self-study topics: Basic concept of segmentation. Practical topics: Problems on Pseudo-color Image Processing <b>RBT Level:</b> L1, L2, L3
<b>Module-5</b>	
<b>Restoration:</b> A model of the Image Degradation/Restoration Process, Noise models, Restoration in the Presence of Noise Only using Spatial Filtering and Frequency Domain Filtering, Inverse Filtering, Minimum Mean Square Error (Wiener) Filtering. [Text 1: Chapter 5: Sections 5.1, to 5.4.3, 5.7, 5.8]	
<b>Teaching-Learning Process</b>	Chalk and talk method, PowerPoint Presentation, YouTube videos on Noise models, filters and its applications. Self-study topics: Linear position invariant degradation, Estimation of degradation function. <b>RBT Level:</b> L1, L2, L3
<b>Course outcomes (Course Skill Set)</b> At the end of the course the student will be able to: <ol style="list-style-type: none"> <li>1. Understand image formation and the role of human visual system plays in perception of gray and color image data.</li> <li>2. Compute various transforms on digital images.</li> <li>3. Conduct independent study and analysis of Image Enhancement techniques.</li> <li>4. Apply image processing techniques in frequency (Fourier) domain.</li> <li>5. Design image restoration techniques.</li> </ol>	

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous Internal Evaluation:**

Three Unit Tests each of **20 Marks (duration 01 hour)**

1. First test at the end of 5<sup>th</sup> week of the semester
2. Second test at the end of the 10<sup>th</sup> week of the semester
3. Third test at the end of the 15<sup>th</sup> week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4<sup>th</sup> week of the semester
5. Second assignment at the end of 9<sup>th</sup> week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks (duration 01 hours)**

6. At the end of the 13<sup>th</sup> week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

**CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours**)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module.

**Suggested Learning Resources:****Text Books:**

1. Digital Image Processing- Rafael C Gonzalez and Richard E Woods, PHI, 3<sup>rd</sup> Edition 2010.
2. Fundamentals of Digital Image Processing- A K Jain, PHI Learning Private Limited 2014.

**Reference Book:**

Digital Image Processing- S Jayaraman, S Esakkirajan, T Veerakumar, Tata McGraw Hill, 2014.

**Web links and Video Lectures (e-Resources)**

- Image databases, [https://imageprocessingplace.com/root\\_files\\_V3/image\\_databases.htm](https://imageprocessingplace.com/root_files_V3/image_databases.htm)
- Student support materials, [https://imageprocessingplace.com/root\\_files\\_V3/students/students.htm](https://imageprocessingplace.com/root_files_V3/students/students.htm)
- NPTEL Course, Introduction to Digital Image Processing, <https://nptel.ac.in/courses/117105079>
- Computer Vision and Image Processing, <https://nptel.ac.in/courses/108103174>
- Image Processing and Computer Vision – Matlab and Simulink, <https://in.mathworks.com/solutions/image-video-processing.html>

**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

- Verilog /VHDL coding for Image manipulation.
- Simulink models for Image processing.

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**VII Semester**

DSP Algorithms & Architecture			
Course Code	21EC723	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	3:0:0:1	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3
<b>Course objectives:</b> This course will enable the students to <ul style="list-style-type: none"><li>Understand the concepts of digital signal processing techniques.</li><li>Understand the computational building blocks of DSP processors and its speed issues.</li><li>Understand the various addressing modes, peripherals, interrupts and pipelining structure of the TMS320C54xx processor.</li><li>Learn how to interface the external devices to the TMS320C54xx processor in various modes.</li><li>Understand DSP algorithms and applications with their implementation using TMS320C54xx processor.</li></ul>			
<b>Teaching-Learning Process (General Instructions)</b> The sample strategies, which the teacher can use to accelerate the attainment of the various course outcomes are listed in the following: <ol style="list-style-type: none"><li>Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.</li><li>Show Video/animation films to explain the functioning of various techniques.</li><li>Encourage collaborative (Group) Learning in the class</li><li>Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking</li><li>Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.</li><li>Topics will be introduced in multiple representations.</li><li>Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.</li><li>Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.</li></ol>			
<b>Module-1</b>			
<b>Introduction to Digital Signal Processing:</b> Introduction, A Digital Signal – Processing system, Major features of programmable Digital signal processors, The Sampling Process, Discrete Time Sequences, Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear Time-Invariant Systems, Digital Filters, Decimation and Interpolation. Section 1.3, 2.1 to 2.8 of Text 1			
<b>Teaching-Learning Process</b>	Chalk and talk method, Power point presentation <b>RBT Level:</b> L1, L2, L3		
<b>Module-2</b>			
<b>Architectures for Programmable Digital Signal Processing Devices:</b> Introduction, Basic Architectural Features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Speed Issues, Features for External Interfacing. Section 4.1 to 4.9 of Text 1			

<b>Teaching-Learning Process</b>	Chalk and talk method, Power point presentation <b>RBT Level:</b> L1, L2, L3
<b>Module-3</b>	
<b>Programmable Digital Signal Processors:</b> Introduction, Commercial Digital Signal-processing Devices, Data Addressing Modes of TMS320C54XX, Memory Space of TMS320C54xx Processors, Program Control. Detail Study of TMS320C54X & 54xx Instructions and Programming, On – Chip Peripherals, Interrupts of TMS320C54XX Processors, Pipeline Operation of TMS320C54xx Processor. Section 5.1 to 5.10 of Text 1	
<b>Teaching-Learning Process</b>	Chalk and talk method, Power point presentation <b>RBT Level:</b> L1, L2, L3
<b>Module-4</b>	
<b>Implementation of Basic DSP Algorithms:</b> Introduction, The Q – notation, FIR Filters, IIR Filters, Interpolation and Decimation Filters (one example in each case). <b>Implementation of FFT Algorithms:</b> Introduction, An FFT Algorithm for DFT Computation, Overflow and Scaling, Bit – Reversed Index. Generation & Implementation on the TMS320C54xx. Section 7.1 to 7.6 and 8.1 to 8.6 of Text 1	
<b>Teaching-Learning Process</b>	Chalk and talk method, Power point presentation <b>RBT Level:</b> L1, L2, L3
<b>Module-5</b>	
<b>Interfacing Memory and Parallel I/O Peripherals to Programmable DSP Devices:</b> Introduction, Memory Space Organization, External Bus Interfacing Signals. Memory Interface, Parallel I/O Interface, Programmed I/O, Interrupts and I/O Direct Memory Access (DMA). <b>Interfacing and Applications of DSP Processors:</b> Introduction, Synchronous Serial Interface, A CODEC Interface Circuit, DSP Based Bio-telemetry Receiver, A Speech Processing System, An Image Processing System. Section 9.1 to 9.8, 10.1 to 10.5 and 11.1 to 11.5 of Text 1	
<b>Teaching-Learning Process</b>	Chalk and talk method, Power point presentation <b>RBT Level:</b> L1, L2, L3
<b>Course outcome (Course Skill Set)</b> At the end of the course the student will be able to: <ol style="list-style-type: none"> <li>1. Comprehend the knowledge &amp; concepts of digital signal processing techniques.</li> <li>2. Apply knowledge of various types of addressing modes, interrupts, peripherals and pipelining structure of TMS320C54xx processor.</li> <li>3. Develop assembly language programs to implement FIR, IIR filters and FFT algorithms.</li> <li>4. Build the Applications on Programmable DSP devices.</li> </ol>	
<b>Assessment Details (both CIE and SEE)</b> The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.	
<b>Continuous Internal Evaluation:</b> Three Unit Tests each of <b>20 Marks (duration 01 hour)</b> <ol style="list-style-type: none"> <li>1. First test at the end of 5<sup>th</sup> week of the semester</li> <li>2. Second test at the end of the 10<sup>th</sup> week of the semester</li> <li>3. Third test at the end of the 15<sup>th</sup> week of the semester</li> </ol> Two assignments each of <b>10 Marks</b> <ol style="list-style-type: none"> <li>4. First assignment at the end of 4<sup>th</sup> week of the semester</li> </ol>	

5. Second assignment at the end of 9<sup>th</sup> week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks (duration 01 hours)**

6. At the end of the 13<sup>th</sup> week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

**CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours**)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module.

**Suggested Learning Resources:**

**Text Book:**

"Digital Signal Processing", Avatar Singh and S Srinivasan, Thomson Learning, 2004

**Reference Books:**

1. "Digital Signal Processing: A practical approach", Ifeachor E C, Jervis B. W Pearson-Education, PHI, 2002.
2. "Digital Signal Processors", B Venkataramani and M Bhaskar, TMH, 2<sup>nd</sup> Ed., 2010
3. "Architectures for Digital Signal Processing", Peter Pirsch, John Wiley.



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**VII Semester**

Biomedical Signal Processing			
Course Code	21EC724	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	3:0:0:1	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3
<b>Course objectives:</b> This course will enable students to: <ul style="list-style-type: none"><li>• Possess the basic mathematical, scientific and computational skills necessary to analyse ECG and EEG signals.</li><li>• Apply classical and modern filtering and compression techniques for ECG and EEG signals.</li><li>• Develop a thorough understanding on basics of ECG and EEG feature extraction.</li></ul>			
<b>Teaching-Learning Process (General Instructions)</b> The sample strategies, which the teacher can use to accelerate the attainment of the various course outcomes are listed in the following: <ol style="list-style-type: none"><li>1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.</li><li>2. Show Video/animation films to explain the functioning of various techniques.</li><li>3. Encourage collaborative (Group) Learning in the class</li><li>4. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking</li><li>5. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.</li></ol>			
<b>Module-1</b>			
<b>Introduction to Biomedical Signals:</b> The nature of Biomedical Signals, Examples of Biomedical Signals, Objectives of Biomedical Signal analysis, Difficulties in Biomedical Signal analysis. (Text-1: 1.1, 1.2, 1.3, 1.4) <b>Electrocardiography:</b> Techniques used in electrocardiography, ECG Electrodes, the cardiac equivalent generator, genesis of the ECG, the standard and augmented limb leads, 12 lead ECG, the vectorcardiogram, ECG signal characteristics. (Text-2: 2.1, 2.1.1, 2.1.2, 2.1.3, 2.1.4, 2.1.5, 2.2.1, 2.2.2, 2.3) <b>Signal Conversion:</b> Simple signal conversion systems, Conversion requirements for biomedical signals, Signal converter characteristics, D to A converters, A to D converters, Sample and Hold circuit, Analog Multiplexer, Amplifiers (Text-2: 3.2, 3.3, 3.4.1, 3.4.2, 3.4.3, 3.4.4, 3.4.5, 3.4.6).			
<b>Teaching-Learning Process</b>	Chalk and talk method, PowerPoint Presentation, YouTube videos <b>RBT Level:</b> L1, L2, L3		
<b>Module-2</b>			
<b>Signal Averaging:</b> Basics of signal averaging, Signal averaging as a digital filter, a typical averager, Software for signal averaging, Limitations of signal averaging. (Text-2: 9.1, 9.2, 9.3, 9.4, 9.5). <b>Adaptive Filters:</b> Principal noise canceller model, 60-Hz adaptive cancelling using a sine wave model, Applications: Maternal ECG in fetal ECG, Cardiogenic artifact, detection of ventricular fibrillation and tachycardia. (Text-2: 8.1, 8.2, 8.3.1, 8.3.2, 8.3.3).			

<b>Teaching-Learning Process</b>	Chalk and talk method, PowerPoint Presentation, YouTube videos <b>RBT Level:</b> L1, L2, L3
<b>Module-3</b>	
<b>Data Reduction Techniques:</b> Introduction, Turning point algorithm, AZTEC algorithm, Fano algorithm, Huffman coding: Static coding, Modified coding, Adaptive coding, Residual differencing, Runlength coding. (Text-2: 10.1, 10.2, 10.3, 10.4.1, 10.4.2, 10.4.3, 10.4.4, 10.4.5). <b>Time and Frequency domain techniques:</b> The Fourier transform for a discrete nonperiodic and periodic signals, the Fast Fourier transform, Correlation in time domain and in frequency domain, Convolution in time domain and in frequency domain, Power spectrum estimation: Parseval's theorem (Text-2: 11.1.1, 11.1.2, 11.1.3, 11.2.1, 11.2.2, 11.2.3, 11.3.1, 11.3.2, 11.3.3, 11.4.1)	
<b>Teaching-Learning Process</b>	Chalk and talk method, PowerPoint Presentation, YouTube videos <b>RBT Level:</b> L1, L2, L3
<b>Module-4</b>	
<b>ECG QRS detection:</b> Power spectrum of the ECG, Bandpass filtering techniques, Differentiation techniques, Template matching techniques: Template cross correlation, template subtraction, automata based template matching, a QRS detection algorithm. <b>ECG Analysis Systems:</b> Interpretation of the 12 lead ECG, ST segment analyzer, Portable arrhythmia monitor: Holter recording, software and hardware design, arrhythmia analysis (Text -2)	
<b>Teaching-Learning Process</b>	Chalk and talk method, PowerPoint Presentation, YouTube videos <b>RBT Level:</b> L1, L2, L3
<b>Module-5</b>	
<b>Neurological signal processing:</b> The brain and its potentials, origin of brain waves, the EEG signal and its characteristics, EEG analysis, Linear prediction theory, The Autoregressive method, Recursive estimation of AR parameters, Spectral error measure. (Text-3: 4.1, 4.2, 4.3 4.4, 4.5, 4.6, 4.7, 4.8) <b>Event detection and waveform analysis:</b> EEG rhythms, waves and transients, Detection of EEG rhythms, Template matching for EEG spike and wave detection, the matched filter (Text-1: 4.2.4, 4.4.1, 4.4.2, 4.6)	
<b>Teaching-Learning Process</b>	Chalk and talk method, Power point presentation <b>RBT Level:</b> L1, L2, L3
<b>Course outcome (Course Skill Set)</b> At the end of the course the student will be able to: <ol style="list-style-type: none"> <li>1. Describe the origin, properties and suitable models of important biological signals such as ECG and EEG.</li> <li>2. Know the basic signal processing techniques in analysing biological signals.</li> <li>3. Acquire mathematical and computational skills relevant to the field of biomedical signal processing.</li> <li>4. Describe the basics of ECG signal compression algorithms.</li> <li>5. Know the complexity of various biological phenomena.</li> </ol>	
<b>Assessment Details (both CIE and SEE)</b> The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together. <b>Continuous Internal Evaluation:</b> Three Unit Tests each of <b>20 Marks (duration 01 hour)</b> <ol style="list-style-type: none"> <li>1. First test at the end of 5<sup>th</sup> week of the semester</li> </ol>	

2. Second test at the end of the 10<sup>th</sup> week of the semester
3. Third test at the end of the 15<sup>th</sup> week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4<sup>th</sup> week of the semester
5. Second assignment at the end of 9<sup>th</sup> week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks (duration 01 hours)**

6. At the end of the 13<sup>th</sup> week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

**CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours**)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module.

**Suggested Learning Resources:**

**Books:**

1. Biomedical Signal Analysis-Rangaraj M Rangayyan, John Wiley & Sons 2002
2. Biomedical Digital Signal Processing- Willis J Tompkins, PHI2001.
3. Biomedical Signal Processing Principles and Techniques-D C Reddy, McGraw-Hill publications, 2005.

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**VII Semester**

Speech Signal Processing			
Course Code	21EC725	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3
<b>Course objectives:</b> <ul style="list-style-type: none"><li>• Introduce the models for speech production</li><li>• Develop Time domain and frequency domain speech processing techniques</li><li>• Introduce a predictive technique for speech compression</li><li>• Provide fundamental knowledge required to understand and analyze speech recognition, synthesis and speaker identification systems.</li></ul>			
<b>Teaching-Learning Process (General Instructions)</b> <p>The sample strategies, which the teacher can use to accelerate the attainment of the various course outcomes are listed in the following:</p> <ol style="list-style-type: none"><li>1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.</li><li>2. Show Video/animation films to explain the functioning of various techniques.</li><li>3. Encourage collaborative (Group) Learning in the class</li><li>4. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking</li><li>5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.</li><li>6. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.</li></ol>			
<b>Module-1</b>			
<b>Fundamentals of Human Speech Production:</b> The Process of Speech Production, Short-Time Fourier representation of Speech, The Acoustic Theory of Speech production, Digital Models for Sampled Speech Signals.			
<b>Teaching-Learning Process</b>	Chalk and talk method, Power point presentations, Animation of process of speech production <b>RBT Level:</b> L1, L2, L3		
<b>Module-2</b>			
<b>Time-Domain Methods for Speech Processing:</b> Introduction to Short-Time Analysis of Speech, Short-Time Energy and Short-Time Magnitude, Short-Time Zero-Crossing Rate, The Short-Time Autocorrelation Function, Speech vs Silence detection.			
<b>Teaching-Learning Process</b>	Chalk and talk method, Power point presentation Simulation of Short Time analysis algorithm using tools like Matlab/simulink <b>RBT Level:</b> L1, L2, L3		
<b>Module-3</b>			
<b>Frequency Domain Representations:</b> Discrete-Time Fourier Analysis, Short-Time Fourier Analysis, Overlap Addition (OLA) and Filter Bank Summation (FBS) Method of Synthesis, Time-Decimated Filter Banks, Two-Channel Filter Banks, Modifications of the STFT.			
<b>Teaching-Learning Process</b>	Chalk and talk method, Power point presentation Visualization of speech using spectrogram <b>RBT Level:</b> L1, L2, L3		

<b>Module-4</b>	
<b>The Cepstrum and Homomorphic Speech Processing:</b> Introduction, Homomorphic Systems for Convolution, Homomorphic Analysis of the Speech Model, Computing the Short-Time Cepstrum and Complex Cepstrum of Speech, Homomorphic Filtering of Natural Speech, Cepstrum Analysis of All-Pole Models, Cepstrum Distance Measures.	
<b>Teaching-Learning Process</b>	Chalk and talk method, Power point presentation <b>RBT Level:</b> L1, L2, L3
<b>Module-5</b>	
<b>Linear Predictive Analysis of Speech Signals:</b> Introduction to Basic Principles of Linear Predictive Analysis, Computation of the Gain for the Model, Frequency Domain Interpretations of Linear Predictive Analysis, Solution of the LPC Equations, The Prediction Error Signal.	
<b>Teaching-Learning Process</b>	Chalk and talk method, Power point presentation <b>RBT Level:</b> L1, L2, L3
<b>Course outcomes (Course Skill Set)</b> At the end of the course the student will be able to: <ol style="list-style-type: none"> <li>1. Model speech production system and describe the fundamentals of speech.</li> <li>2. Apply time domain and frequency domain algorithms, on speech to find, enhance and modify speech parameters.</li> <li>3. Choose an appropriate processing technique for a given application.</li> <li>4. Analyse speech recognition, synthesis and speaker identification systems</li> </ol>	
<b>Assessment Details (both CIE and SEE)</b> The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together. <b>Continuous Internal Evaluation:</b> Three Unit Tests each of <b>20 Marks (duration 01 hour)</b> <ol style="list-style-type: none"> <li>1. First test at the end of 5<sup>th</sup> week of the semester</li> <li>2. Second test at the end of the 10<sup>th</sup> week of the semester</li> <li>3. Third test at the end of the 15<sup>th</sup> week of the semester</li> </ol> Two assignments each of <b>10 Marks</b> <ol style="list-style-type: none"> <li>4. First assignment at the end of 4<sup>th</sup> week of the semester</li> <li>5. Second assignment at the end of 9<sup>th</sup> week of the semester</li> </ol> Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for <b>20 Marks (duration 01 hours)</b> <ol style="list-style-type: none"> <li>6. At the end of the 13<sup>th</sup> week of the semester</li> </ol> The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be <b>scaled down to 50 marks</b> (to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course). <b>CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.</b> <b>Semester End Examination:</b>	

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours**)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module.

#### **Suggested Learning Resources:**

##### **Text Books**

1. **Digital Processing of Speech Signals** - L R Rabiner and R W Schafer, Pearson Education Asia, 2004.
2. **Theory and Applications of Digital Speech Processing**-Rabiner and Schafer, Pearson Education 2011.

##### **Reference Books**

1. **Fundamentals of Speech Recognition**- Lawrence Rabiner and Biing-Hwang Juang, Pearson Education, 2003.
2. **Speech and Language Processing**-An Introduction to Natural Language Processing, Computational Linguistics, and Speech Recognition- Daniel Jurafsky and James H Martin, Pearson Prentice Hall, 2009.

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**VII Semester**

IoT & Wireless Sensor Networks			
Course Code	21EC731	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3
<b>Course objectives:</b> <ul style="list-style-type: none"><li>To provide an exposure to the broad perspective of Internet of Things with respect to the characteristics, design, technologies and applications.</li><li>To provide a basic understanding of the important aspects of Wireless sensor networks covering applications, sensor and transmission technology &amp; systems, middleware, performance and traffic management.</li></ul>			
<b>Teaching-Learning Process (General Instructions)</b> <p>The sample strategies, which the teacher can use to accelerate the attainment of the various course outcomes are listed in the following:</p> <ol style="list-style-type: none"><li>Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.</li><li>Show Video/animation films to explain the various concepts.</li><li>Encourage collaborative (Group) Learning in the class</li><li>Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking</li><li>Adopt Problem Based Learning (PBL), which fosters students’ Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.</li><li>Topics will be introduced in multiple representations.</li><li>Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.</li><li>Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.</li></ol>			
<b>Module-1</b>			
Internet of Things: Introduction, Physical design, Logical design, Enabling technologies, Levels & deployment templates. Text 1: Chapter 1			
<b>Teaching-Learning Process</b>	Chalk and talk method, Power point presentation <b>RBT Level:</b> L1, L2, L3		
<b>Module-2</b>			
Domain Specific IoTs: Home automation, cities, environment, energy, retail, logistics, agriculture, industry, health & lifestyle. Text 1: Chapter 2			
<b>Teaching-Learning Process</b>	Chalk and talk method, Power point presentation <b>RBT Level:</b> L1, L2, L3		
<b>Module-3</b>			
Wireless Sensor Networks: Introduction, applications of sensor networks, basic overview of the technology, basic sensor network architectural elements, present day sensor network research, challenges and hurdles, examples of Category 2 WSN applications, examples of Category 1 WSN applications			

Text 2: Chapter 1 – 1.1, 1.1.2, 1.2, 1.2.1, 1.2.2 (phase 4), 1.2.3 Chapter 2: 2.4, 2.5	
<b>Teaching-Learning Process</b>	Chalk and talk method, Power point presentation <b>RBT Level:</b> L1, L2, L3
<b>Module-4</b>	
<b>Wireless sensor technology:</b> Introduction, sensor node technology – overview, hardware and software, sensor taxonomy, WN operating environment, WN trends. <b>Wireless Transmission technology and systems:</b> Introduction, Campus applications, MAN/WAN applications. Text 2: Chapter 3: 3.1, 3.2 – 3.2.1, 3.2.2, 3.3, 3.4, 3.5 Chapter 4: 4.1, 4.3.1, 4.3.2	
<b>Teaching-Learning Process</b>	Chalk and talk method, Power point presentation <b>RBT Level:</b> L1, L2, L3
<b>Module-5</b>	
<b>Middleware for WSNs:</b> Introduction, principles, architecture, data related functions <b>Performance and traffic management:</b> background, WSN Design issues, performance modelling of WSNs. Text 2: Chapter 8: 8.1, 8.2, 8.3, 8.3.1 Chapter 11: 11.2, 11.3, 11.4	
<b>Teaching-Learning Process</b>	Chalk and talk method, Power point presentation <b>RBT Level:</b> L1, L2, L3
<b>Course outcome (Course Skill Set)</b> At the end of the course the student will be able to: <ol style="list-style-type: none"> <li>1. Understand the characteristics, building blocks, enabling technologies of the IoT systems</li> <li>2. Describe the characteristics and applications of domain specific IoTs.</li> <li>3. Discuss the overview of the Wireless sensor networks characteristics and applications.</li> <li>4. Present the sensor, transmission technology and systems associated with WSN.</li> <li>5. Understand the concepts of middleware, performance evaluation and traffic management in WSN.</li> </ol>	
<b>Assessment Details (both CIE and SEE)</b> The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.	
<b>Continuous Internal Evaluation:</b> Three Unit Tests each of <b>20 Marks (duration 01 hour)</b> <ol style="list-style-type: none"> <li>1. First test at the end of 5<sup>th</sup> week of the semester</li> <li>2. Second test at the end of the 10<sup>th</sup> week of the semester</li> <li>3. Third test at the end of the 15<sup>th</sup> week of the semester</li> </ol> Two assignments each of <b>10 Marks</b> <ol style="list-style-type: none"> <li>4. First assignment at the end of 4<sup>th</sup> week of the semester</li> <li>5. Second assignment at the end of 9<sup>th</sup> week of the semester</li> </ol> Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for <b>20 Marks (duration 01 hours)</b> <ol style="list-style-type: none"> <li>6. At the end of the 13<sup>th</sup> week of the semester</li> </ol> The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be <b>scaled down to 50 marks</b> (to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).	



**CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours**)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module.

**Suggested Learning Resources:**

**Text Books:**

1. 'Internet of Things', Arshdeep Bagha and Vijay Madiseti, Universities Press, 2015
2. 'Wireless Sensor Networks', Kazem Sohraby, Daniel Minoli and Taieb Znati, Wiley, 2015.

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**VII Semester**

Network Security			
Course Code	21EC732	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	3:0:0:1	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3
<b>Course objectives:</b> <ul style="list-style-type: none"><li>• <b>Preparation:</b> To prepare students with fundamental knowledge/ overview in the field of Network Security with knowledge of security mechanisms and services.</li><li>• <b>Core Competence:</b> To equip students with a basic foundation of Network Security by delivering the basics of Transport Level Security, Secure Socket Layer, Internet Protocol security, Intruders, Intrusion detection and Malicious Software, Firewalls, Firewall characteristics, Biasing and Configuration.</li></ul>			
<b>Teaching-Learning Process (General Instructions)</b> <p>These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.</p> <ol style="list-style-type: none"><li>1. Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.</li><li>2. Show Video/animation films to explain the different Network Security Techniques / Algorithms</li><li>3. Encourage collaborative (Group) Learning in the class</li><li>4. Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking</li><li>5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.</li><li>6. Topics will be introduced in a multiple representation.</li><li>7. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.</li><li>8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.</li><li>9. Adopt Flipped class technique by sharing the materials / Sample Videos prior to the class and have discussions on the that topic in the succeeding classes</li><li>10. Give Programming Assignments</li></ol>			
<b>Module-1</b>			
Attacks on Computers and Computer Security: Need for Security, Security Approaches, Principles of Security Types of Attacks. <b>(Text2: Chapter1)</b> Security Mechanisms, Services and Attacks, A model for Network security <b>(Text1: Chapter1: 3, 4, 5, 6)</b> Network Access Control, Extensible Authentication Protocol <b>(Text1: Chapter 16: Section 1,2)</b>			
<b>Teaching-Learning Process</b>	Chalk and talk method, YouTube videos, Flipped Class Technique <b>RBT Level:</b> L1, L2, L3		
<b>Module-2</b>			
Transport Level Security: Web Security Considerations, Secure Sockets Layer, Transport Layer Security, HTTPS, Secure Shell (SSH) <b>(Text1: Chapter15)</b>			
<b>Teaching-Learning Process</b>	Chalk and talk method YouTube videos, Flipped Class Technique and PPTs. Self-study topics: Block cipher modes, Cryptographic Hash functions and MAC codes <b>RBT Level:</b> L1, L2, L3		

<b>Module-3</b>	
<b>IP Security:</b> Overview of IP Security (IPSec), IP Security Architecture, Modes of Operation, Security Associations (SA), Authentication Header (AH), Encapsulating Security Payload (ESP), Internet Key Exchange. <b>(Text1: Chapter19)</b>	
<b>Teaching-Learning Process</b>	Chalk and talk method, YouTube videos, Flipped Class Technique and PPTs. Self-study topics: OSI Model <b>RBT Level:</b> L1, L2, L3
<b>Module-4</b>	
<b>Intruders:</b> Intruders, Intrusion Detection, Password Management. <b>(Chapter20-Text1)</b> <b>MALICIOUS SOFTWARE:</b> Viruses and Related Threats, Virus Countermeasures, <b>(Chapter21-Text1)</b>	
<b>Teaching-Learning Process</b>	Chalk and talk method, YouTube videos, Flipped Class Technique and PPTs. <b>RBT Level:</b> L1, L2, L3
<b>Module-5</b>	
<b>Firewalls:</b> The Need for firewalls, Firewall Characteristics, Types of Firewalls, Firewall Biasing, Firewall location and configuration <b>(Chapter 22-Text 1)</b>	
<b>Teaching-Learning Process</b>	Chalk and talk method, YouTube videos, Flipped Class Technique and PPTs. <b>RBT Level:</b> L1, L2, L3
<b>Course outcomes (Course Skill Set)</b> At the end of the course the student will be able to: <ol style="list-style-type: none"> <li>1. Explain network security services and mechanisms and explain security concepts</li> <li>2. Understand the concept of Transport Level Security and Secure Socket Layer.</li> <li>3. Explain Security concerns in Internet Protocol security</li> <li>4. Explain Intruders, Intrusion detection and Malicious Software</li> <li>5. Describe Firewalls, Firewall Characteristics, Biasing and Configuration</li> </ol>	
<b>Assessment Details (both CIE and SEE)</b> The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.	
<b>Continuous Internal Evaluation:</b> Three Unit Tests each of <b>20 Marks (duration 01 hour)</b> <ol style="list-style-type: none"> <li>1. First test at the end of 5<sup>th</sup> week of the semester</li> <li>2. Second test at the end of the 10<sup>th</sup> week of the semester</li> <li>3. Third test at the end of the 15<sup>th</sup> week of the semester</li> </ol> Two assignments each of <b>10 Marks</b> <ol style="list-style-type: none"> <li>4. First assignment at the end of 4<sup>th</sup> week of the semester</li> <li>5. Second assignment at the end of 9<sup>th</sup> week of the semester</li> </ol> Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for <b>20 Marks (duration 01 hours)</b> <ol style="list-style-type: none"> <li>6. At the end of the 13<sup>th</sup> week of the semester</li> </ol> The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be <b>scaled down to 50 marks</b> (to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).	

**CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours**)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module.

**Suggested Learning Resources:**

**Text Books:**

1. William Stallings, "Cryptography and Network Security Principles and Practice", Pearson Education Inc., 5<sup>th</sup> Edition, 2014, ISBN: 978-81-317- 6166-3
2. Atul Kahate, "Cryptography and Network Security", TMH, 2003.

**Reference Books:**

1. Cryptography and Network Security, Behrouz A Forouzan, TMH, 2007.
2. Introduction to Computer Security, Matt Bishop, Sathyanarayana S V, Pearson Education, 2006, ISBN 81-7758-425/1.

**Web links and Video Lectures (e-Resources)**

<https://nptel.ac.in/courses/106105031>  
<https://nptel.ac.in/courses/128106006>

**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

- Programming Assignments / Mini Projects can be given to improve programming skills.

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**VII Semester**

Fabrication Technology			
Course Code	21EC733	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	3:0:0:1	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3
<b>Course objectives:</b> <ul style="list-style-type: none"><li>Familiarise with the concepts of different processes involved in fabrication process and also with packaging issues.</li><li>Apply principles to identify and analyse the various steps for the fabrication of various components.</li><li>Introduce the fundamental concepts relevant to VLSI fabrication.</li><li>Enable the students to understand the various VLSI fabrication techniques.</li></ul>			
<b>Teaching-Learning Process (General Instructions)</b> <p>The sample strategies, which the teacher can use to accelerate the attainment of the various course outcomes are listed in the following:</p> <ol style="list-style-type: none"><li>Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.</li><li>Show Video/animation films to explain the functioning of various techniques.</li><li>Encourage collaborative (Group) Learning in the class.</li><li>Topics will be introduced in multiple representations.</li><li>Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.</li></ol>			
<b>Module-1</b>			
<b>Crystal Growth and Wafer Preparation:</b> Introduction, Electronic grade Silicon, Czochralski Crystal Growing, Silicon Shaping <b>Epitaxy:</b> Introduction, Vapor-Phase Epitaxy <b>Text Book</b> 1.1 to 1.4, 2.1 to 2.2			
<b>Teaching-Learning Process</b>	Chalk and talk method, PowerPoint Presentation, Videos on crystal growth process Self-study topics: Mask Preparation <b>RBT Level:</b> L1, L2, L3		
<b>Module-2</b>			
<b>Epitaxy:</b> Molecular beam epitaxy, Epitaxial evaluation <b>Oxidation:</b> Introduction, Growth mechanism and kinetics, Thin oxides, oxidation techniques, oxide properties, redistribution of dopants, oxidation of polysilicon, oxidation-induced defects <b>Text Book</b> 2.3 and 2.5, 3.1 to 3.8			
<b>Teaching-Learning Process</b>	Chalk and talk method, Power point presentation, videos on Epitaxial process Self-study topics: Advanced oxidation techniques <b>RBT Level:</b> L1, L2, L3		
<b>Module-3</b>			
<b>Lithography:</b> Introduction, Optical Lithography, Electron Lithography, X-ray lithography, Ion Lithography <b>Text Book</b> 4.1 to 4.5			

<b>Teaching-Learning Process</b>	Chalk and talk method, PowerPoint Presentation, Videos on Lithography Self-study topics: Sputtering and edge lithography <b>RBT Level:</b> L1, L2, L3
<b>Module-4</b>	
<b>Diffusion:</b> Introduction, Models of diffusion in solids, Fick's 1D diffusion equation, atomic diffusion mechanism, Diffusivities, Measurement techniques, fast diffusants in silicon, diffusion in polycrystalline silicon, diffusion in SiO <sub>2</sub> <b>Ion Implantation:</b> Introduction, Implantation equipment <b>Text Book</b> 7.1 to 7.9, 8.1 and 8.3	
<b>Teaching-Learning Process</b>	Chalk and talk method, PowerPoint Presentation, Videos on diffusion method Self-study topics: Effect of doping concentration in diffusion process <b>RBT Level:</b> L1, L2, L3
<b>Module-5</b>	
<b>Ion Implantation:</b> Annealing, Shallow Junctions, High energy implantation <b>Metallization:</b> Introduction, Metallization applications, metallization choices, Metallization problems, New role of metallization. <b>Text Book</b> 8.4 to 8.6, 9.1 to 9.7 (except 9.4 and 9.5)	
<b>Teaching-Learning Process</b>	Chalk and talk method, Power point presentation, Videos on Annealing process Self-study topics: e-beam evaporation, plasma spray deposition <b>RBT Level:</b> L1, L2, L3
<b>Course outcome (Course Skill Set)</b> At the end of the course the student will be able to: <ol style="list-style-type: none"> <li>1. Understanding the process in the field of Fabrication technology.</li> <li>2. Understand the properties and growth mechanism of oxidation.</li> <li>3. Relate to the competing methods of various lithographic techniques and their limitations.</li> <li>4. Analyse the diffusion profiles and models in various materials.</li> <li>5. Describe the Metallization choices, properties and selection of optimum deposition process.</li> </ol>	
<b>Assessment Details (both CIE and SEE)</b> The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together. <b>Continuous Internal Evaluation:</b> Three Unit Tests each of <b>20 Marks (duration 01 hour)</b> <ol style="list-style-type: none"> <li>1. First test at the end of 5<sup>th</sup> week of the semester</li> <li>2. Second test at the end of the 10<sup>th</sup> week of the semester</li> <li>3. Third test at the end of the 15<sup>th</sup> week of the semester</li> </ol> Two assignments each of <b>10 Marks</b> <ol style="list-style-type: none"> <li>4. First assignment at the end of 4<sup>th</sup> week of the semester</li> <li>5. Second assignment at the end of 9<sup>th</sup> week of the semester</li> </ol> Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for <b>20 Marks (duration 01 hours)</b> <ol style="list-style-type: none"> <li>6. At the end of the 13<sup>th</sup> week of the semester</li> </ol> The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be <b>scaled down to 50 marks</b> (to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).	

**CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours**)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module.

**Suggested Learning Resources:**

**Text Book:**

VLSI Technology, S M Sze, 2<sup>nd</sup> edition, Mc Graw Hill.

**Reference Books:**

1. VLSI Fabrication Principles, S K Gandhi, John Willey & Sons.
2. Micromachined transducer, G T A Kovacs, McGraw Hill.

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**VII Semester**

Machine Learning with Python			
Course Code	21EC734	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	2:0: 2:1	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3
<b>Course objectives:</b> <ul style="list-style-type: none"><li>• To understand the basic theory underlying machine learning.</li><li>• To be able to formulate machine learning problems corresponding to different applications.</li><li>• To understand a range of machine learning algorithms along with their strengths and weaknesses.</li><li>• To be able to apply machine learning algorithms to solve problems of moderate complexity.</li><li>• To apply the algorithms to a real-world problem, optimize the models learned and report on the expected accuracy that can be achieved by applying the models.</li></ul>			
<b>Teaching-Learning Process (General Instructions)</b> <p>These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.</p> <ol style="list-style-type: none"><li>1. In addition to the traditional lecture method, different types of innovative teaching methods may be adopted so that the delivered lessons shall develop student’s theoretical and programming skills.</li><li>2. State the need for learning Machine Learning with real-life examples.</li><li>3. Support and guide the students for self–study.</li><li>4. You will also be responsible for assigning homework, grading assignments and quizzes, and documenting students &amp; progress</li><li>5. Encourage the students for group learning to improve their creative and analytical skills.</li><li>6. Show short, related video lectures in the following ways:<ul style="list-style-type: none"><li>• As an introduction to new topics (pre-lecture activity).</li><li>• As a revision of topics (post-lecture activity).</li><li>• As additional examples (post-lecture activity).</li><li>• As an additional material of challenging topics (pre-and post-lecture activity).</li><li>• As a model solution of some real world problems. (post-lecture activity).</li></ul></li></ol>			
<b>Module-1</b>			
<b>Introduction:</b> <p>Introduction to Machine Learning, Building intelligent machines to transform data into knowledge, The three different types of machine learning, An introduction to the basic terminology and notations, A roadmap for building machine learning systems, Using Python for machine learning.</p> <b>Training Machine Learning Algorithms for Classification</b> <p>Artificial neurons – a brief glimpse into the early history of machine learning, Implementing a perceptron learning algorithm in Python, Adaptive linear neurons and the convergence of learning.</p> <p>Textbook 1: Chapters 1, 2</p>			
<b>Teaching-Learning Process</b>	Chalk and talk method, Power point presentation <b>RBT Level:</b> L1, L2, L3		
<b>Module-2</b>			
<b>A Tour of Machine Learning Classifiers Using Scikit-Learn</b> <p>Choosing a classification algorithm, First steps with scikit-learn, Modeling class probabilities via logistic regression, Maximum margin classification with support vector machines, Solving nonlinear problems using a kernel SVM, Decision tree learning, K-nearest neighbors – a lazy learning algorithm</p>			



<b>Building Good Training Sets – Data Preprocessing</b> Dealing with missing data, Handling categorical data, Partitioning a dataset in training and test sets, Bringing features onto the same scale, Selecting meaningful features, Assessing feature importance with random forests. Textbook 1: Chapters 3 ,4	
<b>Teaching-Learning Process</b>	Chalk and talk method, Power point presentation <b>RBT Level:</b> L1, L2, L3
<b>Module-3</b>	
<b>Compressing Data via Dimensionality Reduction</b> Unsupervised dimensionality reduction via principal component Analysis, Supervised data compression via linear discriminant analysis, Using kernel principal component analysis for nonlinear mappings <b>Learning Best Practices for Model Evaluation and Hyperparameter Tuning</b> Streamlining workflows with pipelines, Using k-fold cross-validation to assess model performance, Debugging algorithms with learning and validation curves, Fine-tuning machine learning models via grid search, Looking at different performance evaluation metrics <b>Applying Machine Learning to Sentiment Analysis</b> Obtaining the IMDb movie review dataset, Introducing the bag-of-words model, training a logistic regression model for document classification , Working with bigger data – online algorithms and out-of-core learning Textbook 1: Chapters 5,6,8	
<b>Teaching-Learning Process</b>	Chalk and talk method, Power point presentation <b>RBT Level:</b> L1, L2, L3
<b>Module-4</b>	
<b>Embedding a Machine Learning Model into a Web Application</b> Serializing fitted scikit-learn estimators, Setting up a SQLite database for data storage, Developing a web application with Flask, Turning the movie classifier into a web application, Deploying the web application to a public server <b>Predicting Continuous Target Variables with Regression Analysis</b> Introducing a simple linear regression model, Exploring the Housing Dataset, Implementing an ordinary least squares linear regression model, Fitting a robust regression model using RANSAC, Evaluating the performance of linear regression models, Using regularized methods for regression- Turning a linear regression model into a curve – polynomial regression Textbook 1: Chapters 9,10	
<b>Teaching-Learning Process</b>	Chalk and talk method, Power point presentation <b>RBT Level:</b> L1, L2, L3
<b>Module-5</b>	
<b>Working with Unlabeled Data – Clustering Analysis</b> Grouping objects by similarity using k-means, Organizing clusters as a hierarchical tree, <b>Training Artificial Neural Networks for Image Recognition</b> Modeling complex functions with artificial neural networks, Classifying handwritten digits, Training an artificial neural network, Other neural network architectures Textbook 1: Chapters 11,12	
<b>Teaching-Learning Process</b>	Chalk and talk method, Power point presentation <b>RBT Level:</b> L1, L2, L3

**Course outcomes (Course Skill Set)**

At the end of the course the student will be able to:

1. Appreciate the importance of visualization in the data analytics solution
2. Apply structured thinking to unstructured problems
3. Understand a very broad collection of machine learning algorithms and problems
4. Learn algorithmic topics of machine learning and mathematically deep enough to introduce the required theory
5. Develop an appreciation for what is involved in learning from data.

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous Internal Evaluation:**

Three Unit Tests each of **20 Marks (duration 01 hour)**

1. First test at the end of 5<sup>th</sup> week of the semester
2. Second test at the end of the 10<sup>th</sup> week of the semester
3. Third test at the end of the 15<sup>th</sup> week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4<sup>th</sup> week of the semester
5. Second assignment at the end of 9<sup>th</sup> week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks (duration 01 hours)**

6. At the end of the 13<sup>th</sup> week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

**CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours**)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module.

**Suggested Learning Resources:****Text Books:**

1. Python Machine Learning by Sebastian Raschka, Published by Packt Publishing Ltd.
2. Machine Learning with Python for Everyone by Mark E Fenner
3. Machine Learning using Python by Manaranjan Pradhan & U Dinesh Kumar
4. Practical Machine Learning with Python by Dipanjan Sarkar, Raghav Bali &Tushar Sharma

<b>Web links and Video Lectures (e-Resources)</b>
<ul style="list-style-type: none"><li>• <a href="https://www.youtube.com/watch?v=RnFGwxJwx-0">https://www.youtube.com/watch?v=RnFGwxJwx-0</a></li><li>• <a href="https://www.youtube.com/watch?v=eq7KF7JTinU">https://www.youtube.com/watch?v=eq7KF7JTinU</a></li></ul>
<b>Activity Based Learning (Suggested Activities in Class)/ Practical Based learning</b> <ul style="list-style-type: none"><li>• Using IRIS data set implement Adaline rule Classification Algorithm.</li><li>• Implement Logistic Regression algorithm and generate corresponding graphs for overfitting and under fitting.</li><li>• Implement linear SVM algorithm with maximum margin intuition.</li><li>• Implement a kernel SVM to solve nonlinear problems.</li><li>• Implement KNN Algorithm.</li><li>• Implement decision tree algorithm.</li><li>• Implement s rbf_kernel_pca for separating half-moon shapes.</li><li>• Develop web application using flask.</li></ul>

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**VII Semester**

Multimedia Communication			
Course Code	21EC735	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	3:0:0:1	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3
<b>Course objectives:</b> This course will enable students to: <ul style="list-style-type: none"><li>• Understand the importance of multimedia in today’s online and offline information sources and repositories.</li><li>• Understand the how Text, Audio, Image and Video information can be represented digitally in a computer so that it can be processed, transmitted and stored efficiently.</li><li>• Understand the Multimedia Transport in Wireless Networks</li><li>• Understand the Real-time multimedia network applications.</li><li>• Understand the Different network layer based application.</li></ul>			
<b>Teaching-Learning Process (General Instructions)</b> The sample strategies, which the teacher can use to accelerate the attainment of the various course outcomes are listed in the following: <ol style="list-style-type: none"><li>1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.</li><li>2. Show Video/animation films to explain the functioning of various techniques.</li><li>3. Encourage collaborative (Group) Learning in the class</li><li>4. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking</li><li>5. Topics will be introduced in multiple representations.</li><li>6. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.</li></ol>			
Module-1			
<b>Multimedia Communications:</b> Introduction, Multimedia information representation, Multimedia networks, multimedia applications, Application and networking terminology. (Chapter 1 of Text 1)			
<b>Teaching-Learning Process</b>	Chalk and talk method, Power point presentation <b>RBT Level:</b> L1, L2		
Module-2			
<b>Information Representation:</b> Introduction, Digitization principles, Text, Images, Audio and Video. (Chapter 2 of Text 1)			
<b>Teaching-Learning Process</b>	Chalk and talk method, Power point presentation <b>RBT Level:</b> L1, L2, L3		
Module-3			
<b>Text and Image Compression:</b> Introduction, Compression principles, text compression, image Compression. (Chapter 3 of Text 1 )			
<b>Teaching-Learning Process</b>	Chalk and talk method, Power point presentation <b>RBT Level:</b> L1, L2, L3		

<b>Module-4</b>	
<b>Audio and video compression:</b> Introduction, Audio compression, video compression, video compression principles, video compression. (Chapter 4 of Text 1)	
<b>Teaching-Learning Process</b>	Chalk and talk method, Power point presentation <b>RBT Level:</b> L1, L2, L3
<b>Module-5</b>	
<b>Multimedia Information Networks:</b> Introduction, LANs, Ethernet, Token ring, Bridges, FDDI High-speed LANs, LAN protocol (Chap. 8 of Text 1).	
<b>Teaching-Learning Process</b>	Chalk and talk method, Power point presentation <b>RBT Level:</b> L1, L2
<b>Course outcomes (Course Skill Set)</b> At the end of the course the student will be able to: <ol style="list-style-type: none"> <li>1. Understand basics of different multimedia networks and applications.</li> <li>2. Understand different compression techniques to compress audio and video.</li> <li>3. Describe multimedia Communication across Networks.</li> <li>4. Analyse different media types to represent them in digital form.</li> <li>5. Compress different types of text and images using different compression techniques.</li> </ol>	
<b>Assessment Details (both CIE and SEE)</b> The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together. <b>Continuous Internal Evaluation:</b> Three Unit Tests each of <b>20 Marks (duration 01 hour)</b> <ol style="list-style-type: none"> <li>1. First test at the end of 5<sup>th</sup> week of the semester</li> <li>2. Second test at the end of the 10<sup>th</sup> week of the semester</li> <li>3. Third test at the end of the 15<sup>th</sup> week of the semester</li> </ol> Two assignments each of <b>10 Marks</b> <ol style="list-style-type: none"> <li>4. First assignment at the end of 4<sup>th</sup> week of the semester</li> <li>5. Second assignment at the end of 9<sup>th</sup> week of the semester</li> </ol> Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for <b>20 Marks (duration 01 hours)</b> <ol style="list-style-type: none"> <li>6. At the end of the 13<sup>th</sup> week of the semester</li> </ol> The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be <b>scaled down to 50 marks</b> (to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course). <b>CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.</b> <b>Semester End Examination:</b> Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject ( <b>duration 03 hours</b> ) <ol style="list-style-type: none"> <li>1. The question paper will have ten questions. Each question is set for 20 marks.</li> <li>2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), <b>should have a mix of topics</b> under that module.</li> </ol> The students have to answer 5 full questions, selecting one full question from each module.	

**Suggested Learning Resources:****Text Books:**

Multimedia Communications- Fred Halsall, Pearson Education, 2001, ISBN -978813170994

**Reference Books:**

1. Multimedia: Computing, Communications and Applications- Raif Steinmetz, Klara Nahrstedt, Pearson Education, 2002, ISBN-978817758
2. Fundamentals of Multimedia – Ze-Nian Li, Mark S Drew, and Jiangchuan Liu.

**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

- Implementation of compression algorithms using MATLAB/ any open source tools (Python, Scilab, etc.)