

## V Semester

<b>Technological Innovation Management &amp; Entrepreneurship</b>			Semester	V
Course and Course Code	HSMS	<b>BXX501</b>	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0		SEE Marks	50
Total Hours of Pedagogy	40 hours		Total Marks	100
Credits	3		Exam Hours	3
Examination nature (SEE)	Theory			
<p><b>Course objectives:</b>            After completion of the course, the students will be able to</p> <ul style="list-style-type: none"> <li>• Understand basic skills of Management</li> <li>• Understand the need for Entrepreneurs and their skills</li> <li>• Identify the Management functions and Social responsibilities.</li> <li>• Understand the identification of Business, drafting the Business plan and sources of funding.</li> </ul>				
<p><b>Teaching-Learning Process (General Instructions)</b>            These are sample Strategies; that teachers can use to accelerate the attainment of the various course outcomes.</p> <ul style="list-style-type: none"> <li>• Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.</li> <li>• Show Video/animation films to explain the functioning of various techniques.</li> <li>• Encourage collaborative (Group) Learning in the class</li> <li>• Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking</li> <li>• Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.</li> <li>• Topics will be introduced in multiple representations.</li> <li>• Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.</li> <li>• Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.</li> </ul>				
<b>MODULE – 1</b>				
<p><b>Management:</b> Nature and Functions of Management – Importance, Definition, Management Functions, Levels of Management, Roles of Manager, Managerial Skills, Management &amp; Administration, Management as a Science, Art &amp; Profession (Selected topics of Chapter 1, Text 1).</p> <p><b>Planning:</b> Planning-Nature, Importance, Types, Steps and Limitations of Planning; Decision Making – Meaning, Types and Steps in Decision Making( Text 1).</p>				
<b>Teaching-Learning Process RBT Levels</b>		Chalk and talk method, YouTube Videos, Power Point Presentation. L2, L3		
<b>MODULE – 2</b>				
<p><b>Organizing and Staffing:</b> Organization-Meaning, Characteristics, Process of Organizing, Principles of Organizing, Span of Management (meaning and importance only), Departmentalization-Process Departmentalization, Purpose Departmentalization ,Committees- Meaning, Types of Committees. Staffing-Need and Importance, Recruitment and Selection Process.</p>				

<b>Directing and Controlling:</b> Meaning and Requirements of Effective Direction, Giving Orders; Motivation-Nature of Motivation, Motivation Theories (Maslow's Need-Hierarchy Theory and Herzberg's Two Factor Theory); Communication – Meaning, Importance and Purposes of Communication (Text 1).	
<b>Teaching-Learning Process</b> <b>RBT Levels</b>	Chalk and talk method, YouTube Videos, Power Point Presentation. L2, L3
<b>MODULE – 3</b>	
<b>Leadership</b> -Meaning, Characteristics, Behavioural Approach of Leadership; Coordination-Meaning, Types, Techniques of Coordination; Controlling – Meaning, Need for Control System, Benefits of Control, Essentials of Effective Control System, Steps in Control Process ( Text 1). <b>Social Responsibilities of Business:</b> Meaning of Social Responsibility, Social Responsibilities of Business towards Different Groups, Social Audit, Business Ethics and Corporate Governance (Text 1).	
<b>Teaching-Learning Process</b> <b>RBT Levels</b>	Chalk and talk method, YouTube Videos, Power Point Presentation. L1, L2, L3
<b>MODULE – 4</b>	
<b>Entrepreneurship:</b> Introduction, Evolution of the concept of Entrepreneurship, Entrepreneurship today, Types of Entrepreneurs, Entrepreneurship, Entrepreneurial competencies, Capacity Building for Entrepreneurs. <b>Identification of Business Opportunities:</b> Introduction, Mobility of Entrepreneurs, Business opportunities in India, Models for opportunity Evaluation.	
<b>Teaching-Learning Process</b> <b>RBT Levels</b>	Chalk and talk method, YouTube Videos, Power Point Presentation. L1, L2, L3
<b>MODULE – 5</b>	
<b>Business plans:</b> Introduction, purpose of a Business plan, contents of a Business plan, presenting a Business plan, why do some Business plan fail? Procedure for setting up an Enterprise. <b>Institutions supporting Business opportunities:</b> Central level institutions- National Board for micro, small & medium Enterprises(NBMSME),MSME-DO, National Small Industries Corporation. State level institutions- state Directorate Industries and commerce, District Industries Centres, state financial Corporations, State Industrial Development Corporation(SIDC), State Industrial Area Development Board (SIADB). Other Institutions - NABARD, Technical consultancy organisation (TCO), Small Industries Development Bank of India(SIDBI), Export Promotion Councils, Non governmental Organisations.	
<b>Teaching-Learning Process</b> <b>RBT Levels</b>	Chalk and talk method, YouTube Videos, Power Point Presentation. L1, L2, L3
<b>Course outcomes (Course Skill Set):</b> At the end of the course, the student will be able to: 1) Understand the fundamental concepts of Management and its functions. 2) Understand the different functions to be performed by managers/Entrepreneur. 3) Understand the social responsibilities of a Business. 4) Understand the Concepts of Entrepreneurship and to identify Business opportunities. 5) Understand the components in developing a business plan and awareness about various sources of funding and Institutions supporting Entrepreneur.	
<b>Assessment Details (both CIE and SEE)</b> The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/	

course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

### **Continuous Internal Evaluation:**

- For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25 marks.
- The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered
- Any two assignment methods mentioned in the 220B2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.
- For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.

**Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

### **Semester-End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**).

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

### **Suggested Learning Resources:**

#### **Text Books**

- 1) Principles of Management – P.C Tripathi, P.N Reddy, McGraw Hill Education, 6th Edition, 2017. ISBN-13:978-93-5260-535-4.
- 2) Entrepreneurship Development Small Business Enterprises- Poornima M Charantimath, 2nd Edition, Pearson Education 2018, ISBN 978-81-317-6226-4.

#### **Reference Books**

- 1) Essentials of Management: An International, Innovation and Leadership perspective by Harold Koontz, Heinz Weihrich McGraw Hill Education, 10th Edition 2016. ISBN- 978-93-392-2286-4.

### **Web links and Video Lectures (e-Resources):**

- <https://nptel.ac.in/courses/110107094>
- <https://nptel.ac.in/courses/110106141>
- <https://nptel.ac.in/courses/122106031>

### **Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

- Quizzes,
- Assignments,
- Seminars

<b>OBJECT ORIENTED PROGRAMMING USING JAVA</b>		Semester	<b>V</b>
Course Code	<b>BUE502</b>	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:2:0	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory + 8-10 Lab slots	Total Marks	100
Credits	04	Exam Hours	3 Hours
Examination Type (SEE)	Theory		
<p><b>Course Objectives:</b></p> <ul style="list-style-type: none"> <li>To learn primitive constructs in JAVA programming language.</li> <li>To understand Object Oriented Programming Features of JAVA.</li> <li>To gain knowledge on packages, multithreaded programming and exceptions.</li> </ul>			
<p><b>Teaching-Learning Process (General Instructions)</b>  These are sample Strategies; that teachers can use to accelerate the attainment of the various course outcomes.</p> <ol style="list-style-type: none"> <li>Use Online Java Compiler IDE: <a href="https://www.jdoodle.com/online-java-compiler/">https://www.jdoodle.com/online-java-compiler/</a> or any other.</li> <li>Demonstration of programming examples.</li> <li>Chalk and board, Power point presentations.</li> <li>Online material (Tutorials) and video lectures.</li> </ol>			
<b>MODULE-1</b>			
<p><b>Data Types, Variables, and Arrays:</b> The Primitive Types (Integers, Floating-Point Types, Characters, Booleans), Variables, Type Conversion and Casting, Arrays.</p> <p><b>Operators:</b> Arithmetic Operators, Relational Operators, Boolean Logical Operators, The Assignment Operator, The ? Operator, Operator Precedence.</p> <p><b>Control Statements:</b> Java's Selection Statements (if, The Traditional switch), Iteration Statements (while, do-while, for, Nested Loops), Jump Statements (Using break, Using continue, return).</p> <p style="text-align: right;"><b>RBT Levels:</b> L1, L2</p>			
<b>MODULE-2</b>			
<p><b>Introducing Classes:</b> Class Fundamentals, Declaring Objects, Assigning Object Reference Variables, Introducing Methods, Constructors, The this Keyword.</p> <p><b>Methods and Classes:</b> Overloading Methods, Objects as Parameters, Argument Passing, Returning Objects.</p> <p style="text-align: right;"><b>RBT Levels:</b> L1, L2</p>			
<b>MODULE-3</b>			
<p><b>Inheritance:</b> Inheritance Basics, Using super, Creating a Multilevel Hierarchy, When Constructors Are Executed, Method Overriding, Using Abstract Classes.</p> <p><b>Interfaces:</b> Interfaces, Default Interface Methods, Use static Methods in an Interface, Private Interface Methods.</p> <p style="text-align: right;"><b>RBT Levels:</b> L1, L2, L3</p>			
<b>MODULE-4</b>			
<p><b>Packages:</b> Packages, Packages and Member Access, Importing Packages.</p> <p><b>Exceptions:</b> Exception-Handling Fundamentals, Exception Types, Uncaught Exceptions, Using try and catch, Nested try Statements, throw, throws, finally, Java's Built-in Exceptions.</p> <p style="text-align: right;"><b>RBT Levels:</b> L1, L2, L3</p>			
<b>MODULE-5</b>			
<p><b>Multithreaded Programming:</b> The Java Thread Model, The Main Thread, Creating a Thread, Creating Multiple Threads, Using <code>isAlive()</code> and <code>join()</code>.</p> <p><b>Enumerations, Type Wrappers and Autoboxing:</b> Enumerations (The <code>values()</code> and <code>valueOf()</code> Methods), Type Wrappers (Character, Boolean, The Numeric Type Wrappers), Autoboxing (Autoboxing and Methods).</p> <p style="text-align: right;"><b>RBT Levels:</b> L1, L2, L3</p>			



## PRACTICAL COMPONENT OF IPCC

Sl. No.	Experiments
1.	Write a JAVA program that prints all real solutions to the quadratic equation $ax^2+bx+c=0$ . Read in a, b, c and use the quadratic formula.
2.	Create a JAVA class called Student with the following details as variables within it. <ul style="list-style-type: none"><li>• USN</li><li>• Name</li><li>• Branch</li><li>• Phone</li></ul> Write a JAVA program to create n Student objects and print the USN, Name, Branch, and Phone of these objects with suitable headings.
3.	Write a JAVA program for Arithmetic calculator using switch case menu.
4.	Develop a JAVA program to add TWO matrices of suitable order N (The value of N should be read from command line arguments).
5.	Develop a JAVA program to create a class named shape. Create three sub classes namely: circle, triangle and square, each class has two member functions named draw () and erase (). Demonstrate polymorphism concepts by developing suitable methods, defining member data and main program.
6.	Write a JAVA program demonstrating Method overloading and Constructor overloading.
7.	Develop a JAVA program to raise a custom exception (user defined exception) for DivisionByZero using try, catch, throw and finally.
8.	<b>Demo Experiment:</b> Design a super class called Staff with details as Staff_ID, Name, Phone, Salary. Extend this class by writing three subclasses namely Teaching (domain, publications), Technical (skills), and Contract (period). Write a JAVA program to read and display at least 3 staff objects of all three categories.
9.	<b>Demo Experiment:</b> Develop a JAVA application to implement currency converter (Dollar to INR, EURO to INR, Yen to INR and vice versa), distance converter (meter to KM, miles to KM and vice versa), time converter (hours to minutes, seconds and vice versa) using packages.

### Course Outcomes (Course Skill Set):

At the end of the course, the student will be able to:

**CO 1:** Demonstrate proficiency in writing simple programs involving branching and looping structures.

**CO 2:** Design a class involving data members and methods for the given scenario.

**CO 3:** Apply the concepts of inheritance and interfaces in solving real world problems.

**CO 4:** Use the concept of packages and exception handling in solving complex problem.

**CO 5:** Apply concepts of multithreading, autoboxing and enumerations in program development.

### Assessment Details (both CIE and SEE):

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

The IPCC means the practical portion integrated with the theory of the course. CIE marks for the theory component are **25 marks** and that for the practical component is **25 marks**.

### CIE for the theory component of the IPCC:

- 25 marks for the theory component are split into **15 marks** for two Internal Assessment Tests (Two Tests, each of 15 Marks with 01-hour duration, are to be conducted) and **10 marks** for other assessment methods mentioned in 22OB4.2. The first test at the end of 40-50% coverage of the syllabus and the second test after covering 85-90% of the syllabus.
- Scaled-down marks of the sum of two tests and other assessment methods will be CIE marks for the theory component of IPCC (that is for **25 marks**).

- The student has to secure 40% of 25 marks to qualify in the CIE of the theory component of IPCC.

#### **CIE for the practical component of the IPCC:**

- **15 marks** for the conduction of the experiment and preparation of laboratory record, and **10 marks** for the test to be conducted after the completion of all the laboratory sessions.
- On completion of every experiment/program in the laboratory, the students shall be evaluated including viva-voce and marks shall be awarded on the same day.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to **15 marks**.
- The laboratory test (**duration 02/03 hours**) after completion of all the experiments shall be conducted for 50 marks and scaled down to **10 marks**.
- Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **25 marks**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the practical component of the IPCC.

#### **SEE for IPCC:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored by the student shall be proportionally scaled down to 50 Marks.

**The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper may include questions from the practical component.**

- The minimum marks to be secured in CIE to appear for SEE shall be 10 (40% of maximum marks-25) in the theory component and 10 (40% of maximum marks-25) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included. The maximum of 04/05 sub-questions are to be set from the practical component of IPCC, the total marks of all questions should not be more than 20 marks.
- SEE will be conducted for 100 marks and students shall secure 35% of the maximum marks to qualify for the SEE. Marks secured will be scaled down to 50.
- The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

#### **Suggested Learning Resources:**

##### **Textbook:**

1. Java: The Complete Reference, Twelfth Edition, by Herbert Schildt, November 2021, McGraw-Hill, ISBN: 9781260463422.

##### **Reference Books:**

1. Programming with Java, 6th Edition, by E Balagurusamy, Mar-2019, McGraw Hill Education, ISBN: 9789353162337.
2. Thinking in Java, Fourth Edition, by Bruce Eckel, Prentice Hall, 2006 ([https://sd.blackball.lv/library/thinking\\_in\\_java\\_4th\\_edition.pdf](https://sd.blackball.lv/library/thinking_in_java_4th_edition.pdf))

**Web links and Video Lectures (e-Resources):**

- Java Tutorial: <https://www.geeksforgeeks.org/java/>
- Introduction To Programming In Java: <https://ocw.mit.edu/courses/6-092-introduction-to-programming-in-java-january-iap-2010/>
- Java Tutorial: <https://www.w3schools.com/java/>
- Java Tutorial: <https://www.javatpoint.com/java-tutorial>
- Installation of Java: [https://www.java.com/en/download/help/index\\_installing.html](https://www.java.com/en/download/help/index_installing.html)
- <https://nptel.ac.in/>

**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning:**

- Demonstration of online IDEs like geeks for geeks, jdoodle or any other Tools.
- Demonstration of class diagrams for the class abstraction, type visibility, composition and inheritance.
- Programming Assignment / Course Project.

<b>DIGITAL SYSTEM DESIGN USING VERILOG</b>		Semester	<b>V</b>
Course Code	<b>BUE503</b>	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	04	Exam Hours	3 Hours
Examination type (SEE)	<b>Theory</b>		
<p><b>Course objectives:</b></p> <ol style="list-style-type: none"> <li>To know the basic language features of Verilog HDL and the role of HDL in digital logic design.</li> <li>To know the behavioural modeling of combinational and simple sequential circuits.</li> <li>To know the behavioural modeling of algorithmic state machines.</li> <li>To know the synthesis of combinational and sequential descriptions.</li> <li>To know the architectural features of programmable logic devices.</li> </ol>			
<p><b>Teaching-Learning Process (General Instructions)</b>  These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.</p> <ol style="list-style-type: none"> <li>Chalk and Talk</li> <li>PowerPoint Presentation and Videos</li> <li>Flipped Classes</li> <li>Practice session</li> </ol>			
<b>Module-1</b>			
<p><b>Introduction to Digital Design Methodology:</b> Design Methodology-An Introduction, IC Technology Options.  <b>Review of Combinational Logic Design:</b> Glitches and Hazards  <b>Introduction to Logic Design with Verilog :</b> Structural models of combination logic, logic system, design verification and Test methodology, propagation delay, truth table models of combinational and sequential logic with verilog modules.</p> <p style="text-align: right;"><b>RBT Level: L1,L2</b></p>			
<b>Module-2</b>			
<p><b>Logic Design With Behavioral Models of Combinational And Sequential Logic</b>  :Behavioral modeling, A Brief Look at data types for behavioural modeling, Boolean Equation-Based behavioral models of combinational logic, propagation delay and continuous assignments, latches and level sensitive circuits in verilog, cyclic behavioural models of flip flops and latches, cyclic behavior and edge detection, a comparison of styles for behavioral modelling. Behavioral Models of Multiplexers, Encoders, and Decoders, Dataflow Models of a Linear-Feedback Shift Register, Design Documentation with Functions and Tasks: Legacy or Lunacy?</p> <p style="text-align: right;"><b>RBT Level: L1,L2,L3</b></p>			
<b>Module-3</b>			
<p><b>Logic Design With Behavioral Models of Combinational And Sequential Logic</b>  :Algorithmic State Machine Charts for Behavioral Modeling, Behavioral Models of Counters, Shift Registers, and Register Files  <b>Synthesis of Combinational and Sequential Logic :</b> Introduction to Synthesis, Synthesis of Combinational Logic, Synthesis of Sequential Logic with Latches</p> <p style="text-align: right;"><b>RBT Level: L1,L2,L3</b></p>			



<b>Module-4</b>
<p><b>Fundamentals of Sequential Logic Design:</b> Design of Sequential Machines, State-Transition Graphs, Design Example: BCD to Excess-3 Code Converter, Serial-Line Code Converter for Data Transmission.</p> <p><b>Synthesis of Combinational and Sequential Logic:</b> Synthesis of Explicit State Machines, Synthesis of Implicit State Machines, Registers and Counters.</p> <p style="text-align: right;"><b>RBT Level: L1,L2,L3</b></p>
<b>Module-5</b>
<p><b>Programmable Logic and Storage Devices :</b> Programmable Logic Devices, Storage Devices, Programmable Logic Array (PLA), Programmable Array Logic (PAL) ,Programmability of PLDs ,Complex PLDs (CPLDs) ,Field-Programmable Gate Arrays</p> <p style="text-align: right;"><b>RBT Level: L1,L2</b></p>
<p><b>Course outcome (Course Skill Set)</b></p> <p>At the end of the course, the student will be able to :</p> <ol style="list-style-type: none"> <li>1. Demonstrate knowledge on HDL design flow, digital circuits design.</li> <li>2. Design and develop the combinational and sequential circuits using behavioural modelling.</li> <li>3. Solving algorithmic state machines using hardware description language.</li> <li>4. Analyse the process of synthesizing the combinational and sequential descriptions.</li> <li>5. Memorizing the advantages of programmable logic devices and their description in Verilog.</li> </ol>

### **Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

#### **Continuous Internal Evaluation:**

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

**Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

#### **Semester-End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**).

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

#### **Suggested Learning Resources:**

##### **TEXTBOOKS**

1. Michael D Ciletti - Advanced Digital Design with the VERILOG HDL, 2ND Edition, PHI, 2009

##### **REFERENCE BOOK(s):**

1. Stephen Brown and Zvonko Vranesic - Fundamentals of Digital Logic with Verilog, 2nd Edition, TMH, 2008.
2. Z Navabi - Verilog Digital System Design, 2nd Edition, McGraw Hill, 2005.

#### **Web links and Video Lectures (e-Resources):**

- <https://nptel.ac.in/>

**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

- Online Resources and Tutorials
- Verilog Simulation Projects
- Quiz
- Seminars

<b>VERILOG LAB</b>		Semester	<b>V</b>
Course Code	<b>BUEL504</b>	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:0:2:0	SEE Marks	50
Credits	01	Total SEE+CIE	100
<b>Total Hours of Pedagogy</b>	12-14 slots	Exam Hours	2 Hours
Examination type (SEE)	<b>Practical</b>		
<b>Course objectives:</b>			
This course will enable students to:			
<ul style="list-style-type: none"> <li>• Familiarize with the CAD tool to write HDL programs.</li> <li>• Understand simulation and synthesis of digital design.</li> <li>• Program FPGAs/CPLDs to synthesize the digital designs.</li> <li>• Interface hardware to programmable ICs through I/O ports.</li> </ul>			
<b>SL.NO</b>	<b>Write the Verilog Code, Simulate, Synthesize and Implement on the Hardware.</b>		
1	Half Adder, Full Adder using three modelling styles		
2	Flip Flops: MS, RS, JK, D, T		
3	N-Bit Comparator		
4	a) 3:8 Decoder b) 8:3 Priority Encoder		
5	a) 4:1 Multiplexer b) 1:4 Demultiplexer c) BCD to Excess 3 Converter and vice versa d) Binary to Gray Converter and vice versa		
6	a) N-bit Synchronous Up-Down Counter b) N-bit Asynchronous Up-Down Counter		
7	a) 4-Bit Serial Shift Register b) 4 Bit Universal Shift Register		
	<b>Interfacing Experiments</b>		
8	Seven-Segment Light-Emitting Diode (LED) Display.		
9	Stepper motor		
10	ADC/DAC		
11	Elevator		
	<b>Demonstration Experiments</b>		
1.	UART protocol		
2.	I2C protocol		
<b>Course outcomes (Course Skill Set):</b>			
At the end of the course the student will be able to:			
<b>C01.</b>	Understanding of Hardware Description and Synthesis		
<b>C02.</b>	Problem-Solving and Analytical Thinking		
<b>C03.</b>	Synthesis and Optimization Skills		
<b>C04.</b>	Logical and Sequential Circuit Design		
<b>C05.</b>	Verilog Programming Proficiency		

### Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

#### Continuous Internal Evaluation (CIE):

CIE marks for the practical course are **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment is to be evaluated for conduction with an observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments are designed by the faculty who is handling the laboratory session and are made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled down to **30 marks** (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct a test of 100 marks after the completion of all the experiments listed in the syllabus.
- In a test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- The marks scored shall be scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and marks of a test is the total CIE marks scored by the student.

#### Semester End Evaluation (SEE):

- SEE marks for the practical course are 50 Marks.
- **SEE shall be conducted by the two examiners. One from the same institute as an internal examiner and another from a different institute as an external examiner, appointed by the university.**
- The examination schedule and names of examiners are informed to the university before the conduction of the examination. These practical examinations are to be conducted between the schedule mentioned in the academic calendar of the University.
- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.
- Students can pick one question (experiment) from the questions lot prepared by the examiners jointly.
- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% of Marks allotted to the procedure part are to be made zero.

The minimum duration of SEE is 02 hours

#### Suggested Learning Resources:

- <https://nptel.ac.in/>



<b>Digital Communication</b>		Semester	<b>V</b>
Course Code	<b>BUE515A</b>	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	3 Hours
Examination type (SEE)	<b>Theory</b>		
<p><b>Course objectives:</b>  <b>This course will enable students to:</b></p> <ul style="list-style-type: none"> <li>• Understand the mathematical representation of signal, symbol, noise and channels.</li> <li>• Apply the concept of signal conversion to symbols and signal processing to symbols in transmitter and receiver functional blocks.</li> <li>• Compute performance issues and parameters for symbol processing and recovery in ideal and corrupted channel conditions.</li> </ul>			
<p><b>Teaching-Learning Process (General Instructions)</b>  These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.</p> <ol style="list-style-type: none"> <li>1. Chalk and Talk.</li> <li>2. Power Presentation and Videos.</li> <li>3. Flipped Classes.</li> <li>4. Practice Sessions.</li> </ol>			
<b>Module-1</b>			
<p><b>Band-pass Signal to Equivalent Lowpass:</b> Hilbert Transform, Pre-envelopes, Complex envelopes, Canonical representation of bandpass signals, Complex low-pass representation of band pass systems, Complex representation of band pass signals and systems.</p> <p><b>Line codes:</b> Uni-polar, Polar, Bipolar (AMI) and Manchester code and their power spectral densities.  <b>RBT Levels:</b> L1, L2</p>			
<b>Module-2</b>			
<p><b>Signaling over AWGN Channels:</b> Introduction, Geometric representation of signals, Gram Schmidt Orthogonalization procedure, Conversion of the continuous AWGN channel in to a vector channel, Optimum receivers using coherent detection: ML Decoding, Correlation receiver, matched filter receiver.  <b>RBT Levels:</b> L1, L2, L3</p>			
<b>Module-3</b>			
<p><b>Digital Modulation Techniques:</b> Phase shift Keying techniques using coherent detection: generation, detection and error probabilities of BPSK and QPSK, M-ary PSK, M-ary QAM.</p> <p><b>Frequency shift keying techniques using Coherent detection:</b> BFSK generation, detection and error probability.</p> <p><b>Non coherent orthogonal modulation techniques:</b> BFSK, DPSK Symbol representation, Block diagram of Transmitter and Receiver.  <b>RBT Levels:</b> L1, L2, L3</p>			
<b>Module-4</b>			
<p><b>Digital Communication through Band Limited Channels:</b> Characterization of Band-Limited Channels Signal Design for Band-Limited Channels, Design of Band-Limited Signals for No Inter symbol Interference—The Nyquist Criterion, Design of Band-Limited Signals with Controlled ISI—Partial-Response Signals, Data Detection for Controlled ISI, Signal Design for Channels with Distortion, Optimum Maximum-Likelihood Receiver, A Discrete-Time Model for a Channel with ISI.  <b>RBT Levels:</b> L1, L2, L3</p>			
<b>Module-5</b>			
<p><b>Principles of Spread Spectrum:</b> Spread Spectrum Communication Systems: Model of a Spread Spectrum Digital Communication System, Direct Sequence Spread Spectrum Systems, Effect of De-spreading on a narrowband Interference, Probability of error (statement only), Some applications of DS Spread Spectrum Signals, Generation of PN Sequences, Frequency Hopped Spread Spectrum, CDMA based on IS-95.  <b>RBT Levels:</b> L1, L2, L3</p>			

**Course outcome (Course Skill Set)**

At the end of the course, the student will be able to :

**CO 1:** Associate and apply the concepts of Band-pass sampling to well specified signals and channels.

**CO 2:** Analyze and compute performance parameters and transfer rates for low pass and band pass symbol under ideal and corrupted non-band limited channels.

**CO 3:** Test and validate symbol processing and performance parameters at the receiver under ideal and corrupted band-limited channels.

**CO 4:** Demonstrate by simulation and emulation that band pass signals subjected to corrupted and distorted symbols in a band limited channel, can be demodulated and estimated at receiver to meet specified performance criteria.

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous Internal Evaluation:**

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 220B2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

**Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester-End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**).

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

**Suggested Learning Resources:****Text Books:**

1. Simon Haykin – Digital Communication Systems, John Wiley & sons, First Edition, 2014, ISBN978-0-471-64735-5.
2. John G Proakis and Masoud Salehi - Fundamentals of Communication Systems, 2014 Edition, Pearson Education, ISBN978-8-131-70573-5.

**Reference Books:**

1. B. P. Lathi and Zhi Ding - Modern Digital and Analog Communication Systems, Oxford University Press, 4<sup>th</sup> Edition, 2010, ISBN: 978-0-198-07380-2.

2. Ian A Glover and Peter M Grant –Digital Communications, Pearson Education,Third Edition, 2010, ISBN 978-0-273-71830-7.
3. John G Proakis and Masoud Salehi – Communication Systems Engineering, 2<sup>nd</sup> Edition, Pearson Education, ISBN 978-93-325-5513-6.

**Web links and Video Lectures (e-Resources):**

- <https://nptel.ac.in/>

**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

- Quiz
- Seminar

<b>ADVANCED COMPUTER ARCHITECTURE</b>		Semester	V
Course Code	BUE515B	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03
Examination type (SEE)	Theory		
<b>Course objectives:</b>			
<ul style="list-style-type: none"> <li>• To make students understand the basic structure and operation of computer system.</li> <li>• To measure the performance of architectures in terms of right parameters.</li> <li>• To understand the concepts of various memories.</li> <li>• To summarize parallel architecture and the software used for them.</li> </ul>			
<b>Teaching-Learning Process (General Instructions)</b>			
These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.			
<ol style="list-style-type: none"> <li>1. Lecturer methods (L) need not to be only a traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes.</li> <li>2. Use of Video/Animation to explain functioning of various concepts.</li> <li>3. Encourage collaborative (Group Learning) Learning in the class.</li> <li>4. Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking.</li> <li>5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyze information rather than simply recall it.</li> </ol>			
<b>Module-1</b>			
<b>Theory of Parallelism:</b> Parallel Computer Models, The State of Computing, Multiprocessors and Multicomputer, Multivector and SIMD Computers, PRAM and VLSI Models, Program and Network Properties, Conditions of Parallelism, Program Partitioning and Scheduling, Program Flow Mechanisms, System Interconnect Architectures, Principles of Scalable Performance, Performance Metrics and Measures, Parallel Processing Applications, Speedup Performance Laws. For all Algorithm or mechanism any one example is sufficient.			
<b>RBT Levels:</b> L1, L2			
<b>Module-2</b>			
<b>Hardware Technologies 1:</b> Processors and Memory Hierarchy, Advanced Processor Technology, Superscalar and Vector Processors, Memory Hierarchy Technology, Virtual Memory Technology. For all Algorithms or mechanisms any one example is sufficient.			
<b>RBT Levels:</b> L1, L2			
<b>Module-3</b>			
<b>Hardware Technologies 2:</b> Bus Systems, Cache Memory Organizations, Shared Memory Organizations, Sequential and Weak Consistency Models, Pipelining and Superscalar Techniques, Linear Pipeline Processors, Nonlinear Pipeline Processors. For all Algorithms or mechanisms any one example is sufficient.			
<b>RBT Levels:</b> L1, L2			
<b>Module-4</b>			
<b>Parallel and Scalable Architectures:</b> Multiprocessors and Multicomputers, Multiprocessor System Interconnects, Cache Coherence and Synchronization Mechanisms, Message-Passing Mechanisms, Multivector and SIMD Computers, Vector Processing Principles, Multivector Multiprocessors, Compound Vector Processing, Scalable, Multithreaded, and Dataflow Architectures, Latency-Hiding Techniques, Principles of Multithreading, Fine- Grain Multicomputer. For all Algorithms or mechanisms any one example is sufficient.			
<b>RBT Levels:</b> L3, L4			

<b>Module-5</b>
<p><b>Software for parallel programming:</b> Parallel Models, Languages, and Compilers, Parallel Programming Models, Parallel Languages and Compilers, Dependence Analysis of Data Arrays. Instruction and System Level Parallelism, Instruction Level Parallelism, Computer Architecture, Contents, Basic Design Issues, Problem Definition, Model of a Typical Processor, Compiler-detected Instruction Level Parallelism ,Operand Forwarding ,Reorder Buffer, Register Renaming, Tomasulo's Algorithm. For all Algorithms or mechanisms any one example is sufficient.</p> <p style="text-align: right;"><b>RBT Levels: L3, L4</b></p>
<p><b>Course outcome (Course Skill Set)</b></p> <p>At the end of the course, the student will be able to :</p> <p><b>CO 1:</b> Explain the concepts of parallel computing  <b>CO 2:</b> Explain and identify the hardware technologies  <b>CO 3:</b> Compare and contrast the parallel architectures  <b>CO 4:</b> Illustrate parallel programming concepts</p>
<p><b>Assessment Details (both CIE and SEE)</b></p> <p>The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.</p> <p><b>Continuous Internal Evaluation:</b></p> <ul style="list-style-type: none"> <li>• For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25 marks.</li> <li>• The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered</li> <li>• Any two assignment methods mentioned in the 220B2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.</li> <li>• For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.</li> </ul> <p><b>Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.</b></p> <p><b>Semester-End Examination:</b></p> <p>Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (<b>duration 03 hours</b>).</p> <ol style="list-style-type: none"> <li>1. The question paper will have ten questions. Each question is set for 20 marks.</li> <li>2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), <b>should have a mix of topics</b> under that module.</li> <li>3. The students have to answer 5 full questions, selecting one full question from each module.</li> <li>4. Marks scored shall be proportionally reduced to 50 marks</li> </ol>
<p><b>Suggested Learning Resources:</b></p> <p><b>Books</b></p> <p><b>Textbooks:</b></p> <ol style="list-style-type: none"> <li>1. John L.Hennessy and David A Patterson ,Computer architecture : A Quantitative approach ,Morgan</li> </ol>



Kaufmann ,6<sup>th</sup> edition ,2017.

2. Kai Hwang and Naresh Jotwani, Advanced Computer Architecture (SIE): Parallelism, Scalability, Programmability, McGraw Hill Education 3/e. 2015 .

**Reference Books:**

1. William Stallings, “Computer Organization and Architecture – Designing for Performance”, Pearson Education, Ninth Edition, 2012

**Web links and Video Lectures (e-Resources):**

**WEB LINKS FOR REFERENCE**

- <https://nptel.ac.in/>

**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

- Quiz
- Seminar

<b>Software Engineering and Project Management</b>		Semester	V
Course Code	<b>BUE515C</b>	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	3 Hours
Examination type (SEE)	<b>Theory</b>		
<p><b>Course objectives:</b></p> <p><b>This course will enable students to:</b></p> <ul style="list-style-type: none"> <li>• Outline software engineering principles and activities involved in building large software programs.</li> <li>• Identify ethical and professional issues and explain why they are of concern to Software Engineers.</li> <li>• Describe the process of requirement gathering, requirement classification, requirement specification and requirements validation.</li> <li>• Infer the fundamentals of object oriented concepts, differentiate system models, use UML diagrams and apply design patterns.</li> <li>• Explain the role of DevOps in Agile Implementation.</li> <li>• Discuss various types of software testing practices and software evolution processes.</li> <li>• Recognize the importance Project Management with its methods and methodologies.</li> <li>• Identify software quality parameters and quantify software using measurements and metrics.</li> </ul>			
<p><b>Teaching-Learning Process (General Instructions)</b></p> <p>These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.</p> <ol style="list-style-type: none"> <li>1. Lecturer method (L) need not to be only a traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes.</li> <li>2. Use of Video/Animation to explain functioning of various concepts.</li> <li>3. Encourage collaborative (Group Learning) Learning in the class.</li> <li>4. Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking.</li> <li>5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyze information rather than simply recall it.</li> <li>6. Introduce Topics in manifold representations.</li> <li>7. Show the different ways to solve the same problem with different circuits/logic and encourage the students to come up with their own creative ways to solve them.</li> <li>8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.</li> </ol>			
<b>Module-1</b>			
<p><b>Introduction:</b> The evolving role of software, Software, The changing nature of software, Software engineering, A Process Framework, Process Patterns, Process Assessment, Personal and Team Process Models, Process Technology, Product and Process.</p> <p><b>Process Models:</b> Prescriptive models, Waterfall model, Incremental process models, Evolutionary process models, Specialized process models.</p> <p><b>Requirements Engineering:</b> Requirements Engineering Task, Initiating the Requirements Engineering process, Eliciting Requirements, Developing use cases, Building the analysis model, Negotiating Requirements, Validating Requirements, Software Requirement Document.</p> <p style="text-align: right;"><b>RBT Levels: L1,L2</b></p>			
<b>Module-2</b>			

<p><b>Introduction, Modelling Concepts and Class Modelling:</b> What is Object orientation? What is OO development? OO Themes; Evidence for usefulness of OO development; OO modelling history.</p> <p><b>Modelling as Design technique:</b> Modelling, abstraction, The Three models.</p> <p><b>Class Modelling:</b> Object and Class Concept, Link and associations concepts, Generalization and Inheritance, A sample class model, Navigation of class models, Introduction to RUP and UML diagrams.</p> <p><b>Building the Analysis Models:</b> Requirement Analysis, Analysis Model Approaches, Data modelling. Concepts, Object Oriented Analysis, Scenario-Based Modeling, Flow-Oriented Modeling, class Based Modeling, Creating a Behavioral Model.</p> <p style="text-align: right;"><b>RBT Levels: L2,L3</b></p>
<b>Module-3</b>
<p><b>Software Testing:</b> A Strategic Approach to Software Testing, Strategic Issues, Test Strategies for Conventional Software, Test Strategies for Object -Oriented Software, Validation Testing, System Testing, The Art of Debugging.</p> <p><b>Agile Methodology &amp; DevOps:</b> Before Agile – Waterfall, Agile Development.</p> <p><b>Self-Learning Section:</b> What is DevOps?, DevOps Importance and Benefits, DevOps Principles and Practices, 7 C's of DevOps Lifecycle for Business Agility, DevOps and Continuous Testing, How to Choose Right DevOps Tools?, Challenges with DevOps Implementation.</p> <p style="text-align: right;"><b>RBT Levels: L3,L4</b></p>
<b>Module-4</b>
<p><b>Introduction to Project Management:</b> Introduction, Project and Importance of Project Management, Contract Management, Activities Covered by Software Project Management, Plans, Methods and Methodologies, Some ways of categorizing Software Projects, Stakeholders, Setting Objectives, Business Case, Project Success and Failure, Management and Management Control, Project Management life cycle, Traditional versus Modern Project Management Practices.</p> <p style="text-align: right;"><b>RBT Levels: L1,L2</b></p>
<b>Module-5</b>
<p><b>Activity Planning:</b> Objectives of Activity Planning, When to Plan, Project Schedules, Sequencing and Scheduling Activities, Network Planning Models, Forward Pass– Backward Pass, Identifying critical path, Activity Float, Shortening Project Duration, Activity on Arrow Networks.</p> <p><b>Software Quality:</b> Introduction, The place of software quality in project planning, Importance of software quality, software quality models, ISO 9126, quality management systems, process capability models, techniques to enhance software quality, quality plans.</p> <p style="text-align: right;"><b>RBT Levels: L2,L3</b></p>
<p><b>Course outcome (Course Skill Set)</b></p> <p>At the end of the course, the student will be able to :</p> <p><b>CO 1:</b> Understand the activities involved in software engineering and analyze the role of various process models.</p> <p><b>CO 2:</b> Explain the basics of object-oriented concepts and build a suitable class model using modelling techniques.</p> <p><b>CO 3:</b> Describe various software testing methods and to understand the importance of agile methodology and DevOps.</p> <p><b>CO 4:</b> Illustrate the role of project planning and quality management in software development.</p> <p><b>CO 5:</b> Understand the importance of activity planning and different planning models.</p>
<p><b>Assessment Details (both CIE and SEE)</b></p> <p>The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.</p> <p><b>Continuous Internal Evaluation:</b></p> <ul style="list-style-type: none"> <li>• There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.</li> <li>• Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks</li> </ul>

- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

**Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

#### **Semester-End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**).

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

#### **Suggested Learning Resources:**

##### **Text Books:**

1. Roger S. Pressman: Software Engineering-A Practitioners approach, 7th Edition, Tata McGraw Hill.
2. Michael Blaha, James Rumbaugh: Object Oriented Modelling and Design with UML, 2nd Edition, Pearson Education, 2005.
3. Bob Hughes, Mike Cotterell, Rajib Mall: Software Project Management, 6th Edition, McGraw Hill Education, 2018.
4. Deepak Gaikwad, Viral Thakkar, DevOps Tools From Practitioner's Viewpoint, Wiley.
5. Ian Sommerville: Software Engineering, 9th Edition, Pearson Education, 2012.

##### **Reference Book:**

1. Pankaj Jalote: An Integrated Approach to Software Engineering, Wiley India.

##### **Web links and Video Lectures (e-Resources):**

- <https://nptel.ac.in/>

##### **Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

- Case study
- Field visit

<b>ADVANCED IOT</b>		Semester	V
Course Code	<b>BUE515D</b>	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	3 Hours
Examination type (SEE)	<b>Theory</b>		
<p><b>Course objectives:</b>  <b>This course will enable students to:</b></p> <ul style="list-style-type: none"> <li>• To understand the concepts of IOT and its applications in today's scenario.</li> <li>• To study the IoT network architecture and design.</li> <li>• To Understand IOT content generation and transport through networks use cases of IoT.</li> <li>• To Understand the devices employed for IOT data acquisition.</li> </ul>			
<p><b>Teaching-Learning Process (General Instructions)</b>  These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.</p> <ol style="list-style-type: none"> <li>1. Lecturer method (L) need not to be only a traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes.</li> <li>2. Use of Video/Animation to explain functioning of various concepts.</li> <li>3. Encourage collaborative (Group Learning) Learning in the class.</li> <li>4. Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking.</li> <li>5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyze information rather than simply recall it.</li> <li>6. Show the different ways to solve the same problem with different circuits/logic and encourage the students to come up with their own creative ways to solve them.</li> <li>7. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.</li> </ol>			
<b>Module-1</b>			
<p><b>What is IoT?:</b> Genesis of IoT, IoT and Digitization, IoT Impact – Connected Roadways, Connected Factory, Smart Connected Buildings, Smart Creatures, Convergence of IT and OT, Challenges.  <b>IoT Network Architecture and Design:</b> Drivers behind new network Architectures, Simplified IoT Architecture.  <b>RBT Levels:</b> L1,L2</p>			
<b>Module-2</b>			
<p><b>IoT Network Architecture and Design:</b> Core IoT Functional Stack, Things Layer, Communication Network Layer – Access Network Sublayer, Gateways and Backhaul Sublayer, Network Transport Sublayer, IoT Network Management Sublayer. Applications and Analytics Layer, IoT Data Management and Compute Stack.  <b>RBT Levels:</b> L2,L3</p>			
<b>Module-3</b>			
<p><b>Engineering IoT Networks-1:</b> Things in IoT – Sensors, Actuators, MEMS and Smart Objects. WSN, Communications Criteria - Range, Frequency Bands, Power Consumption, Topology, Constrained Devices. Standard Alliances (LTE Cat0, Cat-M).  <b>RBT Levels:</b> L2,L3</p>			
<b>Module-4</b>			
<p><b>Engineering IoT Networks-2:</b> IP as IoT Network Layer – Key advantages of IP. Application Protocols for IoT – Transport Layer, IoT Application Layer Protocols (CoAP, MQTT). Data and Analytics for IoT – Structured and Unstructured data, Data in motion versus data at rest, IoT Data Analytics Overview and Challenges.  <b>RBT Levels:</b> L2,L3</p>			
<b>Module-5</b>			
<p><b>IoT Use Cases:</b>  IoT in Industry - IoT Strategy for Connected manufacturing, Architecture for Connected Factory.  Smart and Connected cities – Smart city network Architecture, Street layer, city layer, Data center layer, services layer. Smart street lighting.  <b>RBT Levels:</b> L3,L4</p>			



### Course Outcome (Course Skill Set)

At the end of the course, the student will be able to :

**CO 1:** Understand the basic concepts IoT Architecture and devices employed.

**CO 2:** Analyze the sensor data generated and map it to IoT protocol stack for transport.

**CO 3:** Apply communications knowledge to facilitate transport of IoT data over various available communications media.

**CO 4:** Design a use case for a typical application in real life ranging from sensing devices to analyzing the data available on a server to perform tasks on the device.

**CO 5:** Apply knowledge of Information technology to design the IoT applications.

### Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

### Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

**Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

### Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**).

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

### Suggested Learning Resources:

#### Text Books:

1. David Hanes, Gonzalo Salgueiro, Patrick Grossetete, Robert Barton, Jerome Henry, "Cisco, IOT Fundamentals – Networking Technologies, Protocols, Use Cases for IOT", Pearson Education; First edition 2017, ISBN: 978-9386873743.
2. Arshdeep Bahga and Vijay Madiseti, "Internet of Things – A Hands on Approach", Orient Blackswan Private Limited - New Delhi; First edition.

### Web links and Video Lectures (e-Resources):

- <https://nptel.ac.in/>

**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

- Quiz
- Seminar

<b>COMPUTER NETWORKS</b>		<b>Semester</b>	<b>VI</b>
<b>Course Code</b>	BUE601	<b>CIE Marks</b>	50
<b>Teaching Hours/Week (L:T:P: S)</b>	3:0:2:0	<b>SEE Marks</b>	50
<b>Total Hours of Pedagogy</b>	30 hours Theory + 20 Lab slots	<b>Total Marks</b>	100
<b>Credits</b>	04	<b>Exam Hours</b>	3 Hours
<b>Examination nature (SEE)</b>	Theory		
<b>Course objectives:</b> <ul style="list-style-type: none"> <li>• Fundamentals of data communication networks.</li> <li>• Software and hardware interfaces</li> <li>• Application of various physical components and protocols</li> <li>• Communication challenges and remedies in the networks.</li> </ul>			
<b>Teaching-Learning Process (General Instructions)</b> These are sample Strategies; that teachers can use to accelerate the attainment of the various course outcomes. <ol style="list-style-type: none"> <li>1. Lecturer method (L) need not to be only traditional lecture method , but alternative effective teaching methods could be adopted to attain the outcomes.</li> <li>2. Use of Video/Animation to explain functioning of various concepts.</li> <li>3. Encourage collaborative (Group Learning) Learning in the class.</li> <li>4. Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking.</li> <li>5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyze information rather than simply recall it.</li> <li>6. Introduce Topics in manifold representations.</li> <li>7. Shows the different ways to solve the same problem and encourage the students come up with their own creative ways to solve them.</li> <li>8. Discuss how every concept can be applied to the real world- and when that's possible, it helps improve the students' understanding.</li> </ol>			
<b>MODULE-1</b>			
<b>Introduction to networks:</b> Network hardware, Network software, Reference models, <b>Physical Layer:</b> Guided transmission media, Wireless transmission <p style="text-align: right;"><b>RBT Levels: L1,L2</b></p>			
<b>MODULE-2</b>			
<b>The Data link layer:</b> Design issues of DLL, Error detection and correction, Elementary data link protocols, Sliding window protocols. <p style="text-align: right;"><b>RBT Levels : L2,L3</b></p>			
<b>MODULE-3</b>			
<b>The medium access control sub layer:</b> The channel allocation problem, Multiple access protocols. Network Layer Design Issues, Routing Algorithms, Congestion Control Algorithms, QoS. <p style="text-align: right;"><b>RBT Levels : L2,L3</b></p>			
<b>MODULE-4</b>			
<b>The Transport Layer:</b> The Transport Service, Elements of transport protocols, Congestion control, The internet transport protocols. <p style="text-align: right;"><b>RBT Levels : L2,L3</b></p>			
<b>MODULE-5</b>			
<b>Application Layer:</b> Principles of Network Applications, The Web and HTTP, Electronic Mail in the Internet, DNS - The Internet's Directory Service. <p style="text-align: right;"><b>RBT Levels : L3,L4</b></p>			

**PRACTICAL COMPONENT OF IPCC**

Sl. NO.	Experiments
1	Implement Three nodes point-to-point network with duplex links between them for different topologies. Set the queue size, vary the bandwidth, and find the number of packets dropped for various iterations.
2	Implement simple ESS and with transmitting nodes in wire-less LAN by simulation and determine the throughput with respect to transmission of packets.
3	Write a program for error detecting code using CRC-CCITT (16-bits).
4	Implement transmission of ping messages/trace route over a network topology consisting of 6 nodes and find the number of packets dropped due to congestion in the network.
5	Write a program to find the shortest path between vertices using bellman-ford algorithm.
6	Implement an Ethernet LAN using n nodes and set multiple traffic nodes and plot congestion window for different source / destination.
7	Write a program for congestion control using leaky bucket algorithm.

**Course outcomes (Course Skill Set):**

At the end of the course, the student will be able to:

- CO1** Learn the basic needs of communication system.
- CO2** Interpret the communication challenges and its solution.
- CO3** Identify and organize the communication system network components
- CO4** Design communication networks for user requirements.

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

The IPCC means the practical portion integrated with the theory of the course. CIE marks for the theory component are **25 marks** and that for the practical component is **25 marks**.

**CIE for the theory component of the IPCC**

- 25 marks for the theory component are split into **15 marks** for two Internal Assessment Tests (Two Tests, each of 15 Marks with 01-hour duration, are to be conducted) and **10 marks** for other assessment methods mentioned in 22OB4.2. The first test at the end of 40-50% coverage of the syllabus and the second test after covering 85-90% of the syllabus.
- Scaled-down marks of the sum of two tests and other assessment methods will be CIE marks for the theory component of IPCC (that is for **25 marks**).
- The student has to secure 40% of 25 marks to qualify in the CIE of the theory component of IPCC.

**CIE for the practical component of the IPCC**

- **15 marks** for the conduction of the experiment and preparation of laboratory record, and **10 marks** for the test to be conducted after the completion of all the laboratory sessions.
- On completion of every experiment/program in the laboratory, the students shall be evaluated including viva-voce and marks shall be awarded on the same day.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to **15 marks**.
- The laboratory test (**duration 02/03 hours**) after completion of all the experiments shall be conducted for 50 marks and scaled down to **10 marks**.

- Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **25 marks**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the practical component of the IPCC.

### SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored by the student shall be proportionally scaled down to 50 Marks

**The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper may include questions from the practical component.**

- The minimum marks to be secured in CIE to appear for SEE shall be 10 (40% of maximum marks-25) in the theory component and 10 (40% of maximum marks -25) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included. The maximum of 04/05 sub-questions are to be set from the practical component of IPCC, the total marks of all questions should not be more than 20 marks.
- SEE will be conducted for 100 marks and students shall secure 35% of the maximum marks to qualify for the SEE. Marks secured will be scaled down to 50.
- The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

### Suggested Learning Resources:

#### Textbooks:

1. Computer-Networks- Andrew S. Tanenbaum and David J. Wetherall, Pearson Education, 5th Edition. ([www.pearsonhighered.com/tanenbaum](http://www.pearsonhighered.com/tanenbaum))
2. Computer Networking A Top-Down Approach -James F. Kurose and Keith W. Ross Pearson Education 7th Edition.

#### Reference Books:

1. Behrouz A Forouzan, Data and Communications and Networking, Fifth Edition, McGraw Hill, Indian Edition
2. Larry L Peterson and Bruce S Davie, Computer Networks, fifth edition, ELSEVIER

#### Web links and Video Lectures (e-Resources):

- <https://nptel.ac.in/>
- VTU e-Shikshana Program

#### Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Simulation of Personal area network, Home area network, achieve QoS etc.

**Note:** For the Simulation experiments modify the topology and parameters set for the experiment and take multiple rounds of reading and analyze the results available in log files. Plot necessary graphs and conclude using NS2. Installation procedure of the required software must be demonstrated, carried out in groups, and documented in the report. Non simulation programs can be implemented using Java.



<b>VLSI Design</b>		Semester	VI
Course Code	<b>BUE602</b>	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	4:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	04	Exam Hours	3 Hours
Examination type (SEE)	<b>Theory</b>		
<p><b>Course objectives:</b>  <b>This course will enable students to:</b></p> <ul style="list-style-type: none"> <li>• To understand the operation of MOS transistor, Scaling and Small Geometry Effects.</li> <li>• To study the Fabrication process, Layout design and Inverter cross section.</li> <li>• To provide the insights of MOSFET characteristics.</li> <li>• To understand the CMOS Inverter static characteristics.</li> <li>• To learn different techniques for dynamic circuits and low power consumption.</li> </ul>			
<p><b>Teaching-Learning Process (General Instructions)</b>  These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.</p> <ol style="list-style-type: none"> <li>1. Chalk and Talk.</li> <li>2. Power Presentation and Videos.</li> <li>3. Flipped Classes.</li> <li>4. Practice Sessions.</li> </ol>			
<b>Module-1</b>			
<p><b>MOS Transistors, CMOS Logic:</b> The inverter, The nand gate, Combinational Logic, TheNOR gate, Compound gates, Pass transistors and transmission gates, Tristates, Multiplexers, Latches and Flip-Flops.  <b>CMOS Fabrication and Layout:</b> Inverter Cross-section, Fabrication process, Layout design rules, Gate Layout, Stick diagrams.  <b>VLSI Design Flow:</b> Design specification, Design entry, Functional simulation, Planning placement and routing, Timing simulation, Fusing/fabrication in to the chip. Fabrication, packaging, and testing.</p> <p style="text-align: right;"><b>RBT Levels: L2,L3</b></p>			
<b>Module-2</b>			
<p><b>MOS Transistors:</b> The metal oxide semiconductor(MOS)structure, The MOS system under external bias, Structure and operation of MOS transistors(MOSFET),MOSFET current-voltage characteristics, MOSFET Scaling and Small-Geometry Effects (Full Scaling, Constant Voltage Scaling only), MOSFET Capacitances (Only Theory Part)</p> <p style="text-align: right;"><b>RBT Levels:L3, L4</b></p>			
<b>Module-3</b>			
<p><b>MOS Inverter: Static Characteristics:</b> Introduction, Resistive-load inverter, Inverters with n-type MOSFET load, CMOS inverter.</p> <p style="text-align: right;"><b>RBT Levels:L3, L4</b></p>			
<b>Module-4</b>			
<p><b>Dynamic Logic Circuits:</b> Introduction, Basic principles of Pass transistor circuits, Voltage Bootstrapping, Synchronous dynamic circuit techniques, Dynamic CMOS circuit techniques, High Performance Dynamic CMOS Circuits (Domino CMOS Logic only)</p> <p style="text-align: right;"><b>RBT Levels: L3,L4</b></p>			
<b>Module-5</b>			
<p><b>Low-Power CMOS Logic Circuits:</b> Introduction, Overview of power consumption, Low power design through voltage scaling, Estimation and Optimization of Switching Activity, Reduction of Switched Capacitance, Adiabatic Logic Circuits.</p> <p style="text-align: right;"><b>RBT Levels: L3, L4</b></p>			

**Course outcome (Course Skill Set)**

At the end of the course, the student will be able to :

**CO1:**Demonstrate understanding of MOS transistor, CMOS fabrication flow and Layout.

**CO2:** Analyze the Structure, Characteristics and operations of MOSFETs.

**CO3:** Interpret the MOSFET Scaling and Small Geometric effects.

**CO4:** Demonstrate static characteristics of Resistive load Inverter, Pass transistor and CMOS Inverter.

**CO5:** Apply the different dynamic circuit techniques and design low power through voltage scaling CMOS.

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous Internal Evaluation:**

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

**Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester-End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**).

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

**Suggested Learning Resources:****Books**

1. "CMOS VLSI Design- A Circuits and Systems Perspective"- Neil H.E. Weste, David Harris, Ayan Banerjee, 3rd Edition, Pearson Education.
2. "CMOS Digital Integrated Circuits Analysis and Design"-Sung-Mo Kang, Yusuf Leblebici, 3<sup>rd</sup> Edition.

**Web links and Video Lectures (e-Resources):**

- <https://nptel.ac.in/>

**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

- Quiz
- Seminar
- Assignments

<b>INFORMATION THEORY AND CODING</b>		<b>Semester</b>	<b>VI</b>
<b>Course Code</b>	<b>BUE613A</b>	<b>CIE Marks</b>	50
<b>Teaching Hours/Week (L:T:P: S)</b>	3:0:0:0	<b>SEE Marks</b>	50
<b>Total Hours of Pedagogy</b>	40	<b>Total Marks</b>	100
<b>Credits</b>	03	<b>Exam Hours</b>	3 Hours
<b>Examination type (SEE)</b>	<b>Theory</b>		
<p><b>Course objectives:</b></p> <ul style="list-style-type: none"> <li>Understand the concept of Entropy, Rate of information and order of the source with reference to dependent and independent source.</li> <li>Study various source encoding algorithms.</li> <li>Model discrete &amp; continuous communication channels.</li> <li>Study various error control coding algorithms.</li> </ul>			
<p><b>Teaching-Learning Process (General Instructions)</b>  These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.</p> <ol style="list-style-type: none"> <li>Lecturer methods (L) need not to be only traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes.</li> <li>Use of Video/Animation to explain functioning of various concepts.</li> <li>Encourage collaborative (Group Learning) Learning in the class.</li> <li>Ask at least three HOT (Higher Order Thinking) questions in the class, which promotes critical thinking.</li> <li>Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyze information rather than simply recall it.</li> <li>Introduce Topics in manifold representations.</li> <li>Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.</li> </ol>			
<b>Module-1</b>			
<p><b>Information Theory:</b> Introduction, Measure of information, Information content of message, Average Information content of symbols in Long Independent sequences, Average Information content of symbols in Long dependent sequences, Markov Statistical Model of Information Sources, Entropy and Information rate of Markoff Sources.</p> <p style="text-align: right;"><b>RBT Levels: L1,L2,L3</b></p>			
<b>Module-2</b>			
<p><b>Source Coding:</b> Source coding theorem, Prefix Codes, Kraft McMillan Inequality property – KMI Encoding of the Source Output, Shannon's Encoding Algorithm Shannon Fano Encoding Algorithm, Huffman codes, Extended Huffman coding, Arithmetic Coding, Lempel – Ziv Algorithm.</p> <p style="text-align: right;"><b>RBT Levels: L1,L2,L3</b></p>			
<b>Module-3</b>			
<p><b>Information Channels:</b> Communication Channels, Channel Models, Channel Matrix, Joint probability Matrix, Binary Symmetric Channel, System Entropies, Mutual Information, Channel Capacity, Channel Capacity of Binary Symmetric Channel, Binary Erasure Channel, Muroga Theorem, Continuous Channels.</p> <p style="text-align: right;"><b>RBT Levels: L1,L2,L3</b></p>			
<b>Module-4</b>			
<p><b>Error Control Coding:</b> Introduction, Examples of Error control coding, methods of Controlling Errors, Types of Errors, types of Codes, Linear Block Codes: matrix description of Linear Block Codes, Error Detection and Error Correction Capabilities of Linear Block Codes, Single Error Correcting hamming Codes, Table lookup Decoding using Standard Array.</p> <p><b>Binary Cyclic Codes:</b> Algebraic Structure of Cyclic Codes, Encoding using an (n-k) Bit Shift register, Syndrome Calculation, Error Detection and Correction</p> <p style="text-align: right;"><b>RBT Levels: L1,L2,L3</b></p>			
<b>Module-5</b>			
<p><b>Some Important Cyclic Codes:</b> Golay Codes, BCH Codes</p> <p><b>Convolution Codes:</b> Convolution Encoder, Time domain approach, Transform domain approach, Code Tree, Trellis and State Diagram, The Viterbi Algorithm)</p> <p style="text-align: right;"><b>RBT Levels: L1,L2,L3</b></p>			

**Course outcome (Course Skill Set)**

At the end of the course, the student will be able to :

- C01.** Explain concept of Dependent & Independent Source, measure of information Entropy, Rate of Information & Order of a source
- C02.** Represent the information using Shannon Encoding, Shannon Fano, Prefix and Huffman Encoding Algorithms
- C03.** Model the continuous and discrete communication channels using input, output and joint probabilities
- C04.** Determine a codeword comprising of the check bits computed using Linear Block codes, cyclic codes & convolutional codes.
- C05.** Design the encoding and decoding circuits for Linear Block codes, cyclic codes, convolutional codes, BCH and Golay codes.

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous Internal Evaluation:**

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

**Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester-End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course **(duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.

Marks scored shall be proportionally reduced to 50 marks.

**Suggested Learning Resources:****Text Books:**

1. Digital and analog communication systems, K. Sam Shanmugam, John Wiley India Pvt. Ltd, 1996.
2. Digital communication, Simon Haykin, John Wiley India Pvt. Ltd, 2008.
3. Information Theory and Coding, Muralidhar Kulkarni, K.S. Shivaprakasha, Wiley India Pvt. Ltd, 2015, ISBN:978-81-265-5305-1.

**Reference Books:**

1. ITC and Cryptography, Ranjan Bose, TMH, II edition, 2007
2. Principles of digital communication, J. Das, S. K. Mullick, P. K. Chatterjee, Wiley, 1986 - Technology & Engineering
3. Digital Communications – Fundamentals and Applications, Bernard Sklar, Second Edition, Pearson Education, 2016, ISBN: 9780134724058.
4. Information Theory and Coding, K.N.Haribhat, D.Ganesh Rao, Cengage Learning, 2017.

**Web links and Video Lectures (e-Resources):**

- <https://nptel.ac.in/>

**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

- Quizzes
- Assignments
- Seminars

<b>ASIC DESIGN</b>		<b>Semester</b>	<b>VI</b>
<b>Course Code</b>	<b>BUE613B</b>	<b>CIE Marks</b>	50
<b>Teaching Hours/Week (L:T:P: S)</b>	3:0:0:0	<b>SEE Marks</b>	50
<b>Total Hours of Pedagogy</b>	40	<b>Total Marks</b>	100
<b>Credits</b>	03	<b>Exam Hours</b>	3 Hours
<b>Examination type (SEE)</b>	<b>Theory</b>		
<p><b>Course objectives:</b></p> <ul style="list-style-type: none"> <li>Recognize and differentiate between ASIC and PLD types across all modules.</li> <li>Understand the complete ASIC design flow and utilize CAD tools effectively.</li> <li>Explore programming technologies like Antifuse, Static RAM, EPROM, etc., relevant to ASIC and PLD design.</li> <li>Examine various types of PLDs such as ROMs, EPROMs, FPGAs, etc., and their applications as discussed in the modules.</li> <li>Gain insight into Full custom, Semi-custom, and Programmable ASICs, and understand the role of ASIC cell libraries throughout the design process.</li> </ul>			
<p><b>Teaching-Learning Process (General Instructions)</b>  These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.</p> <ol style="list-style-type: none"> <li>Lectures &amp; Workshops</li> <li>Labs &amp; Case Studies</li> <li>Group Discussions &amp; Projects</li> <li>Assessments</li> </ol>			
<b>Module-1</b>			
<p><b>Overview of ASIC and PLD:</b> Types of ASICS Design Flow - CAD tools used in ASIC Design  <b>Programming Technologies:</b> Antifuse-Static RAM - EPROM and EEPROM Technology, Programmable Logic Devices: ROMs and EPROMS - PLA - PAL. Gate Arrays - CPLDs and FPGAs</p> <p style="text-align: right;"><b>RBT Levels: L1, L2</b></p>			
<b>Module-2</b>			
<p><b>Introduction to ASICs:</b> Full custom, Semi-custom and Programmable ASICs, ASIC Design flow, ASIC cell libraries.  <b>CMOS Logic:</b> Data path Logic Cells: Data Path Elements, Data path Operators, I/O cells, Cell Compilers.</p> <p style="text-align: right;"><b>RBT Levels: L1, L2</b></p>			
<b>Module-3</b>			
<p><b>ASIC Library Design: Logical effort:</b> Predicting Delay, Logical area and logical efficiency, Logical paths, Multi stage cells, Optimum delay and number of stages, library cell design.  <b>Programmable ASIC Logic Cells:</b> MUX as Boolean function generators, Acted ACT: ACT 1, ACT 2 and ACT 3 Logic Modules, Xilinx LCA:XC3000 CLB, Programmable ASIC I/O Cells: Xilinx and Altera I/O Block</p> <p style="text-align: right;"><b>RBT Levels: L1, L2,L3</b></p>			
<b>Module-4</b>			
<p><b>Low-level design entry:</b> Schematic entry: Hierarchical design, The cell library, Names, Schematic Icons &amp; Symbols, Nets, Schematic Entry for ASICs, Connections, vectored instances &amp; buses, Edit in place, attributes, Netlist screener.  <b>ASIC Construction:</b> Physical Design, CAD Tools System partitioning, Estimating ASIC size.  <b>Partitioning:</b> Goals and objectives, Constructive Partitioning, Iterative Partitioning Improvement,</p> <p style="text-align: right;"><b>RBT Levels: L1, L2,L3</b></p>			
<b>Module-5</b>			
<p><b>Floor planning and placement:</b> Goals and objectives, Measurement of delay in Floor planning, Floor planning tools, Channel definition, I/O and Power planning and Clock planning.  <b>Placement:</b> Goals and Objectives, Min-cut Placement algorithm, Iterative Placement Improvement, Time driven placement methods, Physical Design Flow.  <b>Routing:</b> Global Routing: Goals and objectives, Global Routing Methods, Global routing between blocks, Back- annotation. Detailed Routing: Goals and objectives, Measurement of Channel Density, Left-Edge Algorithm, Special Routing, Circuit extraction and DRC.</p> <p style="text-align: right;"><b>RBT Levels: L1, L2,L3</b></p>			



**Course outcome (Course Skill Set)**

At the end of the course, the student will be able to :

- CO 1:** Understand ASIC and PLD types, design flow, and CAD tools.
- CO 2:** Differentiate programming technologies and their applications.
- CO 3:** Evaluate ASIC types, design flows, and cell libraries.
- CO 4:** Apply logical effort principles for delay prediction and optimization.
- CO 5 :** Implement schematic entry, partitioning, floor planning, and routing techniques in ASIC design

**Assessment Details (both CIE and SEE) :**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%.

The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks).

The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous Internal Evaluation:**

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

**Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester-End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course **(duration 03 hours)**.

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

**Suggested Learning Resources:****Textbook:**

1. Michael John Sebastian Smith, "Application - Specific Integrated Circuits", Addison- Wesley Professional, 2005

**Reference:**

1. "Digital Principles and Logic Design", A. Saha and N. Manna. (ISBN: 978-1-934015-03-2)
2. David A. Hodges, Analysis and Design of Digital Integrated Circuits, 3rd Edition, Tata Mc Graw Hill, 2004.
3. M.J.S. Smith: Application Specific Integrated Circuits, Pearson, 2003.

**Web links and Video Lectures (e-Resources):**

- <https://nptel.ac.in/>

**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

1. Group discussion and CAD tool demos for ASIC and PLD design flow understanding.
2. Interactive case studies and programming exercises for different programming technologies.
3. Role-playing as ASIC designers and comparative analysis of cell libraries.
4. Problem-solving sessions on delay prediction and optimization using logical effort principles.
5. Collaborative design projects and CAD tool workshops for floor planning, placement, and routing techniques.

<b>DATA SCIENCE</b>		Semester	<b>VI</b>
Course Code	<b>BUE613C</b>	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	3 Hours
Examination Type (SEE)	<b>Theory</b>		
<p><b>Course Objectives:</b></p> <ul style="list-style-type: none"> <li>• Demonstrate the proficiency with statistical analysis of data to derive insight from results and interpret the data findings visually.</li> <li>• Utilize the skills in data management by obtaining, cleaning and transforming the data.</li> <li>• Make use of machine learning models to solve the business-related challenges</li> <li>• Experiment with decision trees, neural network layers and data partition.</li> <li>• Demonstrate how social clustering shape individuals and groups in contemporary society.</li> </ul>			
<p><b>Teaching-Learning Process (General Instructions):</b>  These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.</p> <ol style="list-style-type: none"> <li>1. Lecturer methods (L) need not to be only traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes.</li> <li>2. Use of Video/Animation to explain functioning of various concepts.</li> <li>3. Encourage collaborative (Group Learning) Learning in the class.</li> <li>4. Ask at least three HOT (Higher Order Thinking) questions in the class, which promotes critical thinking.</li> <li>5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyze information rather than simply recall it.</li> <li>6. Introduce Topics in manifold representations.</li> <li>7. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.</li> </ol>			
<b>Module-1</b>			
<p><b>Introduction:</b> Visualizing Data, matplotlib, Bar Charts, Line Charts, Scatter plots, Linear Algebra, Vectors, Matrices, Statistics, Describing a Single Set of Data, Correlation, Simpson's Paradox, Some Other Correlational Caveats, Correlation and Causation, Probability, Dependence and Independence, Conditional Probability, Bayes's Theorem, Random Variables, Continuous Distributions, The Normal Distribution, The Central Limit Theorem.</p> <p style="text-align: right;"><b>RBT Levels: L1, L2</b></p>			
<b>Module-2</b>			
<p><b>Hypothesis and Inference:</b> Statistical Hypothesis Testing, Example: Flipping a Coin, p-Values, Confidence Intervals, p-Hacking, Example: Running an A/B Test, Bayesian Inference, Gradient Descent, The Idea Behind Gradient Descent Estimating the Gradient, Using the Gradient, Choosing the Right Step Size, Using Gradient Descent to Fit Models, Minibatch and Stochastic Gradient Descent, Getting Data, stdin and stdout, Reading Files, Scraping the Web, Using APIs, Example: Using the Twitter APIs, Working with Data, Exploring Data, Using NamedTuples, Data classes, Cleaning and Munging, Manipulating Data, Rescaling, An Aside: tqdm, Dimensionality Reduction.</p> <p style="text-align: right;"><b>RBT Levels: L1, L2</b></p>			
<b>Module-3</b>			
<p><b>Machine Learning:</b> What is Machine Learning?, Overfitting and Underfitting, Correctness, The Bias-Variance Tradeoff, Feature Extraction and Selection, k-Nearest Neighbors, Example: The Iris Dataset, The Curse of Dimensionality, Naive Bayes, A Really Dumb Spam Filter, A More Sophisticated Spam Filter, Implementation, Testing Model, Simple Linear Regression, Using Gradient Descent, Maximum Likelihood Estimation, Multiple Regression, Further Assumptions of the Least Squares Model, Fitting the Model, Interpreting the Model, Goodness of Fit, Digression: The Bootstrap, Standard Errors of Regression Coefficients, Regularization, Logistic Regression, The Problem, The Logistic Function, Applying the Model, Goodness of Fit, Support Vector Machines.</p> <p style="text-align: right;"><b>RBT Levels: L1, L2, L3</b></p>			

#### Module-4

**Decision Trees:** What Is a Decision Tree?, Entropy, The Entropy of a Partition, Creating a Decision Tree, Putting It All Together, Random Forests, Neural Networks, Perceptrons, Feed-Forward Neural Networks, Backpropagation, Example: Fizz Buzz, Deep Learning, The Tensor, The Layer Abstraction, The Linear Layer, Neural Networks as a Sequence of Layers, Loss and Optimization, Example: XOR Revisited, Other Activation Functions, Example: Fizz Buzz Revisited, Softmaxes and Cross-Entropy, Dropout, Example: MNIST, Saving and Loading Models, Clustering, The Idea, The Model, Example: Meetups, Choosing k, Example: Clustering Colors, Bottom-Up Hierarchical Clustering.

**RBT Levels:** L1, L2, L3

#### Module-5

**Natural Language Processing:** Word Clouds, n-Gram Language Models, Grammars, An Aside: Gibbs Sampling, Topic Modeling, Word Vectors, Recurrent Neural Networks, Example: Using a Character-Level RNN, Network Analysis, Betweenness Centrality, Eigenvector Centrality, Directed Graphs and Page Rank, Recommender Systems, Manual Curation, Recommending What's Popular, User-Based Collaborative Filtering, Item Based Collaborative Filtering, Matrix Factorization.

**RBT Levels:** L1, L2

#### Course Outcome (Course Skill Set):

At the end of the course, the student will be able to :

**CO 1:** Identify and demonstrate data using visualization tools.

**CO 2:** Make use of Statistical hypothesis tests to choose the properties of data, curate and manipulate data.

**CO 3:** Utilize the skills of machine learning algorithms and techniques and develop models.

**CO 4:** Demonstrate the construction of decision tree and data partition using clustering.

**CO 5:** Experiment with social network analysis and make use of natural language processing skills to develop data driven applications.

#### Assessment Details (both CIE and SEE):

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

#### Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 220B2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

**Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

#### Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**).

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

3. The students have to answer 5 full questions, selecting one full question from each module.

Marks scored shall be proportionally reduced to 50 marks.

**Suggested Learning Resources:**

**Text Books:**

1. Joel Grus, "Data Science from Scratch", 2nd Edition, O'Reilly Publications/Shroff Publishers and Distributors Pvt. Ltd., 2019. ISBN-13: 978-9352138326.

**Reference Books:**

1. Emily Robinson and Jacqueline Nolis, "Build a Career in Data Science", 1st Edition, Manning Publications, 2020. ISBN: 978-1617296246.
2. Aurelien Geron, "Hands-On Machine Learning with Scikit-Learn, Keras, and TensorFlow: Concepts, Tools, and Techniques to Build Intelligent Systems", 2nd Edition, O'Reilly Publications/Shroff Publishers and Distributors Pvt. Ltd., 2019. ISBN-13: 978-1492032649.
3. Francois Chollet, "Deep Learning with Python", 1st Edition, Manning Publications, 2017. ISBN13: 978-1617294433.
4. Jeremy Howard and Sylvain Gugger, "Deep Learning for Coders with fastai and PyTorch", 1st Edition, O'Reilly Publications/Shroff Publishers and Distributors Pvt. Ltd., 2020. ISBN-13: 978-1492045526.
5. Sebastian Raschka and Vahid Mirjalili, "Python Machine Learning: Machine Learning and Deep Learning with Python, scikit-learn, and TensorFlow 2", 3rd Edition, Packt Publishing Limited, 2019. ISBN-13: 978-1789955750.

**Web links and Video Lectures (e-Resources):**

- Using Python : <https://www.python.org>
- R Programming : <https://www.r-project.org/27092022>
- Python for Natural Language Processing : <https://www.nltk.org/book/>
- Data set: <https://archive.ics.uci.edu/ml/datasets.html>
- Data set : [www.kaggle.com/ruiromanini/mtcars](http://www.kaggle.com/ruiromanini/mtcars)
- <https://nptel.ac.in/courses/106/106/106106179/>
- <https://nptel.ac.in/courses/106/106/106106212/>
- <http://nlp-iiith.vlabs.ac.in/List%20of%20experiments.html>
- [https://onlinecourses.nptel.ac.in/noc21\\_cs69/preview](https://onlinecourses.nptel.ac.in/noc21_cs69/preview)
- <https://www.youtube.com/playlist?list=PLw5h0Dij-9PCn4shW4X43FSjEqdBwc1Cn>

**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

- Real world problem solving - Applying the machine learning techniques and developing models
- Quizzes
- Assignments
- Seminars

<b>CRYPTOGRAPHY AND NETWORK SECURITY</b>		Semester	VI
Course Code	<b>BUE613D</b>	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	3 Hours
Examination type (SEE)	<b>Theory</b>		
<b>Course objectives:</b>			
<ul style="list-style-type: none"> <li>To enhance students with a basic foundation of Cryptography by delivering the basics of symmetric key and public key cryptography, Ensuring Message Integrity and Authentication.</li> <li>To equip students with a basic foundation of Network Security by delivering the basics of Transport Level Security, wireless network security and e-mail, Internet Protocol security</li> </ul>			
<b>Teaching-Learning Process (General Instructions)</b>			
<ul style="list-style-type: none"> <li>Chalk and Talk Method</li> <li>Power-point Presentation</li> <li>Videos</li> <li>Flipped class Technique</li> </ul>			
<b>Module-1</b>			
<b>Computer and Network Security Concepts:</b> Computer Security Concepts, Security attacks, A Model for Network Security			
<b>Introduction to Number Theory:</b> The Euclidean Algorithm, Modular Arithmetic.			
<b>Classical Encryption Techniques:</b> Symmetric Cipher Model Cryptography, Substitution Techniques, <b>RBT Levels: L1, L2, L3</b>			
<b>Module-2</b>			
<b>Block Ciphers and the Data Encryption Standard:</b> Traditional Block Cipher Structure, The Data Encryption Standard.			
<b>Advanced Encryption Standard:</b> AES Structure, AES Transformation Functions.			
<b>Public-Key Cryptography and RSA:</b> Principles of Public-Key Cryptosystems, The RSA Algorithm			
<b>Other Public-Key Cryptosystem:</b> Diffie-Hellman key Exchange <b>RBT Levels: L1, L2, L3</b>			
<b>Module-3</b>			
<b>Message Authentication Codes:</b> Message Authentication Requirements, Message Authentication Function			
<b>Cryptographic Hash Functions:</b> Applications of Cryptographic Hash Functions, Secure Hash Algorithm(SHA)			
<b>Digital Signatures:</b> Digital Signatures <b>RBT Levels: L1, L2, L3</b>			
<b>Module-4</b>			
<b>Transport-Level Security:</b> Web Security Considerations, Secure, Transport Layer Security, HTTPS, Secure Shell (SSH)			
<b>Wireless Network Security:</b> Wireless Security, Mobile device Security, IEEE 802.11 Wireless LAN Security <b>RBT Levels: L1, L2, L3</b>			
<b>Module-5</b>			
<b>Electronic Mail Security:</b> Internet Mail Architecture, Email Threats and Comprehensive Email Security, S/MIME, Pretty Good Privacy			
<b>IP:</b> IP Security Overview, IP Security Policy, Encapsulating Security Payload, Internet key Exchange <b>RBT Levels: L1, L2, L3</b>			

**Course outcome (Course Skill Set)**

At the end of the course, the student will be able to:

**CO1:** Identify basic security attacks and explain traditional cryptographic algorithms of encryption and decryption process.

**CO2:** Use symmetric and asymmetric key algorithms for cryptography.

**CO3:** explain the need for message authentication, applications of cryptographic hash functions and explain the need of digital signatures.

**CO4:** Analyze the vulnerabilities in any computing system and hence be able to design a security solution.

**CO5:** Explain Security concerns in electronic-mail and Internet Protocol security

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous Internal Evaluation:**

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

**Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester-End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**).

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.

Marks scored shall be proportionally reduced to 50 marks.

**Suggested Learning Resources:****Textbook:**

1. Cryptography and Network Security: Principles and Practice 7th Global Edition, Pearson Education Limited.



**Reference Book:**

2. Cryptography and Network Security – by Atul Kahate – TMH.
3. Behrouz A. Forouzan, Debdeep Mukhopadhyay, “Cryptography and Network Security”, Second edition, McGraw Hill Education

**Web links and Video Lectures (e-Resources):**

- <https://nptel.ac.in/>

**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

- Quiz
- Seminar
- Assignment

<b>FUNDAMENTALS OF EMBEDDED SYSTEMS</b>		<b>Semester</b>	<b>VI</b>
<b>Course Code</b>	BUE654A	<b>CIE Marks</b>	50
<b>Teaching Hours/Week (L: T:P: S)</b>	3:0:0:0	<b>SEE Marks</b>	50
<b>Total Hours of Pedagogy</b>	40	<b>Total Marks</b>	100
<b>Credits</b>	03	<b>Exam Hours</b>	03
<b>Examination type (SEE)</b>	Theory		
<p><b>Course objectives:</b></p> <ul style="list-style-type: none"> <li>• Understand the basics of computer architecture and memory elements.</li> <li>• Introduce the general characteristics of embedded systems.</li> <li>• Bring the concepts related to microcontroller unit</li> <li>• Bring the interfacing concepts related to embedded systems .</li> </ul>			
<p><b>Teaching-Learning Process (General Instructions)</b>  These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.</p> <ol style="list-style-type: none"> <li>1. Lecturer methods (L) need not to be only a traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes.</li> <li>2. Use of Video/Animation to explain functioning of various concepts.</li> <li>3. Encourage collaborative (Group Learning) Learning in the class.</li> <li>4. Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking.</li> <li>5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyze information rather than simply recall it.</li> </ol>			
<b>Module-1</b>			
<p><b>Basics of computer architecture and the binary number system</b> Basics of computer architecture, computer languages, RISC and CISC architectures, number systems, number format conversions, computer arithmetic, units of memory capacity  <b>RBT Levels: L1, L2,L3</b></p>			
<b>Module-2</b>			
<p><b>Introduction to embedded systems</b> Application domain of embedded systems, desirable features and general characteristics of embedded systems, model of an embedded system, microprocessor Vs microcontroller, example of a simple embedded system, figure of merit for an embedded system, classification of MCUs: 4/8/16/32 bits, history of embedded systems, current trends  <b>RBT Levels: L1, L2,L3</b></p>			
<b>Module-3</b>			
<p><b>Embedded systems</b>-The hardware point of view Microcontroller unit(MCU), a popular 8-bit MCU, memory for embedded systems, low power design, pull up and pull down resistors  <b>RBT Levels: L1, L2,L3</b></p>			
<b>Module-4</b>			
<p><b>Sensors, ADCs and Actuators</b> <b>Sensors:</b> Temperature Sensor, Light Sensor, Proximity/range Sensor;  <b>Analog to digital converters:</b> ADC Interfacing; <b>Actuators</b> Displays, Motors, Opto couplers/Opto isolators, relays.  <b>RBT Levels: L1, L2,L3</b></p>			
<b>Module-5</b>			
<p><b>Examples of embedded systems</b> Mobile phone, automotive electronics, radio frequency identification (RFID), wireless sensor networks(WISENET), robotics, biomedical applications, brain machine interface.  <b>RBT Levels: L1, L2,L3</b></p>			

**Course outcome (Course Skill Set)**

At the end of the course, the student will be able to :

- C01.** Learn about the general principles of computer architecture
- C02.** Learn about the working of a simple embedded system and its application.
- C03.** Learn the hardware aspects of embedded systems
- C04.** Understand the sensors, ADCs and actuators used in embedded systems.
- C05.** Understand the real world examples of embedded systems

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous Internal Evaluation:**

- For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25 marks.
- The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered
- Any two assignment methods mentioned in the 220B2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.
- For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.

**Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester-End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**).

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

**Suggested Learning Resources:****Textbooks:**

1. Lyla B Das, Embedded systems: An Integrated Approach, 1st Ed., Pearson, 2013

**Reference Books:**

1. Shibu, K.V., Introduction to Embedded Systems, 1st Ed., TMH, 2009
2. Kanta Rao B, Embedded Systems, 1st Ed., PHI
3. Frank Vahid & Tony Givargis, Embedded System Design, 2nd Edition, John Wiley,

**Web links and Video Lectures (e-Resources):**

- <https://nptel.ac.in/>

**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

- Quizzes
- Assignments
- Seminar

<b>Introduction to VLSI Circuits and Systems</b>		<b>Semester</b>	<b>VI</b>
<b>Course Code</b>	BUE654B	<b>CIE Marks</b>	50
<b>Teaching Hours/Week (L:T:P: S)</b>	3:0:0:0	<b>SEE Marks</b>	50
<b>Total Hours of Pedagogy</b>	40	<b>Total Marks</b>	100
<b>Credits</b>	03	<b>Exam Hours</b>	3 Hours
<b>Examination type (SEE)</b>	<b>Theory</b>		
<p><b>Course objectives:</b></p> <ul style="list-style-type: none"> <li>To learn Basic Concepts of VLSI.</li> <li>To understand Basic Logic gates in CMOS.</li> <li>To learn Physical Structure of CMOS Integrated Circuits.</li> <li>To understand Design Rules of CMOS Integrated Circuits.</li> <li>To learn Different types of Memories and Programmable Logic.</li> </ul>			
<p><b>Teaching-Learning Process (General Instructions)</b>  These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.</p> <ol style="list-style-type: none"> <li>Chalk and Talk.</li> <li>Power Presentation and Videos.</li> <li>Flipped Classes.</li> <li>Practical Sessions.</li> </ol>			
<b>Module-1</b>			
<p><b>An Overview of VLSI :</b> Complexity and Design, Basic Concept  <b>Logic Design with MOSFETs:</b> Ideal Switches and Boolean Operations, MOSFETs as Switches, Basic Logic Gates in CMOS. <span style="float: right;"><b>RBT Levels: L2</b></span></p>			
<b>Module-2</b>			
<p><b>Logic Design with MOSFETs:</b> Complex Logic Gates in CMOS, Transmission Gate Circuits, <b>Physical Structure of CMOS Integrated Circuits:</b> Integrated Circuit Layers, MOSFETs: nFETs and pFETs, Current Flow in a FET, Driving the Gate Capacitance <span style="float: right;"><b>RBT Levels: L1,L2</b></span></p>			
<b>Module-3</b>			
<p><b>Physical Structure of CMOS Integrated Circuits:</b> CMOS Layers, Designing FET Arrays.  <b>Electrical Characteristics of MOSFETs:</b> MOS Physics, nFET Current-Voltage Equations. <span style="float: right;"><b>RBT Levels:,L3</b></span></p>			
<b>Module-4</b>			
<p><b>Electrical Characteristics of MOSFETs:</b> The FET RC Mode, pFET Characteristics, Modelling of Small MOSFETs.  <b>Electronic Analysis of CMOS Logic Gates:</b> DC Characteristics of the CMOS Inverter, Inverter switching Characteristics <span style="float: right;"><b>RBT Levels: L3,L4</b></span></p>			
<b>Module-5</b>			
<p><b>Electronic Analysis of CMOS Logic Gates:</b> Power Dissipation, DC Characteristics: NAND and NOR Gates,NAND and NOR Transient Response, Analysis of Complex Logic Gates, Gate Design for Transient Performance, Transmission Gates and Pass Transistors. <span style="float: right;"><b>RBT Levels: L4</b></span></p>			

**Course outcome (Course Skill Set)**

At the end of the course, the student will be able to :

**CO1.**Demonstrate understanding of Logic design with MOSFET.

**CO2.**Analyze various Integrated Circuit Layers.

**CO3.**Interpret the Designing of FET Arrays and Basic gates design.

**CO4.** Interpret the CMOS Process Flow and Design Rules.

**CO5.**Demonstrate knowledge of Memories and Programmable Logic Array.

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous Internal Evaluation:**

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

**Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester-End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**).

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

**Suggested Learning Resources:****Books**

1. John P. Uyemura " Introduction to VLSI Circuits and Systems"

**Reference Books:**

1. "CMOS VLSI Design- A Circuits and Systems Perspective"- Neil H.E. Weste, David Harris, Ayan Banerjee, 3rd Edition, Pearson Education.

**Web links and Video Lectures (e-Resources):**

- [http://vlsipd1.blogspot.com/?trk=article-ssr-frontend-pulse\\_little-text-block](http://vlsipd1.blogspot.com/?trk=article-ssr-frontend-pulse_little-text-block)
- [https://vlsipd.blogspot.com/?trk=article-ssr-frontend-pulse\\_little-text-block](https://vlsipd.blogspot.com/?trk=article-ssr-frontend-pulse_little-text-block)
- [https://www.youtube.com/redirect?event=video\\_description&redir\\_token=QUFFLUhqa202NTRGQ1FnVXM0SXg0UGxxV1ZQV1U1TVB5UXxBQ3Jtc0trUE5RM1FvWEINOHdaY1NtMWtkek8wWGdGMV80aEFjRHRaWko4X3pnNTcxX0FjRXNfUnY3eE9GUG5FMlp0NDluajhOVkV2V2V0SU0wWjA3UXFEOUFBR1BNM2tnYXlWZHlCTi1leVBxMUhPQUlzWC1UUUQ&q=http%3A%2F%2FnpTEL.iitm.ac.in%2F&v=Abld-fSxjNM](https://www.youtube.com/redirect?event=video_description&redir_token=QUFFLUhqa202NTRGQ1FnVXM0SXg0UGxxV1ZQV1U1TVB5UXxBQ3Jtc0trUE5RM1FvWEINOHdaY1NtMWtkek8wWGdGMV80aEFjRHRaWko4X3pnNTcxX0FjRXNfUnY3eE9GUG5FMlp0NDluajhOVkV2V2V0SU0wWjA3UXFEOUFBR1BNM2tnYXlWZHlCTi1leVBxMUhPQUlzWC1UUUQ&q=http%3A%2F%2FnpTEL.iitm.ac.in%2F&v=Abld-fSxjNM)

**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

- Quizzes
- Assignments
- Seminars

<b>MICROPROCESSORS AND MICROCONTROLLERS</b>		Semester	VI
Course Code	BUE654C	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03
Examination type (SEE)	Theory		
<p><b>Course objectives:</b></p> <ol style="list-style-type: none"> <li>1. To learn the design aspects of I/O and Memory Interfacing circuits.</li> <li>2. To Study about communication and bus interfacing.</li> <li>3. To Study the Architecture of 8051 microcontroller.</li> <li>4. To get exposed to RISC processors and design ARM microcontroller-based systems</li> </ol>			
<p><b>Teaching-Learning Process (General Instructions)</b></p> <p>These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.</p> <ol style="list-style-type: none"> <li>1. Lecturer methods (L) need not to be only a traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes.</li> <li>2. Use of Video/Animation to explain functioning of various concepts.</li> <li>3. Encourage collaborative (Group Learning) Learning in the class.</li> <li>4. Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking.</li> <li>5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyze information rather than simply recall it.</li> </ol>			
<b>Module-1</b>			
<p><b>8085 MICROPROCESSOR:</b> Microprocessor architecture and its operation, memory, I/O devices, 8085 microprocessor – Core architecture - Various registers- Bus Timings, Multiplexing and Demultiplexing of Address Bus, Decoding and Execution, Instruction set – Classification, Instruction Format, Addressing Modes, 8085 Interrupt Process, Hardware and Software Interrupts.</p> <p style="text-align: right;"><b>RBT Levels: L1,L2</b></p>			
<b>Module-2</b>			
<p><b>8086 MICROPROCESSOR:</b> Core Architecture of the 8086 - Memory Segmentation, Minimum mode Operation and Maximum Mode Operation, Instruction Set of the 8086 processor- Classification - Instruction Format Addressing modes, Simple Assembly Language Programs - Arithmetic operations, Data transfer, String Manipulation, Searching and Sorting .</p> <p style="text-align: right;"><b>RBT Levels: L1,L2</b></p>			
<b>Module-3</b>			
<p><b>I/O INTERFACING:</b> Memory Interfacing and I/O interfacing - Parallel communication interface – Serial Communication interface – D/A and A/D Interface - Timer – Keyboard /display controller – Interrupt controller – DMA controller – Programming and applications Case studies: Traffic Light control, LED display , LCD display, Keyboard display interface and Alarm Controller.</p> <p style="text-align: right;"><b>RBT Levels: L2,L3</b></p>			
<b>Module-4</b>			
<p><b>MICROCONTROLLER:</b> Architecture of 8051 – Special Function Registers (SFRs) - I/O Pins Ports and Circuits – Instruction set- Addressing modes - Assembly language programming - Programming 8051 Timers, Serial Port Programming - Interrupts Programming – LCD &amp; Keyboard Interfacing - ADC, DAC &amp; Sensor Interfacing - External Memory Interface- Stepper Motor and Waveform generation.</p> <p style="text-align: right;"><b>RBT Levels: L1,L2</b></p>			
<b>Module-5</b>			
<p><b>ADVANCED MICROPROCESSOR &amp; MICROCONTROLLER:</b> Advanced coprocessor Architectures- 286, 486, Pentium -RISC Processors- RISC Vs CISC, RISC properties and evolution- ARM Processor – CPU: programming input and output supervisor mode, exceptions and traps – Co-processors, Memory system mechanisms – CPU</p>			



performance- CPU power consumption.

**RBT Levels: L2,L3**

### **Course outcome (Course Skill Set)**

At the end of the course, the student will be able to :

1. Design interfacing peripherals like, I/O, A/D, D/A, timer etc.
2. Develop systems using different microcontrollers.
3. Characterize RISC processors and design ARM microcontroller-based systems

### **Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

#### **Continuous Internal Evaluation:**

- For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25 marks.
- The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.
- For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.

**Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

#### **Semester-End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**).

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

### **Suggested Learning Resources:**

#### **Books**

##### **1. Textbooks:**

1. R. S. Gaonkar, "Microprocessor Architecture: Programming and Applications with the 8085/8080A", Penram International Publishing, Third Edition, 1996.
2. D A Patterson and J H Hennessy, "Computer Organization and Design The hardware and software interface" Morgan Kaufman Publishers, Fourth Edition, 2011.
3. Douglas Hall, "The Microprocessors and its Interfacing", Tata McGraw Hill, Third Edition, 2012.
4. Kenneth J. Ayala, "The 8051 Microcontroller: Architecture Programming & Applications", Penram International Publishing, Second Edition, 1996.
5. Yu-Cheng Liu, Glenn A. Gibson, "Microcomputer Systems: The 8086 / 8088 Family - Architecture, Programming and Design", Second Edition, Prentice Hall of India, 2011.
6. Mohamed Ali Mazidi, Janice Gillispie Mazidi, Rolin McKinlay, "The 8051 Microcontroller and

Embedded Systems: Using Assembly and C”, Second Edition, Pearson education, 2011.
<b>2. Reference Books:</b> <ol style="list-style-type: none"><li>1. Douglas V. Hall, “Microprocessors and Interfacing, Programming and Hardware”, Second Edition, TMH, 2012.</li><li>2. John P. Hayes, “Computer Architecture and Organization”, Third illustrated Edition, Tata McGraw Hill, 2007.</li></ol>
<b>Web links and Video Lectures (e-Resources):</b>
<ul style="list-style-type: none"><li>• <a href="https://nptel.ac.in/">https://nptel.ac.in/</a></li></ul>
<b>Activity Based Learning (Suggested Activities in Class)/ Practical Based learning</b> <ul style="list-style-type: none"><li>• Quizzes</li><li>• Seminar</li></ul>

<b>ELECTRONIC INSTRUMENTATION</b>		<b>Semester</b>	<b>VI</b>
<b>Course Code</b>	<b>BUE654D</b>	<b>CIE Marks</b>	50
<b>Teaching Hours/Week (L:T:P: S)</b>	3:0:0:0	<b>SEE Marks</b>	50
<b>Total Hours of Pedagogy</b>	40	<b>Total Marks</b>	100
<b>Credits</b>	03	<b>Exam Hours</b>	3 Hours
<b>Examination type (SEE)</b>	<b>Theory</b>		
<p><b>Course objectives:</b></p> <ul style="list-style-type: none"> <li>• Define and describe accuracy and precision, and types of errors.</li> <li>• Describe the operation of Ammeters, Voltmeters and Multi-meters and develop circuits for multi range Ammeters and Voltmeters.</li> <li>• Describe functional concepts and operation of various Analog and Digital measuring instruments.</li> <li>• Describe basic concepts and operation of Digital Voltmeters.</li> <li>• Describe and discuss the functioning and types of Oscilloscopes, Signal generators, AC and DC bridges.</li> <li>• Recognize and describe the significance and working of different types of transducers.</li> </ul>			
<p><b>Teaching-Learning Process (General Instructions)</b>            These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.</p> <ol style="list-style-type: none"> <li>1. Lecturer methods (L) need not to be only a traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes.</li> <li>2. Use of Video/Animation to explain functioning of various concepts.</li> <li>3. Encourage collaborative (Group Learning) Learning in the class.</li> <li>4. Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking.</li> <li>5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyze information rather than simply recall it.</li> </ol>			
<b>Module-1</b>			
<p><b>Measurement and Error:</b> Definitions, Accuracy, Precision, Resolution and Significant Figures, Types of Errors, Measurement error combinations.</p> <p><b>Ammeters:</b> DC Ammeter, Multi range Ammeter, The Ayrton Shunt or Universal Shunt, Requirements of Shunt, Extending of Ammeter Ranges, RF Ammeter (Thermocouple), Limitations of Thermocouple.</p> <p><b>Voltmeters and Multi-meters:</b> Introduction, Basic Meter as a DC Voltmeter, DC Voltmeter, Multi range Voltmeter, Extending Voltmeter Ranges, Loading, AC Voltmeter using Rectifiers. True RMS Voltmeter, Multirange Voltmeter. <b>RBT Levels: L1,L2,L3</b></p>			
<b>Module-2</b>			
<p><b>Digital Voltmeters:</b> Introduction, RAMP technique, Dual Slope Integrating Type DVM, Integrating Type DVM, Most Commonly used principles of A DC, Successive Approximations, Resolution and Sensitivity of Digital Meters, General Specifications of DVM</p> <p><b>Digital Instruments:</b> Introduction, Digital Multimeters, Digital Frequency Meter, Digital Measurement of Time, Universal Counter, Digital Tachometer, Digital pH Meter, Digital Phase Meter, Digital Capacitance Meter. <b>RBT Levels: L1,L2,L3</b></p>			
<b>Module-3</b>			
<p><b>Oscilloscopes:</b> Introduction, Basic principles, CRT features, Block diagram of Oscilloscope, Simple CRO, <b>Measurement</b> of Frequency by Lissajous Method, Digital Storage Oscilloscope.</p> <p><b>Signal Generators:</b> Introduction, Fixed and Variable AF Oscillator, Standard Signal Generator, Laboratory Type Signal Generator, AF sine and Square Wave Generator, Function Generator. <b>RBT Levels: L1,L2</b></p>			
<b>Module-4</b>			
<p><b>Measuring Instruments:</b> Field Strength Meter, Stroboscope, Phase Meter, Q Meter, Megger.</p> <p><b>Bridges:</b> Introduction, Wheatstone's bridge, Kelvin's Bridge; AC bridges, Capacitance Comparison Bridge, Inductance Comparison Bridge, Wien's bridge. <b>RBT Levels: L1,L2,L3</b></p>			
<b>Module-5</b>			

**Transducers:** Introduction, Electrical transducers, Selecting a transducer, Resistive transducer, Resistive position transducer, Strain gauges, Resistance the rmo meter, Thermistor, Inductive transducer, LVDT, Piezo electric transducer, Photo voltaic cell, Semiconductor photo diode and transistor  
**RBT Levels: L1,L2,L3**

### Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

- CO1.** Describe instrument measurement errors and calculate them.
- CO2.** Describe the operation of Ammeters, Voltmeters, Multi-meters & develop circuits for multi range Ammeters and Voltmeters.
- CO3.** Describe functional concepts and operation of Digital voltmeters and instruments to measure voltage, frequency, time period, phase difference of signals, rotation speed, capacitance and pH of solutions.
- CO4.** Describe functional concepts and operation of various Analog measuring instruments to measure field Strength, impedance, stroboscopic speed, in/out of phase, Q of coils, insulation resistance.
- CO5.** Describe and discuss functioning and types of Oscilloscopes, Signal generators and Transducers.

### Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

#### Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 220B2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

**Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

#### Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**).

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.

4. Marks scored shall be proportionally reduced to 50 marks.

**Suggested Learning Resources:**

**Text Books:**

1. H.S. Kalsi, - Electronic Instrumentation ||,McGraw Hill, 3rdEdition, 2012, ISBN:9780070702066.
2. David A. Bell,—Electronic Instrumentation & Measurements||, Oxford University Press PHI 2nd Edition, 2006,ISBN81-203-2360-2

**Reference Books:**

1. A. D. Helfrick and W. D. Cooper — Modern Electronic Instrumentation and Measuring Technique, Pearson, 1<sup>st</sup> Edition, 2015, ISBN:9789332556065.
2. A.K.Sawhney,—Electronics and Electrical Measurement, Dhanpat Rai & Sons, ISBN-81-7700-016-0

**Web links and Video Lectures (e-Resources):**

- <https://nptel.ac.in/>

**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

- Quizzes
- Seminars
- Assignments

VLSI Laboratory		Semester	VI
Course Code	BUEL606	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:0:2:0	SEE Marks	50
Credits	01	Total SEE+CIE	100
Total Hours of Pedagogy	12-14 slots	Exam Hours	2 Hours
Examination type (SEE)	Practical		
<b>Course objectives:</b> <ul style="list-style-type: none"> <li>To verify the LVS, DRC, ERC parameters for designed layouts.</li> <li>Understand the features of CAD tool in VLSI design.</li> <li>To learn the fundamental principles of VLSI circuit design in digital domain.</li> <li>Perform ASIC design flow and understand the process of synthesis, synthesis constraints and evaluating the synthesis reports to obtain optimum gate level net list</li> </ul>			
Sl.NO	<b>Experiments</b>		
<b>PART A : ASIC-Digital Design Flow</b> <i>(Experiments to be conducted using any suitable CAD tool)</i>			
Write the Verilog Code and their Test Bench for the following circuits. Observe the waveform, Synthesize the code, do the initial timing verification with gate level simulation.			
1	4 -Bit Ripple Carry Adder		
2	4-Bit Booth Multiplier		
3	a) LFSR b) Parity generators		
4	Master Slave JK Flip Flop		
5	4-Bit Ring Counter		
6	32-Bit ALU Supporting 4-Logical and 4-Arithmetic operations		
<b>PART B : Analog VLSI Design</b> <i>(Experiments to be conducted using any suitable CAD tool)</i>			
Draw the Schematic and Layout for the circuits mentioned below with the help of Suitable CAD tool and verify the following.			
a. Schematic: i) DC Analysis ii) Transient Analysis iii) Parametric analysis			
b. Layout: i) DRC ii) LVS iii) RC Extraction and Back Annotation.			
7	CMOS Inverter		
8	CMOS two input NAND		
9	a) Common Source Amplifier b) Common Drain Amplifier		
10	Current Mirror Circuit		
<b>Demonstration Experiments (For CIE)</b>			
11	Design a 4 bit R-2R based DAC		

12	<p>Design and characterize 3T DRAM cell and measure the following:</p> <ul style="list-style-type: none"> <li>• Read Time, Write Time, Power</li> <li>• Draw Layout of 3T DRAM, use optimum layout methods. Verify for DRC &amp; LVS, extract parasitic and perform post layout simulations, Record the observations.</li> </ul>
<p><b>Course outcomes (Course Skill Set):</b>  At the end of the course the student will be able to:</p> <p><b>C01.</b> Understand the physical design process of Digital Integrated Circuits.  <b>C02.</b> Implement various combinational and sequential circuits using HDL.  <b>C03.</b> Implement schematic and layout of various digital CMOS logic circuits using EDA tools.  <b>C04.</b> Describe procedure for designing of programmable circuits.</p>	
<p><b>Assessment Details (both CIE and SEE)</b></p> <p>The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.</p> <p><b>Continuous Internal Evaluation (CIE):</b>  CIE marks for the practical course are <b>50 Marks</b>.  The split-up of CIE marks for record/ journal and test are in the ratio <b>60:40</b>.</p> <ul style="list-style-type: none"> <li>• Each experiment is to be evaluated for conduction with an observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments are designed by the faculty who is handling the laboratory session and are made known to students at the beginning of the practical session.</li> <li>• Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.</li> <li>• Total marks scored by the students are scaled down to <b>30 marks</b> (60% of maximum marks).</li> <li>• Weightage to be given for neatness and submission of record/write-up on time.</li> <li>• Department shall conduct a test of 100 marks after the completion of all the experiments listed in the syllabus.</li> <li>• In a test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.</li> </ul>	
<p><b>Semester End Evaluation (SEE):</b></p> <ul style="list-style-type: none"> <li>• SEE marks for the practical course are 50 Marks.</li> <li>• <b>SEE shall be conducted by the two examiners. One from the same institute as an internal examiner and another from a different institute as an external examiner, appointed by the university.</b></li> <li>• The examination schedule and names of examiners are informed to the university before the conduction of the examination. These practical examinations are to be conducted between the schedule mentioned in the academic calendar of the University.</li> <li>• All laboratory experiments are to be included for practical examination.</li> <li>• (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. <b>OR</b> based on the course requirement evaluation rubrics shall be decided jointly by examiners.</li> <li>• Students can pick one question (experiment) from the questions lot prepared by the examiners jointly.</li> <li>• Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.</li> </ul> <p>General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)</p>	



Change of experiment is allowed only once and 15% of Marks allotted to the procedure part are to be made zero.

The minimum duration of SEE is 02 hours

**Suggested Learning Resources:**

<https://nptel.ac.in/>

**Reference book :**

Peter J. Ashenden Digital Design (Verilog): An Embedded Systems Approach Using Verilog 1st Edition, Kindle Edition

LATEX SOFTWARE			Semester	VI
Course Code	BUE657A		CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:0:2:0		SEE Marks	50
Credits	01		Total SEE+CIE	100
Total Hours of Pedagogy	12-14 slots		Exam Hours	2 Hours
Examination type (SEE)	Practical			
<b>Course objectives:</b> <ul style="list-style-type: none"> <li>To introduce the basic syntax and semantics of the LaTeX scripting language</li> <li>To understand the presentation of tables and figures in the document</li> <li>To illustrate the LaTeX syntax to represent the theorems and mathematical equations</li> <li>To make use of the libraries (Tikz, algorithm) to design the diagram and algorithms in the document</li> </ul>				
<b>Sl. NO</b>	<b>Experiments</b>			
1	Develop a LaTeX script to create a simple document that consists of 2 sections [Section1, Section2], and a paragraph with dummy text in each section. And also include header [title of document] and footer [institute name, page number] in the document.			
2	Develop a LaTeX script to create a document that displays the sample Abstract/Summary			
3	Develop a LaTeX script to create a simple title page of the VTU project Report [Use suitable Logos and text formatting]			
4	Develop a LaTeX script to create the Certificate Page of the Report [Use suitable commands to leave the blank spaces for user entry]			
5	Develop a LaTeX script to create a document that contains the following table with proper labels.			
	<b>S.No</b>	<b>USN</b>	<b>Student Name</b>	<b>Marks</b>
				<b>Subject1</b> <b>Subject2</b> <b>Subject3</b>
	1	4XX22XX001	Name 1	89      60      90
	2	4XX22XX002	Name 2	78      45      98
	3	4XX22XX003	Name 3	67      55      59
6	Develop a LaTeX script to include the side-by-side graphics/pictures/figures in the document by using the subgraph concept			
7	Develop a LaTeX script to create a document that consists of the following two mathematical equations $x = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a}$ $= \frac{-2 \pm \sqrt{2^2 - 4*(1)*(-8)}}{2*1}$ $= \frac{-2 \pm \sqrt{4+32}}{2}$ $\varphi_{\sigma}^{\lambda} A_t = \sum_{\pi \in C_t} \text{sgn}(\pi) \varphi_{\sigma}^{\lambda} \varphi_{\pi}^{\lambda}$ $= \sum_{\tau \in C_{\sigma t}} \text{sgn}(\sigma^{-1} \tau \sigma) \varphi_{\sigma}^{\lambda} \varphi_{\sigma^{-1} \tau \sigma}^{\lambda}$ $= A_{\sigma t} \varphi_{\sigma}^{\lambda}$			
8	Develop a LaTeX script to demonstrate the presentation of Numbered theorems, definitions, corollaries, and lemmas in the document			
	<b>Demonstration Experiments ( For CIE )</b>			
9	Develop a LaTeX script to create a document that consists of two paragraphs with a minimum of 10 citations in it and display the reference in the section			

10	Develop a LaTeX script to design a simple tree diagram or hierarchical structure in the document with appropriate labels using the Tikz library
11	Develop a LaTeX script to present an algorithm in the document using algorithm/algorithmic/algorithm2e library
12	Develop a LaTeX script to create a simple report and article by using suitable commands and formats of user choice.

**Course outcomes (Course Skill Set):**

At the end of the course the student will be able to:

- C01.** Apply basic LaTeX command to develop simple document
- C02.** Develop LaTeX script to present the tables and figures in the document
- C03.** Illustrate LaTeX script to present theorems and mathematical equations in the document
- C04.** Develop programs to generate the complete report with citations and a bibliography
- C05.** Illustrate the use of Tikz and algorithm libraries to design graphics& algorithms in the document

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous Internal Evaluation (CIE):**

CIE marks for the practical course are **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment is to be evaluated for conduction with an observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments are designed by the faculty who is handling the laboratory session and are made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled down to **30 marks** (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct a test of 100 marks after the completion of all the experiments listed in the syllabus.
- In a test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- The marks scored shall be scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and marks of a test is the total CIE marks scored by the student.

**Semester End Evaluation (SEE):**

- SEE marks for the practical course are 50 Marks.
- **SEE shall be conducted by the two examiners. One from the same institute as an internal examiner and another from a different institute as an external examiner, appointed by the university.**
- The examination schedule and names of examiners are informed to the university before the conduction of the examination. These practical examinations are to be conducted between the schedule mentioned in the academic calendar of the University.
- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be

strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

- Students can pick one question (experiment) from the questions lot prepared by the examiners jointly.
- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% of Marks allotted to the procedure part are to be made zero.

The minimum duration of SEE is 02 hours

**Suggested Learning Resources:**

**BOOK:**

1. A Short Introduction to LaTeX BY FIRUZA KARMALI (AIBARA), A book for beginners,2019
2. Formatting Information: A Beginner's Introduction to Typesetting with LaTeX, BY PETERFLYNN, Comprehensive TeX Archive Network (2005)

**Web links and Video Lectures (e-Resources):**

- <https://nptel.ac.in/>

**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

- Quizzes
- Seminars
- Assignments

<b>APTITUDE VERBAL NUMERICAL AND LOGICAL REASONING</b>		<b>Semester</b>	<b>VI</b>
<b>Course Code</b>	<b>BUE657B</b>	<b>CIE Marks</b>	50
<b>Teaching Hours/Week (L:T:P: S)</b>	1:0:0:0	<b>SEE Marks</b>	50
<b>Total Hours of Pedagogy</b>	15	<b>Total Marks</b>	100
<b>Credits</b>	01	<b>Exam Hours</b>	1 Hour
<b>Examination type (SEE)</b>	<b>MCQ</b>		
<p><b>Course objectives:</b></p> <ul style="list-style-type: none"> <li>To make the students aware of the importance of Aptitude in the present-day Competitive exams .</li> <li>To train the students develop the required skills to think in new and innovative way.</li> <li>To develop basic Aptitude knowledge to understand advanced concept in higher semester.</li> </ul>			
<p><b>Teaching-Learning Process (General Instructions)</b>  These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.</p> <ol style="list-style-type: none"> <li>Lecturer method (L) needs not to be only traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes.</li> <li>Encourage collaborative (Group Learning) Learning in the class.</li> <li>Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking.</li> <li>Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyse information rather than simply recall it.</li> <li>Introduce Topics in manifold representations.</li> <li>Show the different ways to solve the same problem with different circuits/logic and encourage the students to come up with their own creative ways to solve them.</li> <li>Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.</li> </ol>			
<b>Module-1</b>			
<b>Aptitude Verbal:</b> Reading/Comprehension, Sentence Completion (Vocabulary), Sentence Completion (Subject-Verb Agreement), Sentence Completion (Tenses)			
<b>RBT Levels: L1,L2,L3</b>			
<b>Module-2</b>			
<b>Quantitative Ability (Applied &amp; Engineering Mathematics):</b> Logarithm, Permutation and Combinations, Probability, Simple and Compound Interest, Quick Calculation of Percentages, Conversion of Fraction to Percentage Table, Successive Percentage, Concept of 'By' & 'To', Percentage Change, Percentage Point Change, Product Constancy, Increased Value & Increase in Value, Percentage Changes in Numerator & Denominator, Successive Percentage			
<b>RBT Levels: L1,L2,L3</b>			
<b>Module-3</b>			
<b>Quantitative Ability (Applied &amp; Engineering Mathematics):</b> Time, Speed and Distance Time & Work, Ratio and Proportion Duplicate Ratio, Triplicate Ratio, Direct Proportion, Indirect Proportion, Double rule of three or compound proportion, Ratio in investment or partnership, Area			
<b>RBT Levels: L1,L2,L3</b>			
<b>Module-4</b>			
<b>Data Interpretation:</b> Data Interpretation, Tables, Column Graphs, Bar Graphs, Line Charts, Pie Chart, Venn Diagrams Profit, Loss, Cost Price, Selling Price, Marked Price			
<b>RBT Levels: L1,L2,L3</b>			
<b>Module-5</b>			
<b>Logical Reasoning (Deductive Reasoning):</b> Analogy, Blood Relation Relations defined, Generation Verticals, Family Tree, Single Person Blood Relations, Mixed/Chain Blood Relations, Symbol based Blood Relation, Directional Sense, Number and Letter Series, Coding – Decoding, Calendars			
<b>RBT Levels: L1,L2,L3</b>			

**Course outcome (Course Skill Set)**

At the end of the course the student will be able to:

- CO1.** Understand the basic concepts of quantitative ability.
- CO2.** Understand the basic concepts of logical reasoning Skills.
- CO3.** Acquire satisfactory competency in use of reasoning.
- CO4.** Solve campus placements aptitude papers covering Quantitative & Logical Reasoning Ability.
- CO5.** Compete in various competitive exams like CAT, CMAT, GATE, GRE, GATE, UPSC, GPSC etc.

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous internal Examination (CIE)**

- For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25 marks.
- The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered
- Any two assignment methods mentioned in the 220B2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.
- For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.

**Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester End Examinations (SEE)**

SEE paper shall be set for 50 questions, each of the 01 marks. The pattern of the question paper is MCQ (multiple choice questions). The time allotted for SEE is **01 hour**. The student has to secure a minimum of 35% of the maximum marks meant for SEE.

**Suggested Learning Resources:****Text Books**

1. A Modern Approach To Verbal & Non Verbal Reasoning By R S Agarwal
2. Analytical and Logical reasoning By Sijwali B S
3. Quantitative aptitude for Competitive examination By R S Agarwal
4. Analytical and Logical reasoning for CAT and other management entrance test By Sijwali B S
5. Quantitative Aptitude by Competitive Examinations by Abhijit Guha 4 th edition
6. Dr.Ravi Chopra - "Verbal and Non-Verbal Reasoning", MacMillan India

**Web links and Video Lectures (e-Resources):**

- <https://nptel.ac.in/>

**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

- Quizzes
- Seminars
- Assignments

<b>WEB PROGRAMMING (Practical based)</b>			
Course Code	BUEL657D	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	0:0:2:0	SEE Marks	50
Total Hours of Pedagogy	12T + 12P	Total Marks	100
Credits	01	Exam Hours	02
<p><b>Course Objectives:</b></p> <p>CLO 1. Learn Web tool box and history of web browsers.</p> <p>CLO 2. Learn HTML, XHTML tags with utilizations.</p> <p>CLO 3. Know CSS with dynamic document utilizations.</p> <p>CLO 4. Learn JavaScript with Element access in JavaScript.</p> <p>CLO 5. Logically plan and develop web pages..</p>			
<p><b>Teaching-Learning Process (General Instructions)</b></p> <p>These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.</p> <ol style="list-style-type: none"> <li>1. Lecturer method (L) needs not to be only a traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes.</li> <li>2. Use of Video/Animation to explain functioning of various concepts.</li> <li>3. Encourage collaborative (Group Learning) Learning in the class.</li> <li>4. Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking.</li> <li>5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyze information rather than simply recall it.</li> <li>6. Introduce Topics in manifold representations.</li> <li>7. Show the different ways to solve the same problem with different circuits/logic and encourage the students to come up with their own creative ways to solve them.</li> <li>8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.</li> </ol>			
<b>Module-1</b>			
<p><b>Introduction to WEB Programming:</b> Internet, WWW, Web Browsers, and Web Servers, URLs, MIME, HTTP, Security, The Web Programmers Toolbox.</p>			
<b>Teaching-Learning Process</b>	Chalk and board, Active Learning, practical based learning		
<b>Module-2</b>			
<p><b>HTML and XHTML:</b> Origins of HTML and XHTML, Basic syntax, Standard XHTML document structure, Basic text markup, Images, Hypertext Links, Lists, Tables. Forms, Frames in HTML and XHTML, Syntactic differences between HTML and XHTML.</p>			

<b>Teaching-Learning Process</b>	Chalk and board, Active Learning, Demonstration, presentation, problem solving
<b>Module-3</b>	
<b>CSS:</b> Introduction, Levels of style sheets, Style specification formats, Selector forms, Property value forms, Font properties, List properties, Color, Alignment of text, Background images, tags.	
<b>Teaching-Learning Process</b>	Chalk and board, Demonstration, problem solving
<b>Module-4</b>	
<b>Java Script - I:</b> Object orientation and JavaScript; General syntactic characteristics; Primitives, Operations, and expressions; Screen output and keyboard input.	
<b>Teaching-Learning Process</b>	Chalk and board, Practical based learning, practical's
<b>Module-5</b>	
<b>Java Script - II:</b> Control statements, Object creation and Modification; Arrays; Functions; Constructor; Pattern matching using expressions; Errors, Element access in JavaScript.	
<b>Teaching-Learning Process</b>	Chalk and board, MOOC
<b>Course Outcomes (Course Skill Set):</b> At the end of the course the student will be able to: CO 1. Describe the fundamentals of web and concept of HTML. CO 2. Use the concepts of HTML, XHTML to construct the web pages. CO 3. Interpret CSS for dynamic documents. CO 4. Evaluate different concepts of JavaScript & Construct dynamic documents. CO 5. Design a small project with JavaScript and XHTML.	
<b>Assessment Details (both CIE and SEE)</b> The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE). <b>Continuous Internal Evaluation (CIE):</b> <b>NOTE: List of experiments to be prepared by the faculty based on the syllabus mentioned above</b> CIE marks for the practical course is <b>50 Marks</b> . The split-up of CIE marks for record/ journal and test are in the ratio <b>60:40</b> . <ul style="list-style-type: none"> <li>• Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.</li> <li>• Record should contain all the specified experiments in the syllabus and each</li> </ul>	



experiment write-up will be evaluated for 10 marks.

- Total marks scored by the students are scaled down to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct a test of 100 marks after the completion of all the experiments listed in the syllabus.
- In a test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- The marks scored shall be scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and marks of a test is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

- SEE marks for the practical course is 50 Marks.
- SEE shall be conducted jointly by the two examiners of the same institute, examiners are Appointed by the Head of the Institute.
- The examination schedule and names of examiners are informed to the university before the conduction of the examination. These practical examinations are to be conducted between the schedules mentioned in the academic calendar of the University.
- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. OR based on the course requirement evaluation rubrics shall be decided jointly by examiners.
- Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.
- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.
- General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)
- The duration of SEE is 02 hours

Rubrics suggested in Annexure-II of Regulation book

### **Textbooks**

1. Robert W Sebesta, "Programming the World Wide Web", 6th Edition, Pearson Education, 2008.

### **Reference Books**

1. M.Deitel, P.J.Deitel, A.B.Goldberg, "Internet & World Wide Web How to program", 3rd Edition, Pearson Education / PHI, 2004.

2. Chris Bates, "Web Programming Building Internet Applications", 3rd Edition, Wiley India,

2006.

3. Xue Bai et al, "The Web Warrior Guide to Web Programming", Thomson, 2003.

4. Sklar, "The Web Warrior Guide to Web Design Technologies", 1st Edition, Cengage Learning India

**Weblinks and Video Lectures (e-Resources):**

- <https://nptel.ac.in/>

**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

- Demonstration of simple projects

<b>ADVANCED PYTHON PROGRAMMING</b>		Semester	<b>VI</b>
Course Code	<b>BUEL657C</b>	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	0:0:2:0	SEE Marks	50
Credits	01	Total SEE+CIE	100
		Exam Hours	2 Hours
Examination Type (SEE)	<b>Practical</b>		
<b>Course Objectives:</b>			
<ul style="list-style-type: none"> <li>• Demonstrate the use of IDLE or PyCharm IDE to create Python Applications.</li> <li>• Using Python programming language to develop programs for solving real-world problems</li> <li>• Implementation of Matplotlib, Seaborn, Bokeh and Plotly for drawing different Plots.</li> <li>• Demonstrate working with Numpy, Pandas libraries and creation of GUI.</li> </ul>			
<b>Sl. No.</b>	<b>Experiments</b>		
1	a) Write a Python program to Demonstrate how to Draw a Bar Plot using Matplotlib. b) Write a Python program to Demonstrate how to Draw a Scatter Plot using Matplotlib.		
2	a) Write a Python program to Demonstrate how to Draw a Histogram Plot using Matplotlib. b) Write a Python program to Demonstrate how to Draw a Pie Chart using Matplotlib.		
3	a) Write a Python program to illustrate Linear Plotting using Matplotlib. b) Write a Python program to illustrate liner plotting with line formatting using Matplotlib.		
4	Write a Python program to perform the following basic operations on an image: (i) Crop (ii) Scale (iii) Rotate (iv) Flip.		
5	Write a Python program to perform the following operations on an image: (i) Changing contrast and brightness (ii) Edge detection, blur, sharpening.		
6	Write a Python program to perform basic numerical processing using Numpy.		
7	Write a Python program to create a GUI using Widgets.		
8	Write a Python program to perform the following operations using Pandas: (i) Loading a dataset into a dataframe (ii) Selecting Columns from a dataframe (iii) Selecting Rows from a dataframe (iv) Adding new data in a dataframe (v) Deleting data from a dataframe.		
<b>Demonstration Experiments ( For CIE )</b>			
9	Write a Python program to explain working with bokeh line graph using Annotations and Legends.		
10	Write a Python program to draw 3D Plots using Plotly Libraries.		
11	Write a Python program to perform following operations on images: a) Addition of two images b) Subtraction of two images		
12	Write a Python program to detect different Facial features.		

**Course Outcomes (Course Skill Set):**

At the end of the course the student will be able to:

**CO 1:** Demonstrate the use of IDLE or PyCharm IDE to create Python Applications.

**CO 2:** Use Python programming constructs to develop programs for solving real-world problems.

**CO 3:** Use Matplotlib, Seaborn, Bokeh and Plotly for drawing different Plots for visualization.

**CO 4:** Demonstrate working with Numpy, Pandas libraries and creation of GUI.

**Assessment Details (both CIE and SEE):**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous Internal Evaluation (CIE):**

CIE marks for the practical course are **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment is to be evaluated for conduction with an observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments are designed by the faculty who is handling the laboratory session and are made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled down to **30 marks** (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct a test of 100 marks after the completion of all the experiments listed in the syllabus.
- In a test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- The marks scored shall be scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and marks of a test is the total CIE marks scored by the student.

**Semester End Evaluation (SEE):**

- SEE marks for the practical course are 50 Marks.
- **SEE shall be conducted by the two examiners. One from the same institute as an internal examiner and another from a different institute as an external examiner, appointed by the university.**
- The examination schedule and names of examiners are informed to the university before the conduction of the examination. These practical examinations are to be conducted between the schedule mentioned in the academic calendar of the University.
- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.
- Students can pick one question (experiment) from the questions lot prepared by the examiners jointly.
- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be

scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% of Marks allotted to the procedure part are to be made zero.  
The minimum duration of SEE is 02 hours

**Suggested Learning Resources:**

**Textbooks:**

1. Al Sweigart, "Automate the Boring Stuff with Python", 1<sup>st</sup> Edition, No Starch Press, 2015.
2. Reema Thareja "Python Programming Using Problem Solving Approach" Oxford University Press.

**Web links and Video Lectures (e-Resources):**

- <https://nptel.ac.in/>

**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

- Quizzes
- Seminars
- Assignments