B. E. (EC / TC)
Choice Based Credit System (CBCS) and Outcome Based Education (OBE)
SEMESTER – V

Technological Innovation and Management Entrepreneurship

Course Code	BEC501	**CIE Marks**	**50**
Number of Lecture Hours/Week	**03**	**SEE Marks**	**50**
Total Number of Lecture Hours	**40 (08 Hours / Module)**	**Exam Hours**	**03**

CREDITS-03

Course Learning Objectives: This course will enable students to:

- Understand basic skills of Management
- Understand the need for Entrepreneurs and their skills.
- Identify the Management functions and Social responsibilities.
- Understand economic development, creativity and Innovation.
- Understand the Ideation Process, creation of Business Model, Feasibility Study and sources of funding.

MODULE-1	RBT Level
Management: Nature and Functions of Management – Importance, Definition, Management Functions, Levels of Management, Roles of Manager, Managerial Skills, Management & Administration, Management as a Science, Art & Profession **(Selected topics of Chapter 1, Text1).** **Planning:** Planning**-**Nature, Importance, Types, Steps and Limitations of Planning; Decision Making – Meaning, Types and Steps in Decision Making (**Selected topics from Chapters 4 & 5, Text 1).**	**L1,L2**
MODULE-2	
Organizing and Staffing: Organization-Meaning, Characteristics, Process of Organizing, Principles of Organizing, Span of Management (meaning and importance only), Departmentalization, Committees–Meaning, Types of Committees; Centralization Vs Decentralization of Authority and Responsibility; **Staffing**-Need and Importance**,** Recruitment and Selection Process **(Selected topics from Chapters 7, 8 & 11,Text 1).** **Directing and Controlling:** Meaning and Requirements of Effective Direction, Giving Orders; Motivation-Nature of Motivation, Motivation Theories (Maslow's Need-Hierarchy Theory and Herzberg's Two Factor Theory); Communication – Meaning, Importance and Purposes of Communication; Leadership-Meaning, Characteristics, Behavioural Approach of Leadership; Coordination-Meaning, Types, Techniques of Coordination; Controlling – Meaning, Need for Control System, Benefits of Control, Essentials of Effective Control System, Steps in Control Process (**Selected topics from Chapters 15 to 18 and 9, Text 1).**	**L1,L2**
MODULE-3	
Social Responsibilities of Business: Meaning of Social Responsibility, Social Responsibilities of Business towards Different Groups, Social Audit, Business Ethics and Corporate Governance **(Selected topics from Chapter 3, Text 1).** **Entrepreneurship**: Definition of Entrepreneur, Importance of Entrepreneurship, concepts of Entrepreneurship, Characteristics of successful Entrepreneur, Classification of Entrepreneurs, Myths of Entrepreneurship, Entrepreneurial Development models, Entrepreneurial development cycle, Problems faced by Entrepreneurs and capacity building for Entrepreneurship **(Selected topics from Chapter 2, Text 2).**	**L1,L2**
MODULE-4	

Modern Small Business Enterprises: Role of Small Scale Industries, Impact of Globalization and WTO on SSIs, Concepts and definitions of SSI Enterprises, Government policy and development of the Small Scale sector in India, Growth and Performance of Small Scale Industries in India, Sickness in SSI sector, Problems for Small Scale Industries, Ancillary Industry and Tiny Industry (Definition only) (**Selected topics from Chapter1, Text 2**). **Idea Generation and Feasibility Analysis-** Idea Generation; Creativity and Innovation; Identification of Business Opportunities; Market Entry Strategies; Marketing Feasibility; Financial Feasibilities; Political Feasibilities; Economic Feasibility; Social and Legal Feasibilities; Technical Feasibilities; Managerial Feasibility, Location and Other Utilities Feasibilities.**(Selected topics from Chapter 6(Page No. 111-117) & Chapter 7(Page No. 140-142), Text 2)**	**L1,L2**
MODULE-5	
Business model – Meaning, designing, analyzing and improvising; Business Plan – Meaning, Scope and Need; Financial, Marketing, Human Resource and Production/Service Plan; Business plan Formats; Project report preparation and presentation; Why some Business Plan fails? **(Selected topics from Chapter 8 (Page No 159-164, Text 2)** **Financing and How to start a Business?** Financial opportunity identification; Banking sources; Nonbanking Institutions and Agencies; Venture Capital – Meaning and Role in Entrepreneurship; Government Schemes for funding business; Pre launch, Launch and Post launch requirements; Procedure for getting License and Registration; Challenges and Difficulties in Starting an Enterprise **(Selected topics from Chapter 7(Page No 147-149), Chapter 5 (Page No 93-99) & Chapter 8(Page No. 166-172) Text 2)** **Project Design and Network Analysis:** Introduction, Importance of Network Analysis, Origin of PERT and CPM, Network, Network Techniques, Need for Network Techniques, Steps in PERT, CPM, Advantages, Limitations and Differences**.(Selected topics from Chapters 20, Text 3).**	**L1,L2, L3**

Course Outcomes: After studying this course, students will be able to:

1. Understand the fundamental concepts of Management and Entrepreneurship and opportunities in order to setup a business
2. Describe the functions of Managers, Entrepreneurs and their social responsibilities
3. Understand the components in developing a business plan, along with the integration of CSR-Corporate Social Responsibility.
4. Describe the importance of small scale industries in economic development and institutional support to start a small scale industry and understand the concepts of Creativity and Innovation and Identification of Business Opportunities.
5. Awareness about various sources of funding and institutions supporting entrepreneurs

Text Books:

1. Principles of Management – P.C Tripathi, P.N Reddy, McGraw Hill Education, 6th Edition, 2017. ISBN-13:978-93-5260-535-4.
2. Entrepreneurship Development Small Business Enterprises- Poornima M Charantimath, Pearson Education 2008, ISBN 978-81-7758-260-4.
3. Dynamics of Entrepreneurial Development and Management by Vasant Desai. HPH 2007, ISBN: 978-81-8488-801-2.
4. Robert D. Hisrich, Mathew J. Manimala, Michael P Peters and Dean A. Shepherd, "Entrepreneurship", 8th Edition, Tata Mc-graw Hill Publishing Co.ltd.-new Delhi, 2012.

Reference Book:

1. Essentials of Management: An International, Innovation and Leadership perspective by Harold Koontz, Heinz Weihrich McGraw Hill Education, 10th Edition 2016. ISBN- 978-93-392-2286-4.

	Digital Signal Processing	Semester	5
Course Code	**BVL502**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:2:0	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory + 8-10 Lab slots	Total Marks	100
Credits	04	Exam Hours	3 Hours
Examination nature (SEE)	Theory		

Course objectives:

1. Preparation: To prepare students with fundamental knowledge/ overview in the field of Digital Signal Processing
2. Core Competence: To equip students with a basic foundation of Signal Processing by delivering the basics of Discrete Fourier Transforms, their properties, efficient computations & the design of digital filters.

Teaching-Learning Process (General Instructions)

These are sample Strategies; that teachers can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only traditional lecture method, but different type of teachingmethods may be adopted to develop the outcomes.
2. Show Video/animation films to explain the different concepts of Digital Signal Processing
3. Encourage collaborative (Group) Learning in the class
4. Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recallit.
6. Topics will be introduced in a multiple representation.
7. Show the different ways to solve the same problem and encourage the students to come up withtheir own creative ways to solve them.
8. Discuss how every concept can be applied to the real world - and when that's possible, it helpsimprove the students' understanding.
9. Adopt Flipped class technique by sharing the materials / Sample Videos prior to the class and havediscussions on the that topic in the succeeding classes.
10. Give Programming Assignments.

MODULE-1

Introduction: Signals, Systems and Signal Processing, Classification of Signals, The Concept of Frequency in Continuous Time and Discrete Time Sinusoidal Signals. [Text1: 1.1, 1.2, 1.3: 1.3.1, 1.3.2]

Discrete Time Signals and Systems: Discrete Time Signals, Discrete Time Systems, Analysis of Discrete Time Linear Time Invariant Systems.

[Text 1: 2.1.1, 2.1.2, 2.2.1, 2.2.2, 2.2.3, 2.3.1, 2.3.2, 2.3.3, 2.3.5]

MODULE-2

Z-Transforms: The z-Transform, Properties of the z-Transform (Statements only), The System Function of a Linear Time Invariant system. Text1:3.1, 3.2, 3.3.3.

The Discrete Fourier Transform: Frequency Domain sampling and Reconstruction of Discrete Time Signals, The DFT, The DFT as Linear Transformation. Properties of DFT: Periodicity, Linearity and Symmetry for real valued sequence, Multiplication of two DFTs and Circular Convolution.

[Text1: 7.1.1, 7.1.2, 7.1.3, 7.2: 7.2.1, 7.2.2]

MODULE-3

DFT Properties: Time reversal of a sequence, Circular Time shift of a sequence, Circular frequency shift, Complex conjugate property, Multiplication of two sequences, Perceval's theorem. Linear Filtering Methods based on the DFT. (Text 1: 7.3].

Efficient Computation of the DFT- FFT Algorithms: Direct Computation of the DFT, Radix-2 FFT Algorithms: computation of DFT and IDFT in decimation in time.

[Text1: 8.1: 8.1.1, 8.1.3].

MODULE-4

Design of FIR Filters: Characteristics of practical frequency-selective filters, Symmetric and Antisymmetric FIR filters, Design of Linear-phase FIR (low pass and High pass) filters using windows - Rectangular, Hamming and Blackman windows. Structure for FIR Systems: Direct form and Cascade form. [Text1: 10.1.2, 10.2.1, 10.2.2]
MODULE-5
IIR Filter Design: Infinite Impulse response Filter Format, Bilinear Transformation Design Method, Analog Filters using Low pass prototype transformation, Normalized Butterworth Functions, Bilinear Transformation and Frequency Warping, Bilinear Transformation Design Procedure, Digital Butterworth Filter Design (Lowpass and High pass) using BLT. [Text2: 8.1, 8.2, 8.3 (Butterworth filter design), 8.8.1]

PRACTICAL COMPONENT OF IPCC

List of Programs to be implemented & executed using any programming languages like **Moku:Go/ MATLAB/OCTAVE (but not limited to)**

Sl.NO	Experiments
1	Program to generate the following discrete time signals. a) Unit sample sequence, b)Unit step sequence, c) Exponential sequence, d)Sinusoidal sequence, e) Random sequence
2	Program to perform the following operations on signals. a) Signal addition, b) Signal multiplication, c)Scaling, d) Shifting, e)Folding
3	Program to perform convolution of two given sequences (without using built-in function) and display the signals.
4	Consider a causal system y(n) = 0.9y(n-1)+x(n). a) Determine H(z) and sketch its pole zero plot. b) Plot $\|H(e^{j\omega})\|$ and $\angle H(e^{j\omega})$ c) Determine the impulse response h(n).
5	Computation of N point DFT of a given sequence (without using built-in function) and to plot the magnitude and phase spectrum.
6	Using the DFT and IDFT, compute the following for any two given sequences a)Circular convolution b) Linear convolution
7	Verification of Linearity property, circular time shift property & circular frequency shift property of DFT.
8	Develop decimation in time radix-2 FFT algorithm without using built-in functions.
9	Design and implementation of digital low pass FIR filter using a window to meet the given specifications
10	Design and implementation of digital high pass FIR filter using a window to meet the given specifications
11	Design and implementation of digital IIR Butterworth low pass filter to meet the given specifications.
12	Design and implementation of digital IIR Butterworth high pass filter to meet the given specifications

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

- Analyse the different types of signals and systems used in digital signal processing.
- Compute the response of an LTI system using time and frequency domain techniques.
- Develop algorithms for the efficient computations of DFT and IDFT.
- Design of digital FIR filters for the given specifications using different window methods.
- Design of digital IIR digital filters using bilinear transformation method.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

The IPCC means the practical portion integrated with the theory of the course. CIE marks for the theory component are **25 marks** and that for the practical component is **25 marks**.

CIE for the theory component of the IPCC

- 25 marks for the theory component are split into **15 marks** for two Internal Assessment Tests (Two Tests, each of 15 Marks with 01-hour duration, are to be conducted) and **10 marks** for other assessment methods mentioned in 22OB4.2. The first test at the end of 40-50% coverage of the syllabus and the second test after covering 85-90% of the syllabus.
- Scaled-down marks of the sum of two tests and other assessment methods will be CIE marks for the theory component of IPCC (that is for **25 marks)**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the theory component of IPCC.

CIE for the practical component of the IPCC

- **15 marks** for the conduction of the experiment and preparation of laboratory record, and **10 marks** for the test to be conducted after the completion of all the laboratory sessions.
- On completion of every experiment/program in the laboratory, the students shall be evaluated including viva-voce and marks shall be awarded on the same day.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to **15 marks**.
- The laboratory test **(duration 02/03 hours)** after completion of all the experiments shall be conducted for 50 marks and scaled down to **10 marks.**
- Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **25 marks**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the practical component of the IPCC.

SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored by the student shall be proportionally scaled down to 50 Marks

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper may include questions from the practical component.

- The minimum marks to be secured in CIE to appear for SEE shall be 10 (40% of maximum marks-25) in the theory component and 10 (40% of maximum marks -25) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included**.** The maximum of 04/05 sub-questions are to be set from the practical component of IPCC, the total marks of all questions should not be more than 20 marks.
- SEE will be conducted for 100 marks and students shall secure 35% of the maximum marks to qualify for the SEE. Marks secured will be scaled down to 50.
- The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100)

in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Suggested Learning Resources:

Text Books:

1. Proakis & Manolakis, "Digital Signal Processing - Principles Algorithms & Applications", 4th Edition, Pearson education, New Delhi, 2007. ISBN: 81-317-1000-9.
2. Li Tan, Jean Jiang, "Digital Signal processing - Fundamentals and Applications", Academic Press, 2013, ISBN: 978-0-12-415893.
3. Vinay K. Ingle, John G Proakis , "Digital Signal Processing Using MATLAB, A problem Solving Companion", Cengage Learning, 2018, ISBN: 93-86668-11-4

Reference Books:

1. Simon Haykin and Barry Van Veen, "Signals and Systems", 2nd Edition, 2008, Wiley India. ISBN9971-51- 239-4.
2. Sanjit K Mitra, "Digital Signal Processing, A Computer Based Approach", 4th Edition, McGraw Hill Education, 2017. ISBN:978-1-25-909858
3. Oppenheim & Schaffer, "Discrete Time Signal Processing", PHI, 2003.
4. D Ganesh Rao and Vineeth P Gejji, "Digital Signal Processing" Cengage India Private Limited, 2017, ISBN: 9386858231

Web links and Video Lectures (e-Resources):

1. Digital Signal processing, https://nptel.ac.in/courses/117102060

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Programming Assignments / Mini Projects can be given to improve programming skills

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	Digital VLSI Design	Semester	5
Course Code	**BVL503**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	4:0:0:0	SEE Marks	50
Total Hours of Pedagogy	50 Hours	Total Marks	100
Credits	04	Exam Hours	3 Hours
Examination nature (SEE)	Theory		

Course objectives:

1.This course deals with analysis and design of digital CMOS integrated circuits.

2. The course emphasizes on basic theory of digital circuits, design principles and techniques for digital design blocks implemented in CMOS technology.

3. This course will also cover switching characteristics of digital circuits along with delay and power estimation.

4. Understanding the CMOS sequential circuits and memory design concepts.

Teaching-Learning Process (General Instructions)

These are sample Strategies; that teachers can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
2. Show Video/animation films to explain the different concepts of Digital Signal Processing
3. Encourage collaborative (Group) Learning in the class
4. Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyse information rather than simply recall it.
6. Topics will be introduced in a multiple representation.
7. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.
9. Adopt Flipped class technique by sharing the materials / Sample Videos prior to the class and have discussions on the that topic in the succeeding classes.

MODULE-1

Introduction to CMOS Circuits: Introduction, MOS Transistors, MOS Transistor switches, CMOS Logic, Alternate Circuit representation, CMOS-nMOS comparison.

[Text 1: 1.1,1.2,1.3,1.4,1.5.1.6.]

Teaching-Learning Process: Chalk and talk method, YouTube videos, Power point presentation RBT Level: L1, L2

MODULE-2

MOS Transistor Theory: n-MOS enhancement transistor, p-MOS transistor, Threshold Voltage, Threshold voltage adjustment, Body effect, MOS device design equations, V-I characteristics, CMOS inverter DC characteristics, Influence of βn / βp ratio on transfer characteristics, Noise margin, Alternate CMOS inverters. Transmission gate DC characteristics. Latch-up in CMOS.

[Text 1: 2.1,2.2,2.3,2.4,2.5.2.6.]

Teaching-Learning Process:

Chalk and talk method/Power point presentation RBT Level: L1, L2, L3.

MODULE-3

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Circuit Characterization and Performance Estimation: Introduction, Resistance Estimation, Capacitance Estimation, Switching Characteristics, CMOS gate transistor sizing, Determination of conductor size, Power consumption, Charge sharing, Scaling of MOS transistor sizing, Yield.
[Text 1: 4.1,4.2,4.3,4.4,4.5.4.6.4.7,4.8,4.9,4.10]

Teaching-Learning Process:
Chalk and talk method, YouTube videos, Power point presentation RBT Level: L1, L2, L3

MODULE-4

CMOS Circuit and Logic Design: Introduction, CMOS Logic structures, CMOS Complementary logic, Pseudo n-MOS logic, Dynamic CMOS logic, Clocked CMOS Logic, Cascade Voltage Switch logic, Pass transistor Logic, Electrical and Physical design of Logic gates, The inverter, NAND and NOR gates, Body effect, Physical Layout of Logic gates, Input output Pads.

[Text 1: 5.1,5.2,5.2.1, , 5.2.2, 5.2.3, 5.2.4, 5.2.6, 5.2.8, 5.3,5.3.1,5.3.2, 5.3.4 ,5.3.8,5.5]

Teaching-Learning Process:
Chalk and talk method, YouTube videos, Power point presentation RBT Level: L1, L2, L3.

MODULE-5

Sequential MOS Logic Circuits: Introduction, Behavior of Bistable Elements (Excluding Mathematical analysis) SR Latch Circuit, Clocked Latch and Flip-Flop Circuits, Clocked SR Latch, Clocked JK Latch, CMOS D-Latch. 4-bit x 4-bit NOR and NAND-based ROM array. (Only schematic) Three-Transistor DRAM Cell, One-Transistor DRAM Cell.
[Text2: 8.1, 8.2, 8.3, 8.4,8.5,10.2,10.4]

Teaching-Learning Process:
Chalk and talk method/Power point presentation RBT Level: L1, L2, L3

Text Books:

1. Principals of CMOS VLSI Design A System approach Neil H E Weste and Kamran Eshraghain . Addition Wisley Publishing company.
2. "CMOS Digital Integrated Circuits: Analysis and Design", Sung Mo Kang & Yosuf Leblebici, Third Edition, Tata McGraw-Hill.

Reference Books:

1. "CMOS VLSI Design- A Circuits and Systems Perspective", Neil H E Weste, and David Money Harris 4th Edition, Pearson Education.
2. "Basic VLSI Design", Douglas A Pucknell, Kamran Eshraghian, 3rd Edition, Prentice Hall of India publication, 2005.

Course Outcomes: After completing the course, the students will be able to	
CO1	Apply the fundamentals of semiconductor physics in MOS transistors and analyze the geometrical effects of MOS transistors
CO2	Design and realize combinational, sequential digital circuits and memory cells in CMOS logic.
CO3	Analyze the synchronous timing metrics for sequential designs and structured design basics.
CO4	Understand designing digital blocks with design constraints such as propagation delay and dynamic power dissipation.

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03.10.2022

VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI
B.E: Electronics Engineering (VLSI Design and Technology)
NEP, Outcome Based Education (OBE) and Choice Based Credit System (CBCS)
(Effective from the academic year 2022-2023)

V Semester

NOTE: This Laboratory can be conducted using Industry standard EDA tool like Cadence , Synopsis or any equilent VLSI tool.

03.10.2022

Digital VLSI Laboratory			
Course Code	**BVLL504**	CIE Marks	50
Teaching Hours/Week (L: T: P: S)	0:0:2:0	SEE Marks	50
Credits	1	Exam Hours	3

Course objectives:

This laboratory course enables students to

- Design, model, simulate and verify digital circuits.
- Perform ASIC design flow and understand the process of synthesis, synthesis constraints and evaluating the synthesis reports to obtain optimum gate level netlist.
- Perform RTL-GDSII flow and understand the ASIC Design flow.

Sl.No.	Experiments
1	4-Bit Adder • Write Verilog Code • Verify the Functionality using Test-bench • Synthesize the design by setting proper constraints and obtain the netlist. From the report generated identify Critical path, Maximum delay, Total number of cells, Power requirement and Total area required
2	4-Bit Shift and add Multiplier • Write Verilog Code • Verify the Functionality using Test-bench • Synthesize the design by setting proper constraints and obtain the netlist. From the report generated identify Critical path, Maximum delay, Total number of cells, Power requirement and Total area required
3	32-Bit ALU Supporting 4-Logical and 4-Arithmetic operations, using case and if statement for ALU Behavioral Modeling • Write Verilog Code • Verify functionality using Test-bench • Synthesize the design targeting suitable library and by setting area and timing constraints • Tabulate the Area, Power and Delay for the Synthesized netlist • Identify Critical path
4	Latch and Flip-Flop Synthesize the design and compare the synthesis report (D, SR, JK)
5	Four bit Synchronous counter with Asynchronous reset • Write Verilog Code • Verify functionality using Test-bench • Synthesize the design targeting suitable library and by setting area and timing constraints • Tabulate the Area, Power and Delay for the Synthesized netlist Identify Critical path
6	Four bit Synchronous MOD-N counter with Asynchronous reset • Write Verilog Code • Verify functionality using Test-bench • Synthesize the design targeting suitable library and by setting area and timing constraints • Tabulate the Area, Power and Delay for the Synthesized netlist Identify Critical path

03.10.2022

7	Capture the schematic of CMOS inverter with load capacitance of 0.1pF and set the widths of Inverter with Wn = Wp, Wn = 2Wp, Wn = Wp/2 and length at selected technology. Carry out the following:

	i. Set the input signal to a pulse with rise time, fall time of 1ns and pulse width of 10ns and the time period of 20ns and plot the input voltage and output voltage of designed inverter? ii. From the simulation result compute tpHL, tpLH and td for all three geometrical settings of width? iii. Tabulate the results of delay and find the best geometry for minimum delay for CMOS inverter.
8	Capture the schematic of 2-input CMOS NAND gate having similar delay as that of CMOS inverter computed in experiment above. Verify the functionality of NAND gate and also find out the delay td for all four possible combinations of input vectors. Table the results. Increase the drive strength to 2X and 4X and tabulate the results.
9	Capture the schematic of 2-input CMOS NOR gate having similar delay as that of CMOS inverter computed in experiment above. Verify the functionality of NOR gate and also find out the delay td for all four possible combinations of input vectors. Table the results. Increasethe drive strength to 2X and 4X and tabulate the results.
10	Capture the schematic of the Boolean Expression Y= $\overline{AB+CD+E}$ using CMOS Logic. Verify the functionality of the expression find out the delay td for some combination of input vectors. Table the results.
	Demonstration Experiments (For CIE)
11	UART • Write Verilog Code • Verify the Functionality using Test-bench • Synthesize the design targeting suitable library and by setting area and timing constraints • Tabulate the Area, Power and Delay for the Synthesized netlist, Identify Critical path

12	Design and characterize 6T binary SRAM cell and measure the following: • Read Time, Write Time, SNM, Power • Draw Layout of 6T SRAM, use optimum layout methods. Verify for DRC & LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record the observations.

Course outcomes (Course Skill Set):

On the completion of this laboratory course, the students will be able to:

1. Design and simulate combinational and sequential digital circuits using Verilog HDL.
2. Understand the synthesis process of digital circuits using EDA tool.
3. Perform ASIC design flow and understand the process of synthesis, synthesis constraints and evaluating the synthesis reports to obtain optimum gate level netlist.
4. Design and simulate basic CMOS circuits like inverter, NAND gate, NOR gate and any Boolean expression .
5. Perform RTL_GDSII flow and understand the stages in ASIC design.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of the semester and the second test shall be conducted after the 14th week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be

decided jointly by examiners.
Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.
Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.
General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners).
Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.
The duration of SEE is 03 hours.
Rubrics suggested in Annexure-II of Regulation book

03.10.2022

Intelligent Systems and Machine Learning Algorithms		Semester	5
Course Code	**BEC515A**	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03
Examination type (SEE)	THEORY		

Course objectives:

This course will enable students to:

- Gain a historical perspective of AI and its foundations.
- Become familiar with basic principles of AI toward Problem-Solving
- Get to know approaches of inference, perception, knowledge representation, and learning
- Define Machine Learning and understand the basic theory underlying machine learning.
- Differentiate supervised, unsupervised, and reinforcement learning

Teaching-Learning Process (General Instructions)

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These are sample Strategies teachers can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only traditional lecture method; different teaching methods may be adopted to develop the outcomes.
2. Encourage collaborative (Group) Learning in the class.
3. Ask at least three HOTS (Higher Order Thinking) questions in the class, which promotes criticalthinking.
4. Adopt Problem-Based Learning (PBL), which fosters students' Analytical skills, and develops thinking skillssuch as evaluating, generalizing, and analyzing information rather than simply recalling it.
5. Topics will be introduced in a multiple representation.
6. Show the different ways to solve the same problem and encourage the students to come up withcreative ways to solve them.
7. Discuss how every concept can be applied to the real world and when that's possible, it helps improve the student's understanding.
8. Adopt the Flipped class technique by sharing the materials/Sample Videos before the class and having discussions on the topic in the succeeding classes.

Module-1

Introduction: What is AI? Foundations and History of AI Intelligent Agents: Agents and environment, Concept of Rationality, The nature of environment, The structure of agents.

Text book 1: Chapter 1- 1.1, 1.2, 1.3 Chapter 2- 2.1, 2.2, 2.3, 2.4

Module-2

Problem-solving: Problem-solving agents, Example problems, Searching for Solutions Uninformed Search Strategies: Breadth First search, Depth First Search, Iterative deepening depth first search;

Text book 1: Chapter 3- 3.1, 3.2, 3.3, 3.4

Module-3

Informed Search Strategies: Heuristic functions, Greedy best first search, A*search. Heuristic Functions Logical Agents: Knowledge–based agents, The Wumpus world, Logic, Propositional logic, Reasoning patterns in Propositional Logic

Text book 1: Chapter 3-3.5,3.6 Chapter 4 – 4.1, 4.2 Chapter 7- 7.1, 7.2, 7.3, 7.4, 7.5

Module-4
Introduction: Machine learning Landscape: what is ML?, Why, Types of ML, main challenges of ML Concept learning and Learning Problems – Designing Learning systems, Perspectives and Issues – Concept Learning – Find S-Version Spaces and Candidate Elimination Algorithm – Remarks on VS- Inductive bias. Text book 3: Chapter 1, Textbook 4:Chapter 1 and 2
Module-5
End-to-end Machine learning Project: Working with real data, Look at the big picture, Get the data, Discover and visualize the data, Prepare the data, select and train the model, Fine tune your model. Classification: MNIST, training a Binary classifier, performance measure, multiclass classification, error analysis, multi-label classification, multi-output classification Textbook 4: Chapter 2, Chapter 3
Course outcome (Course Skill Set) At the end of the course, the student will be able to: CO1. Apply knowledge of agent architecture, searching, and reasoning techniques for different Applications. CO 2. Compare various Searching and Inferencing Techniques. CO 3. Develop knowledge base sentences using propositional logic and first-order logic CO 4. Understand the concept of Machine Learning and Concept Learning. CO 5. Apply the concept of ML and various classification methods in a project

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

The Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by the University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.

Suggested Learning Resources:

Text Book:

1. Stuart J. Russell and Peter Norvig , Artificial Intelligence, 3rd Edition, Pearson,2015
2. Elaine Rich, Kevin Knight, Artificial Intelligence, 3rd Edition,Tata McGraw Hill,2013.
3. Tom M. Mitchell, Machine Learning, McGraw-Hill Education, 2013
4. Aurelien Geron, Hands-on Machine Learning with Scikit-Learn &Tensor Flow , O'Reilly, Shroff Publishers and Distributors Pvt. Ltd 2019.

Reference Books:

1. George F Lugar, Artificial Intelligence Structure and strategies for complex, Pearson Education, 5th Edition, 2011
2. Nils J. Nilsson, Principles of Artificial Intelligence, Elsevier, 1980
3. Saroj Kaushik, Artificial Intelligence, Cengage learning, 2014.

4. Ethem Alpaydin, Introduction to Machine Learning, PHI Learning Pvt. Ltd, 2nd Ed., 2013
5. T. Hastie, R. Tibshirani, J. H. Friedman, The Elements of Statistical Learning, Springer, 1st edition, 2001
6. Machine Learning using Python, Manaranjan Pradhan, U Dinesh Kumar, Wiley, 2019
7. Machine Learning, Saikat Dutt, Subramanian Chandramouli, Amit Kumar Das, Pearson,2020

Web links and Video Lectures (e-Resources):

- NPTEL Video lectures: https://nptel.ac.in/courses/106105077
- NPTEL Video lectures: https://nptel.ac.in/courses/106102220
- https://archive.nptel.ac.in/courses/106/105/106105152
- https://archive.nptel.ac.in/courses/106/106/106106202
- https://nptel.ac.in/domains/discipline/106?course=106_0

Activity-Based Learning (Suggested Activities in Class)/Practical-Based Learning

- Group Discussion/Quiz
- Mini projects.

Digital Switching and Finite Automata Theory			
Course Code	**BEC515B**	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	42	Total Marks	100
Credits	3	Exam Hours	3

Course objectives:

1. To understand the basics of switching theory, including combinational logic design and testing.
2. To learn finite-state machine design and testing, essential for modeling computational processes.
3. To illustrate methods for logic synthesis and optimization, crucial for efficient digital system design.
4. To understand the modern topics such as CMOS gates, logic design for emerging nanotechnologies, digital system testing, and asynchronous circuit design
5. To assess the practical examples to reinforce the learning and application concepts

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
2. Show Video/animation films to explain the functioning of various techniques.
3. Encourage collaborative (Group) Learning in the class.
4. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Topics will be introduced in multiple representations.
7. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

Logic design: Design with basic logic gates, Logic design with integrated circuits, NAND and NOR circuits, Design of high-speed adders, Metal-oxide semiconductor (MOS) transistors and gates(5.1 to 5.6 of Text1) **Threshold Logic:** Introductory Concepts: Threshold element, capabilities and limitations of threshold logic, Elementary Properties, Synthesis of Threshold networks: Unate functions, Identification and realization of threshold functions, The map as a tool in synthesizing threshold networks. (Sections 7.1, 7.2 of Text 1)

Teaching-Learning Process	Chalk and talk method, PowerPoint Presentation, YouTube videos, **RBT Level:** L1, L2, L3

Module-2	
Testing for Combinational circuits Fault models, Structural testing, IDDQ testing, Delay fault testing, Synthesis for testability, Testing for nanotechnologies (8.1 to 8.6 of Text1)	
Teaching-Learning Process	Chalk and talk method, Power point presentation, YouTube videos, **RBT Level:** L1, L2, L3
Module-3	
Finite-state machines: Introduction to synchronous sequential circuits and iterative networks, Sequential circuits – introductory example, The finite-state model – basic definitions, Memory elements and their excitation functions, Synthesis of synchronous sequential circuits, An example of a computing machine, Iterative networks (9.1 to 9.6 of Text1) **Capabilities, minimization, and transformation of sequential machines** The finite-state model – further definitions, Capabilities and limitations of finite-state machines State equivalence and machine minimization, Simplification of incompletely specified machines (10.1 to 10.4 Text1)	
Teaching-Learning Process	Chalk and talk method, PowerPoint Presentation, YouTubevideos **RBT Level:** L1, L2, L3
Module-4	
Asynchronous sequential circuits: Modes of operation, Hazards, Synthesis of SIC fundamental-mode circuits. **Structure of Sequential Machines:** Introductory example, State assignment using partitions: closed partitions, The lattice of closed partitions, Reduction of output dependency, Input dependence and autonomous clocks, Covers and generation of closed partitions by state splitting: Covers, The implication graph, An application of state splitting to parallel decomposition. (Section 11.1, 11.2, 11.3, 12.1, 12.2, 12.3, 12.4, 12.5, 12.6 of Text1)	
Teaching-Learning Process	Chalkandtalkmethod, PowerPoint Presentation, YouTube videos, **RBT Level:** L1, L2, L3
Module-5	
Memory, definiteness, and information loss lessness of finite automata Memory span with respect to input–output sequences (finite-memory machines), Memory span with respect to input sequences (definite machines), Memory span with respect to output sequences, Information-lossless machines(14.1 to 14.4 of Text1)	
Teaching-Learning Process	Chalk and talk method/Power point presentation, YouTube videos **RBT Level:** L1, L2, L3

Course outcomes (Course Skill Set)

At the end of the course the student will be able to:

1. Make use of mapping tool to synthesize threshold logic
2. Analyze effects of hazards and fault diagnosis in digital logical circuits
3. Examine the capabilities of Finite State Machines by minimization Procedures
4. Model the structures of sequential machines
5. Develop the methods of state identification and fault detection
6. Design the fault detection algorithm

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

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- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB4.2, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
    1. Marks scored shall be proportionally reduced to 50 marks

Suggested Learning Resources:

Text Books:

1. Switching and Finite Automata Theory – Zvi Kohavi and Niraj K. Jha, Cambridge University press, 3rd edition, 2010.

Reference Books:

2. Introduction to switching theory and logic design Fredriac J. Hill, Gerald Peterson, 3rd edition,
3. Fault Tolerant and Fault Testable Hardware Design-Parag K Lala, Prentice Hall Inc. 1985.
4. Digital Circuits and Logic Design. -Charles Roth Jr, Larry L. Kinney, Cengage Learning, 2014, ISBN: 978-1-133-62847-7.

Web links and Video Lectures (e-Resources)

https://onlinecourses.nptel.ac.in/noc20_cs67

https://onlinecourses.nptel.ac.in/noc24_cs61

Data Structures using C++		Semester	5
Course Code	**BEC515C**	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	2:2:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03
Examination type (SEE)	Theory		

Course objectives:

- Learn the Basic Concepts of C++
- Describe the concepts of Pointers and Arrays
- Concepts of Data Structures
- Understanding of the implementation of a linked list and Algorithms

Teaching-Learning Process (General Instructions)

These are sample Strategies teachers can use to accelerate the attainment of the various course outcomes.

1. **Online coding platforms can be used to execute programs**
2. **Mobile applications can be used to execute the codes.**
3. **Presentation of concepts**

Module-1

UNIT-I: Software Engineering Principles And C++ Classes

Software Life Cycle, Software Development Phase, Classes.
Page No. 1-7, 17-33
OOD: Inheritance, Polymorphism, Templates
Page No. 60-78,84-112

UNIT-II: Pointers & Array based Lists

Pointer Data Type and Pointer Variables, Classes & Pointers, Inheritance Pointers &Virtual functions, Abstract Classes & Pure Virtual functions, Array Based Lists
Page No. 131-183

Module-2

UNIT-III: Linked Lists &Stacks

Linked List, Linked List as an ADT, Unordered Linked List, ordered Linked List, Doubly Linked Lists
Page No. 265-320
Stack: Stacks, Implementation of Stacks as Arrays , Linked Implementation of Stacks
Page No. 395-428

Module-3

UNIT-IV: Queues and Algorithms

Queue Operations, Implementation of Queues as Arrays, Linked Implementation of Queues, STL class queue, Priority Queues, Application of Queues: Simulation.
Page No. 451-490
Search Algorithms, Hashing, Sorting Algorithms: Selection sort, Insertion sort, Shell Sort.
Page No. 497-524,533-550

Module-4

UNIT-V: Binary Trees and B-Trees

Binary Trees, Binary Tree Traversal, Binary Search Trees, Binary Search Tree: Analysis, Non-recursive Binary Tree Traversal Algorithms, Binary Tree Traversal and Functions as Parameters, AVL (Height-Balanced) Trees, B-Trees
Page No. 599-675

Module-5

UNIT-VI: Graphs

Introduction, Graph Definitions and Notations, Graph Representation, Operations on Graphs, Graphs as ADTs, Graph Traversals, Shortest Path Algorithm, Minimum Spanning Tree, Topological Order, Euler Circuits

Page No.685-721

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

1. Distinguish between procedures and object-oriented programming.
2. Apply advanced data structure strategies for exploring complex data structures.
3. Compare and contrast various data structures and design techniques in Performance.
4. Implement data structure algorithms through C++. Incorporate data structures into the applications such as binary search trees, AVL, and B Trees
5. Implement all data structures like stacks, queues, trees, lists, and graphs and compare their Performance and trade-offs.

Assessment Details (both CIE and SEE)

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3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

Text Book:

1.D.S.Malik - Data Structures using C++2nd Edition.

Reference Book

1. Sartaj Sahni – Data Structures, Algorithms, and Applications in C++ 2nd Edition

Web links and Video Lectures (e-Resources):

- https://nptel.ac.in/courses/106106127
- https://nptel.ac.in/courses/106102064
- https://nptel.ac.in/courses/106106133

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Students Can use Mobile applications/Online compilers/Code blocks to execute the programs and check output for different cases.