	Embedded System Design	Semester	06
Course Code	BEC601	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:2:0	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory + 8-10 Lab slots	Total Marks	100
Credits	04	Exam Hours	
Examination nature (SEE)	Theory		

Course objectives:

- Identify various components, their purpose, and their application to the embedded system's applicability.
- Program various embedded components using the embedded C program.
- Understand the embedded system's real-time operating system and its application in IoT
- Understand the fundamentals of ARM-based systems, including architecture and its units like registers , debug interface, stack, MPU, Interrupts etc
- Use the various instructions to program the ARM controller.

Teaching-Learning Process (General Instructions)

These are sample Strategies; that teachers can use to accelerate the attainment of the various course outcomes.

1. In addition to the traditional lecture method, different types of innovative teaching methods may be adopted so that the delivered lessons shall develop students' theoretical and applied Mathematical skills.
2. Provide real-life examples.
3. Support and guide the students for self–study.
4. You will assign homework, grading assignments and quizzes, and documenting students' progress.
5. Encourage the students to group learning to improve their creative and analytical skills.
6. Show short related video lectures in the following ways:
   - As an introduction to new topics (pre-lecture activity).
   - As a revision of topics (post-lecture activity).
   - As additional examples (post-lecture activity).
   - As an additional material of challenging topics (pre-and post-lecture activity).
   - As a model solution of some exercises (post-lecture activity).

MODULE-1

Introduction to Embedded System: What is an Embedded Systems? Embedded systems Vs General computing systems, History of Embedded Systems, Classification of Embedded systems, Major Application Areas of Embedded Systems. Purpose of Embedded Systems, The Typical Embedded System, Microprocessor Vs Microcontroller, Differences between RISC and CISC, Harvard V/s Von-Neumann Processor/Controller Architecture, Big-endian V/s Little-endian processors, Memory (ROM and RAM types), Sensors & Actuators, The I/O Subsystem – I/O Devices, Light Emitting Diode (LED), 7-Segment LED Display, Optocoupler, Relay, Piezo buzzer, Push button switch, Communication Interfaces, On-board Communication Interface, External Communication Interface, Embedded Firmware, Other System Components

(Text 1: All the Topics from Ch-1 and Ch-2.)

MODULE-2

Embedded System Design Concepts: Characteristics and Quality Attributes of Embedded Systems, Operational and non-operational quality attributes, Embedded Systems-Application and Domain specific, Hardware Software Co-Design and Program Modeling (excluding UML), Embedded firmware design and development (excluding C language).

Text 1: Ch-3, Ch-4 (4.1, 4.2.1 and 4.2.2 only), Ch-7 (Sections 7.1, 7.2 only), Ch-9 (Sections 9.1, 9.2, 9.3.1, 9.3.2 only)
MODULE-3
RTOS and IDE for Embedded System Design: Operating System basics, Types of operating systems, Task, process and threads (Only POSIX Threads with an example program), Thread preemption, Preemptive Task scheduling techniques, Task Communication, Task synchronization issues – Racing and Deadlock. How to choose an RTOS, Integration and testing of Embedded hardware and firmware, Embedded system Development Environment – Block diagram (excluding Keil). **(Text 1: Ch-10 (Sections 10.1, 10.2, 10.3, 10.5.2 , 10.7, 10.8.1.1, 10.8.1.2 only), Ch-12, Ch-13 (a block diagram before 13.1, only).**
MODULE-4
ARM Embedded Systems: Introduction, RISC design philosophy, ARM design philosophy, Embedded system hardware – AMBA bus protocol, ARM bus technology, Memory, Peripherals, Embedded system software – Initialization (BOOT) code, Operating System, Applications. ARM Processor Fundamentals, ARM core dataflow model, registers, current program status register, Pipeline, Exceptions, Interrupts and Vector Table, Core extensions. **Text 2: Chapter 1, 2**
MODULE-5
Introduction to the ARM Instruction set: Introduction, Data processing instructions, Load – Store instruction, Software interrupt instructions, Program status register instructions, Loading constants, ARMv5E extensions, Conditional Execution. **Text 2: Chapter 3**

PRACTICAL COMPONENT OF IPCC

Conduct the following experiments on an ARM CORTEX M3 evaluation board to learn Assembly Language Program and using evaluation version of Embedded 'C' & Keil uVision-4 tool/compiler.

Sl.NO	Experiments
1	Write a program to find the sum of the first 10 integer numbers.
2	Write an Assembly Language Program (ALP) to i) Multiply two 16-bit numbers. ii) Add two 32-bit numbers.
3	Write a program to find the factorial of a number.
4	Write a program to add an array of 16 bit numbers and store the 32 bit result in internal RAM.
5	Write a program to find the square of a number (1 to 10) using a look-up table.
6	Write a program to find the largest or smallest number in an array of 32 numbers.
7	Write a program to arrange a series of 32 bit numbers in ascending/descending order.
8	Write a program to count the number of ones and zeros in two consecutive memory locations.
9	Interface a Stepper motor and rotate it in clockwise and anti-clockwise direction.
10	Interface a DAC and generate Triangular and Square waveforms.
11	Display the Hex digits 0 to F on a 7-segment LED interface, with a suitable delay in between.
12	Interface a simple Switch and display its status through Relay, Buzzer and LED

Course outcomes (Course Skill Set):
At the end of the course, the student will be able to:

- Describe the architectural features and instructions of 32-bit microcontroller ARM Cortex M3.
- Apply the knowledge gained for Programming ARM Cortex M3 for different applications.
- Understand the basic hardware components and their selection method based on the characteristics and attributes of an embedded system.
- Understand the hardware software co-design and firmware design approaches.
- Explain the need of real time operating system for embedded system applications.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

CIE for the theory component of the IPCC (maximum marks 50)

- IPCC means practical portion integrated with the theory of the course.
- CIE marks for the theory component are **25 marks** and that for the practical component is **25 marks**.
- 25 marks for the theory component are split into **15 marks** for two Internal Assessment Tests (Two Tests, each of 15 Marks with 01-hour duration, are to be conducted) and **10 marks** for other assessment methods mentioned in 22OB4.2. The first test at the end of 40-50% coverage of the syllabus and the second test after covering 85-90% of the syllabus.
- Scaled-down marks of the sum of two tests and other assessment methods will be CIE marks for the theory component of IPCC (that is for **25 marks)**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the theory component of IPCC.

CIE for the practical component of the IPCC

- **15 marks** for the conduction of the experiment and preparation of laboratory record, and **10 marks** for the test to be conducted after the completion of all the laboratory sessions.
- On completion of every experiment/program in the laboratory, the students shall be evaluated including viva-voce and marks shall be awarded on the same day.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to **15 marks**.
- The laboratory test **(duration 02/03 hours)** after completion of all the experiments shall be conducted for 50 marks and scaled down to **10 marks.**
- Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **25 marks**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the practical component of the IPCC.

SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.

4. Marks scored by the student shall be proportionally scaled down to 50 Marks

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper may include questions from the practical component.

Suggested Learning Resources:

Text Books

1. **Shibu K V, "Introduction to Embedded Systems", Tata McGraw Hill Education**
2. **Andrew N Sloss, Dominic System and Chris Wright, "ARM System Developers Guide", Elsevier, Morgan Kaufman publisher, 1st Edition, 2008.**

Reference Book

1. **Raj Kamal, "Embedded Systems: Architecture and Programming", Tata McGraw Hill, 2008.**

Web links and Video Lectures (e-Resources):

1. https://archive.nptel.ac.in/courses/106/105/106105193/
2. https://developer.arm.com/documentation/dui0068/b/ARM-Instruction-Reference
3. https://www.udemy.com/course/introduction-to-arm-cortex-m3-and-m4-processors/
4. www.Nuvoton .com/websites on Advanced ARM Cortex Processors
5. https://alison.com/tag/embedded-systems

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Programming Assignments / Mini Projects can be given to improve programming skills

VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI
B.E: Electronics Engineering (VLSI Design and Technology)
NEP, Outcome Based Education (OBE) and Choice Based Credit System (CBCS)
(Effective from the academic year 2022 – 23)

VI Semester

Analog and Mixed Signal Integrated Circuit Design			
Course Code	**BVL602**	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	4:0:0:0	SEE Marks	50
Total Hours of Pedagogy	52	Total Marks	100
Credits	4	Exam Hours	3

- **Course Learning objectives:**

- To understand the basic operation of MOS switch and Current mirrors in analog CMOS design.
- To study and designing of Single-Stage Amplifiers and Differential Amplifiers.
- To learn Data Converter Specifications and Architectures.

MODULE-1

Analog CMOS Subcircuits:
MOS as switch, MOS as diode/active resistor, Current sinks & sources. Ideal & practical Current sources. Basic current mirror, cascode current mirror, Wilson current mirror.

[Text 1: 4.1,4.2,4.3,4.4]

Teaching-Learning Process: Chalk and talk method, YouTube videos, Power point presentation RBT Level: L1, L2, L3

MODULE-2

Single Stage Amplifiers: General Considerations, Common-Source Stage, Common-Source Stage with Resistive Load, CS Stage with Diode-Connected Load, CS Stage with Current-Source Load, CS Stage with Active Load, Source Follower.

[Text 2: 3.1,3.2,3.3,3.3.1, 3.3.2, 3.3.3, 3.3.4,3.4]

Teaching-Learning Process: Chalk and talk method, YouTube videos, Power point presentation RBT Level: L1, L2, L3

MODULE-3

CMOS Amplifiers : Active Load Inverter , Design & analysis of Differential amplifiers and its types, Design and analysis of cascode amplifiers , current amplifier , output amplifiers.

[Text 1: 5.1,5.2,5.3,5.4,5.5]

Teaching-Learning Process: Chalk and talk method, YouTube videos, Power point presentation RBT Level: L1, L2

MODULE-4

Operational Amplifiers: General considerations of Operational amplifiers, One stage Op amps, Two stage Op amps, Oscillators, LC Oscillators, Colpitts Oscillator (No derivation)

[Text 2: 9.1,9.2, 9.2.1, 9.2.2, 9.2.3,9.3 ,15.1,15.3, 15.3.3]

Teaching-Learning Process: Chalk and talk method, YouTube videos, Power point presentation RBT Level: L1, L2.L3

MODULE-5

Phase Locked Loops: Simple PLL, Phase Detector, Basic PLL Topology, Dynamics of Simple PLL. **D/A and A/D Converters:** Introduction and Characterization of D/A converters**,** Parallel Digital to Analog converters, Introduction and Characterization of A/D converters, Serial Analog to digital Converter, Medium Speed Analog to digital Converter (Only Block diagram).

[Text 2: 16.1, 16.1.1, 16.1.2,16.1.3 Text 1: 10.1,10.2 , 10.5,10.6 , 10.7]

Suggested Learning Resources:

Text Books

1.Philip E Allen & Douglas Hollberg " CMOS Analog Circuit Design ".

2. Behzad Razavi " Design of Analog CMOS _Integrated Circuits ".

Reference Books

1. R . Jacob Baker "CMOS Circuit Design, Layout, and Simulation".

WeblinksandVideoLectures(e-Resources):

1. https://www.youtube.com/watch?v=Q3WYZF5wzgU&list=PLbMVogVj5nJQB44z6h0XO2644Vbv7OM8_

2.https://www.youtube.com/watch?v=311XkpNGs8c&list=PL3pGy4HtqwD0rl7gQoESHR-chSq4OPN5p

3.https://www.youtube.com/watch?v=eLTpf_5di2o&list=PLbMVogVj5nJRlMz5diOg9wBizaU6-egJc

4. https://www.youtube.com/watch?v=dcCj_xAXm4k&list=PLLDC70psjvq5vtrb0EdII4xIKA15ec-Ij

5. VTUe-learningResources.

L ow Power VLSI Design			
Course Code	**BVL613A**	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03(Theory)

Course Learning objectives: This course will enable students to:

· To identify the power dissipation mechanisms in various MOS logic styles

· To familiarize suitable techniques to reduce power dissipation

Module-1

Introduction

Introduction, Sources of power dissipation, designing for low power, Physics of Power dissipation in MOSFET devices MIS structure, Need for low power circuit design, Threshold voltage, body effects.

RBT Levels: L2, L3

Module-2

Power dissipation in CMOS

Sources of power dissipation in CMOS-Switching power dissipation, Short circuit power dissipation, glitching power dissipation, Leakage power dissipation, Transistor leakage mechanisms of deep submicron transistors, Low power design limits - Principles of low power design.

RBT Levels: L2, L3

Module-3

LOW POWER CIRCUIT TECHNIQUES

Low Power Circuit Techniques: Power consumption in circuits, flip-flops & latches, high capacitance nodes, energy recovery, reversible pipelines, high performance approaches.

RBT Levels: L2, L3

Module-4

LOGIC SYNTHESIS FOR LOW POWER ESTIMATION TECHNIQUES

Logic Synthesis for Low Power estimation techniques: Power minimization techniques, low power arithmetic components- circuit design styles, adders, multipliers

RBT Levels: L3, L4

Module-5

LOW POWER MEMORY DESIGN

Low-Voltage Low-Power Memories: Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit, Low Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

RBT Levels: L3, L4

Sl. No.	Description	Blooms Level
CO1	Understand the impact of low power on system performance	L2
CO2	Identify the mechanisms of power dissipation in digital IC systems.	L3
CO3	Apply different circuit techniques to manage the low power	L3
CO4	Analyze the functionality of Low- voltage low -power memories	L4

Text Books:

1. Gray Yeap, Practical low power digital VLSI design, Springer, 1998

2. Kaushik Roy, Sharat C Prasad, Low power CMOS VLSI circuit design, Wiley India, 2000

3. P Rashinkar, Paterson and L. Singh, —Low Power Design Methodologies‖, Kluwer Academic, 2002

REFERENCE BOOKS:

1. J.B.Kulo and J.H Lou, —Low voltage CMOS VLSI Circuits‖, Wiley, 1999.

2. A.P.Chandrasekaran and R.W.Broadersen, —Low power digital CMOS design‖, Kluwer,1995

3. Abdellatif Bellaouar, Mohamed I Elmasry, Low power digital VLSI design, Kluwer Academic, 1995

4. Anatha P Chandrakasan, Robert W Brodersen, Low power digital CMOS Design, Kluwer Academic, 1995

5. Christian Piguet, Low power CMOS circuits, Taylor & Francis, 2006

6. Kiat Seng Yeo, Kaushik Roy, Low voltage, low power VLSI sub systems, Tata McGraw Hill, 2004

Electronics Engineering (VLSI Design and Technology)
Choice Based Credit System (CBCS) and Outcome Based Education (OBE)
SEMESTER – VI

Data Security

Course Code	BEC613B	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory	Total Marks	100
CREDITS - 03			

Course objectives:

This course will enable students to:

- Preparation: To prepare students with fundamental knowledge/ overview in the field of Information Security with knowledge of mathematical concepts required for cryptography.
- Core Competence: To equip students with a basic foundation of Cryptography by delivering the basics of symmetric key and public key cryptography, authentication functions like HASH codes, MACs, digital signatures, as well as key distribution

Teaching-Learning Process (General Instructions)

These are sample Strategies; that teachers can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
2. Show Video/animation films to explain the different concepts of Digital Signal Processing
3. Encourage collaborative (Group) Learning in the class
4. Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Topics will be introduced in a multiple representation.
7. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world - and when that's possible, it helps to improve the students' understanding.
9. Adopt Flipped class technique by sharing the materials / Sample Videos prior to the class and have discussions on the that topic in the succeeding classes.
10. Give Programming Assignments.

MODULE-1	RBTL Level
Classical Encryption Techniques: Symmetric cipher model, Substitution techniques (excluding Hill cipher) (Text 1: Chapter 1: Section 1, 2) **Block Ciphers**: Traditional Block Cipher structure, (Text 1: Chapter 2: Section1) The AES Cipher. (Text 1: Chapter 4: Section 2,4) Block Cipher Modes of Operation (Text 1: Chapter 5: Section 2, 3, 4, 5, 6)	L1, L2, L3
MODULE-2	
Basic Concepts of Number Theory and Finite Fields: Divisibility and The Division Algorithm Euclidean algorithm, Modular arithmetic, Groups, Rings and Fields, Finite fields of the form GF(p), Polynomial Arithmetic, Fields of the Form GF(2_m) (Text 1: Chapter 3)	L1, L2, L3
MODULE-3	

More on Number Theory: Prime Numbers, Fermat's and Euler's theorem, discrete logarithm. (Text 1: Chapter 7: Section 1, 2, 5) **ASYMMETRIC CIPHERS**: Principles of Public-Key Cryptosystems, The RSA algorithm (Text 1: Chapter 8: Section 1, 2), Diffie – Hellman Key Exchange, Elliptic Curve Arithmetic over Z_p, Elliptic Curve Cryptography (Text 1: Chapter 9: Section 1, 3, 4)	L1, L2, L3
MODULE-4	
Cryptographic Hash Functions: Application of Hash Functions, Two Simple Hash Functions, Requirements and Security, Hash function based on Cipher Block Chaining, SHA-512 (Only structural description). (Text 1: Chapter 10: Section 1, 2, 3, 4, 5) **Message Authentication Codes:** Message Authentication Functions, Security of MACs, MACs based on Hash Functions. (Text 1: Chapter 11: Section 2, 4, 5)	L1, L2, L3
MODULE-5	
Digital Signatures: Digital Signatures, NIST Digital Signature Algorithm, Elliptic Curve Digital Signature Algorithm. (Text 1: Chapter 12: Section 1, 4, 5) **Key Management and Distribution:** Symmetric Key Distribution Using Symmetric Encryption, Symmetric Key Distribution Using Asymmetric Encryption, Distribution of Public Keys (Text 1: Chapter 13: Section 1, 2, 3)	L1, L2, L3

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

- Explain traditional cryptographic algorithms of encryption and decryption process.
- Use symmetric and asymmetric cryptography algorithms to encrypt and decrypt the data.
- Apply concepts of modern algebra in cryptography algorithms.
- Explain message authentication using HASH functions, MAC functions and Digital signatures.
- Explain how symmetric and asymmetric encryption algorithms can be used to distribute keys.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks.
- Any two assignment methods mentioned in the 22OB4.2, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks).
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:
Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Text Book

1. William Stallings, "Cryptography and Network Security Principles and Practice", Pearson Education Inc., 6th Edition, 2014, ISBN: 978-93-325-1877-3

Reference Books

1. Bruce Schneier, "Applied Cryptography Protocols, Algorithms, and Source code in C", Wiley Publications, 2nd Edition, ISBN: 9971-51-348-X.
2. Cryptography and Network Security, Behrouz A Forouzan, TMH, 2007.

Web links and Video Lectures (e-Resources):

- https://archive.nptel.ac.in/courses/106/105/106105162

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

1. Experiential Learning by using free and open-source software's SCILAB or OCTAVE or Python

VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI

B.E: Electronics & Communication Engineering / B.E: Electronics & Telecommunication Engineering
NEP, Outcome Based Education (OBE) and Choice Based Credit System (CBCS)
(Effective from the academic year 2021 – 22)

VI Semester

Digital Image Processing			
Course Code	**BEC613C**	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	3:0:0:1	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3

Course objectives:

- Understand the fundamentals of digital image processing.
- Understand the image transform used in digital image processing.
- Understand the image enhancement techniques in spatial domain used in digital image processing.
- Understand the Color Image Processing and frequency domain enhancement techniques in digital image processing.
- Understand the image restoration techniques and methods used in digital image processing.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

1. Show Video/animation films to explain the functioning of various image processing concepts.
2. Encourage cooperative (Group) Learning through puzzles, diagrams, coding etc., in the class.
3. Encourage students to ask questions and investigate their own ideas helps improve their problem-solving skills as well as gain a deeper understanding of academic concepts.
4. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking
5. Students are encouraged to do coding based projects to gain knowledge in image processing.
6. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
7. Topics will be introduced in multiple representations.
8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding
9. Arrange visits to nearby PSUs such as CAIR (DRDO), NAL, BEL, ISRO, etc., and small-scale software industries to give industry exposure.

Module-1

Digital Image Fundamentals: What is Digital Image Processing? Origins of Digital Image Processing, Examples of fields that use DIP, Fundamental Steps in Digital Image Processing, Components of an Image Processing System, Elements of Visual Perception, Image Sensing and Acquisition, Image Sampling and Quantization, Some Basic Relationships Between Pixels.
[Text 1: Chapter 1, Chapter 2: Sections 2.1 to 2.5]

Teaching-Learning Process	Chalk and talk method, PowerPoint Presentation, YouTube videos, Videos on Image processing applications Self-study topics: Arithmetic and Logical operations Practical topics: Problems on Basic Relationships Between Pixels. **RBT Level:** L1, L2, L3

<table>
<tr><th colspan="2">Module-2</th></tr>
<tr><td colspan="2">Image Transforms: Introduction, Two-Dimensional Orthogonal and Unitary Transforms, Properties of Unitary Transforms, Two-Dimensional DFT, cosine Transform, Haar Transform.
Text 2: Chapter 5: Sections 5.1 to 5.3, 5.5, 5.6, 5.9]</td></tr>
<tr><td>Teaching-Learning Process</td><td>Chalk and talk method, PowerPoint Presentation, YouTube videos of various transformation techniques and related applications.
Self-study topics: Sine transforms, Hadamard transforms, KL transform, Slant transform.
Practical topics: Problems on DFT and DCT
RBT Level: L1, L2, L3</td></tr>
<tr><th colspan="2">Module-3</th></tr>
<tr><td colspan="2">Spatial Domain: Some Basic Intensity Transformation Functions, Histogram Processing, Fundamentals of Spatial Filtering, Smoothing Spatial Filters, Sharpening Spatial Filters
[Text: Chapter 3: Sections 3.2 to 3.6]</td></tr>
<tr><td>Teaching-Learning Process</td><td>Chalk and talk method, PowerPoint Presentation, YouTube videos and animations of Intensity Transformation Functions, Histogram Processing, Spatial domain filters.
Self-study topics: Point, line and edge detection.
Practical topics: Problems on Intensity Transformation Functions, Histogram, Spatial domain filters
RBT Level: L1, L2, L3</td></tr>
<tr><th colspan="2">Module-4</th></tr>
<tr><td colspan="2">Frequency Domain: Basics of Filtering in the Frequency Domain, Image Smoothing and Image Sharpening Using Frequency Domain Filters.
Color Image Processing: Color Fundamentals, Color Models, Pseudo-color Image Processing.
[Text 1: Chapter 4: Sections 4.7 to 4.9 and Chapter 6: Sections 6.1 to 6.3]</td></tr>
<tr><td>Teaching-Learning Process</td><td>Chalk and talk method, PowerPoint Presentation, YouTube videos on frequency domain filtering, Color image processing.
Self-study topics: Basic concept of segmentation.
Practical topics: Problems on Pseudo-color Image Processing
RBT Level: L1, L2, L3</td></tr>
<tr><th colspan="2">Module-5</th></tr>
<tr><td colspan="2">Restoration: A model of the Image Degradation/Restoration Process, Noise models, Restoration in the Presence of Noise Only using Spatial Filtering and Frequency Domain Filtering, Inverse Filtering, Minimum Mean Square Error (Wiener) Filtering.
[Text 1: Chapter 5: Sections 5.1, to 5.4.3, 5.7, 5.8]</td></tr>
<tr><td>Teaching-Learning Process</td><td>Chalk and talk method, PowerPoint Presentation, YouTube videos on Noise models, filters and their applications.
Self-study topics: Linear position invariant degradation, Estimation of degradation function.
RBT Level: L1, L2, L3</td></tr>
<tr><td colspan="2">Course outcomes (Course Skill Set)
At the end of the course the student will be able to:
1. Understand image formation and the role of human visual system plays in the perception of gray andcolor image data.
2. Compute various transforms on digital images.
3. Conduct an independent study and analysis of Image Enhancement techniques.
4. Apply image processing techniques in the frequency (Fourier) domain.
5. Design image restoration techniques.</td></tr>
</table>

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

Three Unit Tests each of **20 Marks (duration 01 hour**)

1. First test at the end of 5th week of the semester
2. Second test at the end of the 10th week of the semester
3. Third test at the end of the 15th week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4th week of the semester
5. Second assignment at the end of 9th week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks** (**duration 01 hours**)

6. At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours)**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module. Marks scored out of 100 shall be reduced proportionally to 50 marks

Suggested Learning Resources:

Text Books:

1. Digital Image Processing- Rafael C Gonzalez and Richard E Woods, PHI, 3rd Edition 2010.
2. Fundamentals of Digital Image Processing- A K Jain, PHI Learning Private Limited 2014.

Reference Book:

Digital Image Processing- S Jayaraman, S Esakkirajan, T Veerakumar, Tata McGraw Hill, 2014.

Web links and Video Lectures (e-Resources)

- Image databases, https://imageprocessingplace.com/root_files_V3/image_databases.htm
- Student support materials, https://imageprocessingplace.com/root_files_V3/students/students.htm
- NPTEL Course, Introduction to Digital Image Processing, https://nptel.ac.in/courses/117105079
- Computer Vision and Image Processing, https://nptel.ac.in/courses/108103174
- Image Processing and Computer Vision – Matlab and Simulink,
- https://in.mathworks.com/solutions/image-video-processing.html

Activity Based Learning (Suggested Activities in Class)/ Practical Based Learning

- Verilog /VHDL coding for Image manipulation.
- Simulink models for Image processing.

Digital System Design using Verilog		Semester	6
Course Code	**BEC654A**	CIE Marks	50
Teaching Hours/Week(L:T:P)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	3
Examination type (SEE)	Theory		

Course objectives:

- Learn different Verilog HDL constructs.
- Familiarize the different levels of abstraction in Verilog.
- Understand Verilog Tasks and Functions.
- Understand Timing and Delay Simulation.

Teaching-Learning Process (General Instructions)

The sample strategies, which the teacher can use to accelerate the attainment of the various course outcomes are listed in the following:

1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
2. Show Video/animation films to explain the functioning of various techniques.
3. Encourage collaborative (Group) Learning in the class
4. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
7. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.
8. Give programming assignments.

Module-1

Overview of Digital Design with Verilog HDL: Evolution of Computer-Aided Digital Design (CAD), Emergence of HDLs, Typical Design flow, Importance of HDLs, Popularity of Verilog HDL, Trends in HDLs. (**Text 1: 1.1 to 1.6**)

Hierarchical Modeling Concepts: Design Methodologies, Top-down and Bottom-up design methodology, Modules, Instances, Components of a Simulation, Design Block, Stimulus Block (Test Bench) with example. **(Text 1:2.1 to 2.6)**

Teaching-Learning Process	Chalk and talk method, Power point presentation **RBT Level:** L1, L2, L3

Module-2

Basic Concepts: Lexical Conventions, Data Types, System Tasks, Compiler Directives. **(Text 1: 3.1 to 3.3)**

Modules and Ports: Modules, Ports, Connecting Ports, Hierarchical Names. **(Text 1: 4.1 to 4.3)**

Teaching-Learning Process	Chalk and talk method, Power point presentation **RBT Level:** L1, L2, L3

Module-3	
Gate-Level Modeling: Gate Types-Modeling using basic Verilog gate primitives, Description of AND/OR and BUF/NOT type gates. Gate Delays-Rise, Fall and Turn-Off Delays, Min, Max and Typical Delays. **(Text1: 5.1, 5.2)** **Dataflow Modeling**: Continuous assignments, Delay Specification, Expressions, Operators, Operands, Operator Types, Examples **(Text 1: 6.1 to 6.5)**	
Teaching-Learning Process	Chalk and talk method, Power point presentation **RBT Level:** L1, L2, L3
Module-4	
Behavioral Description: Structured Procedures, Initial and Always statements, Procedural Assignments Blocking and Non-Blocking statements, Conditional statements, Multiway Branching, Loops, Sequential and Parallel blocks, Examples-4-to-1 Multiplexer, 4-bit Counter. **(Text 1: 7.1, 7.2, 7.4, 7.5, 7.6, 7.7, 7.9.1, 7.9.2)**	
Teaching-Learning Process	Chalk and talk method, Power point presentation **RBT Level:** L1, L2, L3
Module-5	
Structural Description: Highlights of Structural Descriptions, Organization of Structural Description, Binding **(Text 2: 4.1, 4.2, 4.3, Listings 4.1 to 4.13 only Verilog)** **Tasks and Functions**: Differences between Tasks and Functions, Declaration and Invocation, Examples **(Text 1: 8.1, 8.2, 8.2.1, 8.2.2, 8.3, 8.3.1, 8.3.2)**	

Course outcomes (Course Skill Set)

At the end of the course the student will be able to:

1. Understand the Verilog HDL design flow.
2. Describe the basic concepts of Verilog HDL programming.
3. Write Verilog programs in Gate, Dataflow, Behavioral, and structural modeling levels of Abstraction.
4. Write the programs more effectively using Verilog Tasks and Functions.
5. Perform Timing and Delay Simulation.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

Three Unit Tests each of **20 Marks (duration 01 hour**)

1. First test at the end of 5th week of the semester
2. Second test at the end of the 10th week of the semester
3. Third test at the end of the 15th week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4th week of the semester
5. Second assignment at the end of 9th week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks** (**duration 01 hours**)

6. At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours)**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module. Marks scored out of 100 shall be reduced proportionally to 50 marks

Suggested Learning Resources:

Text Books:

1. "Verilog HDL: A Guide to Digital Design and Synthesis", Samir Palnitkar, Pearson education, Second edition.
2. "HDL programming (VHDL and Verilog)", Nazeih M Botros, John Wiley India Pvt. Ltd., 2008.

Reference Books:

1. Donald E. Thomas, Philip R. Moorby, "The Verilog Hardware Description Language", Springer Science+Business Media, LLC, Fifth edition.
2. Michael D. Ciletti, "Advanced Digital Design with the Verilog HDL" Pearson (Prentice Hall), Second edition.
3. Padmanabhan, Tripura Sundari, "Design through Verilog HDL", Wiley, 2016 or earlier

	Consumer Electronics		Semester	6
	Course Code	**BEC654B**	CIE Marks	50
	Teaching Hours/Week (L: T:P: S)	3:0:0:0	SEE Marks	50
	Total Hours of Pedagogy	40	Total Marks	100
	Credits	03	Exam Hours	03
	Examination type (SEE)	Theory		

Course objectives:

- To understand the working principles and classifications of various microphones and loudspeakers, and their roles in audio systems.
- To explore the structure, recording, and playback processes of Audio Compact Disc systems, along with error correction techniques and digital-to-analog conversion.
- To analyse the fundamentals of colour television systems, including the transmission of colour signals, and to study recent advances in television technology.
- To gain knowledge of modern consumer electronic devices such as mobile phones, home appliances, and computers, focusing on their applications and technological advancements.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
2. Show Video/animation films to explain the functioning of various EV Architectures.
3. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyse information rather than simply recall it.
4. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

Microphones: Introduction, Requirements, Quality of Microphones, Classification, Moving Coil Microphone, Ribbon Microphone, Condenser (or Capacitor) Microphone, Crystal Microphone, Carbon Microphone, Electret Microphone.

Loudspeakers: Introduction, Features of Loudspeaker, Moving Coil (Cone Type) Loudspeaker, Electrodynamic Loudspeaker, Horn Loudspeaker, Loudspeaker for High Fidelity Systems.

(Text : 5.1 to 5.10 and 6.1 to 6.6)

Module-2

Audio Compact Disc Systems: Introduction, Comparison of CD and Tape, Optical Recording, Details of a Compact Disc, Details of Recording Process, Details of playback Process, Geometry of Audio Disc, Encoding Process and Error Correction, D/A Convertor, Handling of Compact Disc.

(Text : 10.1 to 10.10)

Module-3

Colour Television: Introduction, Light Energy, Primary Colours, Tristimulus Values, Trichromatic Coefficients, Colour Triangle, Mixing of Colours, Grassman's Law, Colour Specifications, Bandwidth for Colour Signal Transmission. Chromaticity Diagram, Spectral and Non-Spectral Colours, Colour Circle, Visibility Curve, Digital Television (DTV) and High Definition Television (HDTV), Recent Advances in TV technology, LCD TV, LED TV, Plasma TV

(Text : 14.1 to 14.9, 14.13 to 14.16 and 14.26 to 14.27)

Module-4

	Cable Television: Introduction, Video Monitor, Closed Circuit Television (CCTV), Cable Television, Cable TV Using Internet. **Miscellaneous Devices:** Digital Watch, Calculator, An Electronic Guessing Game, Cordless Telephone. (Text : 15.1 to 15.5 and 17.1 to 17.4)
	Module-5
	Mobile Telephone, Cellular Telephone, UPS, Inverter, Decorative Lighting, Remote Control for TV and VCR, Facsimile (FAX), Pager, Microwave Oven, LCD Timer with Alarm, Electronic Ignition System for Automobiles, Washing Machine, Organisation of Digital computer, Microprocessor, Note Book, Laptop, Tablet PC, Ultrabook, IPAD, Recent Advances in Consumer Electronics. (Text : 17.6 to 17.7 and 17.13 to 17.27)

Course outcome (Course Skill Set)

At the end of the course, the student will be able to:

1. Understand the functioning and classification of various types of microphones and loudspeakers
2. Demonstrate knowledge of the optical recording and playback processes in audio compact disc systems
3. Analyse the principles of colour television and modern display technologies
4. Evaluate the working of cable television systems and miscellaneous consumer devices
5. Explore advancements in consumer electronics, such as mobile phones, computing devices, and home appliances

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25 marks.
- The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.
- For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Books

1. B.R. Gupta, V. Singhal "Consumer Electronics", S.K. Kataria & Sons, 6th edition, 2013, ISBN 978-93-5014-407-7.
2. R.P.Bali, Consumer Electronics, Pearson Education (2008)

Web links and Video Lectures (e-Resources):

- Android Mobile Application Development: https://onlinecourses.swayam2.ac.in/nou24_ge66/preview
- Microelectronics: Devices to Circuits: https://onlinecourses.nptel.ac.in/noc24_ee139/preview

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Trouble shoot the common consumer electronics products like T.V., Washing machine , microwave oven , FAX, Copier machine.
- Conduct market survey for latest home appliances and compare specifications of reputed brands and prepare a report
- Make visit to service centres of gadgets covered in curriculum and if possible work there for some days on voluntarily basis during holidays.
- Search internet websites for DYS (Do Your Self) repair of electronic gadgets and try your hands to repair some gadgets based on that.

VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI
B.E: Electronics Engineering (VLSI Design and Technology)NEP, Outcome Based Education (OBE) and Choice Based Credit System (CBCS)
(Effective from the academic year 2022 – 23)

VI Semester

PCB Design and Fabrication			
Course Code	**BEC654C**	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3

Course objectives:

The main objective of the course is

- students are able to design an electronic printed circuit board for a specific application
- Understand industry standard software Tools for PCB design
- Able to understand the procedural steps of developing circuit schematic, board files, image transferring, assembly, soldering and testing.

Module-1	
Introduction: What is PCB . Advantages and Disadvantages of PCB , Components of PCB , Electronic components, ,Microprocessors and Microcontrollers, IC's , Surface Mount Devices (SMD) Classification of PCB , Single, double, multilayer and flexible boards , Manufacturing of PCB , PCB standards	
Teaching-Learning Process	Chalk and talk method, YouTube videos, Power point presentation **RBT Level:** L1, L2
Module-2	
Schematic diagram of PCB: General, Mechanical and Electrical design considerations of PCB , Placing and Mounting of components in PCB , Conductor spacing and routing guidelines , Heat sinks and package density of PCB ,Net list , Creating components for library, Tracks, Pads, Vias , Power plane and grounding of PCB	
Teaching-Learning Process	Chalk and talk method/Power point presentation **RBT Level:** L1, L2, L3

Module-3	
Design automation: Design Rule Checking b. Class Test , Exporting Drill and Gerber Files , Footprints and Libraries Adding and Editing Pins . Copper clad laminates materials , Electrical & Physical Properties of laminates ,Types of laminates , Soldering techniques , Image transfer.	
Teaching-Learning Process	Chalk and talk method, YouTube videos, Power point presentation **RBT Level:** L1, L2, L3
Module-4	
Photo printing, Screen Printing, Film master preparation , Plating techniques , Etching techniques , Lead cutting.	
Teaching-Learning Process	Chalk and talk method, YouTube videos, Power point presentation **RBT Level:** L1, L2, L3
Module-5	
Soldering Techniques , Testing of PCB , Quality controls of PCB , Trends in PCB Industries ,Environmental concerns in PCB industry , Class Test	
Teaching-Learning Process	Chalk and talk method/Power point presentation **RBT Level:** L1, L2, L3

Course outcome (Course Skill Set)

- Familiarize with the type of devices/components that may be mounted on PCB
- Understand the PCB layout techniques for optimized component density and power saving.
- Perform design and printing of PCB with the help of various image transfer and soldering techniques
- Understand the trends in the current PCB industry

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

Three Unit Tests each of **20 Marks (duration 01 hour**)

1. First test at the end of 5th week of the semester
2. Second test at the end of the 10th week of the semester
3. Third test at the end of the 15th week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4th week of the semester
5. Second assignment at the end of 9th week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks** (**duration 01 hours**)

6. At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours)**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module. Marks scored out of 100 shall be reduced proportionally to 50 marks

Suggested Learning Resources:

1. Printed Circuit Board – Design, Fabrication, Assembly & Testing, R.S. Khandpur, Tata McGraw Hill Publisher

2. Printed circuit Board – Design & Technology, Walter C. Bosshart, Tata McGraw Hill

VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI
B.E: Electronics Engineering (VLSI Design and Technology)
NEP, Outcome Based Education (OBE) and Choice Based Credit System (CBCS)
(Effective from the academic year 2022 – 23)

VI Semester

Basic VLSI Design			
Course Code	**BEC654D**	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3

Course objectives:

- Impart knowledge of MOS transistor theory and CMOS technologies
- Impart knowledge on architectural choices and performance trade-offs involved in designing and realizing the circuits in CMOS technology
- Cultivate the concepts of subsystem design processes
- Demonstrate the concepts of CMOS testing

Teaching-Learning Process (General Instructions)

The sample strategies, which the teacher can use to accelerate the attainment of the various course outcomes are listed in the following:

1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
2. Show Video/animation films to explain the functioning of various techniques.
3. Encourage collaborative (Group) Learning in the class
4. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
7. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.
8. Incorporate programming examples given under Activity based learning.

Module-1

Introduction: A Brief History, MOS Transistors, MOS Transistor Theory, Ideal I-V Characteristics, Non-ideal I-V Effects, DC Transfer Characteristics (1.1, 1.3, 2.1, 2.2, 2.4, 2.5 of TEXT2).
Fabrication: nMOS Fabrication, CMOS Fabrication [P-well process, N-well process, Twin tub process], BiCMOS Technology (1.7, 1.8, 1.10 of TEXT1).

Teaching-Learning Process	Chalk and talk method, YouTube videos, Power point presentation **RBT Level:** L1, L2

Module-2

MOS and BiCMOS Circuit Design Processes: MOS Layers, Stick Diagrams, Design Rules and Layout.
Basic Circuit Concepts: Sheet Resistance, Area Capacitances of Layers, Standard Unit of Capacitance, Some Area Capacitance Calculations, Delay Unit, Inverter Delays, Driving Large Capacitive Loads (3.1 to 3.3, 4.1, 4.3 to 4.8 of TEXT1).

Teaching-Learning Process	Chalk and talk method/Power point presentation **RBT Level:** L1, L2, L3

Module-3	
Scaling of MOS Circuits: Scaling Models & Scaling Factors for Device Parameters **Subsystem Design Processes**: Some General considerations, An illustration of Design Processes, **Illustration of the Design Processes**: Regularity, Design of an ALU Subsystem, The Manchester Carry-chain and Adder Enhancement Techniques (5.1, 5.2, 7.1, 7.2, 8.2, 8.3, 8.4.1, 8.4.2 of TEXT1).	
Teaching-Learning Process	Chalk and talk method, YouTube videos, Power point presentation **RBT Level:** L1, L2, L3
Module-4	
Subsystem Design: Some Architectural Issues, Switch Logic, Gate (restoring) Logic, Parity Generators, Multiplexers, The Programmable Logic Array (PLA) (6.1 to 6.3, 6.4.1, 6.4.3, 6.4.6 of TEXT1). **FPGA Based Systems**: Introduction, Basic concepts, Digital design and FPGAs, FPGA based System design, FPGA architecture, Physical design for FPGAs (1.1 to 1.4, 3.2, 4.8 of TEXT3).	
Teaching-Learning Process	Chalk and talk method, YouTube videos, Power point presentation **RBT Level:** L1, L2, L3
Module-5	
Memory, Registers and Aspects of system Timing: System Timing Considerations, Some commonly used Storage/Memory elements (9.1, 9.2 of TEXT1). **Testing and Verification**: Introduction, Logic Verification, Logic Verification Principles, Manufacturing Test Principles, Design for testability (12.1, 12.1.1, 12.3, 12.5, 12.6 of TEXT 2).	
Teaching-Learning Process	Chalk and talk method/Power point presentation **RBT Level:** L1, L2, L3

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

1. Demonstrate understanding of MOS transistor theory, CMOS fabrication flow and technology scaling.
2. Draw the basic gates using the stick and layout diagrams with the knowledge of physical design aspects.
3. Interpret Memory elements along with timing considerations
4. Demonstrate knowledge of FPGA based system design
5. Interpret testing and testability issues in VLSI Design
6. Analyze CMOS subsystems and architectural issues with the design constraints.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

Three Unit Tests each of **20 Marks (duration 01 hour**)

1. First test at the end of 5th week of the semester
2. Second test at the end of the 10th week of the semester
3. Third test at the end of the 15th week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4th week of the semester
5. Second assignment at the end of 9th week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks** (**duration 01 hours**)

6. At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours)**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module. Marks scored out of 100 shall be reduced proportionally to 50 marks

Suggested Learning Resources:

Text Books:

1. "Basic VLSI Design"- Douglas A Pucknell & Kamran Eshraghian, PHI, 3rd Edition.
2. "CMOS VLSI Design- A Circuits and Systems Perspective", Neil H E Weste, David Harris, Ayan Banerjee, 3rd Edition, Pearson Education.
3. "FPGA Based System Design", Wayne Wolf, Pearson Education, 2004, Technology and Engineering.

Web links and Video Lectures (e-Resources)

- https://nptel.ac.in/courses/117101058
- https://nptel.ac.in/courses/117106093
- https://youtu.be/9SnR3M3CIm4
- https://nptel.ac.in/courses/108/107/108107129/

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Wherever necessary **Cadence/Synopsis/Menta Graphics tools** must be used.

1.Write Verilog Code for the following circuits and their Test Bench for verification, observe the waveform and synthesize the code with technological library with given Constraints*. Do the initial timing verification with gate level simulation.

i. An inverter
ii. A Buffer
iii. Transmission Gate
iv. Basic/universal gates
v. Flip flop -RS, D, JK, MS, T
vi. Serial & Parallel adder
vii. 4-bit counter [Synchronous and Asynchronous counter]

2.Design an op-amp with given specification* using given differential amplifier Common source and Common Drain amplifier in library** and completing the design flow mentioned below:

a. Draw the schematic and verify the following
i) DC Analysis
ii) AC Analysis
iii) Transient Analysis
b. Draw the Layout and verify the DRC, ERC
c. Check for LVS
d. Extract RC and back annotate the same and verify the Design.

Analog and Mixed Signal IC Design Lab		Semester	5
Course Code	**BVLL 606**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:0:2:0	SEE Marks	50
Credits	01	Total SEE+CIE	100
		Exam Hours	3 Hours
Examination type (SEE)	**Practical**		

- **Course Learning objectives :**

This laboratory course enables students to

- Design, model, simulate and verify the functionality basic analog circuits.
- To understands the concepts of Operational amplifiers and applications of Op-Amps
- Able to understand the Dataconverters

Note: This Laboratory can be conducted using industry standard EDA tool like Cadence, Synopsis VLSI Tool

Sl.NO	Experiments
1	**MOS Characterization:** a. Input characteristics. b. Output/Transfer characteristics
2	a) Construct the schematic of CMOS inverter with load capacitance of 0.1pF and set the widths of inverter with Wn = Wp, Wn = 2Wp, Wn = Wp/2 and length at selected technology. Carry out the following: i. Set the input signal to a pulse with rise time, fall time of 1ns and pulse width of 10ns and the time period of 20ns and plot the input voltage and output voltage of designed inverter? ii. From the simulation result compute tpHL, tpLH and td for all three geometrical settings of width? iii. Tabulate the results of delay and find the best geometry for minimum delay for CMOS inverter. b) Draw layout of inverter with Wp/Wn = 40/20, use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre layout simulations and compare the results.
3	Construct the schematic of 2-input CMOS NOR gate having similar delay as that of CMOS inverter computed in experiment above. Verify the functionality of NOR gate and also find out the delay td for all four possible combinations of input vectors. Tabulate the results. Increase the drive strength to 2X and 4X, tabulate the results .
4	Design a CMOS as a switch with toggling rate of 1MHz and tabulate the Result
5	MOS as Diode/Active Resistor a. Design a MOS to act as Diode/active resistor whose resistance will be 100KΩ b. Find the operating region of the MOS

6	a) Construct the schematic of Common Source Amplifier with PMOS Current Mirror Load and find its transient response and AC response? Measure the Unit Gain Bandwidth (UGB), amplification factor by varying transistor geometries, study the impact of variation in width to UGB. b) Draw Layout of common source amplifier, use optimum layout methods. Verify for DRC & LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record the observations.
7	a) Construct the schematic of two-stage operational amplifier and measure the following: i. Unity gain Bandwidth ii. dB Bandwidth iii. Gain Margin and phase margin with and without coupling capacitance iv. Use the op-amp in the inverting and non-inverting configuration and verify its functionality. v. Study the UGB, 3dB bandwidth, gain and power requirement in op-amp by varying the stage wise transistor geometries and record the observations. b) Draw layout of two-stage operational amplifier with minimum transistor width set to 300 (in 180/90/45 nm technology), choose appropriate transistor geometries as per the results obtained in part a. Use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations and perform the comparative analysis.
8	Design a Diff-Amplifier with Current mirror load & measure the following parameters a. Find Gain b. Plot and find Gain Margin & Phase Margin
9	Design and Verify the functionality of First order Integrator using OPAMP
10	Design a 4- bit R-2R based DAC for the given specification a. Draw the schematic and verify the following i) DC Analysis ii) AC Analysis iii) Transient Analysis b. Draw the Layout and verify the DRC, LVS c. Extract RC and back annotate the same and verify the Design
11	Design and characterize 6T binary SRAM cell and measure the following: • Read Time, Write Time, SNM, Power

12	Demo experiment: Design and characterization of basic PLL for the given specifications

Course outcomes (Course Skill Set):

On the completion of this laboratory course, the students will be able to:

1. Students are able perform the Characterization of the basic MOS .
2. Design and simulate basic CMOS circuits like inverter, NOR gate and perform the post layout functionality check.
3. Design ,implement and analysis of analog, digital and mixed mode circuits
4. Learn the various issues in Mixed signal designs basically data converters

Static Timing Analysis Lab		Semester	5
Course Code	**BVLL657A**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:0:2:0	SEE Marks	50
Credits	01	Total SEE+CIE	100
		Exam Hours	3 Hours
Examination type (SEE)	**Practical**		

- **Course Learning objectives:**
- To understand the STA Environment and concepts.
- To know standard cell library with timing model and delay model.
- To study delay calculations and timing verification concepts of combinational and sequential circuits.

Note: This Laboratory can be conducted using industry standard EDA tool like Cadence, Synopsis VLSI Tool

Sl.NO	Experiments
1	Read the Library, report cells by constraint the design not to use OAI and AOI design also avoid using high capacitance cells.
2	Declaring Ideal Clocks for four bit counter with multiple frequency (Single Clock Domains) a) 10 MHZ b) 50 MHZ Run the design by setting the each clock -Report Slack w.r.t each clock -Report the timing, for each clock
3	Modelling Clock Jitter, Clock Skew and other effects for four-bit counter with 10 MHZ frequency - Run design setting clockk jitter and Skew -Report the timing
4	Net Delay and Buffer Insertion a) Study the impact of interconnect resistance and capacitance on signal delay. b) Use EDA tool to simulate and measure net delay in a simple digital circuit. c) Implement buffer insertion to reduce delay in the critical path.
5	Clock Skew and its effect on Timing a) Analyze clock skew in a flip-flop-based design. b) Measure clock arrival times at different flip-flops.
6	Setup and Hold Time Analysis in a 4-bit Counter a) Perform setup and hold time analysis on a 4-bit binary counter. b) Modify the design and evaluate how changes in clock speed affect setup and hold violations.

	c) Apply timing constraints and analyze the effect on violations.
7	Identifying and Resolving Setup Violations in a Register File a) Run STA on an 8-bit register file design to detect setup violations. b) Investigate the root cause of violations and optimize the design to resolve them. c) Apply appropriate timing constraints to ensure proper operation.
8	Critical Path Identification in a Ripple Carry Adder a) Use EDA tool to identify the longest delay path in a ripple carry adder (RCA). b) Measure the impact of optimization on the design's critical path delay.
9	Multi-Cycle Path Constraints in a 2-Stage Pipeline a) Write and apply multi-cycle path constraints to a pipelined design. b) Analyze the impact of multi-cycle constraints on timing margins and performance. c) Verify timing violations are resolved using EDA Tool.
10	False Path Analysis Using a Multiplexer Circuit a) Identify false paths in a MUX-based control circuit using EDA Tool b) Exclude false paths from STA by applying false path constraints in the SDC file. c) Verify that false paths no longer appear in the timing report.
11	Writing Clock Constraints for a Dual-Clock Domain System a) Write clock constraints for a system with two clock domains operating at different frequencies. b) Define the clock period, uncertain edges, and relationship between the clocks using SDC. c) Verify the correct timing behaviour of the system using EDA Tool.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

- Evaluate the delay of any given digital circuits
- Setup the resources to perform the static timing analysis using EDA tool.
- Prepare timing constraints for the design based on the required specification.
- Generate the timing analysis report using EDA tool for different checks.
- Perform verification and analyse the generated report to identify critical issues and bottleneck for the violation and suggest the techniques to make the design to meet required timing

Suggested Learning Resources:

Bhasker,R Chadha, "Static Timing Analysis for Nanometer Designs: APracticalApproach", Springer2009.

System Modelling using Simulink		Semester	5
Course Code	**BEC657B**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:0:2:0	SEE Marks	50
Credits	01	Total SEE+CIE	100
		Exam Hours	2 Hours
Examination type (SEE)	**Practical**		

Course objectives:

- Understand the basics of MATLAB Simulink used for engineering applications
- Simulation of the trigonometric functions and display of signals.
- Implementations of analog and digital systems using Simulink.
- Implement digital logic circuits using Simulink and display the output.
- Simulation of the analog and digital communication systems using Simulink.

Sl.NO	Experiments
1	a) Generate the following signals using Simulink and display these signals on a single scope with separate inputs. i) sinusoidal signal, ii)square signal, iii) sawtooth signal, and iv) random signal b) Perform the following operations using simulink and display the output. i) y(t) = sin2t, ii) y(t) = $\frac{d(sin2t)}{dt}$, iii)y(t) = $\int sin2t$
2	Solve the second order differential equations shown below using Simulink and display the output. i) $\frac{d^2y}{dt^2} + 2\frac{dy}{dt} + 5y = 1$ ii) $\frac{d^2y}{dt^2} + 3\frac{dy}{dt} + 4y = 5\cos 2t$
3	Design and realize the second order low pass and high pass RC filters using Simulink.
4	Design a BCD adder and use Simulink to simulate and verify its operation.
5	Design and Simulate the following using Simulink and verify its operation. a) 3–bit Up / Down Counter, b) 4–bit Ring Counter
6	Design and simulate the 4x1 Multiplexer and 1x4 Demultiplexer using Simulink
7	Find the step response of the following system functions given below, using Simulink. i) Continuous transfer function H(s) = $\frac{5(s+2)}{s(2s^2+4s+3)}$ ii) Discrete transfer function H(z) = $\frac{z^2-1.2z+1}{z^3-1.3z^2+z-0.2}$
8	Realize the FIR filter given by the impulse response h(n) = {0.08, 0.21,0.54, 0.86, 1, 0.86, 0.54, 0.21 0.08) using Simulink. Obtain the frequency response characteristics.

9	Simulate the Amplitude Modulation and Demodulation using Simulink. Display the output signal and its spectrum.
10	Simulate the modulation & demodulation of a random binary data stream using QPSK using Simulink. Display the output signal and its spectrum.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

- Create Simulink models to perform analog and digital computations.
- Implement the Combinational Digital circuits and Sequential Digital Circuit models using Simulink.
- Implement analog and digital systems using the transfer functions in s-domain and z-domain respectively.
- Demonstration of analog and digital communication modulation and demodulation using Simulink.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation (CIE):

CIE marks for the practical course are **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment is to be evaluated for conduction with an observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments are designed by the faculty who is handling the laboratory session and are made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled down to **30 marks** (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct a test of 100 marks after the completion of all the experiments listed in the syllabus.
- In a test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- The marks scored shall be scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and marks of a test is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

- SEE marks for the practical course are 50 Marks.
- **SEE shall be conducted by the two examiners. One from the same institute as an internal examiner and another from a different institute as an external examiner, appointed by the university.**
- The examination schedule and names of examiners are informed to the university before the conduction of the examination. These practical examinations are to be conducted between the schedule mentioned in the academic calendar of the University.
- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be

strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

- Students can pick one question (experiment) from the questions lot prepared by the examiners jointly.
- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% of Marks allotted to the procedure part are to be made zero.

The minimum duration of SEE is 02 hours

Suggested Learning Resources:

1. Steven T. Karris, "Introduction to Simulink® with Engineering Applications", Orchard Publications, 2011, ISBN : 978-1934404218
2. Devendra K. Chaturvedi, "Modeling and Simulation of Systems Using MATLAB and Simulink", CRC Press Taylor & Francis Group, 2010, ISBN 9780815351382

IoT (Internet of Things) Lab		Semester	6
Course Code	BECL657C	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:0:2:0	SEE Marks	50
Credits	01	Exam Hours	3
Examination type (SEE)	Practical		

Course Objectives:

This course will enable students to

- To impart necessary and practical knowledge of components of the Internet of Things
- To develop skills required to build real-life IoT-based projects.

Sl.No.	Experiments
1(i)	To interface LED/Buzzer with Arduino /Raspberry Pi and write a program to 'turn ON' LED for 1 sec after every 2 seconds.
1(ii)	To interface the Push button/Digital sensor (IR/LDR) with Arduino /Raspberry Pi and write a program to 'turn ON' LED when a push button is pressed or at sensor detection.
2 (i)	To interface the DHT11 sensor with Arduino /Raspberry Pi and write a program to print temperature and humidity readings.
2(ii)	To interface OLED with Arduino /Raspberry Pi and write a program to print its temperature and humidity readings.
3	To interface the motor using a relay with Arduino /Raspberry Pi and write a program to 'turn ON' the motor when a push button is pressed.
4(i)	Write an Arduino/Raspberry Pi program to interface the Soil Moisture Sensor.
4(ii)	Write an Arduino/Raspberry Pi program to interface the LDR/Photo Sensor.
5	Write a program to interface an Ultrasonic Sensor with Arduino /Raspberry Pi.
6	Write a program on Arduino/Raspberry Pi to upload temperature and humidity data to _thingspeak cloud.
7	Write a program on Arduino/Raspberry Pi to retrieve temperature and humidity data from _thingspeak _cloud.
8	Write a program to interface LED using Telegram App.
9	Write a program on Arduino/Raspberry Pi to publish temperature data to the MQTT broker.
10	Write a program to create a UDP server on Arduino/Raspberry Pi and respond with humidity data to the UDP client when requested.
11	Write a program to create a TCP server on Arduino /Raspberry Pi and respond with humidity data to the TCP client when requested.
12	Write a program on Arduino / Raspberry Pi to subscribe to the MQTT broker for temperature data and print it.

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

- Explain the Internet of Things and its hardware and software components.
- Interface I/O devices, sensors & communication modules.
- Remotely monitor data and control devices.

- Develop real-life IoT-based projects.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation (CIE):

CIE marks for the practical course are **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment will be evaluated for conduction with an observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments are designed by the faculty who is handling the laboratory session and are made known to students at the beginning of the practical session.
- The record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- The total marks scored by the students are scaled down to **30 marks** (60% of maximum marks).
- Weightage is to be given for neatness and submission of record/write-up on time.
- The department shall conduct a test of 100 marks after the completion of all the experiments listed in the syllabus.
- In a test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- The marks scored shall be scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and marks of a test is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

- SEE marks for the practical course are 50 Marks.
- **SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the Head of the Institute**.
- The examination schedule and names of examiners are informed to the university before the conduction of the examination. These practical examinations are to be conducted within the schedule mentioned in the university's academic calendar.
- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.
- Students can pick one question (experiment) from the questions lot prepared by the examiners jointly.
- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% of Marks allotted to the procedure part are to be made zero.

The minimum duration of SEE is 02 hours

Suggested Learning Resources:

- Vijay Madisetti, Arshdeep Bahga, Internet of Things. "A Hands-on Approach", University Press
- Dr. SRN Reddy, Rachit Thukral, and Manasi Mishra, "Introduction to Internet of Things: A Practical Approach", ETI Labs
- Pethuru Raj and Anupama C Raman, "The Internet of Things: Enabling Technologies, Platforms, and Use Cases", CRC Press
- Jeeva Jose, "Internet of Things", Khanna Publishing House, Delhi
- Adrian McEwen, "Designing the Internet of Things", Wiley
- Raj Kamal, "Internet of Things: Architecture and Design", McGraw Hill

Python Programming for Machine Learning Applications		Semester	6
Course Code	BECL657D	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:0:2:0	SEE Marks	50
Credits	01	Exam Hours	3
Examination type (SEE)	Practical		

Course Objectives:

This course will enable students to

- To impart necessary and practical knowledge Machine Learning Algorithms
- To develop skills required to build real-life ML Algorithm projects.

Sl.No.	Experiments
1	Solve the Tic-Tac-Toe problem using the Depth First Search technique.
2	Show that the 8-puzzle states are divided into two disjoint sets, such that any state is reachable from any other state in the same set, while no state is reachable from any state in the other set.
3	To represent and evaluate different scenarios using predicate logic and knowledge rules.
4	To apply the Find-S and Candidate Elimination algorithms to a concept learning task and compare their inductive biases and outputs.
5	To construct a decision tree using the ID3 algorithm on a simple classification dataset
6	To assess how the ID3 algorithm performs on datasets with varying characteristics and complexity, examining overfitting, underfitting, and decision tree depth.
7	To examine different types of machine learning approaches (Supervised, Unsupervised, Semi-supervised, and Reinforcement Learning) by setting up a basic classification problem and exploring how each type applies differently
8	To understand how Find-S and Candidate Elimination algorithms search through the hypothesis space in concept learning tasks, and to observe the role of inductive bias in shaping the learned concept.
9	To go through all stages of a real-life machine learning project, from data collection to model fine-tuning, using a regression dataset like the "California Housing Prices."
10	To perform binary and multiclass classification on the MNIST dataset, analyze performance metrics, and perform error analysis.
11	**Demo experiments**
12	Demo experiments

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

- Apply machine learning algorithms to real life problems.
- Able to make use of different machine learning approaches.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation (CIE):

CIE marks for the practical course are **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment will be evaluated for conduction with an observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments are designed by the faculty who is handling the laboratory session and are made known to students at the beginning of the practical session.
- The record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- The total marks scored by the students are scaled down to **30 marks** (60% of maximum marks).
- Weightage is to be given for neatness and submission of record/write-up on time.
- The department shall conduct a test of 100 marks after the completion of all the experiments listed in the syllabus.
- In a test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- The marks scored shall be scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and marks of a test is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

- SEE marks for the practical course are 50 Marks.
- **SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the Head of the Institute**.
- The examination schedule and names of examiners are informed to the university before the conduction of the examination. These practical examinations are to be conducted within the schedule mentioned in the university's academic calendar.
- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.
- Students can pick one question (experiment) from the questions lot prepared by the examiners jointly.
- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%,

Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% of Marks allotted to the procedure part are to be made zero.

The minimum duration of SEE is 02 hours

Suggested Learning Resources:

Text Book:

1. Stuart J. Russell and Peter Norvig , Artificial Intelligence, 3rd Edition, Pearson,2015

2. Elaine Rich, Kevin Knight, Artificial Intelligence, 3rd Edition,Tata McGraw Hill,2013.

3. Tom M. Mitchell, Machine Learning, McGraw-Hill Education, 2013

4. AurelienGeron, Hands-on Machine Learning with Scikit-Learn &Tensor Flow , O'Reilly, Shroff Publishers and Distributors Pvt. Ltd 2019.