**Semester - VII**

| PRINCIPLES OF AI and ML | | | |
|---|---|---|---|
| Course Code | **BUE701** | CIE Marks | 50 |
| Teaching Hours/Week (L:P:SDA) | 3:0:2 | SEE Marks | 50 |
| Total Hours of Pedagogy | 40 hours Theory + 10-12 Lab slots | Total Marks | 100 |
| Credits | 04 | Exam Hours | 03 |

**Course objectives:**

- To understand the main approaches to Artificial intelligence, Machine learning
- To Analyse and interpret data using AI techniques.
- To Design and implement AI-powered applications that meet specific requirements.

**MODULE-1**

**Introduction to Artificial Intelligence:** Introduction, what is AI, Strong Methods and weak Methods. Uses and Limitations:

**Knowledge Representation:** Need for good representation, semantic nets, Frames, , Search Spaces, Semantics Tress, Search Trees, Combinatorial Explosion, Problem reduction, Goal Trees, Combinatorial Explosion.

**RBT Levels:** L1, L2

**MODULE-2**

**Search Methodologies:** Introduction, Problem solving as search, Data driven or goal driven search, Generate and test, Properties of search methods, Depth First Iterative Deepening, Using Heuristics for Search, Hill Climbing, Best-First Search, Identifying Optimal Paths, Constraint Satisfaction search, Forward Checking, Local Search and Meta heuristics, Simulated Annealing. Genetic Algorithms for search, Real time A*, Bidirectional search, Nondeterministic search, non-chronological backtracking.

**RBT Levels:** L1, L2

**MODULE-3**

**Game Playing:** Game Trees, Minimax, Alpha beta pruning.

**Prepositional and Predicate Logic:** Introduction, what is Logic, Why Logic is used in Artificial Intelligence, Logical Operators, translating between English and Logic Notation, The deduction Theorem, Soundness, Completeness, Decidability, Monotonicity, Abduction and Inductive reasoning, Modal logics and possible worlds, Dealing with change.

**Inference and Resolution for Problem Solving:** Introduction, Resolution in prepositional logic: Applications of Resolution, Resolution in Predicate Logic, Normal forms for predicate logic, Skolemization, Resolution Algorithms, Resolution for problem solving.

**RBT Levels:** L2, L3

**MODULE-4**

**Introduction to Machine Learning:** Introduction, Training Rote Learning, Learning Concepts, General-to-Specific Ordering, Version Spaces, Candidate Elimination, Inductive Bias, Decision-Tree Induction, The Problem of Overfitting, The Nearest Neighbor Algorithm, Backpropagation algorithms, Reinforcement Learning.

**Neural Networks:** Introduction, Neurons, Perceptrons, Multilayer Neural Networks, Recurrent Networks, Unsupervised Learning Networks, Evolving Neural Networks.

**RBT Levels:** L2, L3

**MODULE 5**

**Probabilistic Reasoning and Bayesian Belief Networks:** Introduction, Probabilistic Reasoning, Joint Probability Distributions, Bayes' Theorem, Simple Bayesian Concept Learning, Bayesian Belief Networks, The Noisy-V Function, Bayes' Optimal Classifier, The Naïve Bayes Classifier.

**RBT Levels:** L2, L3

**PRACTICAL COMPONENT OF IPCC** *(May cover all / major modules)*

| Sl. No. | Experiments |
|---|---|
| 1 | Implement DFID algorithm and compare its performance with DFS and BFS algorithm |
| 2 | Implement Best-First Search algorithm |
| 3 | Implementation of AND/OR/NOT Gate using single layer perceptron. |
| 4 | Implementation of XOR Gate using<br>a) Multi-layer perceptron/Error back propagation<br>b) Radial Basis Function Network |
| 5 | Implement Hebbian learning rule and Correlation learning rule. |
| 6 | Implement Find-S and candidate elimination algorithms. |
| 7 | Build a linear regression model housing prices. |
| 8 | Implement spam detection using Naïve Bayes Algorithm. |
| 9 | Implement hand writing classification using Support Vector Machines. |
| 10 | Implement FP-tree for finding co-occurring words in a twitter feed. |

**Assessment Details (both CIE and SEE):**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

The IPCC means the practical portion integrated with the theory of the course. CIE marks for the theory component are **25 marks** and that for the practical component is **25 marks**.

**CIE for the theory component of the IPCC:**

- 25 marks for the theory component are split into **15 marks** for two Internal Assessment Tests (Two Tests, each of 15 Marks with 01-hour duration, are to be conducted) and **10 marks** for other assessment methods mentioned in 22OB4.2. The first test at the end of 40-50% coverage of the syllabus and the second test after covering 85-90% of the syllabus.
- Scaled-down marks of the sum of two tests and other assessment methods will be CIE marks for the theory component of IPCC (that is for **25 marks)**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the theory component of IPCC.

**CIE for the practical component of the IPCC:**

- **15 marks** for the conduction of the experiment and preparation of laboratory record, and **10 marks** for the test to be conducted after the completion of all the laboratory sessions.
- On completion of every experiment/program in the laboratory, the students shall be evaluated including viva-voce and marks shall be awarded on the same day.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to **15 marks**.

- The laboratory test **(duration 02/03 hours)** after completion of all the experiments shall be conducted for 50 marks and scaled down to **10 marks.**
- Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **25 marks**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the practical component of the IPCC.

**SEE for IPCC:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored by the student shall be proportionally scaled down to 50 Marks.

**The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper may include questions from the practical component**.

- The minimum marks to be secured in CIE to appear for SEE shall be 10 (40% of maximum marks-25) in the theory component and 10 (40% of maximum marks-25) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included**.** The maximum of 04/05 sub-questions are to be set from the practical component of IPCC, the total marks of all questions should not be more than 20 marks.
- SEE will be conducted for 100 marks and students shall secure 35% of the maximum marks to qualify for the SEE. Marks secured will be scaled down to 50.
- The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Suggested Learning Resources:**

**Text Books**


1. Ben Coppin, Artificial Intelligence Illuminated, Jones and Bartlett, 2004.
2. Tom M. Mitchell, "Machine Learning", Mcgraw-Hill Education (Indian Edition), 2013.


**Reference Books**


1. Elaine Rich Kevin Knight, Shivashankar B Nair: Artificial Intelligence, Tata McGraw Hill 3rd edition 2013.
2. Stuart Russel, Peter Norvig: Artiificial Intelligence A Modern Approach, Pearson 3rd edition 2013.
3. Ethem Alpaydin, "Introduction to Machine Learning", 2nd Edition, PHI Learning Pvt. Ltd., 2013.
4. T Hastie, R. Tibshirani, J.H.Fiedman, "The Elements of statistical learning", Springer, 1st Edition 2001.


**Web links and Video Lectures (e-Resources):**

- **Kaggle:** https://www.kaggle.com/
- **OpenAI:** https://openai.com/
- **TensorFlow:** https://www.tensorflow.org/
- **Scikit-learn:** https://scikit-learn.org/
- **Keras:** https://keras.io/
- https://nptel.ac.in/

**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

- Create a debate on the ethical implications of strong AI.
- Implement different search algorithms to solve classic AI problems like the 8-puzzle or the traveling salesman problem.
- Build a simple machine learning model using a drag-and-drop interface.

**Course outcome (Course Skill Set)**

At the end of the course the student will be able to :

| Sl. No. | Description | Blooms Level |
|---|---|---|
| CO1 | Students will be able to explain the limitations and challenges associated with AI techniques. | 2 |
| CO2 | Students will be able to apply AI concepts to solve real-world problems, such as game playing, problem-solving using search algorithms, and building intelligent systems. | 3 |
| CO3 | Students will be able to analyse the strengths and weaknesses of different AI approaches and choose the most appropriate method for a given task. | 4 |

**Semester - VII**

| SystemVerilog | | | |
|---|---|---|---|
| Course Code | **BUE702** | CIE Marks | 50 |
| Teaching Hours/Week (L:P:SDA) | 3:0:2 | SEE Marks | 50 |
| Total Hours of Pedagogy | 40 hours Theory + 10-12 Lab slots | Total Marks | 100 |
| Credits | 04 | Exam Hours | 03 |

**Course objectives:**

- Understand Digital System Verification Using Object Oriented Methods
- Learn the System Verilog Language for Digital System Verification.
- Create/Build Test Benches for the Design/Methodology.
- Use Constrained Random Tests for Verification
- Understand Concepts of Functional Coverage.

**MODULE-1**

**Verification Guidelines:** The Verification Process, Basic Test Bench Functionality, Directed Testing, Methodology Basics, Constrained Random Stimulus, Randomization, Functional Coverage, Test Bench Components, Layered Test Bench.

**Data Types**: Built-In Data Types, Fixed and Dynamic Arrays, Queues, Associative Arrays, Linked Lists, Array Methods, Choosing A Storage Type, Creating New Types With typedef, Creating User Defined Structures, Type Conversion, EnumeratedTypes, Constants and Strings, Expression Width.

**RBT Levels:** L2, L3

**MODULE-2**

**Procedural Statements and Routines**: Procedural Statements, Tasks, Functions and Void Functions, Task and Function Overview, Routine Arguments, Returning from a Routine, Local Data Storage, Time Values.

**Connecting the Test Bench and Design**: Separating the Test Bench and Design, The Interface Construct, Stimulus Timing, Interface Driving and Sampling, System Verilog Assertions.

**RBT Levels:** L2, L3

**MODULE-3**

**Randomization**: Introduction, Randomization in System Verilog, Constraint Details, Solution Probabilities, Valid Constraints, InLine Constraints, Random Number Functions, Common Randomization Problems, Random Control, Random Number Generators.

**RBT Levels:** L3

**MODULE-4**

**Threads and Inter process Communication**: Working with Threads, Disabling Threads, Inter Process Communication, Events, Semaphores, Mailboxes, Building A Test Bench with Threads and InterProcess Communication.

**RBT Levels:** L3

**MODULE 5**

**Functional Coverage:** Coverage Types, Functional Coverage Strategies, Simple Functional Coverage Example, Anatomy of Cover Group, Triggering a Cover Group, Data Sampling, Cross Coverage, Generic Cover Groups, Coverage Options, Analyzing Coverage Data, MeasuringCoverage Statistics During Simulation.

**RBT Levels:** L3, L4

**PRACTICAL COMPONENT OF IPCC** *(May cover all / major modules)*

| Sl. No. | Experiments |
|---|---|
| 1 | (a) Write a SV code to demonstrate 2-state and 4-state data types.<br>(b) Write a SV code to demonstrate the difference between bit and byte.<br>(c) Write a SV code to demonstrate the difference between int and integer. |
| 2 | (a) Write a SV code to demonstrate for and foreach loops for multidimensional arrays.<br>(b) Write a SV code to demonstrate packed and unpacked array. |
| 3 | (a) Write a SV code to implement a module to store and display a list of student grades using a dynamic array.<br>(b) Develop a module that maps product names to their prices using associative array. |

| | |
|---|---|
| | (c) Write a SV code to demonstrate all the Queue operations. |
| 4 | (a) Write a SV code to demonstrate break and continue statements.<br>(b) Develop a module to demonstrate Tasks, Functions and Void Function. |
| 5 | (a) Write a SV code to demonstrate rand and randc with random class.<br>(b) Write a constraint for removing duplicate elements from queue.<br>(c) Write a constraint to generate even numbers between 10 to 30. |
| 6 | (a) Write a constraint to arrange the initial numbers in ascending order and remaining numbers in descending order.<br>(b) Write a constraint to generate a sequence of 9 99 999 9999 99999. |
| 7 | (a) Write a constraint to generate:<br>• A queue with unique value.<br>• Store a even number at the index of the odd value.<br>• Store a odd number at the index of the even value.<br>(b) Write a constraint to generate a pattern of 000111222333444555. |
| 8 | (a) Demonstrate fork-join, for-join-any, fork-join-none using suitable SV code.<br>(b) Develop module of the mailbox connecting two transactors. |
| 9 | **Demo Experiment -** Demonstrate complete SV design that incorporates the entire SystemVerilog environment for simple digital circuit. |
| 10 | **Demo Experiment –** Demonstrate simple protocol through the SV environment. |

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- Scaled-down marks of the sum of two tests and other assessment methods will be CIE marks for the theory component of IPCC (that is for **25 marks)**.
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**CIE for the practical component of the IPCC:**

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- Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of

IPCC for **25 marks**.

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- SEE will be conducted for 100 marks and students shall secure 35% of the maximum marks to qualify for the SEE. Marks secured will be scaled down to 50.
- The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Suggested Learning Resources:**

**Books**


1. Chris Spear, "System Verilog for Verification – A guide to learning the Test bench language features", Springer Publications Second Edition, 2010.
2. Stuart Sutherland, Simon Davidmann, Peter Flake, "System Verilog for Design- A guide to using system Verilog for Hardware design and modelling", Springer Publications Second Edition, 2006.


**Web links and Video Lectures (e-Resources):**

- https://nptel.ac.in/

**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

- Interact with industry (small, medium, and large).
- Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
- Involve in case studies and field visits/ fieldwork.
- Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
- Handle advanced instruments to enhance technical talent.
- Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
- Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

**Course outcome (Course Skill Set)**

At the end of the course the student will be able to:

| Sl. No. | Description | Blooms Level |
|---|---|---|
| CO1 | Apply the SystemVerilog concepts to verify the design. | L3 |
| CO2 | Apply constrained random tests benches using SystemVerilog. | L3 |
| CO3 | Appreciate Functional Coverage. | L3, L4 |

**VII Semester**

| COMPUTER GRAPHICS AND IMAGE PROCESSING | | | |
|---|---|---|---|
| Course Code | **BUE703** | CIE Marks | 50 |
| Teaching Hours/Week (L:T:P: S) | 4:0:0:0 | SEE Marks | 50 |
| Total Hours of Pedagogy | 50 | Total Marks | 100 |
| Credits | 04 | Exam Hours | 03 |

**Course Learning Objectives:** This course will enable students to:

CLO 1. Overview of Computer Graphics along with its applications.

CLO 2. Exploring 2D and 3D graphics mathematics along with OpenGL API's.

CLO 3. Use of Computer graphics principles for animation and design of GUI's .

CLO 4. Introduction to Image processing and Open CV.

CLO 5. Image segmentation using Open CV.

**Teaching-Learning Process (General Instructions)**

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

1. Lecturer method (L) need not to be only traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes.
2. Use of Video/Animation to explain functioning of various concepts.
3. Encourage collaborative (Group Learning) Learning in the class.
4. Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyse information rather than simply recall it.
6. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
7. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

**Module-1**

**Overview:** Computer Graphics hardware and software and OpenGL: Computer Graphics: Video Display Devices, Raster-Scan Systems Basics of computer graphics, Application of Computer Graphics. OpenGL: Introduction to OpenGL, coordinate reference frames, specifying two-dimensional world coordinate reference frames in OpenGL, OpenGL point functions, OpenGL line functions, point attributes, line attributes, curve attributes, OpenGL point attribute functions, OpenGL line attribute functions, Line drawing algorithms (DDA, Bresenham's).

**RBT Levels:** L1, L2

**Module-2**

**2D and 3D graphics with OpenGL:** 2D Geometric Transformations: Basic 2D Geometric Transformations, matrix representations and homogeneous coordinates, 2D Composite transformations, other 2D transformations, raster methods for geometric transformations, OpenGL raster transformations, OpenGL geometric transformations function, 3D Geometric Transformations: Translation, rotation, scaling, composite 3D transformations, other 3D transformations, OpenGL geometric transformations functions.

**3D Geometric Transformations:** Translation, rotation, scaling, composite 3D transformations, other 3D transformations, OpenGL geometric transformations functions.

**RBT Levels:** L1, L2

**Module-3**

**Interactive Input Methods and Graphical User Interfaces:** Graphical Input Data, Logical Classification of Input Devices, Input Functions for Graphical Data , Interactive Picture-Construction Techniques, Virtual-Reality Environments, OpenGL Interactive Input-Device Functions, OpenGL Menu Functions , Designing a Graphical User Interface.

**Computer Animation:** Design of Animation Sequences, Traditional Animation Techniques, General Computer-Animation Functions, Computer-Animation Languages, Character Animation, Periodic Motions, OpenGL Animation Procedures.

**RBT Levels:** L1, L2

**Module-4**

**Introduction to Image processing:** overview, Nature of IP, IP and its related fields, Digital Image representation, types of images. Digital Image Processing Operations: Basic relationships and distance metrics, Classification of Image processing Operations.

**RBT Levels:** L2, L3

**Module-5**

**Image Segmentation:** Introduction, classification, detection of discontinuities, Edge detection (up to canny edge detection (included), Thresholding, Region-Based Segmentation.

**RBT Levels:** L2, L3

**Course Outcomes:**

At the end of the course the student will be able to:

- CO 1. Construct geometric objects using Computer Graphics principles and OpenGL APIs.
- CO 2. Use OpenGL APIs and related mathematics for 2D and 3D geometric Operations on the objects.
- CO 3. Design GUI with necessary techniques required to animate the created objects
- CO 4. Apply OpenCV for developing Image processing applications.
- CO5. Apply Image segmentation techniques along with programming, using OpenCV.

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous Internal Evaluation:**

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

**Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester-End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.

Marks scored shall be proportionally reduced to 50 marks.

**Suggested Learning Resources:**

**Textbooks**


1. Donald D Hearn, M Pauline Baker and Warren Carithers: Computer Graphics with OpenGL 4th Edition, Pearson, 2014
2. S. Sridhar, Digital Image Processing, second edition, Oxford University press 2016.


**Reference Books**


1. Edward Angel: Interactive Computer Graphics- A Top Down approach with OpenGL, 5th edition. Pearson Education, 2008.
2. James D Foley, Andries Van Dam, Steven K Feiner, John F Huges Computer graphics with OpenGL: Pearson education.

| **Web links and Video Lectures (e-Resources):** |
| --- |
| • https://nptel.ac.in/ |

| Low Power VLSI Design | | Semester | VII |
|---|---|---|---|
| Course Code | **BUE714A** | CIE Marks | 50 |
| Teaching Hours/Week (L:T:P: S) | 3:0:0:0 | SEE Marks | 50 |
| Total Hours of Pedagogy | 40 | Total Marks | 100 |
| Credits | 03 | Exam Hours | 3 Hours |
| Examination type (SEE) | **Theory** | | |

**Course objectives:**

- To study State-of-the art approaches of power estimation and reduction.
- To understand power dissipation at various levels of design
- To measure the performance of power dissipation in various Circuits.

**Teaching-Learning Process (General Instructions)**

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Chalk and Talk
2. PowerPoint Presentation and Videos
3. Flipped Classes
4. Practice session

**Module-1**

**Introduction:** Needs for Low Power VLSI Chips, Charging and Discharging Capacitance, Short-circuit Current in CMOS Circuit, CMOS Leakage Current, Static Current, Basic Principles of Low Power Design, Low Power Figure of Merits

**Simulation Power Analysis:** SPICE Basics, SPICE Power Analysis

**RBT Level: L1, L2**

**Module-2**

**Simulation Power Analysis:** Discrete Transistor Modeling and Analysis, Gate-level Logic Simulation, Architecture-level Analysis, Data Correlation analysis in DSP system

**Probabilistic Power Analysis:** Random Logic Signals, Probabilistic Power Analysis Techniques, Signal Entropy

**RBT Level: L1, L2**

**Module-3**

**Circuit:** Transistor and Gate Sizing, Equivalent Pin Ordering, Network Restructuring and Reorganization, Special Latches and Flip-flops, Low Power Digital Cell Library, Adjustable Device Threshold Voltage

**RBT Level: L1, L2**

**Module-4**

**Logic:** Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic.

**Special Techniques:** Power Reduction in Clock Networks: Clock Gating, Reduced Swing Clock, Oscillator Circuit for Clock Generation, Frequency Division and Multiplication, Other Clock Power Reduction Techniques.

**RBT Level: L2, l3**

**Module-5**

**Special Techniques** :CMOS Floating Node, Low Power Bus, Delay Balancing, Low Power Techniques for SRAM: SRAM Cell, Memory Bank Partitioning, Pulsed Wordline and Reduced Bitline Swing

**Low power Clock Distribution:** Power dissipation in clock distribution, single driver Vs distributed buffers: Clock driving schemes**,** Buffer Insertion in clock tree**,** Zero skew vs Tolerable skew**:** Derivation of Tolerable skew**,** A two level clock distribution scheme**,** Chip package Co-design of clock network.

**RBT Level: L2, L3**

**Course outcome (Course Skill Set)**

At the end of the course, the student will be able to :

1. Identify the sources of power dissipation in CMOS circuits.
2. Perform power analysis using simulation-based approaches and probabilistic analysis
3. Use optimization and trade-off techniques that involve power dissipation of digital circuits.
4. Use special power reduction techniques in SRAM memory cell.
5. Use practical low power design techniques and their analysis at various levels of design abstraction and analyse how these are being captured in the latest design automation environments.

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous Internal Evaluation:**

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

**Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

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Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

**Suggested Learning Resources:**

**TEXTBOOKS**


1. Gary K. Yeap, "Practical Low Power Digital VLSI Design", Kluwer Academic, 1998
2. Jan M. Rabaey, Massoud Pedram, "Low Power Design Methodologies", Kluwer Academic, 2010.


**REFERENCE BOOK(s):**


1. Kaushik Roy, Sharat Prasad, "Low-Power CMOS VLSI Circuit Design" Wiley, 2000
2. P. Chandrasekaran and R. W. Broadersen, "Low power digital CMOS design", Kluwer Academic,1995.
3. A Bellamour and M I Elmasri, "Low power VLSI CMOS circuit design", Kluwer Academic,1995.

| **Web links and Video Lectures (e-Resources):** |
| --- |
| • https://nptel.ac.in/courses |
| **Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**<br>• Quiz<br>• Seminars |

| RISK -V Processor | | Semester | VII |
|---|---|---|---|
| Course Code | **BUE714B** | CIE Marks | 50 |
| Teaching Hours/Week (L:T:P: S) | 3:0:0:0 | SEE Marks | 50 |
| Total Hours of Pedagogy | 40 | Total Marks | 100 |
| Credits | 03 | Exam Hours | 3 Hours |
| Examination type (SEE) | **Theory** | | |

**Course objectives:**

**This course will enable students to:**

- To understand various operands instructions of RISK-V Processor.
- To know the RISK-V Processor architecture.
- To understand the register architecture and addressing modes.
- Analyse the difference between Arrays and Pointers.
- To learn about the RISK-V architecture, instruction set, and ecosystem.

**Teaching-Learning Process (General Instructions)**

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Chalk and Talk.
2. Power Presentation and Videos.
3. Flipped Classes.
4. Practice Sessions.

**Module-1**

**Instructions Language of the Computer:** Introduction , Operations of the Computer: Hardware, Operands of the Computer Hardware: Memory Operands, Constant or Immediate Operands, Signed and Unsigned Numbers.

**RBT Level:**L1,L2

**Module-2**

**Representing Instructions in the Computer:** RISC-V Fields, Logical Operations, Instructions for Making Decisions: Loops, Bounds Check Shortcut, Case/Switch Statement, Supporting Procedures in Computer Hardware: Using More Registers, Nested Procedures, Allocating Space for New Data on the Stack.

**RBT Level:** L1,L2

**Module-3**

**Allocating Space for New Data on the Heap:** Communicating with People, Characters and Strings in Java, RISC-V Addressing for Wide Immediates and Addresses: Wide Immediate Operands, Addressing in Branches**,** Decoding Machine Language, Parallelism and Instructions: Synchronization, Translating and Starting a Program, Compiler, Assembler, Linker.

**RBT Levels:** L1,L2

**Module-4**

**Parallelism and Instructions:** Loader , Dynamically Linked Libraries, Starting a Java Program, A C Sort Example to Put it All Together: The Procedure swap, The Procedure sort , Arrays versus Pointers: Array Version of Clear, Pointer Version of Clear**,** Comparing the Two Versions of Clear**,** Advanced Material: Compiling C and Interpreting Java, Advanced Material: Compiling C and Interpreting Java: Compiling C, The Front End, High-Level Optimizations.

**RBT Levels:** L2,L3

**Module-5**

**Local and Global Optimizations:** Register Allocation**,** Code Generation**,** Interpreting Java, Interpretation, Compiling for Java, Invoking Methods in Java, A Sort Example in Java, MIPS Instructions.

**RBT Levels:** L2,L3

**Course outcome (Course Skill Set)**

At the end of the course, the student will be able to :

**CO1:** Understand the basic hardware of computers and their different operations.

**CO2:** Describe the different fields of RISK V processor and instructions.

**CO3:** Apply and use Programming Techniques for different End Uses

**CO4:** Describe the code design process Java and C interpretation.

**CO5:** Understand the local and global optimization from high level uses.

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous Internal Evaluation:**

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

**Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester-End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

**Suggested Learning Resources:**

**Books**

1. "CMOS VLSI Design- A Circuits and Systems Perspective"- Neil H.E. Weste, David Harris, Ayan Banerjee, 3rd Edition, Pearson Education.
2. "CMOS Digital Integrated Circuits Analysis and Design"-Sung-Mo Kang, Yusuf Leblebici, 3rd Edition.

**Web links and Video Lectures (e-Resources):**

- nptel.ac.in

**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

- Quiz
- Seminar
- Assignments

| CLOUD COMPUTING | | Semester | VII |
|---|---|---|---|
| Course Code | **BUE714C** | CIE Marks | 50 |
| Teaching Hours/Week (L:T:P: S) | 3:0:0 | SEE Marks | 50 |
| Total Hours of Pedagogy | 40 | Total Marks | 100 |
| Credits | 03 | Exam Hours | 3 Hours |
| Examination type (SEE) | **Theory** | | |

**Course objectives:**

- Introduce the rationale behind the cloud computing revolution and the business drivers.
- Introduce various models of cloud computing
- Introduction on how to design cloud native applications, the necessary tools and the design tradeoffs.
- Realize the importance of Cloud Virtualization, Abstraction`s and Enabling Technologies and cloud security.

**Teaching-Learning Process (General Instructions)**

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecturer method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
2. Show Video/animation films to explain functioning of various concepts.
3. Encourage collaborative (Group Learning) Learning in the class.
4. Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Topics will be introduced in a multiple representation.
7. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

**Module-1**

**Introduction:** Introduction ,Cloud Computing at a Glance, Historical Developments, Building Cloud Computing Environments, Amazon Web Services (AWS), Google AppEngine, Microsoft Azure, Hadoop, Force.com and Salesforce.com, Manjrasoft Aneka.

**RBT Levels:** L1, L2

**Module-2**

**Virtualization:** Introduction, Characteristics of Virtualized, Environments Taxonomy of Virtualization Techniques, Execution Virtualization, Other Types of Virtualization, Virtualization and Cloud Computing, Pros and Cons of Virtualization, Technology Examples.

**RBT Levels:** L2

**Module-3**

**Cloud Computing Architecture:** Introduction, Cloud Reference Model, Types of Clouds, Economics of the Cloud, Open Challenges.

**RBT Levels:** L2

**Module-4**

**Cloud Security:** Risks, Top concern for cloud users, privacy impact assessment, trust, OS security, VM Security, Security Risks posed by shared images and management OS.

**RBT Levels:** L2

**Module-5**

**Cloud Platforms in Industry Amazon web services:** Compute services, Storage services, Communication services, Additional services. Google AppEngine: - Architecture and core concepts, Application life cycle, Cost model, Observations.

**Cloud Applications:** Scientific applications: - HealthCare: ECG analysis in the cloud, Biology: gene expression

data analysis for cancer diagnosis, Geoscience: satellite image processing. Business and consumer applications: CRM and ERP, Social networking, media applications.

**RBT Levels:** L2, L3

**Course outcome (Course Skill Set)**

At the end of the course, the student will be able to :

- CO 1. Understand and analyze various cloud computing platforms and service provider.
- CO 2. Illustrate various virtualization concepts.
- CO 3. Identify the architecture, infrastructure and delivery models of cloud computing.
- CO 4. Understand the Security aspects of CLOUD.
- CO 5. Define platforms for development of cloud applications

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous Internal Evaluation:**

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

**Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester-End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.

Marks scored shall be proportionally reduced to 50 marks.

**Suggested Learning Resources:**

**Textbooks:**


1. Rajkumar Buyya, Christian Vecchiola, and Thamrai Selvi Mastering Cloud Computing McGraw Hill Education.
2. Dan C. Marinescu, Cloud Compting Theory and Practice, Morgan Kaufmann, Elsevier 2013.


**Reference Books:**


1. Toby Velte, Anthony Velte, Cloud Computing: A Practical Approach, McGraw-Hill Osborne Media.
2. George Reese, Cloud Application Architectures: Building Applications and Infrastructure in the Cloud, O'Reilly Publication.
3. John Rhoton, Cloud Computing Explained: Implementation Handbook for Enterprises, Recursive Press.

| **Web links and Video Lectures (e-Resources):** |
| --- |
| • https://nptel.ac.in/ |
| **Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**<br>• Seminar<br>• Quiz<br>• Group Discussion |

| BIG DATA ANALYTICS | | Semester | VII |
|---|---|---|---|
| Course Code | **BUE714D** | CIE Marks | 50 |
| Teaching Hours/Week (L:T:P: S) | 3:0:0 | SEE Marks | 50 |
| Total Hours of Pedagogy | 40 | Total Marks | 100 |
| Credits | 03 | Exam Hours | 3 Hours |
| Examination type (SEE) | **Theory** | | |

**Course objectives:**

- Understand fundamentals and applications of Big Data analytics
- Explore the Hadoop framework and Hadoop Distributed File system and essential Hadoop Tools.
- Illustrate the concepts of NoSQL using MongoDB and Cassandra for Big Data.
- Employ MapReduce programming model to process the big data.
- Understand various machine learning algorithms for Big Data Analytics, Web Mining and Social Network Analysis.

**Teaching-Learning Process (General Instructions)**

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecturer method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
2. Show Video/animation films to explain functioning of various concepts.
3. Encourage collaborative (Group Learning) Learning in the class.
4. Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Topics will be introduced in a multiple representation.
7. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

**Module-1**

**Introduction to Big Data Analytics:** Big Data, Scalability and Parallel Processing, Designing Data Architecture, Data Sources, Quality, Pre-Processing and Storing, Data Storage and Analysis, Big Data Analytics Applications and Case Studies.

**RBT Levels:** L1, L2

**Module-2**

**Introduction to Hadoop:** Introduction, Hadoop and its Ecosystem, Hadoop Distributed File System, MapReduce Framework and Programming Model, Hadoop Yarn, Hadoop Ecosystem Tools.

**Hadoop Distributed File System Basics:** HDFS Design Features, Components, HDFS User Commands.
**Essential Hadoop Tools:** Using Apache Pig, Hive, Sqoop, Flume, Oozie, HBase.

**RBT Levels:** L2

**Module-3**

**NoSQL Big Data Management, MongoDB and Cassandra:**: Introduction, NoSQL Data Store, NoSQL Data Architecture Patterns, NoSQL to Manage Big Data, Shared-Nothing Architecture for Big Data Tasks, MongoDB, Databases, Cassandra Databases.

**RBT Levels:** L2

**Module-4**

**Introduction to MapReduce:** Introduction, MapReduce Map Tasks, Reduce Tasks and MapReduce Execution, Composing MapReduce for Calculations and Algorithms, Hive, HiveQL, Pig.

**RBT Levels:** L2

**Module-5**

**Machine Learning Algorithms for Big Data Analytics:** Introduction, Estimating the relationships, Outliers, Variances, Probability Distributions, and Correlations, Regression analysis, Finding Similar Items, Similarity of Sets and Collaborative Filtering, Frequent Itemsets and Association Rule Mining.

**Text, Web Content, Link, and Social Network Analytics:** Introduction, Text mining, Web Mining, Web Content and Web Usage Analytics, Page Rank, Structure of Web and analyzing a Web Graph, Social Network as Graphs and Social Network Analytics.

**RBT Levels:** L2, L3

**Course outcome (Course Skill Set)**

At the end of the course, the student will be able to :

- CO 1. Understand fundamentals and applications of Big Data analytics.
- CO 2. Investigate Hadoop framework, Hadoop Distributed File system and essential Hadoop tools.
- CO 3. Illustrate the concepts of NoSQL using MongoDB and Cassandra for Big Data.
- CO 4. Demonstrate the MapReduce programming model to process the big data along with Hadoop tools.
- CO 5. Apply Machine Learning algorithms for real world big data, web contents and Social Networks to provide analytics with relevant visualization tools.

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous Internal Evaluation:**

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
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- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

**Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester-End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.

Marks scored shall be proportionally reduced to 50 marks.

**Suggested Learning Resources:**

**Textbooks:**

1. Raj Kamal and Preeti Saxena, "Big Data Analytics Introduction to Hadoop, Spark, and MachineLearning", McGraw Hill Education, 2018 ISBN: 9789353164966, 9353164966

2. Douglas Eadline, "Hadoop 2 Quick-Start Guide: Learn the Essentials of Big Data Computing in the Apache Hadoop 2 Ecosystem", 1 stEdition, Pearson Education, 2016. ISBN13: 978-9332570351.

**Reference Books:**

1. Tom White, “Hadoop: The Definitive Guide”, 4 th Edition, O‟Reilly Media, 2015.ISBN-13: 978-9352130672
2. Boris Lublinsky, Kevin T Smith, Alexey Yakubovich, "Professional Hadoop Solutions", 1st Edition, Wrox Press, 2014ISBN-13: 978-8126551071.
3. Eric Sammer, "Hadoop Operations: A Guide for Developers and Administrators", 1st Edition, O'Reilly Media, 2012, ISBN-13: 978-9350239261.
4. Arshdeep Bahga, Vijay Madisetti, "Big Data Analytics: A Hands-On Approach", 1st Edition, VPT Publications, 2018. ISBN-13: 978-0996025577 .

**Web links and Video Lectures (e-Resources):**

- https://nptel.ac.in/

**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

- Seminar
- Quiz
- Group Discussion

| Verilog HDL | | Semester | VII |
|---|---|---|---|
| Course Code | BUE755A | CIE Marks | 50 |
| Teaching Hours/Week(L:T:P:S) | 3:0:0:0 | SEE Marks | 50 |
| Total Hours of Pedagogy | 40 | Total Marks | 100 |
| Credits | 03 | Exam Hours | 03 |
| Examination nature(SEE) | **Theory** | | |

**Course objectives:**

- Learn different Verilog HDL Constructs.
- Familiarize the different levels of abstraction in Verilog.
- Understand Verilog tasks , functions and directives.
- Understand timing and delay simulation.
- Understand the concept of logic synthesis and its impact in verification.

**Teaching-Learning Process (General Instructions)**

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecturer method (L) needs not to be only traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes.
2. Use of Video/Animation to explain functioning of various concepts.
3. Encourage collaborative (Group Learning) Learning in the class.
4. Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyze information rather than simply recall it.
6. Introduce Topics in manifold representations.
7. Show the different ways to solve the same problem with different circuits/logic and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world-and when that's possible, it helps improve the students' understanding.

## Module-1

**Overview of digital design with Verilog HDL:** Evolution of CAD, emergence of HDLs, typical HDL flow, why Verilog HDL? Trends in HDL

**Hierarchical Modelling Concepts:** Top down and bottom-up design methodology, difference between modules andmodule instances, parts of a simulation, design block, stimulus block.

**RBT Levels:** L1, L2

## Module-2

**Basic Concepts:** Lexical conventions, data types, system tasks, compiler directives.

**Modules and ports:** Module definition, port declaration, connecting ports, Hierarchical name referencing.

**RBT Levels:** L1, L2

## Module-3

**Gate level modeling:** Modelling using basic Verilog gate primitives, description of and /or and buf/not type gates,rise, fall and turn off delays, min, max and typical delays

**Data flow modeling:** Continuous assignments, delay specification, expressions, operators, operand sand operate types.

**RBT Levels:** L2

## Module-4

**Behavioral modeling:** Structured procedures, initial and always, blocking and non-blocking statements, delay control, generate statement, event control, conditional statements, multi way branching, loops, sequential and parallel blocks.

**Tasks and functions:** Differences between tasks and functions, declaration, invocation, automatic tasks and functions.

**RBT Levels:** L2, L3

## Module-5

**Useful Modeling techniques:** Procedural continuous assignments, over riding parameters, conditional compilation, andexecution, useful system tasks

**Logic Synthesis with Verilog:** Logic synthesis, impact of logic synthesis, Verilog HDL synthesis, synthesis design flow,verification of gate level net list.

**RBT Levels:** L2, L3

**Course outcome(Course Skill Set)**

At the end of the course, the student will be able to:

- Write Verilog program singate, dataflow(RTL), behavioral and switch modeling levels of abstraction.
- Design and verify the functionality of digital circuit and system, using test benches
- Identify the suitable abstraction level for a particular digital system.
- Write the programs more effectively using Verilog tasks, function sand directives.
- Program timing and delay simulation and interpret the various constructs in logic synthesis.

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous Internal Evaluation:**

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**Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester-End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.

Marks scored shall be proportionally reduced to 50 marks.

**Suggested Learning Resources:**

**Books**

1. Samir Palnitkar, "Verilog HDL: A guide to digital design and synthesis", Pearson Education, II Edition.

**Reference Books:**

1. Donald ET homas, Philip RMoorby, "The Verilog hardware description Language",
2. Springer Science Business Media, LLC, 5th Edition
3. Michael D.Ciletti, "Advanced digital design with the Verilog HDL", Pearson (PHI), II Edition.
4. Padmanabhan, Tripura Sunadri, "Design through Verilog HDL",Wiley, 2016.

**Web links and Video Lectures (e-Resources):**

- https://nptel.ac.in/courses/

**Activity Based Learning (Suggested Activities in Class)/Practical Based learning**

- VHDL based projects for different applications
- Seminars
- Quizzes
- Assignments

| COMPUTER ORGANIZATION | | | |
|---|---|---|---|
| Course Code | **BUE755B** | CIE Marks | 50 |
| Teaching Hours/Week (L:T:P: S) | 3:0:0:0 | SEE Marks | 50 |
| Total Hours of Pedagogy | 3 Hours/weak | Total Marks | 100 |
| Credits | 03 | Exam Hours | 03 |

**Course Objectives:**

- **CLO1.**Understanding of Computer Architecture: Gain foundational knowledge of the key components of computer systems, including CPUs, memory, storage, and input/output systems.
- **CLO2**.Understand the concepts of instruction sets, addressing modes, and how they influence software design and hardware implementation.
- **CLO3**.Explore the organization of memory systems, including cache memory, virtual memory, and storage hierarchies.
- **CLO4**.Develop skills in writing and understanding assembly language to bridge the gap between high-level programming and hardware.
- **CLO5**.Examine concepts of parallelism and distributed systems, including multi-core processors
- **CLO6**.Apply theoretical concepts to real-world scenarios, fostering problem-solving skills through projects and practical exercises.

**Teaching-Learning Process (General Instructions)**

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecturer method (L) need not to be only a traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes.
2. Use of Video/Animation to explain functioning of various concepts.
3. Encourage collaborative (Group Learning) Learning in the class.
4. Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyze information rather than simply recall it.
6. Introduce Topics in manifold representations.
7. Show the different ways to solve the same problem with different circuits/logic and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

**Module-1**

**Basic Structure of Computers:** Functional Units, Basic Operational Concepts, Bus structure, Performance – Processor Clock, Basic Performance Equation, Clock Rate, Performance Measurement.

**MachineInstructions and Programs:** Memory Location and Addresses, Memory Operations, Instruction and Instruction sequencing, Addressing Modes**.**

**RBT Levels: L1,L2**

**Module-2**

**Input/output Organization: Accessing I/O Devices, Interrupts –** Interrupt Hardware, Enabling and Disabling Interrupts, Handling Multiple Devices.

**Direct Memory Access:** Bus Arbitration, Speed, size and Cost of memory systems. Cache Memories – Mapping Functions**.**

**RBT Levels:L1,L2**

**Module-3**

**Basic Processing Unit**: Some Fundamental Concepts: Register Transfers, Performing ALU operations, fetching a word from Memory, Storing a word in memory. Execution of a Complete Instruction.

**Pipelining:** Basic concepts, Role of Cache memory, Pipeline Performance.

**RBT Levels:L1,L2**

**Module-4**

**Embedded Systems:** Examples of embedded Systems, Microwave Oven, Digital Camera, Home Telemetry, Processor Chips for Embedded Applications.

**Embedded Processor Families:** Microcontroller Based on the Intel 8051, Motorola Microcontrollers, ARM Microcontrollers.

**RBT Levels: L2,L3**

**Module-5**

**Large Computer Systems**: Forms of Parallel Processing, Array Processors, The Structure of General-Purpose Multiprocessors.
**Memory Organization in Multiprocessors.**
**Multicomputers**: Local Area Networks, Ethernet(CSMA/CD) BUS, Token Ring, Network of Workstations

**RBT Levels: L2,L3**

**Course Outcomes (Course Skill Set):**
At the end of the course the student will be able to:
**CO1:** Describe the fundamentals of machine instructions, addressing modes and Processor performance.
**CO2**: Explain the approaches involved in achieving communication between processor and I/O devices.
**CO3:** Analyze internal Organization of Memory and Impact of cache/Pipelining on Processor Performance.
**CO4**: Understand the working of Embedded systems and its processor Families.
**CO5:** Design analysis of Large Computer systems and Multicomputers.

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous Internal Evaluation:**

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

**Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester-End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.

Marks scored shall be proportionally reduced to 50 marks.

**Textbooks:**

1. Carl Hamcher, ZvonkoVranesic, SafwatZaky, Computer Organization, 5th Edition, Tata McGraw Hill.

**Weblinks and Video Lectures (e-Resources):**

| ARM MICROCONTROLLER | | Semester | VII |
|---|---|---|---|
| Course Code | **BUE755C** | CIE Marks | 50 |
| Teaching Hours/Week (L:T:P: S) | 3:0:0 | SEE Marks | 50 |
| Total Hours of Pedagogy | 40 | Total Marks | 100 |
| Credits | 03 | Exam Hours | 3 Hours |
| Examination type (SEE) | **Theory** | | |

**Course Objectives:**

- Understand the fundamentals of ARM-based systems.
- Understand ARM programming modules with registers and the CPSR.
- Use the various instructions to program the ARM controller.
- Program various embedded components using the embedded C program.
- Understand the various optimized primitives used in ARM assembly code.

**Teaching-Learning Process (General Instructions)**

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecturer method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
2. Show Video/animation films to explain functioning of various concepts.
3. Encourage collaborative (Group Learning) Learning in the class.
4. Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Topics will be introduced in a multiple representation.
7. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

**Module-1**

**ARM Embedded Systems:** The RISC design philosophy, The ARM Design Philosophy, Embedded System Hardware, Embedded System Software.

**ARM Processor Fundamentals:** Registers, Current Program Status Register, Pipeline, Exceptions Interrupts, and the Vector Table, Core Extensions.

**RBT Levels:** L1, L2

**Module-2**

**Introduction to the ARM Instruction Set:** Data Processing Instructions, Branch Instructions, Software Interrupt Instructions, Program Status Register Instructions, Coprocessor Instructions, Loading Constants, ARMv5E Extensions, Conditional Execution.

**RBT Levels:** L2

**Module-3**

**C Compilers and Optimization:** :Basic C Data Types, C Looping Structures, Register Allocation, Function Calls, Pointer Aliasing, Structure Arrangement, Bit-fields, Unaligned Data and Endianness, Division, Floating Point, Inline Functions and Inline Assembly, Portability Issues.

**RBT Levels:** L2, L3

**Module-4**

**ARM programming using Assembly Language:** Writing Assembly code, Profiling and cycle counting, instruction scheduling, Register Allocation, Conditional Execution, Looping Constructs, Bit Manipulation, Efficient Switches, Handling Unaligned Data.

**RBT Levels:** L2, L3

**Module-5**

**Optimized Primitives:** Double-Precision, Integer Multiplication, Integer Normalization and Count Leading Zeros, Division, Square Roots, Transcendental Functions: log, exp, sin, cos.

**RBT Levels:** L2, L3

**Course outcome (Course Skill Set)**

At the end of the course, the student will be able to :

- CO 1. Describe the ARM microcontroller's architectural features and program module.
- CO 2. Apply the knowledge gained from programming on ARM to different applications.
- CO 3. Explain C-Compilers and optimization.

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous Internal Evaluation:**

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

**Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester-End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.

Marks scored shall be proportionally reduced to 50 marks.

**Suggested Learning Resources:**

**Textbooks:**

1. Andrew N Sloss, Dominic Symes and Chris Wright, ARM system developers guide, Elsevier, Morgan Kaufman publishers, 2008.

**Reference Books:**

1. Raghunandan. G.H, Microcontroller (ARM) and Embedded System, Cengage learning Publication,2019.
2. The Insider's Guide to the ARM7 Based Microcontrollers, Hitex Ltd.,1st edition, 2005.
3. Steve Furber, ARM System-on-Chip Architecture, Second Edition, Pearson, 2015.

**Web links and Video Lectures (e-Resources):**

- https://nptel.ac.in/

**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

- Seminar
- Quiz
- Group Discussion

| OPERATIONAL AMPLIFIER | | | |
|---|---|---|---|
| Course Code | BUE755D | CIE Marks | 50 |
| Teaching Hours/Week (L:T:P: S) | 3:0:0:0 | SEE Marks | 50 |
| Total Hours of Pedagogy | 3 Hours/weak | Total Marks | 100 |
| Credits | 03 | Exam Hours | 03 |

**Course Objectives:**

- CLO1. Define and describe various parameters of Op-Amp, its characteristics and Specifications.
- CLO2. Discuss the effects of Input and Output voltage range upon Op-Amp circuits.
- CLO3. Sketch and Analyze Op-Amp circuits to determine Input Impedances, output Impedances and other performance parameters.
- CLO4. Sketch and Explain typical Frequency Response graphs for each of the Filter circuits. Showing Butterworth and Chebyshev responses where ever appropriate.
- CLO4. Describe and Sketch the various switching circuits of Op-Amps and analyze itsoperations.
- CLO6. Differentiate between various types of DACs and ADCs and evaluate the performanceof each with neat circuit diagrams and assuming suitable inputs.

**Teaching-Learning Process (General Instructions)**

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecturer method (L) need not to be only a traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes.
2. Use of Video/Animation to explain functioning of various concepts.
3. Encourage collaborative (Group Learning) Learning in the class.
4. Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyze information rather than simply recall it.
6. Introduce Topics in manifold representations.
7. Show the different ways to solve the same problem with different circuits/logic and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

**Module-1**

**Operational Amplifier Fundamentals:**

Basic Op-amp circuit, Op-Amp parameters – Input and output voltage, CMRR and PSRR, offset voltages and currents, Input and output impedances, Slew rate and Frequency limitations.

**OP-Amps as DC Amplifiers –** Biasing OP-amps, Direct coupled voltage followers, Non-inverting amplifiers, inverting amplifiers, Summing amplifiers, and Difference amplifiers. Interpretation of OP-amp LM741 & TL081 datasheet.

**RBT Levels: L1, L2**

**Module-2**

**Op-Amps as AC Amplifiers:** Capacitor coupled voltage follower, High input impedance– Capacitor coupled voltage follower, Capacitor coupled non inverting amplifiers, High input impedance – Capacitor coupled Non inverting amplifiers, Capacitor coupled inverting amplifiers, setting the upper cut-off frequency, Capacitor coupled difference amplifier.

**OP-Amp Applications:** Voltage sources, current sources and current sinks, current amplifiers, instrumentation amplifier, precision rectifiers**.**

**RBT Levels: L1, L2**

**Module-3**

**More Applications:** Limiting circuits, Clamping circuits, Peak detectors, Sample andhold circuits, V to I and I to V converters, Differentiating Circuit, Integrator Circuit, Phase shift oscillator, Wien bridge oscillator, Crossing detectors, inverting Schmitt trigger. Log and antilog amplifiers, Multiplier and divider**.**

**RBT Levels: L2,L3**

**Module-4**

**Active Filters:** First order and second order active Low-pass and high pass filters, Bandpass Filter, Bandstop Filter.

**Voltage Regulators:** Introduction, Series Op-amp regulator, IC voltage regulators. 723 general purpose regulators.

**RBT Levels: L2,L3**

**Module-5**

**Phase locked loop:** Basic Principles, Phase detector/comparator, VCO.
**DAC and ADC convertor:** DAC using R-2R, ADC using Successive approximation.
**Other IC Application:** 555 timer, Basic timer circuit, 555 timer used as astable and monostable multivibrator.

**RBT Levels: L2,L3**

**Course Outcomes (Course Skill Set):**

At the end of the course the student will be able to:

**CO1.**Explain Op-Amp circuit and parameters including CMRR, PSRR, Input & OutputImpedances and Slew Rate.

**CO2**.Design Op-Amp based Inverting, Non-inverting, Summing & Difference Amplifier, and AC Amplifiers including Voltage Follower.

**CO3**.Test circuits of Op-Amp based Voltage/ Current Sources & Sinks, Current, Instrumentation and Precision Amplifiers.

**CO4**. Test circuits of Op-Amp based linear and non-linear circuits comprising of limiting, clamping, Sample & Hold, Differentiator/ Integrator Circuits, Peak Detectors, Oscillators and Multiplier & Divider.

**CO5.**Design first & second order Low Pass, High Pass, Band Pass, Band Stop Filters and Voltage Regulators using Op-Amps.

**CO6**.Explain applications of linear ICs in phase detector, VCO, DAC, ADC and Timer.

**Assessment Details (both CIE and SEE)**

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**Textbooks**


1. Operational Amplifiers and Linear IC's||, David A. Bell, 2nd edition, PHI/Pearson, 2004. ISBN 978-81-203-2359-9.
2. Linear Integrated Circuits||, D. Roy Choudhury and Shail B. Jain, 4thedition, Reprint 2006, New Age International ISBN 978-81-224-3098-1.


**Reference Books**


1. Ramakant A Gayakwad, "Op-Amps and Linear Integrated Circuits", Pearson, 4th Ed, 2015. ISBN 81-7808-501-1.
2. B Somanathan Nair, "Linear Integrated Circuits: Analysis, Design & Applications", Wiley India, 1st Edition, 2015.
3. James Cox, "Linear Electronics Circuits and Devices", Cengage Learning, Indian Edition, 2008, ISBN-13: 978-07-668-3018-7


**Weblinks and Video Lectures (e-Resources):**

- https://nptel.ac.in/