Verification using System Verilog		Semester	7
Course Code	**BVL701**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:2:0	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory + 8-10 Lab slots	Total Marks	100
Credits	04	Exam Hours	3 Hours
Examination nature (SEE)	**Theory**		

Course objectives:

This course will enable students to:

- Understand methods and techniques to verify the functionality of digital electronic systems using System Verilog.
- Learn the System Verilog Language for Digital System Verification.
- To develop the ability to create structured and modular testbenches for verifying digital designs
- Use Constrained Random Tests for Verification
- To understand and utilize the concepts of functional coverage

Teaching-Learning Process (General Instructions)

The sample strategies, which the teacher can use to accelerate the attainment of the various course outcomes are listed in the following:

1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
2. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking
3. Adopt Problem Based Learning (PBL), which fosters students' analytical skills, develop thinking skills such as the ability to evaluate, generalize & analyze information rather than simply recall it.
4. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.
5. Using videos for demonstration of the fundamental principles to students for better understanding of concepts.
6. Demonstration of microwave devices and Antennas in the lab environment where students can study them in real time.

Module-1

Introduction to System Verilog:

System Verilog standards, Key System Verilog enhancements for hardware design. Advantages of System Verilog over Verilog**, [Text2: 1.1.1, 1.1.2,1.2]**

Data Types: Verilog data types, System Verilog data types, 2 - State Data types, Bit, byte, shortint, int, longint. 4 - State data types. Logic, Enumerated data types, User Defined data types, Struct data types, Strings, Packages, Type Conversion: Dynamic casting, Static Casting, Memories: Arrays, Dynamic Arrays, Multidimensional Arrays, Packed Arrays, Associative Arrays, Queues, Array Methods. **[Text2: 3.3.1, 3.3.2, 3.3.3, 3.3.4, 4.1,4.2, 5.1, 5.7, 2.1, 3.9.1.3.9.2] [Text 1: 2.4, 2.5,2.6, 2.8]**

RBT Levels: L1, L2

Module-2

Connecting the Test Bench and Design: Separating the Test Bench and Design, The Interface Construct, Stimulus Timing, Interface Driving and Sampling, System Verilog Assertions. [Text 1: 5.2,5.3, 5.4,5.5, 5.9]

Procedural Statements and Routines: Procedural Statements, Tasks, Functions and Void Functions, Task and Function Overview, Routine Arguments, Returning from a Routine, Local Data Storage, Time Values. **[Text1: 3.2, 3.3, 3.4,3.5, 3.6, 3.7,3.8]**

RBT Levels: L2, L3

Module-3

Randomization: Introduction, Randomization in System Verilog, Constraint Details, Solution Probabilities, Valid Constraints, InLine Constraints, Random Number Functions, Common Randomization Problems, Random Control, Random Number Generators. **[Text1: 6.1,6.3,6.4, 6.5, 6.6, 6.7,6.8, 6.9,6.11, 6.14, 6.15]**

RBT Levels: L2,L3

Module-4

Functional Coverage: Introduction, Coverage Types, Functional Coverage Strategies , Anatomy of a Cover Group, Triggering a Cover Group, Data Sampling, Cross Coverage, Coverage Options, Parameterized Cover Groups **[Text1: 9.1,9.2, 9.3, 9.6, 9.7,9.8, 9.9,9.10]**

RBT Levels: L3, L4

Module-5
Complete Design Model Using System Verilog- Case Study: System Verilog ATM Example, Data Abstraction, Interface Encapsulation, Design Top Level Squat, Receivers and Transmitters, Test Bench for ATM. **[Text2: 11.1,11.2, 11.3, 11.4, 11.5, 11.6]** **RBT Levels:** L3, L4

PRACTICAL COMPONENT OF IPCC

Sl.NO	Experiments
1	Develop mux2x1 verilog code in design.sv and develop Test bench for mux2x1 in testbench.sv with different inputs at various times.
2	Write a program to demonstrate two-state and four-state data types.
3	Write a program to demonstrate push_front, pop_front, push_back and pop_back with respect to Queues.
4	Design a full adder using the interface construct to model inter-module communication.
5	Create a program to highlight the difference between rand and randc constructs in constrained randomization.
6	Build a 4-bit adder and verify its functionality using a structured verification environment.
7	Design a UART module using SystemVerilog: a. Develop the transmitter logic b. Implement the receiver logic c. Create a top-level testbench to verify UART operation
8	Design, simulate, and analyze functional coverage to ensure thorough verification of a given design.
9	Design and simulate a verification test that exercises multiple sequences.
10	Create and simulate a configurable Universal Verification Methodology (UVM) test environment.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

1. Understand and explain the principles and methodologies used in verifying the functionality of digital systems.
2. Apply the System Verilog concepts to verify the complex digital circuits.
3. Develop and implement constrained random testbenches using System Verilog
4. Analyze verification quality using functional coverage metrics and implement covergroups
5. Analyze real-world verification scenarios and apply System Verilog methodologies

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

The IPCC means the practical portion integrated with the theory of the course. CIE marks for the theory component are **25 marks** and that for the practical component is **25 marks.**

CIE for the theory component of the IPCC

- 25 marks for the theory component are split into 15 marks for two Internal Assessment Tests (Two Tests, each of 15 Marks with 01-hour duration, are to be conducted) and 10 marks for other assessment

methods mentioned in 22OB4.2. The first test at the end of 40-50% coverage of the syllabus and the second test after covering 85-90% of the syllabus.

- Scaled-down marks of the sum of two tests and other assessment methods will be CIE marks for the theory component of IPCC (that is for 25 marks).
- The student has to secure 40% of 25 marks to qualify in the CIE of the theory component of IPCC.

CIE for the practical component of the IPCC

- **15 marks** for the conduction of the experiment and preparation of laboratory record, and 10 marks for the test to be conducted after the completion of all the laboratory sessions.
- On completion of every experiment/program in the laboratory, the students shall be evaluated including viva-voce and marks shall be awarded on the same day.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to **15 marks.**
- The laboratory test **(duration 02/03 hours)** after completion of all the experiments shall be conducted for 50 marks and scaled down to **10 marks.**
- Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **25 marks.**
- The student has to secure 40% of 25 marks to qualify in the CIE of the practical component of the IPCC.

SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours)**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions**), should have a mix** of topics under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored by the student shall be proportionally scaled down to 50 Marks

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper may include questions from the practical component.

- The minimum marks to be secured in CIE to appear for SEE shall be 10 (40% of maximum marks-25) in the theory component and 10 (40% of maximum marks -25) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included. The maximum of 04/05 sub questions are to be set from the practical component of IPCC, the total marks of all questions should not be more than 20 marks.
- SEE will be conducted for 100 marks and students shall secure 35% of the maximum marks to qualify for the SEE. Marks secured will be scaled down to 50.
- The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Text Books:

1. Chris Spear, "System Verilog for Verification – A guide to learning the Test bench language features", Springer Publications Second Edition, 2010.
2. Stuart Sutherland, Simon Davidmann, Peter Flake, "System Verilog for Design- A guide to using system Verilog for Hardware design and modelling", Springer Publications Second Edition, 2006

Reference Book:

1. Writing Testbenches using SystemVerilog - Janick Bergeron
2. SystemVerilog golden reference guide-A concise guide to System Verilog Doulos ,IEEE Standard-1800- 2009, Version 5.0,ISBN: 0-9547345-9-9, 2012.
3. Step-by-Step Functional Verification with System Verilog and OVM, SasanIman, Hansen Brown Publishing Company,ISBN-13: 978-0-9816-5621-2, 2008.
4. Verification Methodology Manual - Janick Bergeron

Web links and Video Lectures (e-Resources):

1. www.systemverilog.org
2. www.asic-world.com/systemverilog/index.html
3. http://svug.org/

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Programming Assignments / Mini Projects can be given to improve practical skills

Design for Testability		Semester	7
Course Code	BVL702	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:2	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory + 8-10 Lab slots	Total Marks	100
Credits	4	Exam Hours	3
Examination Nature (SEE)	Theory		

Upon successful completion of this course, students will be able to:

- Identify and classify different types of faults in VLSI-based digital circuits.
- Evaluate fault detection techniques in both combinational and sequential circuits to improve system testability.
- Apply test pattern generation and response analysis methods for effective testing of modern VLSI systems.
- Understand fault modelling in RAM and implement strategies for accurate fault diagnosis.
- Acquire hands-on experience with key VLSI testing methodologies, including GATPAT, walking pattern tests, and Built-In Self-Test (BIST) schemes.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
2. Show Video/animation films to explain evolution of communication technologies.
3. Encourage collaborative (Group) Learning in the class
4. Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
7. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students understanding.

Module:1 - Introduction to Faults in Digital Circuits

Failures and Faults, Modeling of faults, Temporary Faults, Levels of abstraction in VLSI testing, Historical Review of VLSI Test Technologies.

Text 1: 1.1, 1.2, 1.3 Text 2: 1.4, 1.5

Module:2 - Test Generation for Combinational Logic Circuits

Fault Diagnosis of digital circuits, Test generation techniques for combinational circuits, Detection of multiple faults in Combinational Logic Circuits, Testing of Sequential circuits as Iterative Combinational Circuits

Text 1: 2.1, 2.2, 2.3, 4.1

Module: 3 - Design of Testable Sequential circuits

Design of testable sequential circuits: Controllability and observability, Ad-Hoc design rules for improving testability, design of diagnosable sequential circuits, the scan-path technique for testable sequential circuit design, Level Sensitive Scan Design (LSSD), Random Access Scan Technique, Partial scan, testable sequential circuit design using Non scan Techniques, Cross check, Boundary Scan.

Text 1:5.1, 5.2, 5.3, 5.4, 5.5, 5.5.1, 5.6, 5.7, 5.8, 5.9, 5.10

Module: 4 - Logic BIST

Built-In Self-Test: Test pattern generation for BIST, Exhaustive Testing, Pseudo Exhaustive Pattern Generation, Pseudo-Random Pattern Generator, Deterministic Testing, Output Response Analysis, Transition Count, Syndrome Checking, Signature Analysis, Circular BIST, BIST Architectures, BILBO (Built-In Logic Block Observer), STUMPS (Self-Testing Using an MISR and Parallel Shift Register Sequence Generator), LOCST (LSSD On-Chip Self-Test)

Text 1:6.1, 6.2, 6.3, 6.4

Module: 5 - Testable memory Design

RAM Full Models, Test Algorithms for RAMs, GALPAT (Galloping Os and 1s), Walking Os and Is, March Test, Checkerboard Test, Detection of Patterns sensitive faults, BIST Techniques for RAM Chips

Text 1: 7.1, 7.2, 7.3, 7.4

Laboratory Experiments:

Note: Experiments are conducted using industry-standard tools such as Modus, Tessent, or any other equivalent testing and validation software.

Sl. No.	Experiments
1	**Fault Simulation and Test Generation** Perform fault simulation and generate test patterns for combinational circuits: a. 4-bit Adder b. 4:1 Multiplexer
2	**Automatic Test Pattern Generation (ATPG) for Combinational Circuits** Generate ATPG-based test patterns for: a. 4-bit Adder b. 4:1 Multiplexer
3	**Fault Simulation and Test Generation for Complex Circuits** Perform fault simulation and test generation for: a. Arithmetic Logic Unit (ALU) b. Decoder
4	**ATPG Pattern Generation for Digital circuits Circuits** Generate ATPG test patterns for: a. Arithmetic Logic Unit (ALU) b. Decoder
5	**Design for Testability (DFT) Implementation** a. Insert DFT structures into a 4-bit synchronous counter. b. Generate ATPG patterns for the counter and validate test coverage.
6	**Delay Fault ATPG** Perform delay fault ATPG pattern generation for a full adder circuit.
7	**Scan Chain Insertion and Verification.** • Insert scan chains into a sequential circuit (e.g., 4-bit register). • Perform Design Rule Check (DRC) and verify scan insertion through scan simulation.
8	**Fault Modeling and Simulation** • Model and simulate common digital circuit faults (e.g., stuck-at, bridging) using ATPG tools.
9	**Boundary Scan Testing (BST)** • Implement and perform boundary scan testing on a digital counter circuit

10	**Built-In Self-Test (BIST) for Memory** • Insert BIST structures into an SRAM memory module using industry tools (e.g., Cadence Modus or Synopsys Tessent). • Validate BIST functionality and analyze repair mechanisms for SRAM fault scenarios.

Course outcomes (Course Skill Set):

By the end of this course, students will be able to:

1. Evaluate the importance of fault modelling and testing in ensuring the reliability of digital circuits.
2. Develop fault lists and implement test compression techniques to enhance testing efficiency.
3. Utilize boundary scan methods to assess and verify the performance of digital systems.
4. Design and implement Built-In Self-Test (BIST) architectures for testing complex digital circuits.
5. Analyze various RAM fault types, apply appropriate testing methodologies, and perform memory testing using BIST strategies.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

The IPCC means the practical portion integrated with the theory of the course. CIE marks for the theory component are **25 marks** and that for the practical component is **25 marks**.

CIE for the theory component of the IPCC

- 25 marks for the theory component are split into **15 marks** for two Internal Assessment Tests (Two Tests, each of 15 Marks with 01-hour duration, are to be conducted) and **10 marks** for other assessment methods mentioned in 22OB4.2. The first test at the end of 40-50% coverage of the syllabus and the second test after covering 85-90% of the syllabus.
- Scaled-down marks of the sum of two tests and other assessment methods will be CIE marks for the theory component of IPCC (that is for **25 marks)**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the theory component of IPCC.

CIE for the practical component of the IPCC

- **15 marks** for the conduction of the experiment and preparation of laboratory record, and **10 marks** for the test to be conducted after the completion of all the laboratory sessions.
- On completion of every experiment/program in the laboratory, the students shall be evaluated including viva-voce and marks shall be awarded on the same day.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of

the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to **15 marks**.

- The laboratory test **(duration 02/03 hours)** after completion of all the experiments shall be conducted for 50 marks and scaled down to **10 marks.**
- Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **25 marks**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the practical component of the IPCC.

SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored by the student shall be proportionally scaled down to 50 Marks

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper may include questions from the practical component.

- The minimum marks to be secured in CIE to appear for SEE shall be 10 (40% of maximum marks-25) in the theory component and 10 (40% of maximum marks -25) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included**.** The maximum of 04/05 sub-questions are to be set from the practical component of IPCC, the total marks of all questions should not be more than 20 marks.
- SEE will be conducted for 100 marks and students shall secure 35% of the maximum marks to qualify for the SEE. Marks secured will be scaled down to 50.
- The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Suggested Learning Resources:

Text Books

1) Lala Parag K, "Digital Circuit Testing and Testability", New York, Academic Press 1997.
2) Wang, Wu and Wen Morgan" VLSI Test Principles and Architectures" Kaufmann, 2006.

References Books

1) N. Jha & S.D. Gupta, "Testing of Digital Systems", Cambridge, 2003.
2) Michael L. Bushnell & Vishwani D. Agrawal," Essentials of Electronic Testing for Digital, mem & Mixed signal VLSI Circuits", Kluwar Academic Publishers. 2000.
3) Abramo vici M, Breuer M A, "Digital Systems Testing and Testable Design and Friedman AD", Wiley 1994.
4) WilliamK.Lam, "Hardware Design Verification: Simulation and Formal Method - Based Approaches", Prentice Hall

Web links and Video Lectures (e-Resources):

https://www.youtube.com/watch?v=05lyBoWR-PA&list=PLx98Qgh5zPjh6oWI73QfQHZAmAiyt8Wkf
https://www.youtube.com/watch?v=Abld-fSxjNM&list=PLbMVogVj5nJTClnafWQ9FK2nt3cGG8kCF
https://www.youtube.com/watch?v=MEaMm423t0w&list=PLZjlBaHNchvOFBWBAtAP9exwQgYpKqs04&index=1

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

CAD for VLSI		Semester	7
Course Code	BVL703	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	4:0:0:0	SEE Marks	50
Total Hours of Pedagogy	50 Hours	Total Marks	100
Credits	04	Exam Hours	3 Hours
Examination nature (SEE)	**Theory**		

Course Objectives:

This course is designed to equip students with the following skills and knowledge:

- Apply graph theory to various phases of VLSI circuit physical design
- Understand and utilize graph-theoretic, heuristic, and genetic algorithms
- Explore and implement different optimization techniques
- Gain insight into key placement and routing methodologies

Module-1

Introduction to Design Methodologies: The VLSI Design Problem, The Design Domains, Design Actions, Design Methods and Technologies. **[Text1: 1.1,1.2,1.3,1.4]**
VLSI Design Automation tools: Algorithmic and System Design, Structural and Logic Design, Transistor-level Design, Layout Design, Verification Methods, Design Management Tools.
[Text1: 2.1,2.2,2.3,2.4,2.5,2.6]

RBT Levels: L1, L2

Module-2

Algorithmic graph theory and computational complexity: Terminology, Data Structures for the Representation of Graphs, Computational Complexity, Examples of Graph Algorithms.
[Text1: 3.1,3.2,3.3,3.4]
Tractable and intractable problems: Combinational optimization problems, Decision Problems, Complexity Classes, NP-completeness and NP-hardness, Consequences. **[Text1: 3.1,3.2,3.3,3.4,3.5]**

RBT Levels: L1, L2

Module-3

Partitioning: Problem formulation, Classification of Partitioning Algorithms. [Text2: 4.1, 4.2]
Group migration algorithms: Kernighan-Lin algorithm, Simulated Annealing, Simulated Evolution. **[Text2: 4.3, 4.31, 4.4,4.41,4.42]**
Placement: Problem formulation, Classification of Placement Algorithm. **[Text2: 5.1, 5.1.1, 5.1.2]**
Floor Planning: Problem formulation, Classification of Floor planning Algorithms, Constraint based floor planning, Rectangular dualization. **[Text2: 5.2, 5.2.1, 5.2.2, 5.2.3]**

RBT Levels: L1,L2,L3

Module-4

Global Routing: Problem formulation, Classification of Global routing algorithms, Maze routing algorithms: Lee's algorithm, Soukup's algorithm and Hadlock's Algorithm, Line probe algorithms. **[Text2: 6.1, 6.2, 6.3, 6.4]**
Detailed Routing: Problem formulation, Routing considerations, models, channel routing and switch box routing problems, Single-Layer Routing Algorithms, General river routing problem, Single row routing problem, Two-layer channel routing algorithms: Basic Left Edge Algorithm, Dogleg router, Symbolic router-YACR2. **[Text2: 7.1, 7.3.1, 7.3.2, 7.4,7.4.2.1, 7.4.2.2]**

RBT Levels: L1,L2,L3

Module-5

Simulation and Logic Synthesis: Simulation, Gate-level modeling and simulation, Switch-level modeling and simulation, Combinational Logic Synthesis, Binary Decision Diagrams, Two Level Logic Synthesis. **[Text1: 10.1,10.2, 10.3, 11.1, 11.2, 11.3]**

RBT Levels: L1,L2,L3

Course Outcomes (Course Skill Set):
Upon successful completion of this course, students will be able to:

- Demonstrate an understanding of various design methodologies in VLSI physical design
- Apply graph-theoretic concepts to solve VLSI-related problems
- Develop generalized algorithms for design automation
- Analyze and evaluate the computational complexity of algorithms
- Design and implement algorithms for VLSI automation tasks

Assessment Details (both CIE and SEE)
The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks.
- Any two assignment methods mentioned in the 22OB4.2, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:
Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course **(duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), should have a mix of topics under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:
Text Book

1. S.H. Gerez, *Algorithms for VLSI Design Automation*, John Wiley & Sons, 2nd Edition.
2. N. Sherwani, *Algorithms for VLSI Physical Design Automation*, KAP, 1999.
3. Charles J. Alpert, Dinesh P. Mehta and Sachin S Sapatnekar, *"Handbook of Algorithms for Physical Design Automation, CRC Press, 1st Edition, 2.*

Web links and Video Lectures (e-Resources):

- Notes by KiaBazargan from Univ. of Minnesota [©Bazargan]
  - http://www.ece.umn.edu/users/kia/Courses/EE5301
- Notes by Kurt Keutzerfrom UC-Berkeley [©Keutzer]
  - http://www-cad.eecs.berkeley.edu/~niraj/ee244/index.htm
- Notes by Rajesh Gupta, UC-San Diego [©Gupta]
  - http://www.ics.uci.edu/~rgupta/ics280.html

Application Specific Integrated Circuits			
Course Code	**BEC714A**	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03(Theory)

Course Learning Objectives:

By the end of this course, students will be able to:

- Comprehend ASIC design methodologies and utilize programmable logic cells for implementing functions on integrated circuits.
- Analyze the back-end physical design flow, including key stages such as partitioning, floor planning, placement, and routing.
- Evaluate performance parameters relevant to FPGA and ASIC-based VLSI chip designs.

Module-1

Introduction to ASICs: Full custom, Semi-custom and Programmable ASICs, ASIC Design flow, ASIC cell libraries. **CMOS Logic:** Data path Logic Cells: Data Path Elements, Adders: Carry skip, Carry bypass, Carry save, Carry select, Conditional sum, Multiplier (Booth encoding), Data path Operators, I/O cells, Cell Compilers.

Text 1: [1.1,1.2,1.5,2.6,2.7,2.8]

RBT Levels: L2

Module-2

ASIC Library Design: Logical effort: Predicting Delay, Logical area and logical efficiency, Logical paths, Multi-stage cells, Optimum delay and number of stages, library cell design.
Programmable ASIC Logic Cells: MUX as Boolean function generators, Acted ACT: ACT 1, ACT 2 and ACT 3 Logic Modules, Xilinx LCA:XC3000 CLB, Altera FLEX and MAX, Programmable ASIC I/O Cells: Xilinx and Altera I/O Block

Text 1: [3.3,3.4,5.1,5.2,5.3,5.4]

RBT Levels: L2, L3

Module-3

Low-level design entry: Schematic entry: Hierarchical design, The cell library, Names, Schematic Icons & Symbols, Nets, Schematic Entry for ASICs, Connections, vectored instances & buses, Edit in place, attributes, Netlist screener.
ASIC Construction: Physical Design, CAD Tools System partitioning, Estimating ASIC size. Partitioning: Goals and objectives, Constructive Partitioning, Iterative Partitioning Improvement, KL, FM and Look Ahead algorithms.

Text 1: [9.1,15.2, 15.3, 15.4,15.7]

RBT Levels: L2, L3

Module-4

Floor planning and placement: Goals and objectives, Measurement of delay in Floor planning, Floor planning tools, Channel definition, I/O and Power planning and Clock planning.
Placement: Goals and Objectives, Min-cut Placement algorithm, Iterative Placement Improvement, Time driven placement methods, Physical Design Flow.

Text 1: [16.1,16.2,16.3]

RBT Levels: L2, L3

Module-5

Routing: Global Routing - Goals and objectives, Global Routing Methods, Global routing between blocks, Back-annotation. Detailed Routing - Goals and objectives, Measurement of Channel Density, Left-Edge Algorithm, Area-Routing Algorithms, Multilevel routing, Timing –Driven detailed routing, Final routing steps, Special Routing, Circuit extraction and DRC.
Text 1: [17.1,17.2,17.3 , 17.4]

RBT Levels: L3, L4

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks(18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions(for 100 marks), selecting one full question from each module.

1. Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Text Books:

1. Michael John Sebastian Smith, "Application - Specific Integrated Circuits", Addison- Wesley Professional, 2005
2. Khosrow Golshan Conexant Systems, Inc. 2007 Springer Science Business Media " Physical Design Essentials " An ASIC Design Implementation Perspective

Reference Books:

1. Neil H.E. Weste, David Harris, and Ayan Banerjee, "CMOS VLSI Design: A Circuits and Systems Perspective" , Addison Wesley/ Pearson education 3rdedition, 2011
2. Vikram Arkalgud Chandrasetty, "VLSI Design: A Practical Guide for FPGA and ASIC Implementations" Springer, ISBN: 978-1-4614-1119-2. 2011
3. Rakesh Chadha, Bhasker J, "An ASIC Low Power Primer", Springer, ISBN: 978-14614-4270-7.

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Web links and Video Lectures (e-Resources):

- https://nptel.ac.in/

Skill Development Activities Suggested

- **Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**
- **Real world Problem Solving: Applying the ASIC front end and backend concepts.**

Course Outcomes (Course Skill Set):

By the end of the course, students will be able to:

Sl.No	Description	Blooms Level
CO1	Explain ASIC design methodologies, data path components, and the concept of logical effort.	L2
CO2	Analyze ASIC designs for specific applications, carry out design entry, and describe the physical design flow.	L3
CO3	Design data path components for ASIC cell libraries and calculate optimal path delays.	L3
CO4	Develop floorplans with partitioning and routing using relevant algorithms and EDA tools.	L3,L4
CO5	Design CAD algorithms and explain their integration within the ASIC design process.	L3 ,L4

B. E. Electronics Engineering (VLSI Design and Technology)
Choice Based Credit System (CBCS) and Outcome Based Education (OBE)
SEMESTER – VII

Computer and Network Security

Course Code	BEC714B	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory	Total Marks	100

CREDITS – 03

Course objectives:

This course will enable students to:

- Preparation: To prepare students with fundamental knowledge/ overview in the field of Network Security with knowledge of security mechanisms and services, Vulnerabilities in the host machines.
- Core Competence: To equip students with a basic foundation on computer as well as network security by delivering the basics of malicious software, intrusion detection, vulnerability Analysis, auditing as well as securities related to network, system, user and programs

Teaching-Learning Process (General Instructions)

These are sample Strategies; that teachers can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
2. Show Video/animation films to explain the different concepts of Digital Signal Processing
3. Encourage collaborative (Group) Learning in the class
4. Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Topics will be introduced in a multiple representation.
7. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world - and when that's possible, it helps to improve the students' understanding.
9. Adopt Flipped class technique by sharing the materials / Sample Videos prior to the class and have discussions on the that topic in the succeeding classes.

MODULE-1	RBTL Level
Attacks on Computers and Computer Security: Need for Security, Security Approaches, Principles of Security Types of Attacks. **(Text2: Chapter1)** Security Mechanisms, Services and Attacks, A model for Network security **(Text1: Chapter1: 3, 4, 5, 6)**	L1, L2, L3
MODULE-2	
Malicious Logic: Introduction, Trojan Horses, Computer Viruses, Computer Worms, Other Forms of Malicious Logic, Defenses (Text 3: Chapter 12) **Vulnerability Analysis:** Introduction, Penetration Studies, Vulnerability Classification, Frameworks (Text 3: Chapter 13)	L1, L2, L3
MODULE-3	

Auditing: Definitions, Anatomy of an Auditing System, Designing an Auditing System, A Posterior Design, Auditing Mechanisms, Examples, Audit Browsing (Text 3: Chapter 14) **Intrusion Detection**: Principles, Basic Intrusion Detection, Models, Architecture, Organization of Intrusion Detection Systems, Intrusion Response (Text 3: Chapter 15)	L1, L2, L3
MODULE-4	
Network Security: Introduction, Policy Development, Network Organization, Availability and Network Flooding, Anticipating Attacks (Text 3: Chapter 16) **System Security:** Introduction, Policy, Networks, Users, Authentication, Processes, Files, Retrospective (Text 3: Chapter 17)	L1, L2, L3
MODULE-5	
User Security: Policy, Access, Files and Devices, Processes, Electronic Communications (Text 3: Chapter 18) **Program Security:** Introduction, Requirements and Policy, Design, Refinement and Implementations (Text 3: Chapter 19: Section 1, 2, 3, 4)	L1, L2, L3

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

- Explain the various types of attacks on computer and network security from malicious logic and intruders.
- Explain how to analyze the various vulnerabilities in the system which can compromise the security.
- Explain how auditing is essential to detect intrusion or suspicious activities in the system.
- Explain the process involved to provide security with respect to network, system, user and program.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks.
- Any two assignment methods mentioned in the 22OB4.2, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks).
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Text Book

1. William Stallings, "Cryptography and Network Security Principles and Practice", Pearson Education Inc., 6th Edition, 2014, ISBN: 978-93-325-1877-3
2. Atul Kahate, "Cryptography and Network Security", TMH, 2003.
3. Matt Bishop, Sathyanarayana S Venkatramanayya, "Introduction to Computer Security", Pearson Education, 2006, ISBN 81-7758-425-1

Reference Books

1. Cryptography and Network Security, Behrouz A Forouzan, TMH, 2007.

Web links and Video Lectures (e-Resources):

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

1. Experiential Learning by using free and open-source software's SCILAB or OCTAVE or Python

Machine Learning for VLSI Course Code: BVL714C / **03 credits**

Course Learning Objectives:

- Students will focus on the **Register Transfer Level (RTL) design phase**, gaining a deep understanding of this critical stage in VLSI chip design.
- The course emphasizes the application of **machine learning techniques** from RTL design and verification through to synthesis.
- Students will explore how machine learning enhances traditional design strategies by offering intelligent solutions that improve **accuracy, speed, and resource efficiency** across the VLSI design pipeline.

Module – 1

Linear and Logistic Regression Introduction: Aims and applications of machine learning, learning systems, various aspects of developing a learning system, Linear and Logistic Regression: Linear regression, Decision trees, overfitting

Module – 2

Instance based learning: Instance based learning, Feature reduction, Collaborative filtering-based recommendation. Bayesian learning: Probability and Bayes learning

Module – 3

Logistic Regression & Neural Network: Logistic Regression, Support Vector Machine, Kernel function and Kernel SVM Neural network: Perceptron, multilayer network, backpropagation, introduction to deep neural network

Module – 4

Computational learning: Computational learning theory, PAC learning model, Sample complexity, VC Dimension, Ensemble learning Clustering: k-means, adaptive hierarchical clustering, Gaussian mixture model

Module – 5

Machine Learning in VLSI Design: A Taxonomy for Machine Learning in VLSI Design Machine Learning for Lithographic Process Models: Masks, and Physical Design, Yield Enhancements, Machine Learning based Aging Analysis Machine Learning Hardware: Energy-Efficient Design of Advanced Machine Learning Hardware

Text Books:

1) Pattern Recognition and Machine Learning. Berlin: Springer-Verlag., Bishop, C., 2006.

2) Machine Learning in VLSI Computer-Aided Design., Elfadel, Ibrahim M., Duane S. Boning, and Xin Li, eds, Springer, 2019.

References:

1) Introduction to Machine Learning, Ethem Alpaydin, PHI,2006.
2) The Elements of Statistical Learning Data Mining, Inference, and Prediction, Trevor Hastie, Robert Tibshirani, Jerome Friedman, Second Edition, 2009.

Course Outcomes:

C01: Understand the objectives, practical applications, categories, and key design considerations involved in machine learning techniques. *(Level 2)*

CO2: Evaluate and compare various machine learning algorithms. *(Level 3)*

CO3: Explain the role and implementation of machine learning in VLSI computer-aided design. *(Level 3)*

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks(18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions(for 100 marks), selecting one full question from each module.

Marks scored shall be proportionally reduced to 50 marks.

MICROFABRICATION and MEMS

Semester 7

Course Code **BVL5714D** CIE Marks 50
Teaching Hours/Week (L: T:P: S) 3:0:0 SEE Marks 50
Total Hours of Pedagogy 40 Total Marks 100
Credits 03 Exam Hours 03
Examination type (SEE) THEORY

Course objectives:

This course will enable students to:

- Identify the typical materials used for fabrication of micro systems explain the principles of standard micro fabrication techniques
- Describe the challenges in the design and fabrication of Micro systems
- Identify commonly used mechanical structures in MEMS.
- Explain the application of scaling laws in the design of micro systems
- Describe the working principles and applications of micro sensors and actuators

Teaching-Learning Process (General Instructions):

These are sample Strategies teachers can use to accelerate the attainment of the various course outcomes.
1. Lecture method (L) does not mean only traditional lecture method; different teaching methods may be adopted to develop the outcomes.
2. Encourage collaborative (Group) Learning in the class.
3. Ask at least three HOTS (Higher Order Thinking) questions in the class, which promotes Critical thinking.
4. Adopt Problem-Based Learning (PBL), which fosters students' Analytical skills, and develops thinking skills such as evaluating, generalizing, and analyzing information rather than simply recalling it.
5. Topics will be introduced in a multiple representation.
6. Show the different ways to solve the same problem and encourage the students to come up With creative ways to solve them.
7. Discuss how every concept can be applied to the real world and when that's possible, it helps improve the student's understanding.
8. Adopt the Flipped class technique by sharing the materials/Sample Videos before the class and having discussions on the topic in the succeeding classes.

Module-1

Materials for MEMS – Silicon – Silicon compounds – Silicon Nitride, Silicon Dioxide, Silicon carbide, Poly Silicon, GaAs , Silicon Piezo resistors. Polymers in MEMS – SU-8, PMMA, PDMS, Langmuir – Blodgett Films.
Micro System fabrication – Photolithography – Ion implantation- Diffusion – Oxidation – Chemical vapour deposition – Etching

Module-2

Overview of Micro manufacturing – Bulk micro manufacturing, Surface micro machining , LIGA process –Microstereo lithography
Micro system Packaging: general considerations in packaging design – Levels of Micro system packaging. Bonding techniques for MEMS: Surface bonding, Anodic bonding, Silicon - on - Insulator, wire bonding, Sealing – Assembly of micro systems.

Module-3

Review of Mechanical concepts: Stress, Strain, Modulus of Elasticity, yield strength, ultimate strength – General stress strain relations – compliance matrix. Overview of commonly used mechanical structures in MEMS - Beams, Cantilevers, Plates, Diaphragms – Typical applications

Flexural beams: Types of Beams, longitudinal strain under pure bending – Deflection of beams – Spring constant of cantilever – Intrinsic stresses

Module-4

Scaling laws in miniaturization - scaling in geometry, scaling in rigid body dynamics, Trimmer force scaling vector, scaling in electrostatic and electromagnetic forces, scaling in electricity and fluidic dynamics, scaling in heat conducting and heat convection.

Module-5

MEMS and Microsystems: Applications – multidisciplinary nature of MEMS – principles and examples of Micro sensors and micro actuators – micro accelerometer –comb drives - Micro grippers – micro motors, micro valves, micro pumps, Shape Memory Alloys.

Actuation and Sensing techniques: Thermal sensors and actuators, Electrostatic sensors and actuators, Piezoelectric sensors and actuators, magnetic actuators

Overview of MEMS areas : RF MEMS, BioMEMS, MOEMS, NEMS

Course Outcomes (Course Skill Set)

Upon successful completion of this course, students will be able to:

CO1: Recognize common materials used in micro system fabrication and explain the core principles behind standard microfabrication techniques.

CO2: Analyze the key challenges associated with the design, fabrication, and packaging of microsystems.

CO3: Identify widely used mechanical structures in Micro-Electro-Mechanical Systems.

CO4: Apply scaling laws to the design of microsystems, with a focus on the effects of miniaturization.

CO5: Explain the operating principles and practical applications of various micro sensors and actuators.

1. .

Suggested Learning Resources:

Text Book:

1. Chang Liu, Foundations of MEMS, Pearson 2012
2. Tai-Ran Hsu, MEMS and Microsystems Design and Manufacture, TMH, 2002

Reference Books:

1. Chang C Y and Sze S. M., VLSI Technology, McGraw-Hill, New York, 2000
2. Julian W Gardner, Microsensors: Principles and Applications, John Wiley & Sons, 1994
3. Mark Madou, Fundamentals of Micro fabrication, CRC Press, New York, 1997
4. Stephen D. Senturia, Microsystem design, Springer (India), 2006.
5. Thomas B. Jones, Electromechanics and MEMS, Cambridge University Press, 2001
6. Gregory T.A. Kovacs, Micromachined Transducers Sourcebook, McGraw Hill, 1998

Assessment Details (both CIE and SEE)

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Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
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- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions(for 100 marks), selecting one full question from each module. Marks scored shall be proportionally reduced to 50 marks.

E-Waste Management		Semester	7
Course Code	**BEC 715A**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03
Examination type (SEE)	Theory		

Course objectives:

- **Understanding e-waste**: To learn about e-waste, its different types, and how it's generated
- **E-waste rules and directives**: To understand the rules and directives for e-waste in different countries
- **E-waste management**: To learn how to manage e-waste throughout its life cycle
- **Environmental and health impacts**: To understand the environmental and health impacts of e-waste

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
2. Show Video/animation films to explain the functioning of various techniques.
3. Encourage collaborative (Group) Learning in the class.
4. Ask at least three HOTS(Higher-order Thinking)questions in the class, which promotes critical thinking
5. Topics will be introduced in multiple representations.
6. Discuss how every concept can be applied to the real world-and when that's possible, it helps improve the students' understanding.

Module-1

Introduction: Preamble, What is e-waste, E-waste Sources and generation, Growth of Electrical and Electronics Industry in India, Global Context of e-waste Management, Indian Scenario on e-waste Management,

E-WASTE: E-waste Definition, Classification of e-waste, Characterization of e-waste

Text 1: Chapter 1 & 2

Module-2

Regulatory Framework: Global e-waste Regulations, Waste Electronics and Electrical Equipment (WEEE Directive 82), International norms – Basel Convention, Evolution of e-waste regulations in India, E-waste Management Rules 2016 (amendments to 2011 Rules), Regulatory Compliance Mechanisms, E-waste Management Guidelines (Text 1: 3.1 to 3.7)

Module-3

Extended Producer Responsibility (EPR): E-waste – A post Consumer Waste, E-waste value Chain, E-waste Collection Systems, Extended Producer Responsibility (EPR), Collective Responsibility, Producer Responsible Organization (PRO) (Text 2: 4.1 to 4.6)

Module-4

E-Waste Handling: Characterization & Classification, Packaging and Labelling, Transportation, Storage, Safety in Handling – Precautionary Principles: Text 1- Chapter 5

Module-5

Restrictions on Use of Hazardous Substances (ROHS): Hazardous substances in e-waste, Global ROHS compliances (ROHS Directive 84), ROHS compliance requirements in India: Text 1: Chapter 6

E-Waste Recycling: E-waste Recycling Operations, Dismantling & Segregation, Recycling & Recovery, Recycling Technologies – Text 1: Chapter 7 (7.1 to 7.4)

Course outcome (Course Skill Set)

At the end of the course, the student will be able to:

1. Understand the environmental impacts of e-waste
2. Distinguish the role of various national and internal act and laws applicable for e-waste management and handling
3. Analyse the e-waste handling methods & restrictions
4. Analyze the e-waste recycling techniques

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25 marks.
- The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.
- For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Text Books

1. Lakshmi Raghupathy, Introduction to E-Waste Management, TERI Press, New Delhi

Reference Books:

1. Johri R., E-waste: implications, regulations, and management in India and current global best practices, TERI Press, New Delhi

Web links and Video Lectures (e-Resources):

- https://news.mit.edu/2013/ewaste-mit

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Conduct market survey for the generated e-waste and its management and prepare a report
- Field visit to explore the possibility of various e-waste management techniques

	Embedded Systems Applications		Semester	7
	Course Code	**BTE715C**	CIE Marks	50
	Teaching Hours/Week (L: T:P: S)	3:0:0:0	SEE Marks	50
	Total Hours of Pedagogy	40	Total Marks	100
	Credits	03	Exam Hours	03
	Examination type (SEE)	Theory		

Course objectives:

- Understand the fundamental concepts, characteristics, and applications of embedded systems across various domains.
- Analyse the hardware components of embedded systems, including microcontrollers, memory, and low-power design techniques.
- Explore the role of sensors, ADCs, and actuators in embedded systems, and their interfacing with digital systems.
- Apply embedded systems design principles in real-world applications such as mobile phones, automotive electronics, RFID, and biomedical systems.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
2. Show Video/animation films to explain the functioning of various EV Architectures.
3. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyse information rather than simply recall it.
4. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

Introduction to embedded systems: Application domain of embedded systems, desirable features and general characteristics of embedded systems, model of an embedded system, microprocessor Vs microcontroller, example of a simple embedded system, figure of merit for an embedded system, classification of MCUs: 4/8/16/32 bits, history of embedded systems, current trends.

(Text: 1.1 to 1.9)

Module-2

Embedded systems-The hardware point of view: Microcontroller unit (MCU), The Processor, The Harvard Architecture, A popular 8-bit MCU: General Purpose I/O (GPIO), Clock; Memory for embedded systems: Semiconductor Memory, Random Access Memory (RAM), Static RAM (SRAM), An SRAM Chip. Low Power Design, Pull up and Pull Down Resistors.

(Text: 2.1 to 2.2.2, 2.3 to 2.3.2.2 and 2.4 to 2.5)

Module-3

Sensors, ADCs and Actuators

Sensors: Temperature Sensor, Light Sensor, Proximity/range Sensor; Analog to digital converters: ADC Interfacing, Control Interface, Data Interface; Actuators: Displays, Light Emitting Diodes (LED), Seven Segment LED; Motors: Stepper Motors, DC Motors.

(Text: 3.1.1 to 3.1.3, 3.2 to 3.2.1.2, 3.3 to 3.3.1.2 and 3.3.2 to 3.3.2.2)

Module-4

	Examples of embedded systems: Mobile phone, Automotive electronics, Radio Frequency Identification (RFID), Wireless Sensor Networks (WISENET), Robotics, Biomedical applications, Brain machine interface. (Text: 4.1 to 4.7)
	Module-5
	Embedded Design-A Systems Perspective: A Typical Example, Product Design, The Design Process, Testing, Bulk Manufacturing. (Text: 18.1 to 18.5)

Course outcome (Course Skill Set)

At the end of the course, the student will be able to:

1. Understand the fundamental concepts and characteristics of embedded systems, including their classification and modern trends.
2. Analyse the architecture and hardware components of MCUs and their role in embedded systems.
3. Apply knowledge of sensors, ADCs, and actuators for interfacing and control in embedded systems.
4. Evaluate real-world embedded system applications such as mobile phones, automotive electronics, RFID, and robotics.
5. Develop an understanding of the embedded design process, from concept to bulk manufacturing, including testing and product design.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25 marks.
- The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.
- For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Books

1. Das, LyLa B.. Embedded Systems: An Integrated Approach. India: Pearson Education India, ISBN 9788131787663, 2013.

Web links and Video Lectures (e-Resources):

- Embedded Systems: https://nptel.ac.in/courses/108102045
- Embedded Systems Design: https://onlinecourses.nptel.ac.in/noc20_cs14/preview
- Android Mobile Application Development: https://onlinecourses.swayam2.ac.in/nou24_ge66/preview

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Conduct market survey for latest home appliances and compare specifications of reputed brands and prepare a report
- Students can interface a temperature sensor with an ADC and display the digital output on a seven-segment display, demonstrating sensor integration with actuators.

Introduction to Mathlab Programming		Semester	7
Course Code	**BVL 715D**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03
Examination type (SEE)	Theory		

Course Objectives:

- To introduce the students to MATLAB as programming and scientific computing tool.
- To enable the students to solve basic problems and matrix operations using MATLAB.
- To introduce the students to basic numerical techniques to solve first order ordinary differential equations, numerical integration
- To familiarize the students with basic plotting tools available in MATLAB

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
2. Show Video/animation films to explain the functioning of various techniques.
3. Encourage collaborative (Group) Learning in the class.
4. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking
5. Topics will be introduced in multiple representations.
6. Discuss how every concept can be applied to the real world-and when that's possible, it helps improve the students' understanding.

Module-1

Starting MATLAB, working in command window, arithmetic operations, display formats, elementary maths built in functions, defining scalar variables, useful command for managing variables, script files.

Module-2

One and Two dimensional arrays, addition and subtraction, array multiplication and division, element-by-element operations, generation of random numbers, analyzing arrays using built-in maths functions. Math lab program to access specific numbers in arrays using their position. Math lab to generate of random numbers.

Module-3

Basic plot commands: plot, fplot, formatting a plot, subplots, basic 2D and 3D plots: Line plots, mesh and surface plots, contour, View command, To create subplots and application of view command

Module-4

Conditional statements, loops, nested loops, application of break and continue commands, To write simple programs involving loops using commands like for, while, if-else, return, etc.

Module-5

Algebraic equations: Eigen values, Eigen vectors, solution of a system of linear equations. Introduction to ordinary differential equations (ODE), solution of first order ODE, numerical techniques: Trapezoidal rule, Simpson's rule.

Program to evaluate the Eigen values and Eigen vectors of a given matrix

, to solve a system of linear equations using Gauss elimination method and Gauss Seidel method , to solve a first order ODE by Euler's method and Runge Kutta method

Course outcome (Course Skill Set)

Course Outcomes

After completing this course, learners will be able to:

1. Gain a broad understanding of MATLAB and its core functionalities.
2. Effectively utilize MATLAB for data analysis and visualization.
3. Demonstrate a solid understanding of MATLAB's fundamental data structures and apply them proficiently.
4. Create and manage basic plots, graphical user interface (GUI) components, and graphical objects within MATLAB.
5. Develop simple MATLAB programs to solve numerical problems such as systems of linear equations, numerical integration, and ordinary differential equations (ODEs).

Assessment Details (both CIE and SEE)

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1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

1. **Text Book:**

A Guide to MATLAB - for Beginners and Experienced Users", 2nd Ed., Brian R. Hunt, Ronald L. Lipsman, Jonathan M. Rosenberg, Cambridge University Press, 2006.

Reference Books:

1. Pratap Rudra, Getting started with MATLAB: A quick Introduction for Scientist and Engineers, Oxford University Press, 2010.

2. Wolfram S., The Mathematica, Cambridge University Press, 2003.