SEMESTER – V

VLSI Fabrication Technology

Course Code	**BVL515D**	CIE Marks	50
Number of Lecture Hours/Week	03	SEE Marks	50
Total Number of Lecture Hours	40(08Hours/Module)	Exam Hours	03

CREDITS-03

Course Learning Objectives: This course will enable the students to:

- Understand the Fabrication Process of IC Technology
- Understand the concept of conversion of a single crystal of silicon into an IC requires.
- Exposer to different fabrication steps such as epitaxy, oxidation, chemical vapor deposition, metallization.
- Understand the concepts of ion implantation, etching and lithography.

MODULE-1	RBT Level
VLSI Process Integration: Introduction , Fundamental Considerations for IC Processing, NMOS IC Technology , CMOS IC Technology ,MOS Memory IC Technology , IC Fabrication. **Text 1.** 11.1 ,11.2, 11.3, 11.4 , 11.5, 11.7	**L1,L2,L3**
MODULE-2	
Crystal Growth and Wafer Preparation: Introduction , Electronic grade Silicon , Czochralski Crystal Growing , Silicon Shaping , Processing Considerations **Text 1.** 1.1 ,1.2, 1.3, 1.4 , 1.5	**L1,L2,L3**
MODULE-3	
Epitacy :Introduction , Vapor Phase Epitaxy , Molecular Beam Epitaxy, Silicon on Insulators , Epitaxial Evaluation . **Oxidation :** Introduction , Growth Mechanism and Kinematics , Thin Oxides ,Oxidation Techniques and Systems .Oxidation of Polysilicon **Text 1.** 2.1 ,2.2,2 .3, 2.4 , 2.5 ,3.1 ,3.2, 3.3, 3.4,3.7	**L1,L2**
MODULE-4	
Lithography : Introduction , Optical Lithography , Electron Lithography , Ion Lithography , Plasma properties , Feature size control and Anisotropic Etch Mechanism, Reactive Plasma Etching Techniques and Equipment , Specific Etch Process . **Text 1.** 4.1 ,4.2, 4.3, 4.5 , 5.2, 5.3,5.6 .	**L1,L2**
MODULE-5	
Dielectric and Polysilicon Film Deposition : Introduction , Deposition Process ,Polysilicon, Silicon Dioxide , Automatic Diffusion Mechanism, Measurement Techniques, Range Theory, Metalization , Metalization Applications ,Metalization Choices , Patterning, Metalization Problems. **Text 1.** 6.1 ,6.2,6.3,6.4 , 7.4, 7.6,8.2,9.2 ,9.3,9.5 ,9.6	**L1,L2, L3**

Course Outcomes: After studying this course, students will be able to:

1. Understand the basic steps of MOS transistor fabrication.
2. Learn the basics theory of Crystal Growth and Wafer Preparation.
3. Students understands theconcepts of Epitaxy, Diffusion, Oxidation, Lithography and Etching.
4. Understands the process of film deposition and metallization in Chip manufacturing

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks(18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.

Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks

Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)

The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

The question paper will have ten questions. Each question is set for 20 marks.

There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions(for 100 marks), selecting one full question from each module.

4. Marks scored shall be proportionally reduced to 50 marks.

TEXT BOOKS

1. S.M.Sze"VLSI Technology", McGraw Hill Companies Inc. (2nd Edition)"
2. C.Y. Chang and S.M.Sze (Ed), "ULSI Technology", McGraw Hill Companies Inc.

REFERENCE BOOKS

1. Stephena, Campbell, "The Science and Engineering of Microelectronic Fabrication",Second Edition, Oxford University Press.
2. James D.Plummer, Michael D.Deal, "Silicon VLSI Technology" Pearson Education
3. VLSI Technology by Wai-Kai Chen Editor in Chief CRC press