DIGITAL SYSTEM DESIGN USING VERILOG			
Course Code	BUE503	Semester	V
Teaching Hours/Week (L:T:P: S)	4:0:0:0	CIE Marks	50
Total Hours of Pedagogy	50	SEE Marks	50
Credits	04	Total Marks	100
Examination type (SEE)	Theory	Exam Hours	3 Hours

Course objectives:

1. To know the basic language features of Verilog HDL and the role of HDL in digital logic design.
2. To know the behavioural modeling of combinational and simple sequential circuits.
3. To know the behavioural modeling of algorithmic state machines.
4. To know the synthesis of combinational and sequential descriptions.
5. To know the architectural features of programmable logic devices.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Chalk and Talk
2. PowerPoint Presentation and Videos
3. Flipped Classes
4. Practice session

Module-1

Introduction to Digital Design Methodology: Design Methodology-An Introduction, IC Technology Options.

Review of Combinational Logic Design: Glitches and Hazards

Introduction to Logic Design with Verilog : Structural models of combination logic, logic system, design verification and Test methodology, propagation delay, truth table models of combinational and sequential logic with verilog modules.

RBT Level: L1,L2

Module-2

Logic Design With Behavioral Models of Combinational And Sequential Logic: Behavioral modeling, A Brief Look at data types for behavioural modeling, Boolean Equation-Based behavioral models of combinational logic, propagation delay and continuous assignments, lathes and level sensitive circuits in verilog, cyclic behavioural models of flip flops and latches, cyclic behavior and edge detection, a comparison of styles for behavioral modelling. Behavioral Models of Multiplexers, Encoders, and Decoders, Dataflow Models of a Linear-Feedback Shift Register, Design Documentation with Functions and Tasks: Legacy or Lunacy?

RBT Level: L1,L2,L3

Module-3

Logic Design With Behavioral Models of Combinational And Sequential Logic: Algorithmic State Machine Charts for Behavioral Modeling, Behavioral Models of Counters, Shift Registers, and Register Files

Synthesis of Combinational and Sequential Logic: Introduction to Synthesis, Synthesis of Combinational Logic, Synthesis of Sequential Logic with Latches.

RBT Level: L1,L2,L3

Module-4

Fundamentals of Sequential Logic Design: Design of Sequential Machines, State-Transition Graphs, Design Example: BCD to Excess-3 Code Converter, Serial-Line Code Converter for Data Transmission.

Synthesis of Combinational and Sequential Logic: Synthesis of Explicit State Machines, Synthesis of Implicit State Machines, Registers and Counters.

RBT Level: L1,L2,L3

Module-5

Programmable Logic and Storage Devices : Programmable Logic Devices, Storage Devices, Programmable Logic Array (PLA), Programmable Array Logic (PAL), Programmability of PLDs ,Complex PLDs (CPLDs) ,Field-Programmable Gate Arrays.

RBT Level: L1,L2

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

1. Demonstrate knowledge on HDL design flow, digital circuits design.
2. Design and develop the combinational and sequential circuits using behavioural modelling.
3. Solving algorithmic state machines using hardware description language.
4. Analyse the process of synthesizing the combinational and sequential descriptions.
5. Memorizing the advantages of programmable logic devices and their description in Verilog.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.

Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Textbooks:

1. Michael D Ciletti - Advanced Digital Design with the VERILOG HDL, 2ND Edition, PHI, 2009

Reference Books:

1. Stephen Brown and ZvonkoVranesic - Fundamentals of Digital Logic with Verilog, 2nd Edition, TMH, 2008.
2. Z Navabi - Verilog Digital System Design, 2nd Edition, McGraw Hill, 2005.

Web links and Video Lectures (e-Resources):

• https://nptel.ac.in/
Activity Based Learning (Suggested Activities in Class)/ Practical Based learning: • Online Resources and Tutorials • Verilog Simulation Projects • Quiz • Seminars

Sir,

Modification required in the Syllabus. Teaching hours/week given are 4:0:0:0 for credits 4.

19/11/24

Sir, for kind needful

19/11/24