Electric Circuit Analysis			
IPCC Course Code	BEE301	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40 hours	Total Marks	100
Credits	03	Exam Hours	03

Course objectives:

- To familiarize the basic laws, source transformations, theorems and the methods of analyzing electrical circuits.
- To explain the use of network theorems and the concept of resonance.
- To familiarize the analysis of three-phase circuits, two port networks and networks with non-sinusoidal inputs.
- To explain the importance of initial conditions, their evaluation and transient analysis of R-L and R-C circuits.
- To impart basic knowledge on network analysis using Laplace transforms.

Teaching-Learning Process (General Instructions)

These are sample Strategies; which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecturer method (L) needs not to be only traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes.
2. Use of Video/Animation to explain functioning of various concepts.
3. Encourage collaborative (Group Learning) Learning in the class.
4. Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyse information rather than simply recall it.
6. Introduce Topics in manifold representations.
7. Show the different ways to solve the same problem with different circuits/logic and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

MODULE-1

Basic Concepts: Active and passive elements, Concept of ideal and practical sources. star – delta transformation.

Analysis of networks by (i) Network reduction method (ii) Mesh and Node voltage methods for ac and DC circuits with independent and dependent sources. Concept of Super-Mesh and Super node analysis Duality.

Teaching-Learning Process	Chalk and Board, Problem based learning.

MODULE-2

Network Theorems: Super Position theorem, Thevenin's theorem, Norton's theorem, and Maximum power transfer theorem. Analysis of networks (only with independent AC and D C sources).

Teaching-Learning Process	Chalk and Board, Problem based learning.

MODULE-3

Resonant Circuits: Analysis of simple series RLC and parallel RLC circuits under resonances. Problems on Resonant frequency, Bandwidth and Quality factor at resonance

Transient Analysis: Behavior of circuit elements under switching action, Evaluation of initial and final conditions. Transient analysis of RL and RC circuits under DC excitations.

Teaching-Learning Process	Chalk and Board, Problem based learning.

MODULE-4

Laplace Transformation (LT): Laplace transformation definition, LT of Impulse, Step, Ramp, Sinusoidal signals and shifted functions, periodic functions. Waveform synthesis. Initial and Final value theorems.

Teaching-Learning Process	Chalk and Board, Problem based learning.

MODULE 5

Unbalanced Three Phase Systems: Analysis of three phase systems, calculation of real and reactive Powers and analysis as applicable to star/delta connected load.

Two Port networks: Definition, Open circuit impedance, Short circuit admittance, h-parameters and Transmission parameters and their evaluation for simple circuits.

Teaching-Learning Process	Chalk and Board, Problem based learning.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

1. Understand the basic concepts, basic laws and methods of analysis of DC and AC networks and reduce the complexity of network using source shifting, source transformation and network reduction using transformations.
2. Solve complex electric circuits using network theorems.
3. Discuss resonance in series and parallel circuits and also the importance of initial conditions and their evaluation.
4. Synthesize typical waveforms using Laplace transformation.
5. Solve unbalanced three phase systems and also evaluate the performance of two port networks.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25 marks.

The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered

Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.

For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

The question paper will have ten questions. Each question is set for 20 marks.

There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module. Marks scored shall be proportionally reduced to 50 marks

Suggested Learning Resources:

(1)Engineering Circuit Analysis, William H Hayt et al, Mc Graw Hill, 8th Edition,2014.

(2)Network Analysis, M.E. Vanvalkenburg, Pearson, 3rd Edition,2014.

(3)Fundamentals of Electric Circuits, Charles K Alexander Matthew N O Sadiku, Mc Graw Hill, 5th Edition, 2013.

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Activity Based Learning, Quizzes, Seminars.

Analog Electronic Circuits		Semester	III
Course Code	BEE302	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:2:0	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory + 8-10 Lab slots	Total Marks	100
Credits	04	Exam Hours	03
Examination nature (SEE)	Theory		

Course objectives:

- To provide the knowledge for the analysis of transistor biasing and thermal stability circuits.
- To develop skills to design the electronic circuits like amplifiers, power amplifiers and oscillators.
- To understand the importance of FET and MOSFET and FET/MOSFET amplifiers

Teaching-Learning Process (General Instructions)

These are sample Strategies; that teachers can use to accelerate the attainment of the various course outcomes.

1. Lecturer method (L) needs not to be only traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes.
2. Use of Video/Animation to explain functioning of various concepts.
3. Encourage collaborative (Group Learning) Learning in the class.
4. Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyze information rather than simply recall it.
6. Introduce Topics in manifold representations.
7. Show the different ways to solve the same problem with different circuits/logic and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world-and when that's possible, it helps improve the students' understanding.

MODULE-1

Diode Circuits: Diode clipping and clamping circuits.

Transistor Biasing and Stabilization:

The operating point, load line analysis, DC analysis and design of fixed bias circuit, emitter stabilized bias circuit, collector to base bias circuit, voltage divider bias circuit, modified DC bias with voltage feedback.

Bias stabilization and stability factors for fixed bias circuit, collector to base bias circuit and voltage divider bias circuit, bias compensation, Transistor switching circuits.

MODULE-2

Transistor at Low Frequencies:

Hybrid model, h-parameters for CE, CC and CB modes, mid-band analysis of single stage amplifier, simplified hybrid model, analysis for CE, CB and CC(emitter voltage follower circuit) modes, Millers Theorem and its dual, analysis for collector to base bias circuit and CE with un bypassed emitter resistance.

Transistor frequency response:

General frequency considerations, effect of various capacitors on frequency response, Miller effect capacitance, high frequency response, hybrid - pi model, CE short circuit current gain using hybrid pi model, multistage frequency effects.

MODULE-3

Multistage amplifiers:

Cascade connection , analysis for CE-CC mode, CE-CE mode, CASCODE stage-unbypassed and bypassed emitter resistance modes, Darlington connection using h-parameter model.

Feedback Amplifiers:

Classification of feedback amplifiers, concept of feedback, general characteristics of negative feedback amplifiers, Input and output resistance with feedback of various feedback amplifiers, analysis of different practical feedback amplifier circuits.

MODULE-4
Power Amplifiers: Classification of power amplifiers, Analysis of class A, Class B, class C and Class AB amplifiers, Distortion in power amplifiers, second harmonic distortion, harmonic distortion in Class B amplifiers, cross over distortion and elimination of cross over distortion. **Oscillators:** Concept of positive feedback, frequency of oscillation for RC phase oscillator, Wien Bridge oscillator, Tuned oscillator circuits, Hartley oscillator, Colpitt's oscillator , crystal oscillator and its types.
MODULE-5
FETs: Construction, working and characteristics of JFET and MOSFET(enhance and Depletion type) Biasing of JFET and MOSFET. Fixed bias configuration, self bias configuration, voltage divider biasing. Analysis and design of JFET (only common source configuration with fixed bias) and MOSFET amplifiers.

PRACTICAL COMPONENT OF IPCC

Sl.NO	Experiments
1	Experiments on series, shunt and double ended clippers and clampers.
2	Design and Testing of Full wave – centre tapped transformer type and Bridge type rectifier circuits with and without Capacitor filter. Determination of ripple factor, regulation and efficiency.
3	Static Transistor characteristics for CE, CB and CC modes and determination of h parameters.
4	Frequency response of single stage BJT and FET RC coupled amplifier and determination of half power points, bandwidth, input and output impedances.
5	Design and testing of BJT -RC phase shift oscillator for given frequency of oscillation.
6	Design and testing of Wien bridge oscillator for given frequency of oscillation
7	Design and testing of Hartley and Colpitt's oscillator for given frequency of oscillation
8	Determination of gain, input and output impedance of BJT Darlington emitter follower with and without bootstrapping.
9	Design and testing of Class A and Class B power amplifier and to determine conversion efficiency.
10	Testing of a transformer less Class – B push pull power amplifier and determination of its conversion efficiency.

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

1. Utilize the characteristics of transistor for different applications.
2. Design and analyze biasing circuits for transistor.
3. Design, analyze and test transistor circuitry as amplifiers and oscillators

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

CIE for the theory component of the IPCC (maximum marks 50)

- IPCC means practical portion integrated with the theory of the course.
- CIE marks for the theory component are **25 marks** and that for the practical component is **25 marks**.
- 25 marks for the theory component are split into **15 marks** for two Internal Assessment Tests (Two Tests, each of 15 Marks with 01-hour duration, are to be conducted) and **10 marks** for other assessment methods mentioned in 22OB4.2. The first test at the end of 40-50% coverage of the syllabus and the second test after covering 85-90% of the syllabus.
- Scaled-down marks of the sum of two tests and other assessment methods will be CIE marks for the theory component of IPCC (that is for **25 marks)**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the theory component of IPCC.

CIE for the practical component of the IPCC

- **15 marks** for the conduction of the experiment and preparation of laboratory record, and **10 marks** for the test to be conducted after the completion of all the laboratory sessions.
- On completion of every experiment/program in the laboratory, the students shall be evaluated including viva-voce and marks shall be awarded on the same day.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to **15 marks**.
- The laboratory test **(duration 02/03 hours)** after completion of all the experiments shall be conducted for 50 marks and scaled down to **10 marks.**
- Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **25 marks**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the practical component of the IPCC.

SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scoredby the student shall be proportionally scaled down to 50 Marks

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper may include questions from the practical component.

Suggested Learning Resources:

Text Books

1. Electronic Devices and Circuit Theory, Robert L Boylestad Louis Nashelsky, Pearson, 11th Edition, 2015

2. Electronic Devices and Circuits, Millman and Halkias, Mc Graw Hill, 4th Edition, 2015

3. Electronic Devices and Circuits, David A Bell, Oxford University Press, 5th Edition, 2008

Reference Books

1. Microelectronics CircuitsAnalysis and Design, Muhammad Rashid, Cengage Learning, 2nd Edition, 2014

2. A Text Book of Electrical Technology, Electronic Devices and Circuits, B.L. Theraja, A.K. Theraja, S. Chand,

Reprint, 2013
3. Electronic Devices and Circuits, Anil K. Maini, ,VashaAgarval, Wiley, 1st Edition, 2009
4. Electronic Devices and Circuits, S. Salivahanan, Suresh, Mc Graw Hill, 3rd Edition, 2013
5. Fundamentals of Analog Circuits, Thomas L Floyd, Pearson, 2nd Edition, 2012

Web links and Video Lectures (e-Resources):

www.nptel.ac.in

https://www.ti.com/design-resources/design-tools-simulation/analog-circuits/overview.html

https://www.analog.com/en/education/education-library/tutorials/analog-electronics.html

DIGITAL LOGIC CIRCUITS		Semester	III
Course Code	**BEE 303**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:2:0	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory + 8-10 Lab slots	Total Marks	100
Credits	04	Exam Hours	03
Examination nature (SEE)	Theory		

Course objectives:

- To illustrate simplification of algebraic equations using Karnaugh Maps and Quine-McClusky methods
- To design decoders, encoders, digital multiplexer, adders, subtractors and binary comparators
- To explain latches and flip-flops , registers and counters
- To analyze Melay ad Moore Models
- To develop state diagrams synchronous sequential circuits
- To understand the applications of sequential circuits

Teaching-Learning Process (General Instructions)

These are sample Strategies; that teachers can use to accelerate the attainment of the various course outcomes.

1. Lecturer method (L) needs not to be only traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes.
2. Use of Video/Animation to explain functioning of various concepts.
3. Encourage collaborative (Group Learning) Learning in the class.
4. Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyze information rather than simply recall it.
6. Introduce Topics in manifold representations.
7. Show the different ways to solve the same problem with different circuits/logic and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world-and when that's possible, it helps improve the students' understanding.

MODULE-1

Principles of Combinational Logic: Definition of combinational logic, canonical forms, Generation of switching equations from truth tables, Karnaugh maps-3,4,5 variables, Incompletely specified functions (Don‘t care terms) Simplifying Max term equations, Quine-McCluskey minimization technique, Quine-McCluskey using don‘t care terms, Reduced prime implicants Tables.

MODULE-2

Analysis and Design of Combinational logic: General approach to combinational logic design, Decoders, BCD decoders, Encoders, digital multiplexers, Using multiplexers as Boolean function generators, Adders and subtractors, Cascading full adders, Look ahead carry, Binary comparators.

MODULE-3

Flip-Flops: Basic Bistable elements, Latches, Timing considerations, The master-slave flip-flops (pulse triggered flip-flops): SR flip-flops, JK flip-flops, Edge triggered flip- flops, Characteristic equations.

MODULE-4

Flip-Flops Applications: Registers, binary ripple counters, synchronous binary counters, Counters based on shift registers, Design of a synchronous counter, Design of a synchronous mod-n counter using clocked T, JK, D and SR flip-flops.

MODULE-5
Sequential Circuit Design: Mealy and Moore models, State machine notation, Synchronous Sequential circuit analysis, Construction of state diagrams, counter design. Memories: Read only and Read/Write Memories, Programmable ROM, EPROM, Flash memory.

PRACTICAL COMPONENT OF IPCC

Sl.NO	Experiments
1	Simplification and realization of Boolean expressions using logic gates/Universal gates.
2	Realization of half/full adder and half/full subtractors using logic gates.
3	Realization of parallel adder/subtractors using 7483 chip- BCD to Excess-3 code conversion and Vice - Versa.
4	Design and implementation of 1-bit and 2-bit comparators using basic gates
5	Design and implementation of half/full adder and half/full subtractors using IC 74153
6	To realize the following flip-flops using NAND gates S-R flip-flop, D&T flip-flop
7	To realize the following flip-flops using IC7476 master-slave JK flip-flop
8	Realize the following shift registers using IC7495 a)Ring counter b)Johnson Counter
9	Realize the following shift registers using IC7495 a)SISO b)SIPO c)PISO d)PIPO
10	To design and implement: a)mod-N synchronous UP counter and down counter using 7476 JK Flip-Flop b)mod-N counter using IC 7490/7476 c)synchronous counter using IC 74192

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

- Explain the concept of combinational and sequential logic circuits
- Analyse and design combinational circuits
- Describe and characterize flip flops and its applications
- Design the sequential circuits using SR, JK, D and T flip-flops and Melay and Moore applications
- Design applications of combinational and sequential circuits
- Employ the digital circuits for different applications

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

CIE for the theory component of the IPCC (maximum marks 50)

- IPCC means practical portion integrated with the theory of the course.
- CIE marks for the theory component are **25 marks** and that for the practical component is **25 marks**.
- 25 marks for the theory component are split into **15 marks** for two Internal Assessment Tests (Two Tests, each of 15 Marks with 01-hour duration, are to be conducted) and **10 marks** for other assessment methods mentioned in 22OB4.2. The first test at the end of 40-50% coverage of the syllabus and the second test after covering 85-90% of the syllabus.
- Scaled-down marks of the sum of two tests and other assessment methods will be CIE marks for the theory component of IPCC (that is for **25 marks)**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the theory component of IPCC.

CIE for the practical component of the IPCC

- **15 marks** for the conduction of the experiment and preparation of laboratory record, and **10 marks** for the test to be conducted after the completion of all the laboratory sessions.
- On completion of every experiment/program in the laboratory, the students shall be evaluated including viva-voce and marks shall be awarded on the same day.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to **15 marks**.
- The laboratory test **(duration 02/03 hours)** after completion of all the experiments shall be conducted for 50 marks and scaled down to **10 marks.**
- Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **25 marks**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the practical component of the IPCC.

SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scoredby the student shall be proportionally scaled down to 50 Marks

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper may include questions from the practical component.

Suggested Learning Resources:

Books

1) John M Yarbrough , Digital logic applications and design, Thomson Learning, 2001.

2)Donald D Givone, Digital Principles and design, MC Graw Hill 2002

3)Charles H Roth Jr, Larry L Kinney, Fundamentals of logic design , Cengage Learning, 7th Edition

Reference books:

1)D.P.Kothari and J S Dhillon, -Digital circuits and design, Pearson, 2016

2)Morris Mano, Digital Design, PHI, 3rd edition

3)K.A. Navas, Electronics Lab Manual, Vol.1, PHI 5th edition, 2015.

Web links and Video Lectures (e-Resources):

- https://onlinecourses.nptel.ac.in/noc20_ee32/preview
- YouTube videos on digital electronics
- National Instruments: https://education.ni.com/teach/resources/1104/digital-electronics

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- To develop mini projects on digital electronics
- Simple applications like Smart Digital School Bell With Timetable Display, Stop and Go Queue Entry Manager System, Digital Car Turning and Braking Indicator, Digital Nameplate with Visitor Sensing, electronic watch dog etc
- Applications based on PLAs, FPGA, CPLD etc

Transformers and Generators		Semester	III
Course Code	BEE304	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03
Examination nature (SEE)	Theory		

Course objectives:

- To understand the construction, working and various tests of single phase Transformer.
- To understand the construction, working and parallel operation of three phase Transformer.
- To understand the construction, working and analysis of Synchronous Generator.
- To understand the construction, working of solar and wind power generators.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecturer method (L) needs not to be only traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes.
2. Use of Video/Animation to explain functioning of various concepts.
3. Encourage collaborative (Group Learning) Learning in the class.
4. Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyze information rather than simply recall it.
6. Introduce Topics in manifold representations.
7. Show the different ways to solve the same problem with different circuits/logic and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world-and when that's possible, it helps improve the students' understanding.

Module-1

Single phase Transformers:

Necessity of transformer, principle of operation, Types and construction, EMF equation, equivalent circuit, Operation of practical transformer under no-load and on-load with phasor diagrams. Losses and methods of reducing losses, efficiency and condition for maximum efficiency. Polarity test, Sumpner's test.

Open circuit and Short circuit tests, calculation of equivalent circuit parameters. Predetermination of efficiency, voltage regulation and its significance. Numerical.

Module-2

Three-phase Transformers: Introduction, Constructional features of three-phase transformers. Transformer connection for three phase operation– star/star, delta/delta and star/delta, comparative features. Labelling of three-phase transformer terminals.

Parallel Operation of Transformers: Necessity of Parallel operation, conditions for parallel operation– Single phase and three phase. Load sharing in case of similar and dissimilar transformers. Numerical.

Auto transformers and Tap changing transformers: Introduction to autotransformer-copper economy, equivalent circuit, no load and on load tap changing transformers. Numerical.

Module-3

Synchronous Generators: Construction, working, Armature windings, winding factors, EMF equation. Harmonics–causes, reduction and elimination. Armature reaction, Synchronous reactance, Equivalent circuit.

Synchronous Generators Analysis: Open circuit and short circuit characteristics, Assessment of reactance-short circuit ratio, Alternator on load. Voltage regulation. Voltage regulation by EMF and MMF methods. Excitation control for constant terminal voltage. Numerical.

Module-4

Synchronous Generators (Salient Pole): Effects of saliency, two-reaction theory, Parallel operation of generators and load sharing. Methods of Synchronization, Synchronizing power.

Performance of Synchronous Generators: Power angle characteristic (salient and non salient pole), power angle diagram, reluctance power, Capability curve for large turbo generators. Hunting and damper windings. Numerical.

Module-5

Wind power Generator –Basic components of wind energy conversion system, types of wind generators- Horizontal and vertical axis. Advantages and disadvantages of WECS.

Solar power generator - principle of solar cell, Basic Solar Photo voltaic, system for power generation, Advantages and disadvantages.

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

1. Explain the construction, working and various tests of single phase Transformer.
2. Explain the construction, working and parallel operation of three phase Transformer.
3. Explain the construction, working and analysis of Synchronous Generator.
4. Explain the construction, working of solar and wind power generators.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25 marks.
- The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.
- For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored sha ll be proportionally reduced to 50 marks

Suggested Learning Resources:

Textbooks

1. Electric Machines, D. P. Kothari, et al, 4th Edition, 2011.
2. Principals of Electrical Machines, V.K Mehta, Rohit Mehta, S Chand, 2nd edition, 2009
3. Non conventional Energy sources by G D Rai

Reference Books

1. Electric Machines, Mulukuntla S. Sarma, at el, Cengage, 1st Edition, 2009.
2. Electrical Machines, Drives and Power systems, Theodore Wildi, Pearson, 6th Edition, 2014.
3. Electric Machines, Ashfaq Hussain, Dhanpat Rai & Co, 2nd Edition, 2013.

Web links and Video Lectures (e-Resources):

- www.nptel.ac.in

Scilab / MATLAB for Transformers & Generators			
Course Code	**BEEL358A**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:0:2:0	SEE Marks	50
Credits	01	Exam Hours	02

Course objectives:

(1) Along with prescribed hours of teaching –learning process, provide opportunity to perform the experiments/programmes at their own time, at their own pace, at any place as per their convenience and repeat any number of times to understand the concept.

(2) Provide unhindered access to perform whenever the students wish.

(3) Vary different parameters to study the behavior of the circuit without the risk of damaging equipment/device or injuring themselves.

Sl. NO	Experiments
1	Open Circuit and Short circuit tests on single phase step up or step down transformer and predetermination of (i) Efficiency and regulation (ii) Calculation of parameters of equivalent circuit.
2	Sumpner's test on similar transformers and determination of combined and individual transformer efficiency.
3	Parallel operation of two dissimilar single-phase transformers of different kVA and determination of load sharing and analytical verification given the Short circuit test data.
4	Separation of hysteresis and eddy current losses in single phase transformer.
5	Voltage regulation of an alternator by EMF and MMF methods.
6	Voltage regulation of an alternator by ZPF method.
7	Power angle curve of synchronous generator.
8	Slip test – Measurement of direct and quadrature axis reactance and predetermination of regulation of salient pole synchronous machines.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

- Analyse in an intelligent manner, think better, and perform better.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination(SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8^{th} week of the semester and the second test shall be conducted after the 14^{th} week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to 20 marks (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

- SEE marks for the practical course is 50 Marks.
- SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University
- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. OR based on the course requirement evaluation rubrics shall be decided jointly by examiners.
- Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.
- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners. General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in - 60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)
- Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero. The duration of SEE is 03 hours.
- Rubrics suggested in Annexure-II of Regulation book.

555 IC Laboratory			
Course Code	**BEEL358B**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:0:2:0	SEE Marks	50
Credits	01	Exam Hours	02

Course objectives:

(1) Along with prescribed hours of teaching –learning process, provide opportunity to perform the experiments/programmes at their own time, at their own pace, at any place as per their convenience and repeat any number of times to understand the concept.

(2) Provide unhindered access to perform whenever the students wish.

(3) Vary different parameters to study the behaviour of the circuit without the risk of damaging equipment/device or injuring themselves.

Sl. NO	Experiments
1	Construct Astable Multivibrator circuit using IC-555 Timer.
2	Construct Mono-stable Multivibrator circuit using IC-555 Timer.
3	Construct and test Sequential timer using IC-555.
4	Generate Pulse Width Modulator (PWM) signal using IC-555 Timer.
5	Construct Burglar Alarm circuit using IC-555 Timer.
6	Construct and generate Frequency Shift Keying (FSK) signal using IC-555 Timer.
7	Construct and test Running LED circuit using IC-555 Timer.
8	Construct water level indicator using IC-555 Timer.
9	Construct continuity tester using IC-555 Timer.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

- Analyse in an intelligent manner, think better, and perform better.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination(SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8^{th} week of the semester and the second test shall be conducted after the 14^{th} week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.

- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).
- The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the totalCIE marks scored by the student.

- **Semester End Evaluation (SEE):**
- SEE marks for the practical course is 50 Marks.
- SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by theUniversity
- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointlyby examiners.
- Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.
- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners. General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by theexaminers)
- Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.The duration of SEE is 03 hours
- Rubrics suggested in Annexure-II of Regulation book.

Circuit Laboratory using P-spice			
Course Code	**BEEL358C**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:0:2:0	SEE Marks	50
Credits	01	Exam Hours	02

Course objectives:

(1) Along with prescribed hours of teaching –learning process, provide opportunity to perform the experiments/programmes at their own time, at their own pace, at any place as per their convenience and repeat any number of times to understand the concept.

(2) Provide unhindered access to perform whenever the students wish.

(3) Vary different parameters to study the behaviour of the circuit without the risk of damaging equipment/ device or injuring themselves.

Sl. NO	Experiments
1	Simulate Series RL & RC circuit and observe phase difference between waveforms of voltage and current.
2	Simulation and verification of Kirchhoff's Current Law & Kirchhoff's Voltage Law.
3	Simulation of Mesh analysis for a given circuit.
4	Simulation of Nodal analysis for a given circuit.
5	Determination of Z & Y parameters of a given two-port network.
6	Simulate and verify Super Positions theorem.
7	Simulation and verification Reciprocity theorem.
8	Simulation and verification Thevenin's and Norton's theorem.
9	Simulation and verification Maximum Power Transfer theorem.
10	Simulation and verification Millman's theorem.
11	Simulation of Series and Parallel Resonance circuit.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

- Analyse in an intelligent manner, think better, and perform better.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination(SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8^{th} week of the semester and the second test shall be conducted after the 14^{th} week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.

- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

- SEE marks for the practical course is 50 Marks.
- SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by theUniversity
- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointlyby examiners.
- Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.
- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners. General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scoredmarks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by theexaminers)
- Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.The duration of SEE is 03 hours
- Rubrics suggested in Annexure-II of Regulation book.

Electrical Power Generation and Economics		Semester	III
Course Code	BEE306A	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03
Examination nature (SEE)	Theory		

Course objectives:

- To understand the basics of hydro electric power plant, merits and demerits of hydroelectric power plants, site selection, arrangement and elements of hydro electric plant.
- To understand the working, site selection and arrangement of Steam, Diesel and Gas Power Plants.
- To understand the working, site selection and arrangement of Nuclear Power Plants.
- To understand importance of different equipments in substation, Interconnection of power stations and different types of grounding.
- To understand the economics of power generation.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecturer method (L) needs not to be only traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes.
2. Use of Video/Animation to explain functioning of various concepts.
3. Encourage collaborative (Group Learning) Learning in the class.
4. Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyze information rather than simply recall it.
6. Introduce Topics in manifold representations.
7. Show the different ways to solve the same problem with different circuits/logic and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world-and when that's possible, it helps improve the students' understanding.

Module-1

Hydroelectric Power Plants: Hydrology, run off and stream flow, hydrograph, flow duration curve, Mass curve, reservoir capacity, dam storage. Hydrological cycle, merits and demerits of hydroelectric power plants, Selection of site. General arrangement of hydel plant, elements of the plant, Classification of the plants based on water flow regulation, water head and type of load the plant has to supply. Water turbines – Pelton wheel, Francis, Kaplan and propeller turbines. Characteristic of water turbines Governing of turbines, selection of water turbines. Underground, small hydro and pumped storage plants. Choice of size and number of units, plant layout and auxiliaries.

Module-2

Steam Power Plants: Introduction, Efficiency of steam plants, Merits and demerits of plants, selection of site. Working of steam plant, Power plant equipment and layout, Steam turbines, Fuels and fuel handling, Fuel combustion and combustion equipment, Coal burners, Fluidized bed combustion, Combustion control, Ash handling, Dust collection, Draught systems, Feed water, Steam power plant controls, plant auxiliaries.

Diesel Power Plant: Introduction, Merits and demerits, selection o f site, elements of diesel power plant, applications.

Gas Turbine Power Plant: Introduction Merits and demerits, selection of site, Fuels for gas turbines, Elements of simple gas turbine power plant, Methods of improving thermal efficiency of a simple gas power plant, Closed cycle gas turbine power plants. Comparison of gas power plant with steam and diesel power plants.

Module-3

Nuclear Power Plants: Introduction, Economics of nuclear plants, Merits and demerits, selection of site, Nuclear reaction, Nuclear fission process, Nuclear chain reaction, Nuclear energy, Nuclear fuels,Nuclear plant and layout, Nuclear reactor and its control, Classification of reactors, power reactors in use, Effects of nuclear plants, Disposal of nuclear waste and effluent, shielding.

Module-4

Substations: Introduction to Substation equipment; Transformers, High Voltage Fuses, High Voltage Circuit Breakers and Protective Relaying, High Voltage Disconnect Switches, Lightning Arresters, High Voltage Insulators and Conductors, Voltage Regulators, Storage Batteries, Reactors, Capacitors, Measuring Instruments, and power line carrier communication equipment. Classification of substations – indoor and outdoor, Selection of site for substation, Bus-bar arrangement schemes and single line diagrams of substations.

Interconnection of power stations. Introduction to gas insulated substation, Advantages and economics of Gas insulated substation.

Grounding: Introduction, Difference between grounded and ungrounded system. System grounding – ungrounded, solid grounding, resistance grounding, reactance grounding, resonant grounding. Earthing transformer. Neutral grounding and neutral grounding transformer.

Module-5

Economics: Introduction, Effect of variable load on power system, classification of costs, Cost analysis. Interest and Depreciation, Methods of determination of depreciation, Economics of Power generation, different terms considered for power plants and their significance, load sharing. Choice of size and number of generating plants. Tariffs, objective, factors affecting the tariff, types. Types of consumers and their tariff. Power factor, disadvantages, causes, methods of improving power factor, Advantages of improved power factor, economics of power factor improvement and comparison of methods of improving the power factor. Choice of equipment.

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

1. Explain the basics of hydro electric power plant, merits and demerits of hydroelectric power plants, site selection, arrangement and elements of hydro electric plant.
2. Explain the working, site selection and arrangement of Steam, Diesel and Gas Power Plants.
3. Explain the working, site selection and arrangement of Nuclear Power Plants.
4. Explain the importance of different equipments in substation, Interconnection of power stations and different types of grounding.
5. Explain the economics of power generation.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25 marks.
- The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.
- For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

Suggested Learning Resources:

Text Books

1. Power Plant Engineering, P.K. Nag, Mc Graw Hill, 4th Edition, 2014
2. Generation of Electrical Energy, B.R.Gupta, S. Chand, 2015
3. Electrical power Generation, Transmission and Distribution, S.N. Singh, PHI, 2nd Edition, 2009

Reference Books

1. A Course in Power Systems, J.B. Gupta, Katson, 2008
2. Electrical Power Distribution Systems, V. Kamaraju, McGrawHill, 1st Edition, 2009
3. A Text Book on Power SystemEngineering, A. Chakrabarti, et al, Dhanpath Rai, 2nd Edition, 2010
4. Electrical Distribution Engineering, Anthony J. Pansini, CRC Press, 3rd Edition, 2006
5. Electrical Distribution Systems, Dale R PatrickEt al, CRC Press, 2nd Edition, 2009

Web links and Video Lectures (e-Resources):

- www.nptel.ac.in

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Visit to power station.
- Walk through videos

Electrical Measurements and Instrumentation		Semester	III
Course Code	BEE306B	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03
Examination nature (SEE)	Theory		

Course objectives:

- To understand the significance and methods of Measurements, elements of generalised measurement system and errors in measurements.
- To measure resistance, inductance, capacitance by use of different bridges.
- To study the construction, working and characteristics of various instrument transformers.
- To have the working knowledge of electronic instruments and display devices.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecturer method (L) needs not to be only traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes.
2. Use of Video/Animation to explain functioning of various concepts.
3. Encourage collaborative (Group Learning) Learning in the class.
4. Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyze information rather than simply recall it.
6. Introduce Topics in manifold representations.
7. Show the different ways to solve the same problem with different circuits/logic and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world-and when that's possible, it helps improve the students' understanding.

Module-1

Measurements and Measurement systems: Introduction, significance and methods of Measurements, Instruments and measurement systems, Mechanical, electrical and electronic instruments. Classification of instruments. Functions and applications of Measurement systems. Types of Instrumentation systems, information and signal processing. Elements of generalised measurement system. Input-output configurations of measuring instruments and measurement systems. Methods of correction for interfering and modifying inputs, errors in measurements, Accuracy and precision.

Module-2

Measurement of Resistance: Wheatstone's bridge, sensitivity, limitations. Kelvin's double bridge. Earth resistance measurement by fall of potential method and by using Megger.

Measurement of Inductance and Capacitance: Sources and detectors, Maxwell's inductance and capacitance bridge, Hay's bridge, Anderson's bridge, Desauty's bridge, Schering bridge. Shielding of bridges. (Derivations and Numerical as applicable).

Module-3

Instrument Transformers: Introduction, Use of Instrument transformers. Burden on Instrument transformer.

Current transformer (CT): Relationships in CT, Errors in CT, characteristics of CT, causes and reduction of errors in CT, Construction and theory of CT.

Potential transformer (PT): Difference between CT and PT, Relationships in PT, Errors in PT,

characteristics of PT, reduction of errors in PT.

Magnetic measurements: Introduction, measurement of flux/ flux density, magnetising force and leakage factor.

Module-4

Electronic and Digital Instruments: Introduction. Essentials of electronic instruments, Advantages of electronic instruments. True RMS reading voltmeter. Electronic multimeters. Digital voltmeters (DVM) - Ramp type DVM, Integrating type DVM and Successive - approximation DVM. Q meter. Principle of working of electronic energy meter (with block diagram), extra features offered by present day meters and their significance in billing.

Module-5

Display Devices: Introduction, character formats, segment displays, Dot matrix displays, Bar graph displays. Cathode ray tubes, Light emitting diodes, Liquid crystal displays, Nixes, Incandescent, Fluorescent, Liquid vapour and Visual displays.

Recording Devices: Introduction, Strip chart recorders, Galvanometer recorders, Null balance recorders, Potentiometer type recorders, Bridge type recorders, LVDT type recorders, Circular chart and xy recorders. Digital tape recording, Ultraviolet recorders. Electro Cardio Graph (ECG).

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

1. Explain the significance and methods of Measurements, elements of generalised measurement system and errors in measurements.
2. Measure resistance, inductance and capacitance by different methods.
3. Explain the construction, working and characteristics of various instrument transformers.
4. Explain the working of different electronic instruments and display devices.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25 marks.
- The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.
- For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

Suggested Learning Resources:

Text Books

1. Electrical and Electronic Measurements and Instrumentation, A.K. Sawhney, Dhanpat Rai & Co, 10th Edition
2. A Course in Electronics and Electrical Measurements and Instrumentation, J. B. Gupta, Katson Books, 2013

Reference Books

1. Electrical and Electronic Measurements and Instrumentation, R.K. Rajput, S Chand, 5th Edition, 2012
2. Electrical Measuring Instruments and Measurements, S.C. Bhargava, BS Publications, 2013
3. Modern Electronic Instrumentation and Measuring Techniques, Cooper D and A.D. Heifrick, Pearson, First Edition, 2015
4. Electronic Instrumentation and Measurements, David A Bell, Oxford University, 3rd Edition, 2013
5. Electronic Instrumentation, H.S.Kalsi, Mc Graw Hill, 3rd Edition,2010

Web links and Video Lectures (e-Resources):

- www.nptel.ac.in
- https://www.eeweb.com/

ELECTRIC MOTORS		Semester	IV
Course Code	BEE401	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03
Examination nature (SEE)	Theory		

Course objectives:

1 To study the constructional features of Motors and select a suitable drive for specific Application.
2 To study the constructional features of Three Phase and Single phase induction Motors.
3 To study different test to be conducted for the assessment of the performance characteristics of motors.
4 To study the speed control of motor by a different methods.
5 Explain the construction and operation of Synchronous motor and special motors.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecturer method (L) needs not to be only traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes.
2. Use of Video/Animation to explain functioning of various concepts.
3. Encourage collaborative (Group Learning) Learning in the class.
4. Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyse information rather than simply recall it.
6. Introduce Topics in manifold representations.
7. Show the different ways to solve the same problem with different circuits/logic and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

DC Motors: Construction and working principle. Back E.M.F and its significance, Torque equation, Classification, Characteristics of shunt, series & compound motors, Speed control of shunt motor, Application of motors.

Losses and Efficiency- Losses in DC motors, power flow diagram, efficiency, condition for maximum efficiency.

Testing of DC Motors: Direct & indirect methods of testing of DC motors- Swinburne's test, Field's test, merits and demerits of tests. (numerical as applicable)

Module-2

Three Phase Induction Motors: Concept and generation of rotating magnetic field, Principle of operation, construction, classification and types; squirrel-cage, slip-ring. Slip and its significance, Torque equation, torque-slip characteristic covering motoring, generating and braking regions of operation, Maximum torque, (numerical as applicable)

Module-3
Performance of Three-Phase Induction Motor: Phasor diagram of induction motor on no-load and on load, equivalent circuit, losses, efficiency, No-load and blocked rotor tests. Performance of the motor from the equivalent circuit. Cogging and crawling. High torque rotors-double cage and deep rotor bars. Induction motor working as induction generator, construction and working of doubly fed induction generator. (numerical as applicable)
Module-4
Starting and Speed Control of Three-Phase Induction Motors: Necessity of starter. Direct on line, Star-Delta, and autotransformer starting. Rotor resistance starting. Speed control by frequency. **Single-Phase Induction Motor:** Double revolving field theory and principle of operation. Construction and operation of split-phase, capacitor start and capacitor run and shaded pole motors. Comparison of single phase motors and applications. (numerical as applicable)
Module-5
Synchronous Motor: Principle of operation, phasor diagrams, torque and torque angle, effect of change in load, effect of change in excitation. V and inverted V curves. Synchronous condenser, **Other Motors:** Construction and operation of Universal motor, AC servomotor, Linear induction motor, PMSM, SRM and BLDC.

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

1. Understand the construction and operation, characteristics, Testing of DC Motors and determine losses and efficiency.
2. Understand the construction and operation, classification and types of Three phase Induction motors.
3. Describe the performance characteristics and applications of three phase Induction motors.
4. Demonstrate and explain Speed Control methods of three phase induction motor and types of single phase induction motors.
5. Understand the construction and operation, V and inverted V curves of synchronous motors.
6. Construction and operation of Universal motor, AC servomotor, Linear induction motor, PMSM, SRM and BLDC motors.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25 marks.
- The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.
- For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

Suggested Learning Resources:

Text Books

1. Electric Machines, D. P. Kothari, I. J. Nagrath, McGraw Hill, 4th edition, 2011.
2. Theory of Alternating Current Machines, Alexander Langsdorf, McGraw Hill, 2nd Edition, 2001.
3. Electric Machines, AshfaqHussain, DhanpatRai& Co, 2nd Edition, 2013.

Reference Books

1. Electrical Machines, Drives and Power systems, Theodore Wildi, Pearson, 6th Edition, 2014
2. Electrical Machines, M.V. Deshpande, PHI Learning, 2013
3. Electric Machinery and Transformers, Bhag S. Guru at el, Oxford University Press, 3rd Edition, 2012
4. Electric Machinery and Transformers, Irving Kosow, Pearson, 2nd Edition, 2012
5. Principles of Electric Machines and power Electronic, P.C.Sen, Wiley, 2nd Edition, 2013
6. Electrical Machines, R.K. Srivastava, Cengage Learning, 2nd Edition, 2013

Web links and Video Lectures (e-Resources):
• https://nptel.ac.in • http:// acl.digimat.in/nptel/courses/video/108105017/108105017.html
Activity Based Learning (Suggested Activities in Class)/ Practical Based learning • Quizzes. • Seminars. • Cut sectional view of ac and dc motors • Animated/NPTEL videos • PPTs

Transmission and Distribution		Semester	IV
Course Code	BEE402	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	4:0:0	SEE Marks	50
Total Hours of Pedagogy	50 Hours	Total Marks	100
Credits	04	Exam Hours	03
Examination nature (SEE)	Theory		

Course objectives:

- To understand the structure of electrical power system, its components, advantages of high voltage AC and DC transmission, various conductors used for transmission, sag and its calculation.
- To understand various types of insulators, methods to improve string efficiency.
- To understand the various transmission line parameters, their effects on transmission of electricity.
- To understand the various parameters that influences the performance of transmission line and to calculate performance parameters of various transmission lines.
- To understand carona and its effects, underground cables, its construction, classification, limitations and specifications.
- To understand and evaluate different types of distribution systems.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecturer method (L) needs not to be only traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes.
2. Use of Video/Animation to explain functioning of various concepts.
3. Encourage collaborative (Group Learning) Learning in the class.
4. Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyze information rather than simply recall it.
6. Introduce Topics in manifold representations.
7. Show the different ways to solve the same problem with different circuits/logic and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world-and when that's possible, it helps improve the students' understanding.

Module-1

Introduction to Power System: Structure of electric power system: generation, transmission and distribution. Advantages of higher voltage transmission: HVAC, EHVAC, UHVAC and HVDC. Interconnection. Feeders, distributors and service mains.

Overhead Transmission Lines: A brief introduction to types of supporting structures and line conductors- Conventional conductors; Aluminium Conductor steel reinforced (ACSR), All – aluminium alloy conductor (AAAC) and All –aluminium conductor (AAC). High temperature conductors; Thermal resistant aluminium alloy (ATI),Super thermal resistant aluminium alloy (ZTAI), Gap type thermal resistant aluminium alloy conductor steel reinforced (GTACSR), Gap type super thermal resistant aluminium alloy conductor steel reinforced (GZTACSR). Bundle conductor and its advantages. Importance of sag, Sag calculation – supports at same and different levels, effect of wind and ice. Line vibration and vibration dampers. Overhead line protection against lightening; ground wires.

Overhead Line Insulators: A brief introduction to types of insulators, material used- porcelain, toughened glass and polymer (composite). Potential distribution over a string of suspension insulators. String efficiency, Methods of increasing string efficiency. Arcing horns.

Module-2
Line Parameters: Introduction to line parameters- resistance, inductance and capacitance. Calculation of inductance of single phase and three phase lines with equilateral spacing, unsymmetrical spacing, double circuit and transposed lines. Inductance of composite – conductors, geometric mean radius (GMR) and geometric mean distance (GMD). Calculation of capacitance of single phase and three phase lines with equilateral spacing, unsymmetrical spacing, double circuit and transposed lines. Capacitance of composite – conductor, geometric mean radius (GMR) and geometric mean distance (GMD). Advantages of single circuit and double circuit lines.
Module-3
Performance of Transmission Lines: Classification of lines – short, medium and long. Current and voltage relations, line regulation and Ferranti effect in short length lines, medium length lines considering Nominal T and nominal circuits, and long lines considering hyperbolic form equations. Equivalent circuit of a long line. ABCD constants in all cases.
Module-4
Corona: Phenomena, disruptive and visual critical voltages, corona loss. Advantages and disadvantages of corona. Methods of reducing corona. **Underground Cable:** Types of cables, constructional features, insulation resistance, thermal rating, charging current, grading of cables – capacitance and inter-sheath. Dielectric loss. Comparison between ac and DC cables. Limitations of cables. Specification of power cables.
Module-5
Distribution: Primary AC distribution systems – Radial feeders, parallel feeders, loop feeders and interconnected network system. Secondary AC distribution systems – Three phase 4 wire system and single phase 2 wire distribution, AC distributors with concentrated loads. Effect of disconnection of neutral in a 3 phase four wire system. **Reliability and Quality of Distribution System:** Introduction, definition of reliability, failure, probability concepts, limitation of distribution systems, power quality, Reliability aids.

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

1. Explain the structure of electrical power system, its components, advantages of high voltage AC and DC transmission, various conductors used for transmission, sag and its calculation.
2. Explain various types of insulators and methods to improve string efficiency.
3. Explain the various transmission line parameters, their effects on transmission of electricity.
4. Evaluate the parameters that influence the performance of transmission line and to calculate performance parameters of various transmission lines.
5. Explain carona and its effects, underground cable and its construction, classification, limitations and specifications.
6. Evaluate different types of distribution systems.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25 marks.
- The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.
- For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

Suggested Learning Resources:

Text Books:

1. A Course in Electrical Power, Sony Gupta and Bhatnagar, Dhanpat Rai
2. Principles of Power System, V.K. Mehta, Rohit Mehta, S. Chand, 1st Edition 2013

Reference Books:

1. Power System Analysis and Design, J. Duncan Gloverat el, Cengage Learning, 4th Edition 2008
2. Electrical power Generation, Transmission and Distribution, S.N. Singh, PHI, 2nd Edition,2009
3. Electrical Power, S.L.Uppal, Khanna Publication
4. Electrical Power Systems, C. L. Wadhwa, New Age, 5th Edition, 2009
5. Electrical Power Systems, Ashfaq Hussain, CBS Publication
6. Electric Power Distribution, A.S. Pabla, McGraw-Hill, 6th Edition,2012

Web links and Video Lectures (e-Resources):

- www.nptel.ac.in

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Visit to Power Stations, Receiving Stations.
- Seminars

Microcontrollers		Semester	IV
Course Code	BEE403	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:2:0	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory + 8-10 Lab slots	Total Marks	100
Credits	04	Exam Hours	03
Examination nature (SEE)	Theory		

Course objectives:

At the end of the course the student will be able to:

1. To explain the internal organization and working of Computers, microcontrollers and embedded processors.
2. Compare and contrast the various members of the 8051family.
3. To explain the registers of the 8051 microcontroller, manipulation of data using registers and MOV instructions.
4. To explain in detail the execution of 8051 Assembly language instructions and data types
5. To explain loop, conditional and unconditional jump and call, handling and manipulation of I/O instructions.
6. To explain different addressing modes of 8051, arithmetic, logic instructions, and programs.
7. To explain develop 8051C programs for time delay, I/O operations, I/O bit manipulation, logic.
8. To explain writing assembly language programs for data transfer, arithmetic, Boolean and logical instructions.
9. To explain writing assembly language programs for code conversions.
10. To explain writing assembly language programs using subroutines for generation of delays, counters, configuration of SFRs for serial communication and timers.
11. To perform interfacing of stepper motor and DC motor for controlling the speed.
12. To explain generation of different waveforms using DAC interface.

Teaching-Learning Process (General Instructions)

These are sample Strategies; that teachers can use to accelerate the attainment of the various course outcomes.

1. Lecturer method (L) needs not to be only traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes.
2. Use of Video/Animation to explain functioning of various concepts.
3. Encourage collaborative (Group Learning) Learning in the class.
4. Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyze information rather than simply recall it.
6. Introduce Topics in manifold representations.
7. Show the different ways to solve the same problem with different circuits/logic and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world-and when that's possible, it helps improve the students' understanding.

MODULE-1

8051 Microcontroller Basics: Inside the Computer, Microcontrollers and Embedded Processors, Block Diagram of 8051, PSW and Flag Bits, 8051 Register Banks and Stack, Internal Memory Organization of 8051, IO Port Usage in 8051, Types of Special Function Registers and their uses in 8051, Pins of 8051. Memory Address Decoding, 8031/51 Interfacing With External ROM And RAM.8051 Addressing Modes.

MODULE-2

Assembly Programming and Instruction of 8051: Introduction to 8051 assembly programming, Assembling and running an 8051 program, Data types and Assembler directives Arithmetic, logic instructions and programs, Jump, loop and call instructions, IO port programming.

MODULE-3

8051 Programming in C: Data types and time delay in 8051C, IO programming in 8051C, Logic operations in 8051 C, Data conversion program in 8051 C, Accessing code ROM space in 8051C, Data serialization using 8051C.

8051 Timer Programming in Assembly and C: Programming 8051 timers, Counter programming, Programming timers 0 and 1 in 8051 C.

MODULE-4

8051 Serial Port Programming in Assembly and C: Basics of serial communication, 8051 connection to RS232, 8051 serial port programming in assembly, serial port programming in 8051 C.

8051 Interrupt Programming in Assembly and C: 8051 interrupts, Programming timer, external hardware, serial communication interrupt, Interrupt priority in 8051/52, Interrupt programming in C.

MODULE-5

Interfacing: LCD interfacing, Keyboard interfacing.

ADC, DAC and Sensor Interfacing: ADC 0808 interfacing to 8051, Serial ADC Max1112 ADC interfacing to 8051, DAC interfacing, Sensor interfacing and signal conditioning.

Motor Control: Relay, PWM, DC and Stepper Motor: Relays and opt isolators, stepper motor interfacing, DC motor interfacing and PWM.

8051 Interfacing with 8255: Programming the 8255, 8255 interfacing, C programming for 8255.

PRACTICAL COMPONENT OF IPCC

Sl.NO	Experiments
	(to be carried out using discrete components)
Note: For the experiments 1 to 7, 8051 assembly programming is to be used.	
1	Data transfer – Program for block data movement, sorting, exchanging, finding largest element in an array.
2	Arithmetic instructions: Addition, subtraction, multiplication and division. Square and cube.
3	Up/Down BCD/ Binary Counters
4	Boolean and logical instructions (bit manipulation).
5	Conditional call and return instructions.
6	Code conversion programs – BCD to ASCII, ASCII to BCD, ASCII to decimal, Decimal toASCII, Hexa.
7	Programs to generate delay, Programs using serial port and on-chip timer/counters.
Note: Single chip solution for interfacing 8051 is to be with C Programs for the followingexperiments.	
8	Stepper motor interfacefor direction and speed control.
9	DC motor interface for direction and speed control using PWM.
10	Alphanumerical LCD panel interface.
11	Generate different waveforms: Sine, Square, Triangular, Ramp using DAC interface.
12	External ADC and Temperature control interface.
13	Elevator interface.

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

1. Outline the 8051 architecture, registers, internal memory organization, addressing modes.
2. Discuss 8051 addressing modes, instruction set of 8051, accessing data and I/O port programming.
3. Develop 8051C programs for time delay, I/O operations, I/O bit manipulation, logic and arithmetic operations, data conversion and timer/counter programming.
4. Summarize the basics of serial communication and interrupts, also develop 8051 programs for serial data communication and interrupt programming.

5. Program 8051to work with external devices for ADC, DAC, Stepper motor control, DC motor control
6. Develop various 8051 based projects.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

CIE for the theory component of the IPCC (maximum marks 50)

- IPCC means practical portion integrated with the theory of the course.
- CIE marks for the theory component are **25 marks** and that for the practical component is **25 marks**.
- 25 marks for the theory component are split into **15 marks** for two Internal Assessment Tests (Two Tests, each of 15 Marks with 01-hour duration, are to be conducted) and **10 marks** for other assessment methods mentioned in 22OB4.2. The first test at the end of 40-50% coverage of the syllabus and the second test after covering 85-90% of the syllabus.
- Scaled-down marks of the sum of two tests and other assessment methods will be CIE marks for the theory component of IPCC (that is for **25 marks)**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the theory component of IPCC.

CIE for the practical component of the IPCC

- **15 marks** for the conduction of the experiment and preparation of laboratory record, and **10 marks** for the test to be conducted after the completion of all the laboratory sessions.
- On completion of every experiment/program in the laboratory, the students shall be evaluated including viva-voce and marks shall be awarded on the same day.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to **15 marks**.
- The laboratory test **(duration 02/03 hours)** after completion of all the experiments shall be conducted for 50 marks and scaled down to **10 marks.**
- Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **25 marks**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the practical component of the IPCC.

SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored by the student shall be proportionally scaled down to 50 Marks

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper may include questions from the practical component.

Suggested Learning Resources:

Books

1. The 8051 Microcontroller and Embedded Systems Using Assembly and C, Muhammad Ali Mazadi, Pearson, 2nd Edition, 2008.
2. The 8051 Microcontroller, Kenneth Ayala, Cengage, 3rd Edition, 2005.
3. Microcontrollers: Architecture, Programming, Interfacing and System Design, Raj Kamal, Pearson, 1st Edition, 2012.

Web links and Video Lectures (e-Resources):

- NPTEL course on 8051 microcontrollers:**https://nptel.ac.in/courses/108105102**
- You tube videos on 8051 microccontrollers
- 8051 programming online course: Complete 8051 Microcontroller Programming Course | Udemy

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Mini projects using 8051 microcontroller
- Seminars
- Quizzes
- Assignments

DIGITAL SYSTEM DESIGN USING VHDL		Semester	IV
Course Code	**BEE405A**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory	Total Marks	100
Credits	03	Exam Hours	03
Examination nature (SEE)	Theory		

Course objectives:

- Learn different Verilog HDL Constructs
- Familiarize the different levels of abstraction in Verilog
- Understand Verilog tasks , functions and directives
- Understand timing and delay simulation
- Understand the concept of logic synthesis and its impact in verification

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecturer method (L) needs not to be only traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes.
2. Use of Video/Animation to explain functioning of various concepts.
3. Encourage collaborative (Group Learning) Learning in the class.
4. Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyze information rather than simply recall it.
6. Introduce Topics in manifold representations.
7. Show the different ways to solve the same problem with different circuits/logic and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world-and when that's possible, it helps improve the students' understanding.

Module-1

Over view of digital design with Verilog HDL:

Evolution of CAD, emergence of HDLs, typical HDL flow, why Verilog HDL? trends in HDL

Hierarchical Modelling Concepts:

Top down and bottom-up design methodology, difference between modules and module instances, parts of a simulation, design block, stimulus block.

Module-2

Basic Concepts:

Lexical conventions, data types, system tasks, compiler directives.

Modules and ports:

Module definition, port declaration, connecting ports, Hierarchical name referencing.

Module-3

Gate level modelling:

Modelling using basic Verilog gate primitives, description of and /or and buf/not type gates, rise, fall and turn off delays, min, max and typical delays

Dataflow modelling:

Continuous assignments, delay specification, expressions, operators, operands and operate types.

Module-4
Behavioral modelling: Structured procedures, initial and always, blocking and non-blocking statements, delay control, generate statement, event control, conditional statements, multiway branching, loops, sequential and parallel blocks. **Tasks and functions:** Differences between tasks and functions, declaration , invocation, automatic tasks and functions.
Module-5
Useful Modeling techniques: Procedural continuous assignments, overriding parameters, conditional compilation, and execution, useful system tasks **Logic Synthesis with Verilog:** Logic synthesis, impact of logic synthesis, Verilog HDL synthesis, synthesis design flow, verification of gate level netlist, (Chapter 14, till 14.5 of Text 1)
Course outcome (Course Skill Set) At the end of the course, the student will be able to : 1. Write Verilog programs in gate, dataflow (RTL), behavioral and switch modeling levels of abstraction 2. Design and verify the functionality of digital circuit and system ,using test benches 3. Identify the suitable abstraction level for a particular digital system 4. Write the programs more effectively using Verilog tasks , functions and directives 5. Program timing and delay simulation and interpret the various constructs in logic synthesis.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25 marks.
- The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.
- For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

Suggested Learning Resources:

Books

1) SamirPalnitkar, "Verilog HDL : A guide to digital design and synthesis", Pearson Education, II Edition.

Reference Books:

1) Donald E Thomas, Philip R Moorby, "The Verilog hardware description Language", Springer Science Business Media , LLC, 5th Edition

2) Michael D. Ciletti, "Advanced digital design with the Verilog HDL", Pearson (PHI),II Edition

3) Padmanabhan, Tripura Sunadri, "Design through Verilog HDL", Wiley, 2016.

Web links and Video Lectures (e-Resources):

- NPTEL course on VHDL: https://nptel.ac.in/courses/117108040
- You tube videos on VHDL

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- VHDL based projects for different applications
- Seminars
- Quizzes
- Assignments

OPAMPS AND LIC		Semester	IV
Course Code	BEE405B	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40 hours	Total Marks	100
Credits	03	Exam Hours	03
Examination nature (SEE)	Theory		

Course objectives:

- To understand the basics of Linear ICs such as Op-amp, Regulator, Timer & PLL.
- To learn the designing of various circuits using linear ICs.
- To use these linear ICs for specific applications.
- To understand the concept and various types of converters.
- To use these ICs, in Hardware projects.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecturer method (L) needs not to be only traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes.
2. Use of Video/Animation to explain functioning of various concepts.
3. Encourage collaborative (Group Learning) Learning in the class.
4. Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyze information rather than simply recall it.
6. Introduce Topics in manifold representations.
7. Show the different ways to solve the same problem with different circuits/logic and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world-and when that's possible, it helps improve the students' understanding.

Module-1

Operational amplifiers: Introduction, Block diagram representation of a typical Op-amp, schematicsymbol, characteristics of an Op-amp, ideal op-amp, equivalent circuit, ideal voltage transfercurve,open loop configuration, differential amplifier, inverting & non –inverting amplifier, Op-amp withnegative feedback ; voltage series feedback amplifier-gain, input resistance, output resistance,voltage shunt feedback amplifier- gain, input resistance, output resistance. **General Linear Applications**: D.C. & A.C amplifiers, peaking amplifier, summing, scaling & averaging amplifier, inverting and non-inverting configuration, differential configuration, instrumentation amplifier

Module-2

Active Filters: First & Second order high pass & low pass Butterworth filters, higher order filters, Band pass filters, Band reject filters & all pass filters.

DC Voltage Regulators: voltage regulator basics, voltage follower regulator, adjustable output regulator, LM317 & LM337 Integrated circuits regulators.

Module-3

Signal generators: Working and derivation of frequency of oscillation for Phase shift oscillator, Wien bridge oscillator, square wave generator, sawtooth wave generator, triangular wave generator, rectangular wave generator.

Comparators & Converters: Basic comparator, zero crossing detector, inverting & non-invertingSchmitt trigger circuit, voltage to current converter with grounded load, current to voltageconverterand basics of voltage to frequency and frequency to voltage converters.

Module-4

Signal processing circuits: Precision half wave & full wave rectifiers limiting circuits, clamping circuits, peak detectors, sample & hold circuits.

A/D & D/A Converters: Basics, R–2R D/A Converter, Integrated circuit 8-bit D/A, successive approximation ADC, linear ramp ADC, dual slope ADC, digital ramp ADC

Module-5

Phase Locked Loop (PLL): Basic PLL, components, performance factors, applications of PLL IC 565. Timer: Internal architecture of 555 timer, Mono stable, Astable-multivibrators and applications

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

1. Explain the basics of linear ICs.
2. Design circuits using linear ICs.
3. Demonstrate the application of Linear ICs.
4. Use ICs in the electronic projects

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25 marks.
- The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.
- For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.
- Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (duration 03 hours).

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), should have a mix of topics under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

Suggested Learning Resources:

Books

1. Op-Amps and Linear Integrated Circuits, Ramakant A Gayakwad , Pearson, 4th Edition, 2015
2. Operational Amplifiers and Linear ICs, David A. Bell ,Oxford, 3rd Edition 2011
3. Linear Integrated Circuits , S. Salivahanan, et al, Wiley India , 2013
4. Op-Amps and Linear Integrated Circuits, Concept and Application, James M Fiore, Cengage, 2009

Web links and Video Lectures (e-Resources):

- NPTEL course on opamps : https://nptel.ac.in/courses/108108114
- You tube videos on opamps and in Linear Integrated Circuits.

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- To develop mini projects based on opamp
- To develop mini projects based on timer and PLL IC
- Seminars
- Quizzes
- Assignments

Engineering Materials		Semester	IV
Course Code	BEE405C	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03
Examination nature (SEE)	Theory		

Course objectives:

- To understand wave particle duality, tunnelling phenomenon, electron theory of metals.
- To understand the free electron theory of conduction in metals.
- To understand the polarization under static fields, behavior of dielectrics in alternating fields, Inorganic materials, organic materials,), resins and varnishes, liquid insulators.
- To understand the mechanism of conduction in semiconductors.
- To understand the magnetic materials, their classification and magneto materials.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecturer method (L) needs not to be only traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes.
2. Use of Video/Animation to explain functioning of various concepts.
3. Encourage collaborative (Group Learning) Learning in the class.
4. Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyse information rather than simply recall it.
6. Introduce Topics in manifold representations.
7. Show the different ways to solve the same problem with different circuits/logic and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

THEORY OF METALS

Elementary Quantum mechanical ideas: Wave Particle Duality, Wave function, schrodinger's equation, operator notation, expected value, Infinite Potential Well: A confined electron. Finite Potential Barrier: Tunnelling Phenomenon. Free electron theory of metals: Electron in a linear solid, Fermi energy, Degenerate states, Number of States, Density of States, Population Density. Fermi-Dirac Distribution Function. Thermionic Emission: Richardson's Equation, Schottky Effect. Contact Potential: Fermi level at Equilibrium.

Module-2

FREE ELECTRON THEORY OF CONDUCTION IN METAL

Crystalline structure: Simple cubic structure, Body centered cubic, Face centered cubic. Band Theory of Solids. Effective mass of Electron. Thermal Velocity of Electron at equilibrium. Electron mobility, conductivity and resistivity.

Module-3

DIELECTRICS and INSULATING MATERIALS

DIELECTRICS: Dielectric, polarization under static fields- electronic ionic and dipolar polarizations, behavior of dielectrics in alternating fields, Factors influencing dielectric strength and capacitor materials. Insulating materials, complex dielectric constant, dipolar relaxation and dielectric loss.

INSULATING MATERIALS: Inorganic materials (mica, glass, porcelain, asbestos), organic materials (paper, rubber, cotton silk fiber, wood, plastics and bakelite), resins and varnishes, liquid insulators(transformer oil) gaseous insulators (air, SF6 and nitrogen) and ageing of insulators.

Module-4

SEMICONDUCTORS

Mechanism of conduction in semiconductors, density of carriers in intrinsic semiconductors, the energy gap, types of semiconductors. Hall effect, compound semiconductors, basic ideas of amorphous and organic semiconductors.

Module-5

Magnetic materials

Magnetic materials: Classification of magnetic materials- origin of permanent magnetic dipoles, ferromagnetism, Magnetic Domains: Domain structure, Domain Wall motion, Hysteresis loop, Eddy current losses, Demagnetization, hard and soft magnetic materials, magneto materials used in electrical machines, instruments and relays.

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

1. Explain wave particle duality, tunnelling phenomenon, electron theory of metals.
2. Explain the free electron theory of conduction in metals.
3. Explain the polarization under static fields, behavior of dielectrics in alternating fields, Inorganic materials, organic materials,), resins and varnishes, liquid insulators.
4. Explain the mechanism of conduction in semiconductors.
5. Explain the magnetic materials, their classification and magneto materials.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

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Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

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Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

Suggested Learning Resources:

Books

1. Bhadra Prasad Pokharel and Nava Raj Karki,"Electrical Engineering Materials", Sigma offset Press, Kamaladi, Kathmandu, Nepal,2004.
2. R.C. Jaeger, "Introduction to Microelectronic Fabrication- Volume IV", Addison Wesley publishing Company,Inc., 1988.
3. Introduction to Electrical Engineering Materials 4th Edn. 2004 Edition by Indulkar C, S. Chand & Company Ltd-New Delhi.
4. Electrical and Electronic Engineering Materials by SK Bhattacharya, Khanna Publishers, New Delhi.

Web links and Video Lectures (e-Resources):

- www.nptel.ac.in

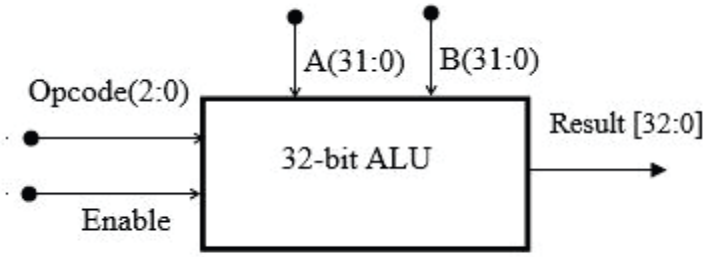
Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Seminars
- Quizzes

BASICS OF –VHDL LAB		Semester	IV
Course Code	**BEE456A**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:0:2:0	SEE Marks	50
Credits	01	Exam Hours	03
Examination nature (SEE)	Practical/Viva-Voce		

Course objectives:

1. Along with prescribed hours of teaching –learning process, provide opportunity to perform the experiments/programmes at their own time, at their own pace, at any place as per their convenience and repeat any number of times to understand the concept.
2. Provide unhindered access to perform whenever the students wish.
3. Vary different parameters to study the behaviour of the circuit without the risk of damaging equipment/device or injuring themselves.

Sl.NO	Experiments
	Note: Programming can be done using any compiler. Download the programs on a FPGA/CPLD board and performance testing may be done using 32 channel pattern generator and logic analyser, apart from verification by simulation with tools such as Altera/Modelsim or equivalent
1	Write Verilog program for the following combinational design along with test bench to verify the design: a) 2 to 4 decoder realization using NAND gates only (structural model) b) 8 to 3 encoder with priority encoder and without priority encoder (behavioral model) c) 8 to 1 Multiplexer using case statement and if statement d) 4 bit binary to gray code converter using 1 bit gray to binary converter 1 bit adder and subtractor.
2	Model in Verilog for a full adder and add functionality to perform logical operations of XOR, XNOR, AND and OR gates. Write test bench with appropriate input patterns to verify the modelled behavior.
3	Verilog 32 bit ALU shown in figure below and verify the functionality of ALU by selecting appropriate test patterns. The functionality of the ALU is shown in Table-1. a) Write test bench to verify the functionality of the ALU considering all possible input patterns b) The enable signal will set the output to required functions if enabled, if disabled all the outputs are set to tri-state. c) The acknowledge signal is set high after every operation is complete. 

<table>
<tr><td></td><td>ALU Top Level Diagram
Table -1 ALU functions:
<table>
<tr><th>Opcode (2:0)</th><th>ALU Operation</th><th colspan="2">Remarks</th></tr>
<tr><td>000</td><td>A + B</td><td>Addition of two numbers</td><td rowspan="2">Both A and B are in two's complement format</td></tr>
<tr><td>001</td><td>A – B</td><td>Subtraction of two numbers</td></tr>
<tr><td>010</td><td>A + 1</td><td>Increment Accumulator by 1</td><td rowspan="2">A is in two's complement format</td></tr>
<tr><td>011</td><td>A - 1</td><td>Decrement accumulator by 1</td></tr>
<tr><td>100</td><td>A</td><td>True</td><td rowspan="4">Inputs can be in any format</td></tr>
<tr><td>101</td><td>A Complement</td><td>Complement</td></tr>
<tr><td>110</td><td>A OR B</td><td>Logical OR</td></tr>
<tr><td>111</td><td>A AND B</td><td>Logical AND</td></tr>
</table></td></tr>
<tr><td>4</td><td>Write Verilog code for SR, D and JK and verify the flip flop</td></tr>
<tr><td>5</td><td>Write Verilog code for 4 bit BCD synchronous counter</td></tr>
<tr><td>6</td><td>Write Verilog code for counter with given input clock and check whether it works as clock divider performing division of clock by 2, 4, 8 and 16 . Verify the functionality of the code.</td></tr>
<tr><td></td><td>PART B
Note;
Interfacing and Debugging:
(ED) WinXp, PSpice, MultiSim, Proteus, CircuitLab, or any other equivalent tool can be used.</td></tr>
<tr><td></td><td>Demonstration Experiments (For CIE)</td></tr>
<tr><td>7</td><td>Write a Verilog code to design a clock divider circuit that generates ½, 1/3rd, 1/4th ,clock from given input clock . Port the design to FPGA and validate the functionality through CRO.</td></tr>
<tr><td>8</td><td>Interface a DC motor to FPGA and write Verilog code to change its speed and direction</td></tr>
<tr><td>9</td><td>Interface a stepper motor to FPGA and write Verilog code to control the stepper motor rotation which in turn may control a Robatic arm. External switches to be used for different controls like rotate the stepper motor:
a)+ N steps if the switch number 1 of a DIP switch is closed.
b)+N/2 steps if switch number 2 of a DIP switch is closed.
c)-N steps if switch number 3 of a DIP switch is closed etc.</td></tr>
<tr><td>10</td><td>Interface a DAC to FPGA and write Verilog code to generate a sine wave of frequency f KHz, ex f = 100 KHz, or 200 KHz etc, . Modify the code to down sample the frequency to f/2 KHz.
Display the original and down sampled signals by connecting them to CRO.</td></tr>
<tr><td>11</td><td>Write Verilog code using FSM to simulate elevator operation.</td></tr>
<tr><td>12</td><td>Write Verilog code to convert an analog input signal of a sensor to digital form and to display the same on a suitable display like simple set of LEDs , 7 segment display digits or LCD display</td></tr>
</table>

Course outcomes (Course Skill Set):
At the end of the course the student will be able to:

1. Write the VHDL/Verilog programs to simulate combinational circuits in data flow, behavioral, gate level abstractions.
2. Describe sequential circuits like flip-flops, counters, in behavioral descriptions and obtain simulated waveforms.
3. Use FPGA/CPLD kits for downloading Verilog codes and check output.
4. Synthesize combinational and sequential circuits on programmable ICs and test the hardware
5. Interface the hardware programmable chips and obtain the required output.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together

Continuous Internal Evaluation (CIE):

CIE marks for the practical course are**50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment is to be evaluated for conduction with an observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments are designed by the faculty who is handling the laboratory session and are made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled down to **30 marks** (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct a test of 100 marks after the completion of all the experiments listed in the syllabus.
- In a test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- The marks scored shall be scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and marks of a test is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

- SEE marks for the practical course are 50 Marks.
- SEE shall be conducted jointly by the two examiners of the same institute, examiners are

appointed by the Head of the Institute.

- The examination schedule and names of examiners are informed to the university before the conduction of the examination. These practical examinations are to be conducted between the schedule mentioned in the academic calendar of the University.
- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.
- Students can pick one question (experiment) from the questions lot prepared by the examiners jointly.
- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% of Marks allotted to the procedure part are to be made zero.

The minimum duration of SEE is 02 hours

Suggested Learning Resources:

- HDL Programming fundamentals , VHDL and Verilog, N. Botros, Cengage Learning,

Scilab / MATLAB for Electrical and Electronic Measurements			
Course Code	**BEEL456B**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:0:2:0	SEE Marks	50
Credits	01	Exam Hours	02

Course objectives:

(1) Along with prescribed hours of teaching –learning process, provide opportunity to perform the experiments/programmes at their own time, at their own pace, at any place as per their convenience and repeat any number of times to understand the concept.

(2) Provide unhindered access to perform whenever the students wish.

(3) Vary different parameters to study the behaviour of the circuit without the risk of damaging equipment/ device or injuring themselves.

Sl. NO	Experiments
1	Design and Analysis of measurement of Resistance using Wheatstone and Kelvins double bridge.
2	Design and Analysis of measurement of Inductance using Schering and De-Sauty's Bridges.
3	Design and Analysis of measurement of Inductance using Maxwells and Anderson Bridges.
4	Design and Analysis of measurement of Frequency in Single and Three Phase Circuits.
5	Design and Analysis of measurement of Real Power, Reactive and Power Factor in Three Phase Circuits.
6	Design and Analysis of measurement of Energy in Three Phase Circuits.
7	Design and Analysis of measurement of Flux and Flux density.
8	Testing and Analysis of Current Transformer using Silsbees Deflection Method.
9	Testing and Analysis of Voltage Transformer using Silsbees Deflection Method.
10	Design and Analysis of True RMS Reading Volt Meters.
11	Design and Analysis of Integrating and Successive approximation type Digital Volt Meters.
12	Design and Analysis of Q Meter.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

- Analyse in a systematic way, think better, and perform better.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.

- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of the semester and the second test shall be conducted after the 14th week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).
- The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the totalCIE marks scored by the student.

Semester End Evaluation (SEE):

- SEE marks for the practical course is 50 Marks.
- SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by theUniversity
- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointlyby examiners.
- Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.
- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners. General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by theexaminers)
- Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.The duration of SEE is 03 hours
- Rubrics suggested in Annexure-II of Regulation book.

Scilab / MATLAB for Electric Motors			
Course Code	**BEEL456C**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:0:2:0	SEE Marks	50
Credits	01	Exam Hours	02

Course objectives:

(1) Along with prescribed hours of teaching –learning process, provide opportunity to perform the experiments/programmes at their own time, at their own pace, at any place as per their convenience and repeat any number of times to understand the concept.

(2) Provide unhindered access to perform whenever the students wish.

(3) Vary different parameters to study the behaviour of the circuit without the risk of damaging equipment/ device or injuring themselves.

Sl. NO	Experiments
1	Load test on dc shunt motor to draw speed – torque and horse power – efficiency characteristics
2	Field Test on dc series machines.
3	Speed control of dc shunt motor by armature and field control.
4	4 Swinburne's Test on dc motor.
5	Regenerative test on dc shunt machines.
6	No load and Blocked rotor test on three phase induction motor to draw (i) equivalent circuit and (ii) circle diagram. Determination of performance parameters at different load conditions from (i) and (ii).
7	Load test on three phase induction motor.
8	Load test on single phase induction motor to draw output versus torque, current, power and efficiency characteristics.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

- Analyse in a systematic way, think better, and perform better.

Assessment Details (both CIE and SEE)

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