ವಿಶ್ವೇಶ್ವರಯ್ಯ ತಾಂತ್ರಿಕ ವಿಶ್ವವಿದ್ಯಾಲಯ
("ವಿ ಟಿ ಯು ಅಧಿನಿಯಮ ೧೯೯೪" ರ ಅಡಿಯಲ್ಲಿ ಕರ್ನಾಟಕ ಸರ್ಕಾರದಿಂದ ಸ್ಥಾಪಿತವಾದ ರಾಜ್ಯ ವಿಶ್ವವಿದ್ಯಾಲಯ)

VISVESVARAYA TECHNOLOGICAL UNIVERSITY

(State University of Government of Karnataka Established as per the VTU Act, 1994)"Jnana Sangama" Belagavi-590018, Karnataka, India)

Prof. B. E. Rangaswamy, Ph.D.
REGISTRAR

Phone: (0831) 2498100
Fax: (0831) 2405467

REF: VTU/BGM/BOS/New UG-PG Prog/2023-24/4874 DATE: 13 DEC 2023

CIRCULAR

Subject: Updated syllabus of courses BRI303 and BRI304 regarding...
Reference: Chairperson's approval dated 05.12.2023
The Hon'ble Vice Chancellor's approval Dated 13.12.2023

The following updates to the BRI303: Analog and Digital Electronic Circuits and BRI304: Data Structure and Algorithm syllabus are in effect:

- Modules 03 and 04 of **BRI303: Analog and Digital Electronics Circuits** were duplicated, and module 04 will now be replaced by **counters**.
- **BRI304: Data Structure and Algorithm**, revised to include reference books and missing text books

All the Principals are hereby informed to bring the content of the CIRCULAR to the notice of all faculty and students concerned.

Sd/-
Registrar

To,
All the Principals of Affiliated and Constituent Engineering Colleges under the ambit of the University
The Chairperson / Program Coordinator, University Department at Kalaburagai, Belagavi, Bengaluru and Mysuru

Copy to:

1. The Hon'ble Vice-Chancellor through the secretary to VC VTU Belagavi for information
2. The Registrar (Evaluation) VTU Belagavi for information and needful
3. The Chairpersons and Members of BoS in Mechanical Engineering of VTU Belagavi
4. The Chairperson and Members BoE of VTU Belagavi
5. The Special Officer, QPDS Examination Section VTU Belagavi for information.
6. The Special Officer Academic Section VTU Belagavi for information
7. Office Copy

13/12/23
REGISTRAR

Analog and Digital Electronic Circuits		Semester	III
Course Code	BRI303	CIE Marks	50
Teaching Hours/Week(L:T:P:S)	3:0:2:0	SEE Marks	50
Total Hours of Pedagogy	40hours Theory+12Labslots	Total Marks	100
Credits	04	Exam Hours	3
Examination nature(SEE)	Theory		

Courseobjectives:

Thiscoursewillenablestudents:

- To understand the basics and applications of diodes and transistors
- To understand the basics and applications of OPAMPS
- To Illustrate simplification of Algebraic equations using Karnaugh Mapsand Quine-Mc Clusky Techniques.
- To Design Decoders, Encoders,Digital Multiplexer, Adders, Subtractors and Binary Comparators.
- To Describe Latches and Flip-flops, Registers and Counters.

Teaching-Learning Process(General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecturer method(L) does not mean only the traditional lecture method, but adifferent type of teaching method may be adopted to develop the outcomes.
2. Show Video/animation films to explain the functioning of various analog and digital circuits.
3. Encourage collaborative(Group)Learning in the class.
4. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Discus show every concept can be applied to the real world-and when that's possible, it helps improve the students' understanding.

Module-1

Junction diode for HW and FW rectification, Clippers and Clamping circuits, Transistor biasing, Dc load line analysis, Different biasing circuits, stability factors(without derivation), Transistor switching networks.

Concept of Amplifiers : RC Coupled Amplifier (Analysis), Feedback Amplifiers: Different types of feedback amplifers (Analysis),Power Amplifiers: Concept of Power Amplifiers , Class A and Class B , Push-pull power amplifier, Oscillators: Concept, Audio and Radio Frequency Oscillators, JFET and MOSFET - Working Principle and Biasing., (Text-1)

Module-2

OPAMP :Dual-input Balanced output Differential amplifier, Block diagram representation of an opamp, Interpretation of datasheets (Ideal V/s) practical values, Frequency response of an OPMAP, OPAMP Configurations: inverting, Non- inverting, Differential:

OPAMP Applications: Summer, integrator, differentiator, Schmitt triggers.555 Timer Applications: Astable and Monostable Multivibrator, Active Filtes. Binary weighted Resistor D/A converter and Successive Approximation A/D converter.(Text-2)

Module-3

Analysis and design of combinational logic: Decoders, Encoders, Digital multiplexers, Adders and subtractors, Look ahead carry, Binary comparators.(Text 3 - Chapter 4).

Programmable Logic Devices, Complex PLD, FPGA. (Text 5 - Chapter 9, 9.6 to 9.8)

Module-4

Counters: Counters: Asynchronous Counters, Decoding Gates, Synchronous Counters Decade Counters, Pre settable Counters, Counter Design as a Synthesis problem, A Digital Clock,. D/A Conversion and A/D Conversion: Variable, Resistor Networks, Binary Ladders, D/A Converters, D/A Accuracy and Resolution, A/D Converter-Simultaneous. Text book 6:- Ch 10.1,10.2, 10.3 Ch 10: 10.5 to 10.8. Ch 12: 12.1 to 12.5.

Module-5

Flip-Flops and its Applications: Basic Bitable elements, Latches, The master-slave flip flops (pulse-triggered flip-flops): SR flip-flops, JK flip-flops, Characteristic equations, Registers, binary ripple counters, and synchronous binary counters.(Text4-Chapter6)

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

1. CO1: Understand analyse clippers, clampers, amplifier and D/A and A/D converter circuits.
2. CO2: Explain opamp basics and Analyze OPAMP applications.
3. CO3: Explain the concept of combinational and sequential logic circuits.
4. CO4: Design the combinational logic circuits.
5. CO5:Design the sequential circuit susing SR, JK,D, T flip-flops

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

The IPCC means the practical portion integrated with the theory of the course. CIE marks for the theory component are **25 marks** and that for the practical component is **25 marks**.

CIE for the theory component of the IPCC

- 25 marks for the theory component are split into **15 marks** for two Internal Assessment Tests (Two Tests, each of 15 Marks with 01-hour duration, are to be conducted) and **10 marks** for other assessment methods mentioned in 22OB4.2. The first test at the end of 40-50% coverage of the syllabus and the second test after covering 85-90% of the syllabus.
- Scaled-down marks of the sum of two tests and other assessment methods will be CIE marks for the theory component of IPCC (that is for **25 marks**).
- The student has to secure 40% of 25 marks to qualify in the CIE of the theory component of IPCC.

CIE for the practical component of the IPCC

- **15 marks** for the conduction of the experiment and preparation of laboratory record, and **10 marks** for the test to be conducted after the completion of all the laboratory sessions.
- On completion of every experiment/program in the laboratory, the students shall be evaluated including viva-

voce and marks shall be awarded on the same day.

- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to **15 marks**.
- The laboratory test **(duration 02/03 hours)** after completion of all the experiments shall be conducted for 50 marks and scaled down to **10 marks.**
- Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **25 marks.**
- The student has to secure 40% of 25 marks to qualify in the CIE of the practical component of the IPCC.

SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course **(duration 03 hours)**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored by the student shall be proportionally scaled down to 50 Marks

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper may include questions from the practical component.

- The minimum marks to be secured in CIE to appear for SEE shall be 10 (40% of maximum marks-25) in the theory component and 10 (40% of maximum marks -25) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included. The maximum of 04/05 sub-questions are to be set from the practical component of IPCC, the total marks of all questions should not be more than 20 marks.
- SEE will be conducted for 100 marks and students shall secure 35% of the maximum marks to qualify for the SEE. Marks secured will be scaled down to 50.
- The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Suggested Learning Resources:

Books

1. Analog Electronic Circuits: A simplified approach by U.B. Mahadevaswamy, Pearson Education India, 2010
2. OPAMPS and Linear IC's by Ramakant Gayakwad, Fourth Edition,PearsonEducation,20015.
3. John M Yarbrough,-Digital Logic Applications and Design,Thomson Learning,2001.
4. DonaldD. Givone,—DigitalPrinciplesandDesign,McGrawHill,2002.
5. Charles H RothJr. ,LarryL.Kinney—Fundamentals of Logic Design, Cengage Learning, 7th Edition, 2013.

Web links and Video Lectures(e-Resources):

- E-book versions are available at' https://www.knimbus.com/'of the VTU consortium. Remote login available through respective college IDs.
- Youtube videos

PRACTICALCOMPONENTOFIPCC*(Maycoverall/majormodules)*

1. To construct and observe clipping for different configurations.
2. To construct and find band width of RC coupled amplifier.
3. To construct and check oscillation frequency for RC phase shift oscillator.
4. To construct and obtain OPAMP astable multi-vibrator.
5. Design and implement (i) Half Adder &Full Adderusing i)basicgates. ii)NAND gates (ii)Half Sub-tractor & Full Sub-tractor using i)basic gates ii)NAND gates.
6. Design and implement 4-bitParallel Adder/Sub-tractor using IC7483.
7. Design and Implementation of 1-bit Comparator.
8. Realize 4-variable function using IC74151(8:1MUX).
9. Realize the following flip-flops using NAND Gates. JK,DFlip-Flop.
10. Realize 4bit SISO, SIPO, PIPO using D Flip flop.
11. Realize 3bita synchronous counter using JK flip flop.
12. Realize 3bit synchronous counter using D flip flop

DATA STRUCTURES AND ALGORITHMS		Semester	III
Course Code	**BRI304**	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03
Examination nature (SEE)	Theory		

COURSE OVERVIEW:

Robotics is an interdisciplinary branch of electronic engineering and mechanical engineering. Robotics involves design, construction, operation, and use of robots. The goal of robotics is to design machines that can help and assist humans. Robotics integrates fields of mechanical engineering, electrical engineering, information engineering, mechatronics, electronics, bioengineering, computer engineering, control engineering, software engineering, mathematics, etc.

COURSE OBJECTIVES:

The objectives of this course are to:

1. Develop proficiency in designing and implementing fundamental data structures.
2. Learn various sorting and searching algorithms and analyze their time complexity.
3. Understand algorithmic problem-solving techniques, including recursion and dynamic programming.
4. Explore advanced data structures like trees, graphs, and hash tables.
5. Apply data structures and algorithms knowledge to solve real-world programming challenges efficiently.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. The lecturer's approach (L) does not have to be limited to traditional methods of teaching. It is possible to incorporate alternative and effective teaching methods to achieve the desired outcomes.
2. Utilize videos and animations to illustrate the functioning of different techniques used in the manufacturing of smart materials.
3. Foster collaborative learning exercises within the classroom to encourage group participation and engagement.
4. Pose a minimum of three Higher Order Thinking (HOT) questions during class discussions to stimulate critical thinking among students.
5. Implement Problem-Based Learning (PBL) as an approach that enhances students' analytical skills and nurtures their ability to design, evaluate, generalize, and analyze information, rather than solely relying on rote memorization.

Module-1

Introduction: Data Structure, Classification (Primitive and non-operations. Pointers: Definition and Concepts, Array of pointers, Structure and pointers

Linear Data Structures –Stacks: Introduction and Definition, Representation of stack: Array and structure representation of stacks, Operations on stacks.

Stack Applications: Conversion of Expressions, Evaluation of expressions.

Module-2
Linear Data Structures - Singly Linked lists: Definition and concepts singly linked List: Representation of link list in memory, Operations on singly Linked List. Linked List representation of stack and queues. Linear Data Structures –Queues: Introduction and Definition Representation of Queue: Array representation of queues. Linear Data Structures- Doubly Linked lists: Operations
Module-3
Nonlinear Data Structures -Basic Terminologies, Binary Trees: Properties, Representation of Binary Tree: Linear representation, Linked representation, Operations on Binary Tree: Insertion, Simple Deletion, Traversals, Binary search trees. graphs using adjacency matrix and linked list. Understanding and representing graphs using adjacency matrix AND LINKED LIST
Module-4
Introduction to Algorithms: Fundamentals of Algorithmic Problem Solving, Fundamentals of the Algorithms Efficiency: Analysis Framework, Asymptotic Notations and Basic Efficiency Classes, Mathematical Analysis of Non-Recursive Algorithms and Recursive Algorithms. Sorting And Searching Algorithms: Linear Search and Binary Search.
Module-5
Decrease & Conquer: Concept of Decrease and Conquer, Graph traversal algorithms Depth First Search, Breadth First Search. Dynamic Programming: Concept of Dynamic Programming, Computing a Binomial Coefficient. Greedy Method: Concept of Greedy technique, Prim's algorithm.
Course Outcomes (COs) (Course Skill Set) At the end of the course, the student will be able to: 1. Master the implementation and application of key data structures in programming. 2. Demonstrate the ability to analyze algorithm efficiency and optimize code. 3. Solve complex problems by applying algorithmic strategies and techniques. 4. Design and implement algorithms for tasks involving searching, sorting, and graph traversal. 5. Utilize data structures and algorithms to enhance software performance and scalability

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- For the Assignment component of the CIE, there are 25 marks and for the InternalAssessment Test component, there are 25 marks.
- The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-basedthen only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.
- For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination (SEE):

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course **(duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (witha maximum of 3 sub-questions), **should have a mix of topics** under that module.

Suggested Learning Resources:

TEXT BOOKS:

1. Ellis Horowitz and Sartaj Sahni, Fundamentals of Data Structures in C, 2nd Ed, Universities Press, 2014.
2. Introduction to the Design and Analysis of Algorithms, Anany Levitin: 2nd Edition, 2009. Pearson.
3. Seymour Lipschutz, Data Structures Schaum's Outlines, Revised 1st Ed, McGraw Hill, 2014.

REFERENCEBOOKS:

1. Reema Thareja, Data Structures using C, 3rd Ed, Oxford press, 2012.
2. Gilberg and Forouzan, Data Structures: A Pseudo-code approach with C, 2ndEd, CengageLearning,2014.
3. Jean-Paul Tremblay & Paul G. Sorenson, An Introduction to Data Structures withApplications,2nd Ed, McGraw Hill, 2013.
4. Computer Algorithms/C++, Ellis Horowitz, SatrajSahni and Rajasekaran, 2nd Edition, 2014, Universities Press.

Web links and Video Lectures (e-Resources):

- https://archive.nptel.ac.in/courses/106/102/106102064/
- https://archive.nptel.ac.in/courses/106/106/106106127/
- https://nptel.ac.in/courses/106102064
- http://elearning.vtu.ac.in/econtent/courses/video/CSE/06CS35.html
- https://nptel.ac.in/courses/106/105/106105171/
- http://www.nptelvideos.in/2012/11/data-structures-and-algorithms.html
- http://elearning.vtu.ac.in/econtent/courses/video/CSE/06CS43.html
- https://nptel.ac.in/courses/106/101/106101060/

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Real world problem solving using group discussion.

- Back/Forward stacks on browsers.
- Undo/Redo stacks in Excel or Word.
- Linked list representation of real-world queues -Music player, image viewer
- Real world problem solving and puzzles using group discussion. E.g., Fake coin identification, Peasant, wolf, goat, cabbage puzzle, Konigsberg bridge puzzle etc.,
- Demonstration of solution to a problem through programming.