This file contains the proposed syllabus for VLSI, 3rd semester. The assessment and rubrics for Mathematics and Community Project (Project Based Learning) Societal Project courses are provided along with the individual syllabus. The assessment and rubrics for all other subjects (PCC, IPCC, PCC-L and AEC) are provided at the end of this file. The rubrics provided are suggested by the BoS, however individual departments may modify them as required.

	Transform Techniques and Optimization Theory			
	Course Code	**1BMATEC301**	Scheme	2025
	Type of Course	Applied Science Course (ASC)	Semester	III
	Teaching Hours/Week (L:T:P)	3:2:0	CIE Marks	50
	Total Hours of Pedagogy per semester L /T/P/SL&TW:	42:28:0:50	SEE Marks	50
	Credits	**4**	Total Marks	100
	Examination type (SEE)	Theory	Exam Hours	3

Course outcome (Course Skill Set)

At the end of the course, the student will be able to:

CO1: Develop Fourier series representations of periodic functions and perform harmonic analysis for functions with different periodicities, discontinuities, and symmetry properties.

CO2: Apply Fourier transforms, including sine, cosine, discrete Fourier transforms (DFT), and Fast Fourier Transforms (FFT), to analyze signals and solve engineering problems involving differential equations.

CO3: Utilize Z-transforms, their properties, inverse transforms, and convolution techniques to analyze discrete-time systems and solve difference equations.

CO4: Formulate and solve Linear Programming Problems using graphical, simplex, and Big-M methods to obtain optimal solutions in engineering and management applications.

CO5: Apply transportation and assignment models, including optimization techniques such as Vogel's Approximation Method and Hungarian Method, to solve resource allocation and decision-making problems

Module-1: Fourier series

Periodic functions, Euler's Formula, Conditions for Fourier expansion(Dirichlet's condition), Fourier series of functions i) having points of discontinuity, ii) with period 2π, iii) with change of interval (arbitrary period) and iv) Even and odd functions. Half rang Fourier series. Practical harmonic analysis.

Number of Hours:8+5

Module-2: Fourier transforms.

Fourier Transforms: Infinite Fourier transform, Infinite Fourier sine and cosine transforms, Properties-Linear property, Change of scale, shifting property, Modulation theorem. Inverse transforms, Convolution theorem and its significance, Fourier transform of derivatives and integrals, Solution of PDE's using Fourier transforms. Discrete Fourier transform (DFT), Inverse DFT, Fast Fourier transform (FFT)

Number of Hours:9+6

Module-3: Discrete Transforms - Z transforms

Z-transform of Standard functions, Linearity property, Damping rule, Shifting property, Initial and final value theorems, Inverse Z-transform- Power series method, Partial fraction method, inverse integral method. Convolution theorem, Application of Z-transforms to solve difference equations.

Number of Hours:9+6

Module-4: Linear programming problems

Introduction to optimization techniques, nature and characteristics of operation research;
Introduction to Linear programming, graphical solution, solution by simplex and Big M method.

Number of Hours:8+5

Module-5: Transportation problems

Formulation of transportation problem, Initial Basic feasible solution by North-West Corner method, Least cost method, Vogel's approximation method. Optimal solutions-Problems. Formulation of assignment problems, Hungarian method-Problems

Number of Hours:8+6

Suggested Learning Resources: (Text Book/ Reference Book/ Manuals):

Text books:

1. **B.S. Grewal**, *Higher Engineering Mathematics*, 45th Edition, Khanna Publishers.
2. **Erwin Kreyszig**, *Advanced Engineering Mathematics*, 10th Edition, Wiley India.
3. **H.K. Dass and Er. Rajnish Verma**, *Higher Engineering Mathematics*, S. Chand Publications.

Reference books / Manuals:

1. **Ruel V. Churchill and James Ward Brown**, *Fourier Series and Boundary Value Problems*, McGraw-Hill Education.
2. **Hamdy A. Taha**, *Operations Research: An Introduction*, Pearson Education.
3. **Schaum's Outline of Fourier Analysis and Applications**, McGraw-Hill.
4. **Murray R. Spiegel, John Schiller and R. Alu Srinivasan**, *Schaum's Outline of Probability and Statistics*, McGraw-Hill.
5. **S. D. Sharma**, *Operations Research*, Kedar Nath Ram Nath Publications.

Web links and Video Lectures (e-Resources):

- NPTEL Courses on Engineering Mathematics
- MIT Open Course Ware Mathematics
- SWAYAM Online Courses

Teaching-Learning Process (Innovative Delivery Methods):

The following are sample strategies that educators may adopt to enhance the effectiveness of the teaching-learning process and facilitate the achievement of course outcomes.

1. **Flipped Classroom Approach**
   - Students review video lectures and reading materials before class.
   - Classroom sessions focus on problem-solving, discussions, and applications of transform techniques and optimization models.
2. **Problem-Based Learning (PBL)**
   - Real-world engineering problems involving Fourier Transforms, Z-Transforms, and Linear Programming are assigned for collaborative solution development.
3. **ICT-Enabled Teaching** (may be conducted in Tutorial hours)
   - Use of MATLAB, Python, and online simulation tools to visualize transforms, optimization problems, and signal-processing applications.
4. **Collaborative Learning** (may be conducted in Tutorial hours)
   - Group assignments and mini-projects on optimization models and transform applications.

Assessment Structure:

The assessment in each course is divided equally between Continuous Internal Evaluation (CIE) and the Semester End Examination (SEE), with each carrying 50% weightage.

- To qualify and become eligible to appear for SEE, in the **CIE**, a student must score at least **40% of 50 marks**, i.e., **20 marks**.
- To pass the **SEE**, a student must score at least **35% of 50 marks**, i.e., **18 marks**.
- Notwithstanding the above, a student is considered to have **passed the course,** provided the combined total of **CIE and SEE** is at least **40 out of 100 marks**.

Continuous Comprehensive Assessments (CCA)+ Internal Assessment Test (IA) = Continuous Internal EvaluationCIE [25+25=50 marks]

A minimum of **two Internal Assessment Tests(IA)**shall be conducted, carrying a total of **25 marks**.

In addition, **Continuous Comprehensive Assessment (CCA)** shall be conducted for a total of **25 marks.**

It is recommended to include **a maximum of two learning activities** as part of the CCA to foster the **holistic development of students**. These activities shall be:

Sl. No.	Name of the Learning activity	Maximum Marks
1.	Assignment (at RBL3 levels)	10
2.	GATE-based Aptitude Test	15

Rubrics **for Learning Activity–1: Assignment (10 Marks)**

Performance Indicator	Superior (10)	Good (8)	Fair (6)	Needs Improvement (5)
Understanding of Concepts	Demonstrates excellent conceptual clarity and application	Good understanding with minor errors	Basic understanding	Poor understanding
Problem Solving Ability	Solves all problems correctly with proper methodology	Solves most problems correctly	Partial solutions with errors	Unable to solve problems effectively
Mathematical Accuracy	Calculations and derivations are error-free	Minor computational errors	Several errors	Significant errors
Presentation & Organization	Well-structured, neat, and professionally presented	Organized with minor deficiencies	Average presentation	Poor presentation

Rubrics for Learning Activity–2: GATE-Based Aptitude Test (15 Marks)

Performance Indicator	**Superior (15)**	**Good (12)**	**Fair (10)**	**Needs Improvement (8)**
Quantitative Aptitude	≥90% correct responses	75–89% correct	60–74% correct	<60% correct
Analytical Thinking	Excellent logical reasoning and interpretation	Good reasoning ability	Moderate reasoning	Weak reasoning
Time Management	Completes all questions within allotted time	Completes most questions	Requires additional time	Unable to complete
Accuracy & Precision	Very high accuracy	Good accuracy	Moderate accuracy	Low accuracy

Suggested Learning Activities may include (but are not limited to):

- Course Project
- Case Study Presentation
- Programming Assignment
- Tool/Software Exploration
- Literature Review
- Open Book Test (preferably at RBL4 and RBL5 levels)
- GATE-based Aptitude Test
- Assignment (at RBL3, RBL4, or RBL5 levels)
- Any other relevant and innovative academic activity
- Use of MOOCs and Online Platforms

Suggested Innovative Delivery Methods may include (but are not limited to):

- Flipped Classroom
- Problem-Based Learning (PBL)
- Case-Based Teaching
- Simulation and Virtual Labs
- Partial Delivery of course by Industry expert/ industrial visits
- ICT-Enabled Teaching
- Role Play

Term Work (TW) and Self Learning (SL) components in Number of Hours per semester		
Term work (includes assignments, seminars, micro projects, industrial visits, any other student activities etc.)		
Sl. No.	**Term Work (TW) Activity**	**Number of Hours / Semester**
1.	Seminar on Fourier Series of periodic functions and harmonic analysis	5
2.	MATLAB/Python Simulation of Fourier and Z-Transform problems	5
3.	Mini Project on Linear Programming Models in Engineering Applications	5
4.	Case Study on Signal Processing using Transform Techniques	5
SL: Self Learning, MOOCs, spoken tutorials, online educational resources etc.		
Sl. No.	**Self-Learning (SL) Activity**	**Number of Hours / Semester**
1.	Application of Fourier Series in signal representation and on harmonic analysis of periodic signals.	6

	2.	Explore applications of DFT and FFT in digital signal processing.	6
	3.	Solve a set of difference equations using Z-transforms	6
	4.	Develop and solve two real-world optimization problems	6
	5.	Study industrial applications of transportation and assignment models	6

Continuous Internal Evaluation (CIE)

1. The CIE marks shall be decided based on internal tests and other outcome-based activities. The continuous internal evaluation shall be carried out by the teacher handling the course.
2. Out of 50 marks earmarked for CIE, 25 marks shall be assigned for internal tests. The first test shall be conducted after completing two modules of the syllabus and the second one after completing the remaining three modules.
3. The remaining 25 marks shall be assigned for Continuous Course Assessment (CCA), conducted as per the rubrics listed in the assessment section of the respective syllabus.
4. A student shall obtain a minimum of 40% marks or 20 out of 50 marks allotted to CIE to become eligible to appear for the SEE.

Passing requirement in SEE

1. For a pass in the Semester End Examination (SEE), a student shall secure a minimum of 35 marks out of 100.
2. For the declaration of a pass grade, the sum of the Continuous Internal Evaluation (CIE) marks (out of 50) marks and the SEE marks scaled down to 50 shall be greater than or equal to 40 marks.
3. If the total (CIE + SEE) is less than 40 marks, the student shall be awarded the grade ‘F’ (Fail).

Digital System Design using Verilog

Course Code	**1BEC302**	Scheme	2025
Type of course	**Theory and Lab**	Semester	III
Teaching Hours/Week (L:T:P)	3:0:2	CIE Marks	50
Total Hours of Pedagogy L:T:P:SL&TW	42:0:28:50	SEE Marks	50
Credits	**04**	Total Marks	100
Type of Examination (IPCC):	Theory- CIE +SEE, Lab- CIE only.	Exam Hours	3

Course outcome (Course Skill Set)
At the end of the course, students will be able to:

CO1: Apply Boolean algebra principles to simplify logic functions using Karnaugh Maps (K-Maps) and the Quine–McCluskey minimization technique.
CO2: Analyze the operation and behavior of combinational logic circuits and standard logic building blocks.
CO3: Design combinational digital systems using logic gates, multiplexers, decoders, and arithmetic circuits.
CO4: Analyze and design synchronous and asynchronous sequential circuits using SR, JK, D, and T flip-flops.
CO5: Model, simulate, and verify combinational and sequential digital circuits using the Verilog Hardware Description Language (HDL).

Module-1

Principles of Combinational Logic: Definition of combinational logic, Canonical forms, Generation of switching equations from truth tables, Karnaugh maps-up to 4 variables, Quine McCluskey Minimization Technique. Quine-McCluskey using Don't Care Terms. (Section 3.1 to 3.5 of Text1).

Number of Hours: 08

Module-2

Logic Design with MSI Components and Programmable Logic Devices: Binary Adders and Subtractors, Decimal Adders, Comparators, Decoders, Encoders, Multiplexers, Programmable Logic Devices (PLDs) (Section 5.1 to 5.7 of Text 2)

Number of Hours: 08

Module-3

Introduction to Verilog: Structure of Verilog module, Styles of Description, Ports, Operators, Data Types,. (Section 1.1 to 1.6.2 (only Verilog), Text 3)
Verilog Data flow description: Highlights of Data flow description, Signal Declaration And Assignment Statement, Structure of Data flow description. (Section 2.1 to 2.2 (only Verilog) of Text3)

Number of Hours: 08

Module-4

Flip-Flops and its Applications: The Master-Slave Flip-flops(Pulse-Triggered flip-flops): The basic bistable element, Latches, Timing Considerations, SR flip flops, JK flip flops, Characteristic equations, Registers, Binary Ripple Counters, Synchronous Binary Counters, Counters based on Shift Registers, Design of Synchronous mod-n Counter using clocked T, J K, D and SR flip-flops.(Section 6.1 to 6.4, 6.6 to 6.9 (Excluding 6.9.3) of Text2)

Number of Hours: 10

Module-5

Verilog Behavioral Description: Structure, Variable Assignment Statement, Sequential Statements, Loop Statements, Verilog Behavioral Description of Multiplexers. (Section 3.1 to 3.4 (only Verilog) of Text 3)
Verilog Structural Description: Highlights of Structural description, Organization of structural description, Structural description of ripple carry adder.(Section4.1 to 4.2 of Text 3)

Number of Hours: 10

PRACTICAL COMPONENTS OF IPCC

PART – A: FIXED SET OF EXPERIMENTS

1. To simplify the given Boolean expressions and realize using Verilog program
2. To realize Adder/Subtractor (Full/half) circuits using Verilog data flow description.
3. To realize 4-bit ALU using Verilog program.
4. To realize the following Code converters using Verilog Behavioral description a) Gray to binary and vice versa b) Binary to excess3 and vice versa
5. To realize using Verilog Behavioral description:8:1mux, 8:3encoder, Priority encoder
6. To realize using Verilog Behavioral description:1:8Demux, 3:8 decoder,2 –bit Comparator
7. To realize using Verilog Behavioral description: Flip-flops: a)JK type b)SR type c)T type and d) D type
8. To realize Counters-up/down (BCD and binary) using Verilog Behavioral description.
9. Verilog programs to interface Switches and LEDs to the FPGA/CPLD and demonstrate its working.

PART – B: OPEN ENDED EXPERIMENTS

Open-ended experiments are a type of laboratory activity where the outcome is not predetermined and students are given the freedom to explore, design, and conduct the experiment based on the problem statements as per the concepts defined by the course coordinator. It encourages creativity, critical thinking, and inquiry-based learning.

1. Design and Optimization of a Combinational Logic System
2. Configurable Arithmetic Logic Unit (ALU) Design
3. Design of a Finite State Machine (FSM) for a Real-Time Application
4. Sequential Circuit Design Using Flip-Flops

Suggested Learning Resources: (Textbook/ Reference Book/ Manuals):

Textbooks:

1. J. M. Yarbrough, Digital Logic Applications and Design. Clifton Park, NY, USA: Thomson Learning, 2006.
2. D. D. Givone, Digital Principles and Design. New York, NY, USA: McGraw-Hill, 2002.
3. N. Botros, HDL with Digital Design: VHDL and Verilog. Dulles, VA, USA: Mercury Learning and Information, 2015

Reference books / Manuals:

1. Fundamentals of logic design, by Charles H Roth Jr., Cengage Learning
2. Fundamentals of HDL, by Cyril PR, Pearson/Sanguine 2010
3. Logic Design, by Sudhakar Samuel, Pearson/Sanguine, 2007

Web links and Video Lectures (e-Resources):

1. www.chipverify.com
2. https://www.youtube.com/watch?v=vHLBO05TeyU&list=PLwdnzlV3ogoVlY7iVqr-FhWUQEX7JDdiP
3. https://www.youtube.com/playlist?list=PLbRMhDVUMngePP5JcezxImF-FzOC9wstz

Teaching-Learning Process (Innovative Delivery Methods):

The following are sample strategies that educators may adopt to enhance the effectiveness of the teaching-learning process and facilitate the achievement of course outcomes.

1. Interactive lectures using digital design visualization tools and multimedia presentations to explain logic design concepts.
2. Simulation-based learning using Verilog HDL simulators to model, simulate, and verify digital

circuits.

3. Flipped classroom methodology, where students study digital design concepts before class and engage in design exercises during class.
4. Mini-projects and project-based learning involving the design and verification of digital systems such as counters, ALUs, finite state machines, and controllers.
5. Collaborative learning activities through group discussions, peer reviews, and team-based design projects.
6. Continuous assessment through quizzes, Verilog coding challenges, and design reviews to reinforce learning and provide timely feedback.

Network Analysis

Course Code	**1BEC303**	Scheme	2025
Type of Course	**PCC**	Semester	III
Teaching Hours/Week (L:T:P)	3:2:0	CIE Marks	50
Total Hours of Pedagogy per semester L /T/P/SL&TW:	42:28:0:50	SEE Marks	50
Credits	**4**	Total Marks	100
Examination type (SEE)	Theory	Exam Hours	3

Course outcome (Course Skill Set)

At the end of the course, the student will be able to:

1. **Analyze** electronic networks using mesh and nodal analysis techniques for DC and AC circuits with dependent and independent sources.
2. **Evaluate** electronic circuit responses (currents, voltages, and power) using network theorems.
3. **Analyze** RL, RC, and RLC circuits under transient conditions using initial and final condition concepts.
4. **Analyze** linear electronic circuits using Laplace transform techniques.
5. **Evaluate** the performance of two-port networks by determining parameters and impedance characteristics.

Module-1

Basic Concepts- Mesh and Node Analysis: Introduction, Source of Electrical Energy, Kirchoffs Laws, Source transformations, General Network Transformations, Mesh and Node analysis with linearly dependent and independent sources for DC and AC networks.

Number of Hours: 15

Module-2

Network Theorems: Introduction, Superposition Theorem, Reciprocity Theorem, Conditions for Reciprocity, Examples of Reciprocal/Non-Reciprocal circuits, Thevenin's Theorem, Maximum Power transfer theorem.

Case Study–1: Maximum Power Transfer in Electronic Systems Design

Number of Hours: 13

Module-3

Transient behavior and initial conditions: Behavior of circuit elements under switching condition and their Representation, Evaluation of initial and final conditions in RL, RC and RLC circuits for AC and DC excitations.

Case Study: RC Circuit–Based Power-ON Delay in Electronic Indicator Systems

Number of Hours: 14

Module-4

Laplace Transformation &Applications: Solution of networks, step, ramp and impulse responses, Waveform Synthesis, Transfer function of elementary passive circuits, Network Synthesis

Case Study: Concept of poles for first order passive filters and their use in computing time response characteristics and bandwidth

Number of Hours: 14

Module-5

Two -Port Network: Introduction, Characterisation of Linear Time-invariant Two-port Networks, Open- Circuit Impedance Prameters, Short- circuit Admittance Parameters, Transmission Parameters, Short introduction to Hybrid parameters (1 hour material), Why multiple representations are required, Two-port Symmetry, Input impedance interms of Two-port Parameters, Output Impedance

Number of Hours: 14

Suggested Learning Resources: (Textbook/ Reference Book/ Manuals):

Textbooks:

1. M. E. VanValkenburg (2000), Network Analysis, Prentice Hall of India, 3rdedition, 2000, ISBN:9780136110958.
2. Roy Choudhury-Networks and Systems, 2nd edition, New Age International Publications, 2006, ISBN: 9788122427677

Reference books / Manuals:

1. Hayt, Kemmerly and Durbin-Engineering Circuit Analysis, TMH7th Edition, 2010.
2. J. David Irwin/ R. Mark Nelms- Basic Engineering Circuit Analysis JohnWiley, 8th ed,2006.
3. Charles K Alexander and Mathew NO Sadiku-Fundamentals of Electric Circuits, Tata Page 17 BE III Semester in ECE/TCE 15.09.2023 McGraw-Hill,3rc1 Ed,2009.

Web links and Video Lectures (e-Resources):

https://nptel.ac.in/courses/108105159

Teaching-Learning Process (Innovative Delivery Methods):

The following are sample strategies that educators may adopt to enhance the effectiveness of the teaching-learning process and facilitate the achievement of course outcomes.

1. Ensure at least 2 hours of review of mathematical concepts such as matrix algebra, complex variables, first and second order differential equations during the tutorial sessions

2.Present case studies for each module which have industry relevance

3. Use of simulation tool or even hardware demonstrations in the classroom to illustrate complex concepts

Analog Electronics and Linear Integrated Circuits

Course Code	**1BEC304**	Scheme	2025
Type of Course	**PCC**	Semester	III
Teaching Hours/Week (L:T:P)	3:0:0	CIE Marks	50
Total Hours of Pedagogy per semester L /T/P/SL&TW:	42:0:0:48	SEE Marks	50
Credits	**3**	Total Marks	100
Examination type (SEE)	Theory	Exam Hours	3

Course outcome (Course Skill Set)

At the end of the course, the student will be able to:

1. Describe the working principle, fundamental characteristics of various semiconductor devices such as transistors, MOSFETs, and operational amplifiers in basic electronic circuits.
2. Analyze basic amplifier circuits using the principles BJTs, MOSFETS, and operational amplifiers.
3. Illustrate the fundamental concepts of oscillators and timers.
4. Design basic filters and power amplifiers.
5. Analyze the fundamental concepts of linear Op-Amps, linear Op-Amps and their applications.
6. Analyzethe electronic circuit schematic and its working.

Module-1

BJT AC Models: Base Biased Amplifier, Emitter Biased Amplifier, Small Signal Operation, AC Beta, AC Resistance of The Emitter Diode, Two Transistor Models, Analyzing Amplifier.
Voltage Amplifiers: Voltage Gain, Multistage Amplifiers.
CC And CB Amplifiers: CC Amplifier, Output Impedance, Cascading CE And CC, Darlington Connections, Voltage Regulation, The Common Base Amplifier.
Text book 1: 8.1-8.7, 8.9, 9.1, 9.3-9.8
Number of Hours:9

Module-2

MOSFET Biasing in MOS Amplifier Circuits: Fixing VGS, Fixing VG, Drain to Gate Feedback Resistor.
Small Signal Operation and Modelling: The DC Bias Point, Signal Current in Drain, Voltage Gain, Small Signal Equivalent Circuit Models, Transconductance, The T Equivalent Circuit Model.
MOSFET Amplifier Configuration: Basic Configurations, Characterizing Amplifiers, CS Amplifier with And Without Source Resistance, The Common Gate Amplifier, Source Follower.
Text book 2: 7.2, 7.2.1, 7.3, 7.3.1 - 7.3.6, 7.4, 7.4.1
Number of Hours:9

Module-3

Negative Feedback: Four Types of Negative Feedback, VCVS Voltage Gain, Other VCVS Equations, ICVS Amplifier, VCIS Amplifier, ICIS Amplifier (No Mathematical Derivation).
Oscillator: Theory of Sinusoidal Oscillation, The Wein-Bridge Oscillator, RC Phase Shift Oscillator, The Colpitts Oscillator, Hartley Oscillator, Crystal Oscillator.
The 555 Timer: Monostable Operation, Astable Operation.
Text book 1: 17.1-17.6, 21.1-21.8
Number of Hours:8

Module-4

Power Amplifiers: Amplifier Terms, Two Load Lines, Class A Operation, Class B Operation, Class B Push Pull Emitter Follower, Class C Operation.
Active Filters: Ideal Responses, First Order Stages, VCVS Unity Gain Second Order Low Pass Filters, VCVS Equal Component Low Pass Filters, VCVS High Pass Filters, MFB Bandpass Filters, Bandstop Filters.
Text book 1: 10.1-10.5, 10.8, 19.1, 19.4, 19.5, 19.7-19.10
Number of Hours:8

Module-5

Linear Op-amp Circuits: Digital to Analog Conversion: Weighted Resistor DAC, R-2R DAC, Analog to Digital Conversion: Digital RAMP ADC, Successive Approximation ADC. Signal Processing Circuits: Saturating and Non Saturating Precision HWR, Precision FWR Using HWR and Summing Circuit.
Nonlinear Op-Amp Circuits: Zero Crossing Detector, Inverting Schmitt Trigger Circuit, Non-Inverting Schmitt Trigger Circuit.
DC Voltage Regulators: Introduction, Voltage Regulator Basics.
Text book 3: 15.2, 15.4, 9.1, 9.2, 8.2-8.4, 13.1
Number of Hours:8

Suggested Learning Resources: (Text Book/ Reference Book/ Manuals):

Text books:

1. Albert Malvino, David J Bates, Patrick E. Hoppe, Electronic Principles, 9th Edition, Mc Graw Hill Education, 2021.
2. Adel S Sedra, Kenneth C Smith, Microelectronic Circuits, 7th Edition, Oxford University Press, 2015.
3. David A. Bell, Operational Amplifiers and Linear ICs, 3rd Edition, Oxford University Press, 2011.

Reference books / Manuals:

1. Integrated Electronics: Analog and Digital Circuits and Systems, Jacob Millman, Christos C. Halkias, McGraw-Hill, 2015.
2. Electronic Devices and Circuit, Boylestad&Nashelsky, Eleventh Edition, Pearson, January 2015.

Web links and Video Lectures (e-Resources):

- https://nptel.ac.in/courses/108102112
- https://onlinecourses.nptel.ac.in/noc25_ee157/preview
- https://nptel.ac.in/courses/108106188

Teaching-Learning Process (Innovative Delivery Methods):
The following are sample strategies that educators may adopt to enhance the effectiveness of the teaching-learning process and facilitate the achievement of course outcomes.
1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
2. Show Video/animation films to explain the functioning of various analog and digital circuits.
3. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyse information rather than simply recall it.
4. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
5. Arrange visits to nearby industries to give brief information about the electronics manufacturing industry.
6.. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Fundamentals of Signal Processing

Course Code	**1BVL305**		Scheme	2025
Type of Course	**PCC**		Semester	III
Teaching Hours/Week (L:T:P)	3:0:0		CIE Marks	50
Total Hours of Pedagogy per semester L /T/P/SL&TW:	42:0:0:48		SEE Marks	50
Credits	**3**		Total Marks	100
Examination type (SEE)	Theory		Exam Hours	3

Course outcome (Course Skill Set)
At the end of the course, the student will be able to:

CO1: Identify and characterize different classes of signals and systems
CO2: Analyze the signals in time and frequency domain for non-periodic signals
CO3: Characterize LTI systems in the frequency domain
CO4: Compute discrete Fourier transform efficiently
CO5: Implement discrete time systems and basic signal processing algorithms

Module-1

Introduction to Signals and Systems: Definition of signals and systems, Classification of signals, Basic Operations on signals, Elementary signals, Overview of Specific Systems, Properties of Systems, The convolution sum Convolution sum evaluation procedure (Sections 1.1 to 1.8, 2.1-2.3 of Textbook 1)

Number of Hours: 8

Module-2

Frequency Analysis of Signals: The concept of frequency in continuous tine and discrete time signals, The Fourier Transform for Discrete Time Aperiodic Signals, Energy Density Spectrum of Aperiodic Signals, Relationship of the Fourier Transform to the z-transform (Sections 4.1, 4.3.3, 4.3.6 of Textbook 2)

Number of Hours: 8

Module-3

Frequency Domain Analysis of LTI Systems: Frequency Response of a system with a rational system function, Computation of frequency response function, Ideal Filter Characteristics, Lowpass, Highpass, and Band pass filters, Digital Resonators, Notch Filters, Comb Filters, All pass filters (Sections 5.2-5.3, 5.4.1-5.4.5 of Textbook 2)

Number of Hours: 8

Module-4

Discrete Fourier Transform: Ideal sampling and reconstruction of continuous-time signals, Discrete-Time Processing of Continuous-Time Signals, Frequency-Domain Sampling and Reconstruction of discrete-time signals, Discrete Fourier Transform, DFT as a linear transformation, properties of DFT: Time & Frequency shift, time scaling, convolution, Parsevals theorem, Spectral analysis using DFT. Fast Fourier Transform: Radix-2 four point DIT (Sections 7.1-7.2, 8.1.1, 8.1.2, 8.1.3 of Textbook 2)
Number of Hours: 10

Module-5

Implementation of Discrete-Time Systems: Structures for realization of discrete-time systems, Structures for FIR systems: Direct form, cascade form, Structure for IIR Systems: Direct-Form, Casacde form and Parallel form (Sections 9.1, 9.2.1, 9.2.2, 9.3.1, 9.3.3, 9.3.4)

Number of Hours: 8

Analog Electronics and Linear Integrated Circuit Lab		Scheme	2025
Course Code	**1BECL306**	Semester	III
Teaching Hours/Week (L:T:P)	0:0:2	CIE Marks	50
Total Hours of Pedagogy L:T:P:SL/TW	0:0:28:2	SEE Marks	50
Credits	1	Total Marks	100
Examination type (SEE)	**Practical**	Exam Hours	3

Course Outcome (Course Skill Set)

At the end of the course, the student will be able to:

1. Apply the knowledge of BJT circuit to determine gain, bandwidth and impedance.
2. Apply the knowledge of FET circuit to determine gain, bandwidth and impedance.
3. Understand the working of oscillators.
4. Realize Op-Amp circuit for the application as voltage follower, integrator, and differentiator.
5. Apply modulation technique.

Note:

1. The laboratory syllabus consists of PART-A and PART-B. While PART-A has 8 conventional experiments, PART-B has 4 typical open-ended experiments. The maximum marks for the laboratory course are 100.
2. Both PART-A and PART-B are considered for CIE and SEE.
3. Students have answer 1(one) question from PART-A and 1(one) question from PART-B.
   a. The questions set for SEE shall be from among the experiments under PART-A. It is evaluated for **70 marks** out of the maximum 100 marks.
   b. The open-ended question set for SEE shall be any other open-ended question and not selected from the experiments under PART-A. It shall be evaluated for **30 marks.**
4. For Continuous Internal Evaluation (CIE) during the semester, classwork shall typically include open-ended questions from **Part-B**, along with other similar questions designed to enhance the students' skills.

PART – A
FIXED SET OF EXPERIMENTS

1. Design and Set-up the BJT Common Emitter Voltage Amplifier with and Without Feedback and Determine the Gain, Bandwidth, Input and Output Impedance.
2. Design and Set-up BJT/ FET Based I) Colpitts Oscillator, II) Crystal Oscillator
3. Realize BJT Darlington Emitter Follower and Determine Gain, Input and Output Impedances.
4. Design 4-Bit R - 2R OP-Amp Digital to Analog Converter: I) For A 4-Bit Binary Input Using Toggle Switches, II) By Generating Digital Inputs Using Mod-16
5. Design and Test the Second Order Active Filters and Plot the Frequency Response: I) Low Pass Filter, II) High Pass Filter
6. Design and Testing of Precision Rectifiers: I) Half-Wave Precision Rectifier, II) Full-Wave Precision Rectifier
7. Design and Test Monostable and Astable Multivibrator Using 555 Timer.
8. Design and Test a Regulated Power Supply Using IC 7805 And IC 7905.

PART – B
OPEN ENDED EXPERIMENTS

Open-ended experiments are a type of laboratory activity where the outcome is not predetermined and

students are given the freedom to explore, design, and conduct the experiment based on the problem statements as per the concepts defined by the course coordinator. It encourages creativity, critical thinking, and inquiry-based learning.
1. Concept 1Design a FET Voltage Series Feedback Amplifier and Determine the Gain, Input and Output Impedances. 2. Concept 2Design and Experimental Study of a Class-C Tuned Amplifier 3. Concept 3Design of a Schmitt Trigger for Given UTP And LTP. 4. Concept 4Design and Testing of a Sample and Hold Circuit.

Suggested Learning Resources: (Text Book/ Reference Book/ Manuals):

Textbooks:

1. Electronic Devices and Circuits, David A Bell, 5th Edition, Oxford, 2018.
2. Op-amps and Linear Integrated Circuits, Ramakanth A Gayakwad, Pearson Education, 4th Edition.
3. Basic Electronics, D.P Kothari and I J Nagrath, McGraw Hill Education Pvt ltd, 2015.
4. Robert L. Boylestad, Louis Nashelsky, "Electronic Devices and Circuit Theory", 11th Edition, PHI, 2016.

Web links and Video Lectures (e-Resources):

- http://digimat.in/nptel/courses/video/108102112/L01.html
- https://www.youtube.com/playlist?list=PLp6ek2hDcoNDAw1BehPFazZ5ogPV8UlQa

Teaching-Learning Process (Innovative Delivery Methods):

The following are sample strategies that educators may adopt to enhance the effectiveness of the teaching-learning process and facilitate the achievement of course outcomes.

1. While explaining each experiment, also focus on the application of that particular experiment in the electronics industry
2. In labs utilizing software programming, the emphasis must be on student understanding of the logic (e.g. pseudo-code) of the code, which libraries are required, which important functions calls need to be made and expected output. Faculty should not penalize students for making syntax errors in codes in the write up – however students must be able to debug the errors during program execution
3. Students should not memorize pin diagrams, these must be provided to the student during CIE and SEE
4. For record writing, faculty should ensure students write the main objective, design and procedure in their own words – and do not copy from manuals/online. Also, record writing should involve higher Blooms levels and not just Remember and Understand levels.

	Data Structures using Python			
	Course Code	**1BVLL307A**	Scheme	2025
	Type of Course	Ability Enhancement Course (Laboratory)	Semester	III
	Teaching Hours/Week (L:T:P)	0:0:2	CIE Marks	50
	Total Hours of Pedagogy L:T:P:SL&TW	0:0:28:02	SEE Marks	50
	Credits	01	Total Marks	100
	Type of Examination	Practical	Exam Hours	3

Course outcome (Course Skill Set)

At the end of the course, the student will be able to:

1. Implement basic data structures using a programming language (Python).
2. Perform operations on arrays, stacks, queues, and linked lists.
3. Analyze simple problems and select an appropriate data structure.
4. Develop small programs using data structures for practical applications.

SET OF PROGRAMS / EXPERIMENTS using PYTHON

1. Program for array traversal
2. Insert and delete elements in an array
3. Linear search implementation
4. Stack implementation using array
5. Balanced parentheses using stack
6. Infix to postfix conversion
7. Queue implementation using array
8. Circular queue implementation
9. Linked list creation and traversal
10. Linked list insertion and deletion
11. Reverse a linked list
12. Bubble sort implementation
13. Selection sort implementation
14. Mini application using stack or queue

Suggested Learning Resources: (Text Book/ Reference Book/ Manuals):

Textbooks:

1. R. D. Necaise, Data Structures and Algorithms Using Python. Hoboken, NJ, USA: Wiley, 2016
2. N. Karumanchi, Data Structures and Algorithms Made Easy. Hyderabad, India: CareerMonk Publications.

Web links and Video Lectures (e-Resources):

1. **https://www.youtube.com/watch?v=_uQrJ0TkZlc**
2. **https://www.youtube.com/watch?v=nLRL_NcnK-4**
3. **https://www.youtube.com/playlist?list=PLdo5W4Nhv31bbKJzrsKfMpo_grxuLl8LU**

Teaching-Learning Process (Innovative Delivery Methods):

The following are sample strategies that educators may adopt to enhance the effectiveness of the teaching-learning process and facilitate the achievement of course outcomes.

1. Problem-Based Learning through real-life data structure applications.
2. Visualization and simulation of data structure operations using software tools.
3. Pair Programming and Peer Learning for collaborative code development.
4. Mini Project-Based earning integrating multiple data structures in Python applications.

Simulation of Circuits and Devices

Course Code	**1BVLL307B**	Scheme	2025
Type of Course	Ability Enhancement Course (Laboratory)	Semester	III
Teaching Hours/Week (L:T:P)	0:0:2	CIE Marks	50
Total Hours of Pedagogy L:T:P:SL&TW	0:0:28:02	SEE Marks	50
Credits	01	Total Marks	100
Type of Examination	Practical	Exam Hours	03

Course outcome (Course Skill Set)

At the end of the course, the student will be able to:

1. Use simulation tools to create and analyze basic electronic circuits.
2. Simulate diode and transistor characteristics.
3. Perform DC, AC, and transient analysis of circuits.
4. Interpret simulation results and compare with theoretical expectations.

SET OF EXPERIMENTS

1. Familiarization with the schematic capture and circuit simulation software interface.
2. Draw the schematic of a resistor network and simulate it to verify Ohm's Law.
3. Draw and simulate the schematic of a PN junction diode circuit to obtain its V–I characteristics.
4. Draw and simulate the schematic of a Zener diode circuit to study its characteristics.
5. Draw and simulate the schematic of a BJT circuit to obtain its output characteristics.
6. Draw and simulate the schematic of a MOSFET circuit to obtain its transfer characteristics.
7. Draw and simulate the schematic of a common-emitter amplifier and analyze its performance.
8. Draw and simulate the schematic of a common-source MOSFET amplifier and analyze its performance.
9. Draw and simulate the schematics of RC low-pass and high-pass filters and study their frequency and transient responses.
10. Draw and simulate the schematic of a half-wave rectifier and analyze its output waveform.
11. Draw and simulate the schematic of a full-wave bridge rectifier and analyze its output waveform.
12. Mini Project: Design, draw, simulate, and analyze a simple electronic circuit using schematic capture and circuit simulation software.

Suggested Learning Resources: (Text Book/ Reference Book/ Manuals):

Textbooks:

1. A. S. Sedra and K. C. Smith, Microelectronic Circuits, 7th ed. New York, NY, USA: Oxford University Press, 2015.
2. R. L. Boylestad and L. Nashelsky, Electronic Devices and Circuit Theory, 11th ed. Noida, India: Pearson Education, 2015.

Reference books / Manuals:

1. LTspice XVII User Guide and Help Manual. Wilmington, MA, USA: https://www.analog.com/en/resources/design-tools-and-calculators/ltspice-simulator.html?utm_source=chatgpt.com
2. J. W. Eaton, D. Bateman, S. Hauberg, and the ngspice Development Team, *Ngspice User's Manual*, Version 46. [Online]. Available: https://ngspice.sourceforge.io/docs.html?utm_source=chatgpt.com

Web links and Video Lectures (e-Resources):

1. MIT Open Course Ware – Circuit simulation lectures
   https://ocw.mit.edu/courses/6-002-circuits-and-electronics-spring-2007/resources/lecture-videos/?utm_source=chatgpt.com
2. All About Circuits – SPICE tutorials
   https://www.allaboutcircuits.com/textbook/product/circuit-simulation/?utm_source=chatgpt.com

Teaching-Learning Process (Innovative Delivery Methods):

The following are sample strategies that educators may adopt to enhance the effectiveness of the teaching-learning process and facilitate the achievement of course outcomes.

1. Simulation-Based Experiential Learning using SPICE tools for circuit analysis and verification.
2. Problem-Based Learning through parameter variation and performance evaluation of electronic circuits.
3. Collaborative Learning involving team-based circuit design, simulation, and result analysis.
4. Mini Project-Based Learning for application-oriented electronic circuit development and validation.

Tools that can be used:

Any free following circuit simulation software or any commercial schematic simulation software (such as Siemens EDA, Cadence EDA, Altium etc.):

1. LTspice
2. Ngspice

	Linux Fundamentals and Introduction to Python Programming			
	Course Code	**1BVLL307C**	Scheme	2025
	Type of Course	Ability Enhancement Course (Laboratory)	Semester	III
	Teaching Hours/Week (L:T:P)	0:0:2	CIE Marks	50
	Total Hours of Pedagogy L:T:P:SL/TW	0:0:28:02	SEE Marks	50
	Credits	01	Total Marks	100
	Type of Examination	Practical	Exam Hours	03

Course outcome (Course Skill Set)

At the end of the course, the student will be able to:

1. Use Linux terminal commands for file and directory management.
2. Perform user management, permissions handling, and process control in Linux.
3. Write basic Python programs using variables, operators, and control structures.
4. Implement Python programs using functions and basic data structures.

SET OF EXPERIMENTS

1. Installation and exploration of Linux environment.
2. Practice basic Linux commands for file and directory operations.
3. Working with file permissions using chmod and chown.
4. Searching text using grep and files using find.
5. Monitoring and managing processes in Linux.
6. Writing Python programs for arithmetic operations.
7. Python programs using conditional statements.
8. Python programs using loops.
9. Implementing Python functions.
10. Python programs using lists and strings.
11. File handling in Python

Suggested Learning Resources: (Text Book/ Reference Book/ Manuals):

Textbooks:

1. OccupyTheWeb, Linux Basics for Hackers: Getting Started with Networking, Scripting, and Security in Kali, 1st ed. San Francisco, CA, USA: No Starch Press, 2018.
2. E. Matthes, Python Crash Course: A Hands-On, Project-Based Introduction to Programming, 2nd ed. San Francisco, CA, USA: No Starch Press, 2019.

Web links and Video Lectures (e-Resources):

1. Linux Foundation free Linux tutorials
   https://training.linuxfoundation.org/resources/free-courses/?utm_source=chatgpt.com
2. Python Software Foundation official Python documentation
   https://docs.python.org/3/?utm_source=chatgpt.com

Teaching-Learning Process (Innovative Delivery Methods):

The following are sample strategies that educators may adopt to enhance the effectiveness of the teaching-learning process and facilitate the achievement of course outcomes.

1. Hands-on Experiential Learning through Linux command execution and Python programming.

2. Problem-Based Learning using Linux utilities and Python for practical computing tasks.
3. Collaborative Pair Programming and Peer Learning for program development and debugging.
4. Application-Based Learning through mini projects integrating Linux and Python concepts.

Numerical Computing Laboratory using GNU Octave / Scilab

Course Code	**1BVLL307D**	Scheme	2025
Type of Course	Ability Enhancement Course (Laboratory)	Semester	III
Teaching Hours/Week (L:T:P)	0:0:2	CIE Marks	50
Total Hours of Pedagogy L:T:P:SL/TW	0:0:28:02	SEE Marks	50
Credits	01	Total Marks	100
Type of Examination	Practical	Exam Hours	03

Course outcome (Course Skill Set)

At the end of the course, the student will be able to:

1. Use the GNU Octave / Scilab environment for basic numerical computations.
2. Write simple GNU Octave / Scilab scripts and functions.
3. Plot and analyze engineering data using GNU Octave / Scilab.
4. Apply GNU Octave / Scilab for simple signal processing and electronics applications.

SET OF PROGRAMS / EXPERIMENTS

1. Introduction to GNU Octave / Scilab commands and workspace
2. Matrix and vector operations in GNU Octave / Scilab
3. GNU Octave / Scilab script for mathematical computations
4. Program using conditional statements
5. Program using loops
6. Plotting basic mathematical functions
7. Plot sine and cosine waves
8. Multiple plots using subplot
9. Generation of sinusoidal signals
10. Signal operations (addition, scaling)
11. Solving simultaneous equations using GNU Octave / Scilab
12. Plotting exponential and logarithmic functions
13. Frequency response visualization
14. Mini application using GNU Octave / Scilab

Suggested Learning Resources: (Textbook/ Reference Book/ Manuals):

Textbook:

1. J. W. Eaton, D. Bateman, S. Hauberg, and R. Wehbring, *GNU Octave Manual*, 8th ed. Boston, MA, USA: Free Software Foundation, 2024

Reference books / Manuals:

1. H. Moore, MATLAB for Engineers, 5th ed. Upper Saddle River, NJ, USA: Pearson Education, 2018.
2. S. Attaway, MATLAB: A Practical Introduction to Programming and Problem Solving, 5th ed. Oxford, U.K.: Butterworth-Heinemann, 2021.

Web links and Video Lectures (e-Resources):

1. Octave Tutorial / Matlab Introduction to Octave
   https://www.youtube.com/watch?v=q44zkMy3TWg&list=PLHQqy6aejPhjRPiHEPpxyeSwYfLnbI-lE
2. MATLAB Onramp – MathWorks

https://matlabacademy.mathworks.com/details/matlab-onramp/gettingstarted?utm_source=chatgpt.com 3. MATLAB Tutorials – Tutorials Point https://www.tutorialspoint.com/matlab/index.htm?utm_source=chatgpt.com 4. Signal Processing with MATLAB – MathWorks Examples https://in.mathworks.com/help/signal/examples.html?utm_source=chatgpt.com
Teaching-Learning Process (Innovative Delivery Methods): The following are sample strategies that educators may adopt to enhance the effectiveness of the teaching-learning process and facilitate the achievement of course outcomes. 1. Visualization-Based Learning using graphical representation of mathematical and signal-processing concepts. 2. Problem-Based Learning through numerical computing and engineering applications. 3. Collaborative Pair Programming for script development and debugging. 4. Mini Project-Based Learning using GNU Octave/Scilab for real-world applications

Community Project (Project Based Learning) Societal Project

[Common to all disciplines of Engineering]

CourseCode	**1BCP308**	Scheme	2025
TypeofCourse	SDC	Semester	III
TeachingHours/Week(L:T: P)	30(0:0:0)	CIEMarks	50
TotalHoursofPedagogyCI(L:T):LI(P):SL:TW	30(0:0:0:30)	SEEMarks	50
Credits	1	TotalMarks	100
Typeof Examination	Practical	ExamHours	02

Courseobjective:

Rapid urbanisation, population growth, environmental concerns, energy demand, water scarcity, waste management, transportation issues and rural development challenges have created practical problems affecting communities and public welfare. This course aims to integrate technical knowledge, field exposure and societal engagement so that students identify real community issues, frame problem statements and attempt appropriate, feasible and sustainable engineering responses within the scope of a one-semester project.

Courseoutcome(CourseSkillSet):

Attheendofthecourse,thestudentwillbeableto:

1. **CO1(L2–Understand):**Identifyandanalysesocietalproblemsthroughfieldinteractionandtechnical assessment.
2. **CO2(L3–Apply):**Developskillsinprojectplanning,fieldsurvey,datacollection,implementation, documentation and reporting.
3. **CO3(L4–Analyse):**Formulatefeasibleengineeringproblemstatementsandsolutionsconsidering practical constraints and sustainability aspects.
4. **CO4(L3–Apply):**Applyprinciplesofenvironmentalresponsibility,ethicsandsocietalwelfarein engineering practice through community-oriented interventions.
5. **CO5 (L4 – Analyse):**Exhibit multidisciplinary learning and problem-solving ability based on collected data, user feedback and baseline conditions.
6. **CO6(L5–Evaluate):**Demonstrateteamworkandcommunicationskillswhileinteractingwithtechnical and non-technical stakeholders and reflect on project impact on society.

Restrictionsandprofessionalconduct:

Community / Societal Projects shall remain **academic, socially responsible, technically focused, andpoliticallyneutral**.Studentsandfacultyshallmaintainprofessionalism,ethicalconduct,public respect and institutional integrity while interacting with communities, public groups, organisations and stakeholders.

Studentsandfaculty**shallavoid**thefollowingduringprojectexecution:

- Associationwithpoliticalpartyactivities,campaignsorpropaganda.
- Participationinactivitiesthatmaydisturbcommunalharmony,publicorderorinstitutional reputation.
- Useoftheprojectplatformforpersonal,political,ideologicalorcommercialpromotion.
- Disrespectful,discriminatoryorunethicalinteractionwithcommunitymembersor stakeholders.

Projectsmustalsorecogniseconstraintsrelatedto**cost,resources,environmentandsafety,and stakeholderbehaviour/cooperation/acceptance**whenplanningandimplementingactivities.

Sustainable Development Goals

The faculty shall encourage students to undertake community projects that align with and contribute towards satisfying the National Board of Accreditation (NBA) Criterion 3.6, namely, Evidence of Addressing Sustainable Development Goals (SDGs), which is a major emphasis of the United Nations (UN). The Sustainable Development Goals (SDGs) are illustrated in the figure shown below:

SETOFPROJECTACTIVITIES(TW/SL=30HOURS)

Methodsforprojectidentification:

Studentsmayidentifytheprojecttopicusingoneormoreofthefollowingmethods:

- Interactionwithlocalruralorurbanstakeholderssuchaslocalleaders,corporation/municipality personnel, NGOs, panchayat representatives, etc.
- Reviewofissueshighlightedinprintandelectronicmedia,andsocialnetworks(WhatsApp, Facebook,X,Instagram,etc.).
- After selecting a broad topic, students shall collect data, conduct a feasibility survey, estimate timelinesandresources,approximateexpenditure,andthendefinetheproblemstatementand objectives clearly.

ListofProjectTopicsandEngineeringOutcomes:

Thefollowingstructuredsequenceofactivitiesistobecarriedoutduringthesemester:

Sl. No.	Projecttitle	Measurableengineeringoutcome	MappedPOs	SDGs
1	Ruralandurbanwater conservation and managementsystems	Prepare a site-specific water-saving plan, estimate water demand–supply gap, and propose a feasible conservation intervention with quantified savings.	PO1, PO2, PO3, PO4, PO10,PO11	SDG 6, SDG 11, SDG 12
2	Wastemanagement and recycling	Conduct waste audit, classify waste streams, and design a segregation/recycling workflow with measurable reduction in mixed waste.	PO2, PO3, PO4, PO6, PO8,PO10	SDG 11, SDG 12, SDG 13

Sl. No.	Projecttitle	Measurableengineeringoutcome	MappedPOs	SDGs
3	Afforestation	Identify a degraded area, prepare plantation layout, and demonstrate survival-rate tracking and maintenance schedule for saplings.	PO2, PO3, PO4, PO6, PO7,PO11	SDG 11, SDG 13, SDG 15
4	Biogasgenerationand power generation	Estimate organic waste availability, size a small biogas system, and document expected gas output or energy yield.	PO1, PO2, PO3, PO4, PO5,PO10	SDG 7, SDG 11, SDG 12
5	DPRforsolarpower rural plant	PrepareaDPRwithloadassessment,panel sizing,cost estimate, and projected energy generation and payback.	PO1, PO2, PO3, PO4, PO5,PO10	SDG 7, SDG 9, SDG 11
6	DPRforelectrification ofvillage/tribal community	Map unserved/underserved households, propose electrificationlayout, and estimate coverage,losses,andimplementationcost.	PO1, PO2, PO3, PO4, PO10,PO11	SDG 7, SDG 9, SDG 10
7	DPRforruraldrainage system	Survey drainage bottlenecks, develop a drainage layout, and estimate runoff handlingcapacityandflood-riskreduction.	PO1, PO2, PO3, PO4, PO6,PO10	SDG 6, SDG 9, SDG 11
8	Sustainability and environmentalhealth projects	Assess local environmental health issues and propose interventions with measurable improvement in hygiene, safety, or resource use.	PO2,PO3, PO4,PO6, PO7,PO8	SDG 3, SDG 6, SDG 11, SDG 12
9	Plasticfreecampaigns	Measure plastic usage before and after awareness intervention and report percentage reduction or behavioural change.	PO2, PO3, PO6, PO7, PO8,PO10	SDG 11, SDG 12, SDG 13
10	Healthandnutrition awareness	Conduct baseline and post-program awareness survey and document improvementinawarenessscoreor adoptionofhealthierpractices.	PO2, PO6, PO7, PO8, PO9,PO10	SDG 2, SDG 3, SDG 11
11	Societalprojects involvinghealth wellness	Identify a community health need and develop an awareness/service module with measurable participation and feedback outcomes.	PO2, PO3, PO6, PO8, PO9,PO10	SDG 3, SDG 11, SDG 17
12	Airqualitymonitoring system	Collect air-quality data, compare with reference limits, and present trends along with possible mitigation suggestions.	PO2, PO3, PO4, PO5, PO6,PO10	SDG 3, SDG 11, SDG 13
13	Plasticwastereduction campaign	Track collection, segregation, and replacement actions, and quantify reduction in plastic waste generation or littering.	PO2, PO3, PO6, PO7, PO8,PO10	SDG 11, SDG 12, SDG 13
14	Urbangreening projects	Prepare greening plan, identify planting locations, and assess environmental benefits such as shade, aesthetics, or heat mitigation.	PO2, PO3, PO4, PO6, PO7,PO11	SDG 11, SDG 13, SDG 15

Sl. No.	Projecttitle	Measurableengineeringoutcome	MappedPOs	SDGs
15	Smartagriculture solution	Design a low-cost monitoring or irrigation support solution and estimate improvement in water use efficiency or cropsupport.	PO1, PO2, PO3, PO4, PO5,PO10	SDG 2, SDG 6, SDG9
16	Smartirrigation system	Estimatecropwaterrequirement,propose control logic, and quantify water savings compared with conventional irrigation.	PO1, PO2, PO3, PO4, PO5,PO10	SDG 2, SDG 6, SDG 12
17	Youthmentoring programmes	Deliver a structured mentoring activity andmeasureparticipation,engagement, and skill/awareness improvement.	PO6, PO8, PO9,PO10, PO11	SDG 4, SDG 10, SDG 17
18	Adulteducation	Conduct learner-needs assessment, prepare instructional content, and measure improvement in basic literacy or numeracy indicators.	PO6, PO8, PO9,PO10, PO11	SDG 4, SDG 10, SDG 17
19	Foodsecurity initiatives/cold storage system	Estimate storage need, design a simple cold-chain concept, and document reduction in spoilage or wastage.	PO1, PO2, PO3, PO4, PO5,PO10	SDG 2, SDG 9, SDG 12
20	Human rights awarenesswithlegal systems	Prepare and deliver an awareness module andassessincreaseinlegalawarenessand access-to-rights understanding.	PO6,PO7, PO8,PO9, PO10	SDG 5, SDG 10, SDG 16
21	House tax collection throughdigitalmedia	Develop a simple digital workflow or awareness support and measure improvement in compliance, convenience, or response time.	PO2, PO3, PO4, PO5, PO10,PO11	SDG 9, SDG 11, SDG 16
22	Use of application / applicationprogram	Build or demonstrate a useful community app and measure usability, adoption, or efficiency improvement.	PO1, PO3, PO4, PO5, PO9,PO10	SDG 9, SDG 11, SDG 17
23	CreationofPanchayat library	Plan the library model, catalogue resources, and measure usage, accessibility, or participation outcomes.	PO6, PO8, PO9,PO10, PO11	SDG 4, SDG 10, SDG 11, SDG 17

SuggestedLearningResources:

Textbooks:

1. **Phadke,N.D.**CommunityEngagementandSocialInnovation.1sted.,OxfordUniversityPress,New Delhi.
2. **Garg,N.R.**Project-BasedLearninginEngineeringEducation.1sted.,PearsonIndiaEducation Services, Noida.
3. **Gupta,A.andP.Singh.**ServiceLearningandCommunityProjects.1sted.,McGraw-HillEducation (India), New Delhi.
4. **Wilson,G.**PracticalGuidetoCommunityDevelopmentProjects.2nded.,Routledge,London.

Referencebooks:

1. NPTELcoursesonProject-BasedLearningandSocialInnovation.
2. SWAYAMcoursesoncommunityengagementandsustainability.
3. UNSustainableDevelopmentGoalsportal:https://sdgs.un.org
4. MyGovIndiaandlocalcivicbodyportalsforcommunityinitiatives.
5. YouTuberesourcesondesignthinking,socialinnovation,andcommunityservicelearning.
6. NGO and government field-action case studies related to sanitation, water, health, education, and environment.

Weblinks andVideo Lectures(e-Resources):

1. NPTELcoursesonEngineering Geology(IITRoorkee,IITKharagpur).
2. NPTEL coursesonSoilMechanicsand Foundation Engineering(IITDelhi, IITBombay).
3. Virtual Labs– GeotechnicalEngineeringVirtual Lab(IITKanpur):https://vlab.co.in
4. GeologicalSurvey ofIndia(GSI)–Maps,reports, andpublications: https://www.gsi.gov.in
5. YouTubechannels:CivilEngineeringEssentials,TheEngineeringClassroom(soilmechanics experiments).
6. AmericanSocietyofCivilEngineers(ASCE)–Geotechnicalresourcesandstandards

TeachingLearningProcess:

ThesuggestedTLPforCommunity/SocietalProjectisasfollows;

Week/ Phase	Teaching–Learning Activity	FacultyRole	StudentActivity	Output/Evidence
1	Course introduction, objectives,ethics, conduct,and assessmentbriefing	Explaincoursescope, rules, rubrics, and expecteddeliverables	Understandcourse requirementsandform teams	Teamlist,course plan
2	Communityproblem identificationand topicselection	Guidetopicframing andfeasibility	Identify local issues throughdiscussionand observation	Shortlistedproject topic
3	Stakeholder interactionand preliminarysurvey	Demonstratesurvey methodsand stakeholder engagement	Collectinitialdatafrom community/users	Survey notes, interviewrecord
4	Problemstatement andobjective	Review and refine problemstatement	Prepareproblem statement,scope,and	Approvedproblem statement
	formulation		objectives	
5	Literature/casestudy review and baseline analysis	Suggestrelevant referencesand examples	Studyexistingsolutions andcompare approaches	Baselineanalysis summary

Week/Phase	Teaching–Learning Activity	FacultyRole	StudentActivity	Output/Evidence
6	Projectplanningand roleassignment	Helpteamsorganize tasks, timeline, and responsibilities	Planactivities,divide roles, and prepare schedule	Workplan/Gantt chart
7	Feasibilityanalysis andsolution brainstorming	Checktechnical feasibilityand practicality	Generatepossible engineeringsolutions	Solutionalternatives sheet
8	Selection of final solutionanddesign approach	Reviewfinalconcept and design logic	Finalizeconcept, methods,andexpected outcome	Conceptnote/ designoutline
9	Data processing / calculations/sizing/ mapping	Support computationsand technicalreview	Analyzedata,perform calculations,prepare maps/charts	Technicalanalysis sheet
10	Prototype/model/ audit / DPR / app development	Monitorprogress andcorrecttechnical issues	Developtheselected output	Workingmodel/ draftDPR/map/ app
11	Testing,refinement, andimplementation planning	Evaluatetechnical correctnessand improvements	Test prototype or validateproposalwith users	Test results / revisedoutput
12	Fieldimplementation /demonstration/ awarenessactivity	Facilitatecommunity interactionand documentation	Conduct implementationor demonstration	Photos,attendance, implementation record
13	Documentationof outcomes,feedback, andimpact	Reviewreport structureand completeness	Compilefindings, stakeholderfeedback, andobservations	Draftreport
14	Presentation preparationandviva practice	Conductmock presentationand feedback	Prepareslides/poster andrehearse	Presentationdeck
15	Finalpresentation, submission,and reflection	Evaluate performanceusing rubrics	Presentproject,submit report, reflect on learning	Finalreport, presentation,viva

Assessmentstructure:

A.ContinuousInternalEvaluation(CIE)–50marks

- Students,inbatchesof3–4,shallundertakeatleast oneproject(oracombinationoftworelated activities) aiming, as far as possible, at a logical implemented or implementable outcome.
- CIEwillbeconductedbyadepartmentalcommittee(HoD/nominee,guideandoneseniorfaculty)using the following rubrics totalling 50 marks:

CIEpassrequirement:

- Astudentshallsecureaminimumof20marksoutof50inCIEtobecomeeligibletoappearforSEE.

- StudentswhofailtoearntherequiredCIEmarksmaybegivenadditionalopportunities beforeclosure of the semester; no re-doing of CIE is permitted after the end of the semester.

B.SemesterEndExamination(SEE)–100marks(scaledto 50)

- Examinationduration:2hours.
- Maximumexaminationmarks: 100(enteredas100intheVTUportal;theITI-SMUmodule automatically scales 100 → 50 for result processing).
- TheSEEshallbeconductedbatch-wisebyacommitteeofthreefaculty:projectguide,onefacultyfrom the same department and one from a different department.

SEEpassrequirementandoverallpassingrule:

- ForapassinSEE,astudentshallsecureminimum35marksoutof100.
- Fordeclarationofapassgrade,the sumofCIEmarks(outof50)andscaledSEEmarks(outof50) shall be ≥ 40; otherwise, the student is awarded grade F (Fail).

CIERubric—ContinuousInternalEvaluation(Total50marks):

Criterion	Weight (marks)	Excellent (Full marks)	Good	Fair	Needs Improvement
Problem identification& Relevance to society/industry /community	8	Problemis clearly identified with strongevidence ofsocietal relevance and well-defined scope.	Problem is relevant and scopeisclear withadequate supporting evidence.	Problem definedbut justification orevidence is weak.	Problemunclear ornotrelevant; little/no supporting evidence.
Formationof problemstatement; Engineering approach,innovation & feasibility	10	Problem statementis precise; approachis sound, innovativeand clearly feasible.	Problem statement adequate; approach feasible with minorgaps.	Problem statement partial; approach feasibilityis marginal.	Problem statement missing or approachnot feasible.
Interactionwith stakeholders; Data collection,analysis&interpretation	8	Thorough stakeholder engagement; datacollection is comprehensive; analysisis well-interpreted.	Good engagement; data and analysis adequatewith minorgaps.	Limited engagement; data incomplete andanalysis superficial.	Little/no stakeholder contact; insufficientor no data/ analysis.
Project documentation; Clarity,organization & problem-solving demonstrated	10	Documentation iscomplete, well-organized, analytical, and shows strong problem-solving.	Documentationcompleteand clear withsomeanalytical content.	Documentationbasicwith omissions; problem-solvinglimited.	Documentation missing/poorly organized; no clear problem-solving.
Communication& Presentation skills	6	Presentationis confident, structured,and answersqueries fully; visuals effective.	Presentation clear and satisfactory; responds to most queries.	Presentation acceptable butlacks clarityor confidence; weakresponses.	Presentation poororabsent; unableto respond.
Contribution & Benefitto society (impact, sustainability)	8	Clear, demonstrable societalbenefit and sustainability; realisticpathto implementation.	Benefit plausible; sustainability considered withminor gaps.	Limited or unclear societal benefit; sustainabilitynot well addressed.	Noevident benefit or sustainability; projectnot community-oriented.

NotesforCIErubric:

- MinimumCIEpassrequirement:20/50tobeeligibleforSEE.[Usedepartmentalcommittee (HoD/guide + senior faculty) to apply the rubric and record marks.]

SEERubric—SemesterEndExamination(Entermarksoutof100;scaledto50later):

Criterion	**Weight (marks)**	**Excellent(Fullmarks)**	**Good**	**Fair**	**Needs Improvement**
Problem identification& Relevance to society/industry/ community	16	Problem and relevance are articulated clearly with strong evidence and context.	Problem relevanceclear with reasonable evidence.	Problem statedbut evidence/ contextweak.	Problem poorly defined or irrelevant.
Formationof problem statement; Engineering approach, innovation&feasibility	20	Problemstatementis precise; approach demonstrates engineeringdepth, novelty and feasibility.	Approach is technically soundand feasiblewith minor limitations.	Approach basic;limited technical depthor feasibility concerns.	No viable engineering approachor infeasible plan.
Interactionwith stakeholders;Data collection, analysis & interpretation	16	Excellent stakeholder engagement; rigorous data collection and insightful analysis.	Good engagement andacceptable analysis.	Superficial datacollectionand limited analysis.	Inadequateor nodata; pooranalysis.
Project documentation; Clarity,technical rigor& problem-solving demonstrated	20	Reportiscomprehensive, technicallyrigorous, anddemonstrates systematic problem-solving.	Reportis completeand technically correctwith minorgaps.	Reportlacks technical depthorhas notable omissions.	Report missingkey elementsor technically incorrect.
Communication, Presentation &Viva-voce responses	12	Candidate presents expertly, defends work persuasively and answers all queries correctly.	Good presentation andsatisfactory answersto most queries.	Presentation adequatebut failsto answersome technical questions.	Poor presentation andunableto defendwork.
Contribution & Benefittosociety; Impact assessment&sustainability	16	Clear, evidence-based assessment of social impactand Sustainabilitywith scaling recommendations.	Reasonable impact discussionand sustainability considerations.	Limited evaluationof impactor sustainability.	Nocoherent assessmentofimpactor sustainability.

SEEpassrule:

- Studentmustsecureatleast35/100inSEEitselftobeeligibleforpassconsideration.
- FinalpassingisbasedonCIE(outof50)+SEE(scaledto50)>=40.Otherwise,gradeF(Fail)isawarded.

Suggestedimplementationnotes(forBoS/examcommittees):

- Usenumericalscoresfromtherubricandkeepbriefevaluatorcommentsforeachcriterion.
- Forteamprojects:recordindividualcontributionwithinthedocumentationandadjustindividual marks using a peer-evaluation sheet or guide's assessment.
- Maintainevidence(fieldnotes,photos,questionnaires,DPRs,reports)asannexuresforSEE moderation.
- Usestandardizedscoresheet(spreadsheet)mappingrubricitemstocolumnsforeasyaggregationand archival.

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Assessment Structure for PCC Courses

Assessment Structure:
The assessment in each PCC course is divided equally between Continuous Internal Evaluation (CIE) and the Semester End Examination (SEE), with each carrying 50% weightage.

- To qualify and become eligible to appear for SEE, in the **CIE**, a student must score at least **40% of 50 marks**, i.e., **20 marks**.
- To pass the **SEE**, a student must score at least **35% of 50 marks**, i.e., **18 marks**.
- Notwithstanding the above, a student is considered to have **passed the course,** provided the combined total of **CIE and SEE** is at least **40 out of 100 marks**.

Continuous Comprehensive Assessments (CCA)+ Internal Assessment Test (IA) = Continuous Internal Evaluation CIE [25+25=50 marks].
A minimum of two Internal Assessment Tests(IA) shall be conducted, carrying a total of 25 marks.
In addition, Continuous Comprehensive Assessment (CCA) shall be conducted for a total of 25 marks.
It is recommended to include a maximum of two learning activities as part of the CCA to foster the holistic development of students. The suggested activities shall be

Sl. No.	Name of the Learning activity	Maximum Marks
1	Group seminar	15
2	Assignment (at RBL3, RBL4, or RBL5 levels)	10

Rubrics for assessment of these learning activities are provide in the Rubrics Section.

Suggested Learning Activities may include (but are not limited to):

- Course Project
- Case Study Presentation
- Programming Assignment
- Tool/Software Exploration
- Literature Review
- Open Book Test (preferably at RBL4 and RBL5 levels)
- GATE-based Aptitude Test
- Assignment (at RBL3, RBL4, or RBL5 levels)
- Any other relevant and innovative academic activity
- Use of MOOCs and Online Platforms

Suggested Innovative Delivery Methods may include (but are not limited to):

- Flipped Classroom
- Problem-Based Learning (PBL)
- Case-Based Teaching
- Simulation and Virtual Labs
- Partial Delivery of course by Industry expert/ industrial visits
- ICT-Enabled Teaching
- Role Playing

Term Work (TW) and Self Learning (SL) components in Number of Hours per semester		
Term work (includes assignments, seminars, micro projects, industrial visits, any other student activities etc.)		
Sl. No.	**Term Work (TW) Activity**	**Number of Hours / Semester**
1	Group seminar	24
2	Assignment	24
OR SL: Self Learning, MOOCs, spoken tutorials, online educational resources etc.		
Sl. No.	**Self-Learning (SL) Activity**	**Number of Hours / Semester**
1	NPTEL/MooCs course on Analog Electronics and Linear Integrated Circuits (faculty have to verify the dates that the NPTEL course is being offered)	48

Continuous Internal Evaluation (CIE)

(i) The CIE marks shall be decided based on internal tests and other outcome-based activities. The continuous internal evaluation shall be carried out by the teacher handling the course.
(ii) Out of 50 marks earmarked for CIE, 25 marks shall be assigned for internal tests. The first test shall be conducted after completing two modules of the syllabus and the second one after completing the remaining three modules.
(iii) The remaining 25 marks shall be assigned for Continuous Course Assessment (CCA), conducted as per the rubrics listed in the assessment section of the respective syllabus.
(iv) A student shall obtain a minimum of 40% marks or 20 out of 50 marks allotted to CIE to become eligible to appear for the SEE.

Passing requirement in SEE

For a pass in the Semester End Examination (SEE), a student shall secure a minimum of 35 marks out of 100.
For the declaration of a pass grade, the sum of the Continuous Internal Evaluation (CIE) marks (out of 50) marks and the SEE marks scaled down to 50 shall be greater than or equal to 40 marks.
If the total (CIE + SEE) is less than 40 marks, the student shall be awarded the grade ‘F’ (Fail).

Assessment Structure for IPCC Courses

Assessment Structure:

The assessment for each course is equally divided between Continuous Internal Evaluation (CIE) and the Semester End Examination (SEE), with each component carrying **50% weightage** (i.e., 50 marks each).
The CIE Theory component will be **25 marks** and CIE Practical component will be **25 marks**.

Questions from the practical component of the IPCC subject shall not appear in the theory SEE component.

CIE Theory component: It consists of IA tests for 25 marks. The CIE Practical component for continuous assessments will be for 15 marks through rubrics and for lab tests will be for 10 marks.

- To qualify and become eligible to appear for SEE, in the **CIE theory component**, a student must score at least **40% of 25 marks**, i.e., **10 marks**.
- To qualify and become eligible to appear for SEE, in the **CIE Practical component**, a student must secure **a minimum of 40% of 25 marks**, i.e., **10 marks**.
- To pass the **SEE**, a student must secure **a minimum of 35% of 50 marks**, i.e., **18 marks**.
- A student is deemed to have **successfully completed the course** if the **combined total of CIE and SEE is at least 40 out of 100 marks**.

CIE Practical Component:
The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report using a defined set of rubrics. Each experiment report can be evaluated for 30 marks. The summation of all the experiments marks to be scaled down to 15 marks.

The laboratory test (duration 03 hours) at the end of the last week of the semester /after completion of all the experiments (whichever is early) shall be conducted for 50 marks and scaled down to 10 marks. For laboratory test, the student is required to conduct one experiment each from both Part A and Part B.

Continuous Internal Evaluation (CIE)

(i)Theory component

The CIE marks of 25 shall be earmarked for two tests.
The first test shall be conducted after completing two modules of the syllabus and the second one after completing the rest three modules.
Each test shall be conducted for 25 marks. The average of the two tests scaled down to 25 marks shall constitute the test marks for a maximum of 25 marks.

(ii) Laboratory component

Out of 25 marks, 15 marks shall be assigned for assessment as per the rubrics listed. The remaining 10 marks shall be based on the practical test conducted by two Internal examiners appointed by the HoD. The allotment of marks shall be as per the rubrics defined.

(i) To qualify and become eligible to appear for the SEE of the IC/IPCC, a student shall secure at least 40 % of 25 marks, i.e., 10 marks, in the CIE theory component, and at least 40 % of 25 marks, i.e., 10 marks in the CIE Practical component.

Table – IPCCs Distribution of marks		
Component	**Description**	**Marks**
Allotment of marks for regular class work		
Ability in Conducting Experiments	Initiative, skill, safety practices, teamwork, and independent handling of equipment during regular lab sessions.	5 marks
Laboratory Record / Journal	Regular and neat maintenance of lab record, accuracy of results, and timely submission.	10 marks
	Subtotal	**15**
Allotment of marks for CIE practical test		
Laboratory Test / Experiment Performance	Ability to set up apparatus, follow procedure, take observations, and obtain correct results in the test experiment.	5 marks
Viva-Voce	Understanding of theory, concepts, and experimental procedure; ability to explain results and answer related questions.	5 marks
	Subtotal	**10**
	Total	**25**

Passing Requirements for SEE

For a pass in the Semester End Examination (SEE), a student shall secure a minimum of 35 marks out of 100. For the declaration of a pass grade, the sum of the Continuous Internal Evaluation (CIE) marks (out of 50) marks and the SEE marks scaled down to 50 shall be greater than or equal to 40 marks.
If the total (CIE + SEE) is less than 40 marks, the student shall be awarded the grade 'F' (Fail).

Assessment Structure for PCC-Lab and AEC Lab Courses

Assessment Structure:
The assessment for each course is equally divided between Continuous Internal Evaluation (CIE) and the Semester End Examination (SEE), with each component carrying **50% weightage** (i.e., 50 marks each).

The CIE marks awarded shall be based on the continuous evaluation of the laboratory report using a defined set of rubrics. Each experiment report can be evaluated for 30 marks. Total marks for the all report shall be scaled down to 30 marks. The laboratory test (duration 03 hours) at the end of the last week of the semester /after completion of all the experiments (whichever is early) shall be conducted for 50 marks and Marks scored shall be scaled down to 20 marks. Final average of marks for report and test shall be out of 50 marks.
For both CIE and SEE, the student is required to conduct one experiment each from both Part A and Part B.

- To qualify and become eligible to appear for SEE, in the **CIE component**, a student must secure **a minimum of 40% of 50 marks**, i.e., **20 marks**.
- To pass the **SEE component**, a student must secure **a minimum of 35% of 50 marks**, i.e., **18 marks**.
- A student is deemed to have **successfully completed the course** if the **combined total of CIE and SEE is at least 40 out of 100 marks**

Term Work (TW) and Self Learning (SL) components in Number of Hours per semester (2) Faculty are suggested to offer only TW and not SL.	
Suggested Term Work (TW) Activity	**Number of Hours / Semester**
New Experiment to practice on their own	2
OR	
Practice some of the regular experiments with different design requirements on their own	2

Suggested Rubrics for PCC Courses

Note: the rubrics provided below are a reference and can be modified as required.

Rubrics for Learning Activity1: Group seminar (at RBL3, RBL4, or RBL5 levels)

	Superior (5)	**Good (4)**	**Fair (3)**	**Needs Improvement (2)**	**Unacceptable (1)**
Subject Knowledge (CO/PO Mapping)	Demonstrates deep knowledge of the subject with clear explanation.	Demonstrates adequate knowledge of most topics with clear explanation.	Demonstrates only basic concepts with Superficial knowledge of topic.	Does not have clear understanding of the topic and lacks grasp of information.	No explanation.
Communication Skills (CO/PO Mapping)	Clearly audible by the entire audience.	Audible by most of the audience.	Audience has difficulty to hear and follow the presentation.	Minimal command on vocabulary with inaccurate pronunciation.	Communication characterized by minimal degree of grammatical accuracy with frequent errors.
Viva Voce (CO/PO Mapping)	Able to understand and answer all the questions confidently with relevant explanation.	Able to understand and answer some of the questions with relevant explanation.	Able to answer and explain few questions with less relevance.	Unable to answer most of the questions.	No proper answer.

Rubrics for Learning Activity2: Assignment (at RBL3, RBL4, or RBL5 levels)

	Superior (5)	**Good (4)**	**Fair (3)**	**Needs Improvement (2)**	**Unacceptable (1)**
Problem understanding (CO/PO Mapping)	Demonstrates complete understanding of the question and assumptions.	Demonstrates good understanding with only minor omissions.	Demonstrates partial understanding with only some unclear assumptions.	Shows limited understanding of the questions.	Weak understanding of the question.
Correct application of	Applies all relevant	Applies most of the	Applies a few relevant	Frequent incorrect	Major errors in application of

theory and correctness of solution (CO/PO Mapping)	engineering principles, laws, and analytical methods correctly.	relevant engineering principles, laws, and analytical methods correctly.	engineering principles, laws, and analytical methods correctly	application of engineering principles and analytical methods.	engineering principles and analytical methods.

Suggested Rubrics for IPCC courses

Rubrics for CIE Lab test (50marks – later scaled down to 10marks):

Performance Indicators	**Excellent**	**Very Good**	**Good**	**Satisfactory**
Fundamental Knowledge (10) (PO1)	The student has in depth knowledge of the topics related to the course (9-10)	Student has good knowledge of some of the topics related to course (7-9)	Student is capable of narrating the answer but not capable to show in depth knowledge (6-7)	Student has not understood the concepts clearly (5-6)
Design Of Experiment (15) (PO2, PO3, PO5)	Student is capable of discussing more than one design for his/her problem statement and capable of proving the best suitable design with proper reason (14-15)	Student is capable of discussing few designs for his/her problem statement but not capable of selecting best (12-14)	Student is capable of discussing single design with its merits and de-merits (10-12)	Student is capable of explaining the design (9-10)
Implementation with appropriate HW/SW (15) (PO3 , PO4, PO5, PO8)	Student is capable of implementing the design with best suitable algorithm/HW considering optimal solution explanation. (14-15)	Student is capable of implementing the design with best suitable algorithm/HW and should be capable of explaining it (12-14)	Student is capable of implementing the algorithm/HW with some explanation. (10-12)	Student is just capable of implementing the algorithm/HW , and unsatisfactory explanation. (8-10)
Result &Analysis (10) (PO4, PO5, PO9)	Student is able to run the program on various cases and compare the result with proper analysis. (10)	Student will be able to run the program for most of the cases and provide proper analysis. (7-9)	Student will be able to run the code for few cases and provide analysis for a few cases. (5-7)	Student will be able to run the program for a simple case but not able to analyze the output. (3-5)

Rubrics for CIE – Continuous assessment (30marks – later scaled to 15 marks):

	Superior	**Good**	**Needs Significant Improvement**
Fundamental Knowledge about each experiment (6) (PO1)	The student has in depth knowledge of the topics (4-6)	Student has good knowledge of some of the topics (4)	Student has not understood the concepts clearly (2)
Design Of Experiment (8) (PO2, PO3, PO5)	Student capable of discussing more than one design for problem statement and capable of proving the best suitable design with proper reason (6-8)	Student capable of discussing few designs for problem statement , not capable of selecting best design (6)	Student struggles to explain the design (2-4)
Implementation (10) (PO3, PO4, PO5, PO8)	Student capable of implementing the design (either alone or in a team) with best suitable algorithm considering optimal solution. (8-10)	Student capable of implementing design (either alone or in a team) with best suitable algorithm and capable of explaining it (8)	Student struggle to implement the design (either alone or in a team) . (2-8)
Quality of Record and Observation write up (6) (PO8,PO5,PO9)	Lab record & observation book are well-organized, with clear sections (4-6)	Lab record/ observation book are organized,, but some sections are not well-defined. (4)	The lab record/ observation book poorly organized, with missing or unclear sections. (2-4)

Note: Term Work and Self Learning components are not included in the assessment. IPCC already has theory and lab assessment in CIE, including a TW/SL component may cause burden on students. Faculty may give 50 hours of SL, however this may not be included for assessment.

Suggested Rubrics for PCC-Lab and AEC Lab Courses

Rubrics for CIE – Continuous Lab assessment (30 marks):

	Superior	**Good**	**Fair**	**Needs Improvement**	**Unacceptable**
Fundamental Knowledge about each experiment (4) (PO1)	The student has in depth knowledge of the topics (4)	Student has good knowledge of some of the topics (3)	Student is capable of narrating the answer but not capable to show in depth knowledge (2)	Student has not understood the concepts clearly (1-2)	Student barely has fundamental knowledge (1)
Design Of Experiment (5) (PO2, PO3, PO5)	Student is capable of discussing more than one design for his/her problem statement and capable of proving the best suitable design with proper reason (5)	Student is capable of discussing few designs for his/her problem statement but not capable of selecting best (4-5)	Student is capable of discussing single design with its merits and de-merits (3-4)	Student struggles to explain the design (2-3)	Student has very weak understanding of the design (1-2)
Implementation (8) (PO3, PO4, PO5, PO8)	Student is capable of implementing the design with best suitable algorithm considering optimal solution. (7-8)	Student is capable of implementing the design with best suitable algorithm and should be capable of explaining it (5-6)	Student is capable of implementing the design with proper explanation. (3-4)	Student is capable of implementing the design. (1-2)	Implementation has major errors (1)
Result &Analysis (5) (PO4, PO5, PO9)	Student is able to execute the program/experiment on various cases and compare the result with proper analysis. (4-5)	Student will be able to execute the program/experiment for all the cases. (3-4)	Student will be able to execute the program/experiment for few cases and analyze the output. (2-3)	Student will be able to execute the program/experiment but not able to analyze the output. (1-2)	Program/Experiment execution has important errors and student is incapable to explaining any of them (1)
Quality of Record and	The lab record & observation book	The lab record &	The lab record & observation	The lab record &	Student has not submitted lab

Observation write up (8) (PO8,PO9)	are well-organized, with clear sections (e.g., Introduction, Method, Results, Conclusion). l (7-8)	observation book are organized, with clear sections, but some sections are not well-defined. (5-6)	book lack clear organization or structure. Some sections are unclear or incomplete. (3-4)	observation book are poorly organized, with missing or unclear sections. (1-2)	record or observation book (0)

Rubrics for CIE Lab Test (50 marks, later scaled to 20 marks) and SEE:

Performance Indicators	Excellent	Very Good	Good	Satisfactory
Fundamental Knowledge (5) (PO1)	The student has in depth knowledge of the topics related to the course (4)	Student has good knowledge of some of the topics related to course (3)	Student is capable of narrating the answer but not capable to show in depth knowledge (2)	Student has not understood the concepts clearly (1)
Design Of Experiment (5) (PO2, PO3, PO5)	Student is capable of discussing more than one design for his/her problem statement and capable of proving the best suitable design with proper reason (5)	Student is capable of discussing few designs for his/her problem statement but not capable of selecting best (4)	Student is capable of discussing single design with its merits and de-merits (3)	Student is capable of explaining the design (1-2)
Implementation with appropriate HW/SW (5) (PO3 , PO4, PO5, PO8)	Student is capable of implementing the design with best suitable algorithm/HW considering optimal solution explanation. (7-8)	Student is capable of implementing the design with best suitable algorithm/HW and should be capable of explaining it (5-6)	Student is capable of implementing the algorithm/HW with some explanation. (3-4)	Student is just capable of implementing the algorithm/HW, and unsatisfactory explanation. (1-2)
Result &Analysis (5) (PO4, PO5, PO9)	Student is able to run the program on various cases and compare the result with proper analysis. (5)	Student will be able to run the program for most of the cases and provide proper analysis. (4)	Student will be able to run the code for few cases and provide analysis for a few cases. (3)	Student will be able to run the program for a simple case but not able to analyze the output. (1-2)

This file contains the proposed syllabus for VLSI, 4th semester. The assessment and rubrics for Mathematics, Biology For Electrical And Electronics Engineers and Environmental Science Project courses are provided along with the individual syllabus. The assessment and rubrics for all other subjects (PCC, IPCC, PCC-L and AEC) are provided at the end of this file. The rubrics provided are suggested by the BoS, however individual departments may modify them as required.

Mathematics for Machine Learning			
Course Code	**1BMATEC401**	Scheme	2025
Type of Course	Applied Science Course (ASC)	Semester	IV
Teaching Hours/Week (L:T:P)	42(3:0:0)	CIE Marks	50
Total Hours of Pedagogy per semester L /T/P/SL&TW:	90(42:0:0:48)	SEE Marks	50
Credits	**3**	Total Marks	100
Examination type (SEE)	Theory	Exam Hours	3

Course outcome (Course Skill Set)

At the end of the course, the student will be able to:

CO1: Apply the concepts of vector spaces, linear transformations, basis, dimension, rank, and nullity to solve problems arising in machine learning and data analysis.

CO2: Analyze inner product spaces, orthogonality, orthonormal bases, Gram-Schmidt orthogonalization, and QR decomposition for efficient representation of data.

CO3: Evaluate eigenvalues, eigenvectors, matrix decompositions, positive definite matrices, singular value decomposition, and matrix differentiation techniques used in machine learning algorithms.

CO4: Apply probability distributions, expectation, variance, covariance, and correlation concepts to model uncertainty and analyze data-driven systems.

CO5: Utilize sampling theory, hypothesis testing, confidence intervals, stochastic processes, and Markov chains for statistical inference and predictive modeling applications.

Module-1: Vector spaces

Vector spaces: Definition and examples, subspace, linear span, Linearly independent and dependent sets, Basis and dimension.
Linear transformations: Definition and examples, Matrix of alinear transformation. Change of bases, Rank and nullity of a linear operator, RankNullity theorem.

Number of Hours:8

Module-2: Inner Product Spaces

Inner Product Spaces: Inner product, orthogonal sets, angles and orthogonality, orthonormal Basis, orthogonal projections; Gram-Schmidt orthonormalization process; QR-decomposition.

Number of Hours:8

Module-3: Eigen values and Eigenvectors

Eigen values and Eigenvectors -Diagonalization, Positive definite Matrices and test for positive definiteness, Singular Value Decomposition (2×2).
Matrix derivatives: Jacobian matrix, Hessian matrix, Gradient of vector and matrix with respect to vector and matrix, pseudo inverse.

Number of Hours:8

Module-4:

Review of basic probability theory, Random variables-discrete and continuous Probability distribution function, cumulative distribution function.
Mathematical Expectation: mean and variance.
Binomial, Poisson, Exponential and Normal distribution– Problems.
Joint probability distribution: Joint Probability distribution for two discrete random variables, expectation, covariance and correlation.

Number of Hours:9

Module-5:

Sampling Theory: Sampling, Sampling distributions, standard error, test of hypothesis for means and proportions, confidence limits for means, student's t-distribution, Chi-square distribution as a test of goodness of fit.
Stochastic process: Stochastic processes, probability vector, stochastic matrices, fixed probability vector,regular stochastic matrices, Markov chains, higher transition probability-problems.

Number of Hours:9

Suggested Learning Resources: (Text Book/ Reference Book/ Manuals):

Text books:

1. **Marc Peter Deisenroth, A. Aldo Faisal, and Cheng Soon Ong**. "Mathematics for MachineLearning" , Published by Cambridge University Press, Copyright 2020
2. **Gilbert Strang**, "Linear Algebra and its Applications", 3rd edition, Thomson Learning Asia,2003.
3. **B.S. Grewal**, *Higher Engineering Mathematics*, 45th Edition, Khanna Publishers.
4. **Erwin Kreyszig**, *Advanced Engineering Mathematics*, 10th Edition, Wiley India.
5. **H.K. Dass and Er. Rajnish Verma**, *Higher Engineering Mathematics*, S. Chand Publications.

<u>Reference books / Manuals:</u>

1. **Christopher M. Bishop**, *Pattern Recognition and Machine Learning*, Springer, 2006.
2. **Trevor Hastie, Robert Tibshirani and Jerome Friedman**, *The Elements of Statistical Learning*, 2nd Edition, Springer, 2009.
3. **Sheldon Ross**, *A First Course in Probability*, 10th Edition, Pearson Education, 2019.
4. Kenneth Hoffman and Ray Kunze, *Linear Algebra*, 2nd Edition, Pearson.
5. **David C. Lay**, Steven R. Lay and Judi J. McDonald, *Linear Algebra and Its Applications*, 5th Edition, Pearson.

Web links and Video Lectures (e-Resources):

- https://nptel.ac.in/courses/111107137

- NPTEL Courses on Engineering Mathematics
- MIT Open Course Ware Mathematics
- SWAYAM Online Courses

Teaching-Learning Process (Innovative Delivery Methods):

The following are sample strategies that educators may adopt to enhance the effectiveness of the teaching-learning process and facilitate the achievement of course outcomes.

1. **Flipped Classroom Approach**
   - Students review video lectures and reading materials before class.
   - Classroom sessions focus on problem-solving, discussions, and applications of transform techniques and optimization models.
2. **Problem-Based Learning (PBL)**
   - Real-world engineering problems involving Fourier Transforms, Z-Transforms, and Linear Programming are assigned for collaborative solution development.
3. **ICT-Enabled Teaching**
   - Use of MATLAB, Python, and online simulation tools to visualize transforms, optimization problems, and signal-processing applications.
4. **Collaborative Learning**
   Group assignments and mini-projects on optimization models and transform applications.

Assessment Structure:
The assessment in each course is divided equally between Continuous Internal Evaluation (CIE) and the Semester End Examination (SEE), with each carrying 50% weightage.

- To qualify and become eligible to appear for SEE, in the **CIE**, a student must score at least **40% of 50 marks**, i.e., **20 marks**.
- To pass the **SEE**, a student must score at least **35% of 50 marks**, i.e., **18 marks**.
- Notwithstanding the above, a student is considered to have **passed the course,** provided the combined total of **CIE and SEE** is at least **40 out of 100 marks**.

Continuous Comprehensive Assessments (CCA)+ Internal Assessment Test (IA) = Continuous Internal EvaluationCIE [25+25=50 marks]

A minimum of **two Internal Assessment Tests(IA)**shall be conducted, carrying a total of **25 marks**.

In addition, **Continuous Comprehensive Assessment (CCA)** shall be conducted for a total of **25 marks**.

It is recommended to include **a maximum of two learning activities** as part of the CCA to foster the **holistic development of students**. These activities shall be:

Sl. No.	Name of the Learning activity	Maximum Marks
1.	Assignment at RBL3 and RBL4levels based on Team Work(TW) activities.	10
2.	GATE-based Aptitude Test.	15

Rubrics **for Learning Activity–1: Assignment (10 Marks)**

Performance Indicator	**Superior (15)**	**Good (12)**	**Fair (10)**	**Needs Improvement (8)**
Quantitative Aptitude	≥90% correct responses	75–89% correct	60–74% correct	<60% correct
Analytical Thinking	Excellent logical reasoning and interpretation	Good reasoning ability	Moderate reasoning	Weak reasoning
Time Management	Completes all questions within allotted time	Completes most questions	Requires additional time	Unable to complete
Accuracy & Precision	Very high accuracy	Good accuracy	Moderate accuracy	Low accuracy

Rubrics for Learning Activity–2: GATE-Based Aptitude Test (15 Marks)

Performance Indicator	Superior (10)	Good (8)	Fair (6)	Needs Improvement (5)
Understanding of Concepts	Demonstrates excellent conceptual clarity and application	Good understanding with minor errors	Basic understanding	Poor understanding
Problem Solving Ability	Solves all problems correctly with proper methodology	Solves most problems correctly	Partial solutions with errors	Unable to solve problems effectively
Mathematical Accuracy	Calculations and derivations are error-free	Minor computational errors	Several errors	Significant errors
Presentation & Organization	Well-structured, neat, and professionally presented	Organized with minor deficiencies	Average presentation	Poor presentation

Term Work (TW) and Self Learning (SL) components in Number of Hours per semester		
Term work (includes assignments, seminars, micro projects, industrial visits, any other student activities etc.)		
Sl. No.	**Term Work (TW) Activity**	**Number of Hours / Semester**
1.	Collaborative Problem Solving on Gram-Schmidt Orthogonalization and QR Decomposition	6
2.	Mini Project on Eigenvalues, Eigenvectors and Principal Component Analysis (PCA)	6
3.	Team-Based Analysis of Hypothesis Testing and Confidence Intervals	6
4.	Group Presentation on Applications of SVD in Image Compression and Data Analytics	6
SL: Self Learning, MOOCs, spoken tutorials, online educational resources etc.		
Sl. No.	**Self-Learning (SL) Activity**	**Number of Hours / Semester**
1.	Python Programming Practice using NumPy for Matrix Operations	6
2.	Study of Machine Learning Applications using SVD and PCA	6
3.	Preparation of Summary Notes on Markov Chains and Stochastic Processes	6
4.	Literature Survey on Mathematical Foundations of Machine Learning	6

Continuous Internal Evaluation (CIE)

1. The CIE marks shall be decided based on internal tests and other outcome-based activities. The continuous internal evaluation shall be carried out by the teacher handling the course.
2. Out of 50 marks earmarked for CIE, 25 marks shall be assigned for internal tests. The first test shall be conducted after completing two modules of the syllabus and the second one after completing the remaining three modules.
3. The remaining 25 marks shall be assigned for Continuous Course Assessment (CCA), conducted as per the rubrics listed in the assessment section of the respective syllabus.
4. A student shall obtain a minimum of 40% marks or 20 out of 50 marks allotted to CIE to become eligible to appear for the SEE.

Passing requirement in SEE

1. For a pass in the Semester End Examination (SEE), a student shall secure a minimum of 35 marks out of 100.
2. For the declaration of a pass grade, the sum of the Continuous Internal Evaluation (CIE) marks (out of 50) marks and the SEE marks scaled down to 50 shall be greater than or equal to 40 marks.
3. If the total (CIE + SEE) is less than 40 marks, the student shall be awarded the grade ‘F’ (Fail).

CMOS Digital VLSI Design			
Course Code	1BVL402	Scheme	2025
Type of course	Theory and Lab	Semester	IV
Teaching Hours/Week (L:T:P)	3:2:2	CIE Marks	50
Total Hours of Pedagogy L:T:P:SL:TW	42:0:28:50:0	SEE Marks	50
Credits	**04**	Total Marks	100
Type of Examination (IPCC):	Theory- CIE +SEE, Lab- CIE only.	Exam Hours	3

Course Outcome (Course Skill Set)

At the end of the course, the student will be able to:

1) Understand MOSFET device operation and CMOS fabrication technologies.
2) Analyze CMOS circuits using RC models and estimate delay and power consumption.
3) Model interconnects and design CMOS combinational circuits.
4) Design CMOS sequential circuits.
5) Analyze and design CMOS memory circuits and memory subsystems.

Module-1

Module 1: Introduction to VLSI and MOS Transistor Theory

Introduction to VLSI design: History and trends in VLSI, overview of CMOS logic, design abstraction and partitioning.

MOS transistor fundamentals: MOS structure, operation of MOSFET, long-channel I-V characteristics, MOS capacitance models, DC transfer characteristics of CMOS inverter.

Textbook 1: **Chapter 1:** 1.1 to 1.4 and 1.6;

Chapter 2: 2.1, 2.2, **2.3.1**, 2.5

Number of Hours: 09

Module-2

Module 2: CMOS Fabrication and Layout Basics

Overview of CMOS fabrication technology, n-well and p-well processes, twin-well technology.

Basic fabrication steps in CMOS IC manufacturing. Layout design rules and stick diagrams.

Textbook 1: **Chapter 1:** 1.5;

Chapter 3: 3.1, 3.3.1 **to** 3.3.2

Number of Hours: 08

Module-3

Module 3: Delay and Power in CMOS Circuits

Transient response of CMOS circuits: RC delay model for MOS circuits. Linear delay model and logical effort. Delay in logic gates.

Power dissipation in CMOS circuits: dynamic power, static power, leakage power.

Textbook 1: **Chapter 4:** 4.1, 4.2, 4.3.1 **to** 4.3.6, 4.4.1 **to** 4.4.3;

Chapter 5: 5.1. to 5.3

Number of Hours: 09

Module-4

Module 4: Interconnect and Combinational Circuit Design

Interconnect fundamentals: wire geometry, parasitic resistance, capacitance and inductance. Interconnect modeling and its impact on delay and energy. Cross-talk and signal integrity issues.

CMOS combinational circuit design: static CMOS logic, pass transistor logic, transmission gate logic, introduction to SOI circuits.

Textbook 1: **Chapter 6:** 6.1, 6.2.1 **to** 6.2.3, 6.3.1 **to** 6.3.3, 6.4.1 **to** 6.4.2;

Chapter 9: 9.1, 9.2.1 **to** 9.2.3, 9.2.5, 9.5

Number of Hours: 08

Module-5

Module 5: Sequential Circuits and Memory Subsystems

	Sequential circuit design: CMOS latches and flip-flops, pulsed latches, resettable and enabled flip-flops, dual edge triggered flip-flops. Incorporating logic into latches and flip-flops. **Array subsystems:** SRAM cells, row and column circuitry. Read-only memories, content addressable memories, programmable logicarrays. Textbook 1: **Chapter 10:** 10.1, 10.3.1 **to** 10.3.6 **Chapter 12:** 12.1, 12.2.1 **to** 12.2.3, 12.4, 12.6, 12.7 Number of Hours: 08
	PRACTICAL COMPONENTS OF IPCC
	PART – A: FIXED SET OF EXPERIMENTS
	1. **Study of MOS Transistor Characteristics**: Plot I–V characteristics of NMOS and PMOS transistors. Determine threshold voltage and operating regions. 2. **CMOS Inverter – DC Analysis:** Design a CMOS inverter and obtain Voltage Transfer Characteristics (VTC). Determine switching threshold and noise margins. 3. **Transient Analysis of CMOS Inverter:** Perform transient simulation. Measure propagation delay, rise time, and fall time. 4. **Power Analysis of CMOS Inverter:** Analyze dynamic and static power dissipation. Study the effect of switching activity and load capacitance. 5. **Layout of CMOS Inverter:** Draw layout of CMOS inverter. Verify layout using Design Rule Check (DRC)., Extract RC, simulate the Circuit 6. **CMOS NAND Gate Design and Simulation:** Design and simulate a 2-input CMOS NAND gate. Verify logical functionality. **CMOS NOR Gate Design and Simulation:** Design and simulate a 2-input CMOS NOR gate. Verify logical functionality. 7. **Layout Design of CMOS NAND Gate:** Draw the standard cell layout of a 2-input CMOS NAND gate. Perform DRC and parasitic extraction and simulate 8. **Layout Design of CMOS NOR Gate:** Draw the standard cell layout of a 2-input CMOS NOR gate. Perform DRC and parasitic extraction and simulate 9. **Transmission Gate Design:** Design and simulate a CMOS transmission gate. Analyze bidirectional switching characteristics. 10. **Multiplexer using Transmission Gates:** Implement 2:1 multiplexer using transmission gates. Verify functionality through simulation. 11. **Interconnect Modeling and RC Delay Analysis:** Model interconnect resistance and capacitance. Analyze the effect of wire length on delay. 12. **Design of CMOS D Latch:** Design and simulate CMOS D latch. Analyze timing parameters. 13. **Design of CMOS D Flip-Flop:** Design and simulate edge-triggered D flip-flop. Measure propagation delay. 14. **Design of 6T SRAM Cell:** Design and simulate 6-transistor SRAM cell.
	PART – B: OPEN ENDED EXPERIMENTS Open-ended experiments are a type of laboratory activity where the outcome is not predetermined and students are given the freedom to explore, design, and conduct the experiment based on the problem statements as per the concepts defined by the course coordinator. It encourages creativity, critical thinking, and inquiry-based learning.
	1. **CMOS Inverter Optimization** Design a CMOS inverter and optimize transistor sizing to achieve: Minimum propagation delay, Improved noise margins, Reduced power dissipation Students compare the effect of different W/L ratios and load capacitances. **2. Design and Layout of a CMOS Standard Cell** Design a complete standard cell (such as NAND, NOR, or XOR gate) including: Schematic design, Layout following design rules, Functional verification and delay analysis. **3. CMOS Full Adder Design** Design and simulate a CMOS full adder circuit using any logic style such as: Static CMOS logic, Transmission gate logic, Compare transistor count, delay, and power consumption.

4. SRAM Cell Design and Analysis
Design a 6-transistor CMOS SRAM cell and analyze: Read and write operation, Static noise margin, Effect of transistor sizing on stability.

Suggested Learning Resources: (Text Book/ Reference Book/ Manuals):

Textbook:

1. Neil H. E. Weste, David Harris "CMOS VLSI Design A Circuits and Systems Perspective" Pearson Education Publisher, Fourth Edition, 2015.

Reference books / Manuals:

1. Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic "Digital Integrated Circuits A Design Perspective" Pearson Education Publisher, Second Edition, 2010.
2. John P Uyemura "Introduction to VLSI Circuits and Systems" Wiley Publication, 2002.
3. R. Jcob Baker, Harry W. Li and David E Boyce "CMOS Circuit Design, Layout, and Simulation" PHI, 1998.

Web links and Video Lectures (e-Resources):

1) https://nptel.ac.in/courses/108107129
2) https://nptel.ac.in/courses/117106149

Teaching-Learning Process (Innovative Delivery Methods):
The following are sample strategies that educators may adopt to enhance the effectiveness of the teaching-learning process and facilitate the achievement of course outcomes.

1. **Interactive Lectures and Concept Visualization**
   Use animations, simulation tools, and multimedia presentations to explain MOSFET operation, CMOS fabrication, and circuit behavior.

2. **Simulation-Based Learning**
   Encourage students to design and simulate CMOS circuits using industry-standard or open-source EDA tools such as LTspice, Ngspice, Electric VLSI, Magic VLSI, (where available)
   .

3. **Flipped Classroom Approach**
   Assign video lectures, NPTEL modules, and reading materials before class and utilize classroom time for discussions, problem-solving, and design exercises.

4. **Problem-Based Learning (PBL)**
   Present real-world VLSI design challenges involving power optimization, delay reduction, and interconnect modeling for collaborative analysis and solution development.

5. **Case Studies from Semiconductor Industry**
   Discuss modern VLSI technologies, low-power design techniques, FinFETs, advanced CMOS processes, and semiconductor memory architectures used in contemporary integrated circuits.

6. **Mini Projects and Open-Ended Experiments**
   Encourage students to design optimized CMOS logic gates, arithmetic circuits, memory cells, and standard cells with performance comparison based on area, delay, and power.

7. **Assessment through Design Reviews**
   Conduct schematic reviews, layout reviews, simulation result presentations, and technical seminars to strengthen analytical and communication skills.

8. **Project-Based Learning**
   Facilitate small-scale VLSI design projects such as CMOS full adders, SRAM cells, multiplexers, and low-power logic circuits using simulation and layout tools.

Tools Used: Any Open Source Tools, or corresponding tools from commercial EDAs such as Siemens, Cadence, Altium etc.

	Control Systems		Semester	IV
	Course Code	1BVL403	CIE Marks	50
	Teaching Hours/Week (L:T:P: S)	42:28:0:50	SEE Marks	50
	Total Hours of Pedagogy	120	Total Marks	100
	Credits	4	Exam Hours	3
	Examination type (SEE)	**Theory**		

Course outcome (Course Skill Set)

CO1: Analyze physical systems and their mathematical models using differential equations, transfer functions, and system analogies.
CO2: Evaluate the effect of feedback on control systems by examining block diagrams, signal flow graphs, and overall system behavior.
CO3: Analyze the time response characteristics and steady-state performance of first- and second-order control systems, including the influence of basic controllers.
CO4: Assess the stability and relative stability of control systems using Routh–Hurwitz criterion and root locus techniques.
CO5: Analyze control system stability and performance in the frequency domain using Bode, Polar, and Nyquist plots.

Module-1

Introduction to Control Systems: Types of Control Systems, Effect of Feedback Systems, Differential equation of Physical Systems – Mechanical Systems, Electrical Systems, Analogous Systems. Block diagrams and signal flow graphs: Transfer functions, Block diagram algebra and Signal Flow graphs.

Textbook T1: Chapter 1: 1.1,1.3,1.5,1.6, Chapter 2: 2.1,2.2,2.4,2.5,2.6,2.7
Textbook T2: Chapter 3 **Number of Hours: 14**

Module-2

Time Response of feedback control systems: Standard test signals, Unit step response of First and Second order Systems. Time response specifications, Time response specifications of second order systems, steady state errors and error constants. Introduction to PI, PD and PID Controllers (excluding design).

Textbook T1: Chapter 5:5.1,5.2,5.3,5.4,5.5
Textbook T2: Chapter 3 **Number of Hours: 14**

Module-3

Stability analysis: Concept of stability, necessary conditions for Stability, Routh- stability criterion, Relative stability criterion
Root-Locus Techniques: Root locus concepts, Construction of root loci, Stability of System.

Textbook T1: Chapter 6:6.1,6.2,6.3,6.4,6.5 Chapter 7:7.1,7.2,7.3
Textbook T2: Chapter 3

Number of Hours: 14

Module-4

Frequency domain analysis and stability using Bode plots: Correlation between time and frequency response, Bode Plots, Experimental determination of transfer function.

Textbook T1: Chapter 8: 8.2,8.4,8.5,8.6,8.7

	Textbook T2: Chapter 3 **Number of Hours: 14**
	Module-5
	Frequency domain analysis and stability: Introduction to Polar Plots, Mathematical preliminaries, Nyquist Stability criterion, Nyquist plots. Textbook T1: Chapter 8: 8.1,8.3, Chapter 9: 9.1,9.2,9.3 **Number of Hours: 14**

Suggested Learning Resources: (Text Book/ Reference Book/ Manuals):

Textbooks:

1. J. Nagarath and MGopa1," Control Systems Engineering", NewAge International(p) Limited Publishers, 5th Edition- 2005, ISBN:81-224-2008-7
2. Analysis and design of Control system using MATLAB by Rao V Dukkipati, New Age international (p) Limited Publishers,2006 Publication.

Reference books / Manuals:

1. K.Ogata,"Modem Control Engineering" Pearson .Education Asia I PHI, 4th Edition, 2002.
2. K.ChannaVenkatesh and D. Ganesh Rao, "Control Systems", Sanguine TechnicalPublishers.
3. Chi-Tsong Chen, "Analog and Digital Control System Design Transfer-Function, State-Space, and Algebraic Methods", OUP, 2006

Web links and Video Lectures (e-Resources):

- https://nptel.ac.in/courses/107106081
- https://onlinecourses.nptel.ac.in/noc24_ee65/preview

Teaching-Learning Process (Innovative Delivery Methods):

The following are sample strategies that educators may adopt to enhance the effectiveness of the teaching-learning process and facilitate the achievement of course outcomes.

1. Ensure at least 2 hours of review of mathematical concepts such as matrix algebra, transfer functions, complex variables, first and second order differential equations during the tutorial sessions
2. Present case studies for each module which have industry relevance
3. Use of simulation tools demonstrations in the classroom to illustrate complex concepts

Computer Architecture and Microcontrollers			
Course Code	1BVL404	Scheme	2025
Type of Course	**PCC**	Semester	3
Teaching Hours/Week (L:T:P)	3 : 0 : 0	CIE Marks	50
Total Hours of Pedagogy per semester L /T/P/SL&TW:	42: 0 :0 :48	SEE Marks	50
Credits	**3**	Total Marks	100
Examination type (SEE)	Theory	Exam Hours	3

Course outcome (Course Skill Set)

At the end of the course, the student will be able to:

CO1: Analyze computer organization, instruction execution, addressing modes, and evaluate system performance.

CO2: Evaluate I/O organization, interrupt handling, DMA operations, and cache memory design techniques.

CO3: Examine processing unit operations and assess pipelining performance and efficiency.

CO4: Understand and analyze ARM-based embedded system architecture, processor fundamentals, and basic embedded software development.

CO5: Apply ARM instruction set concepts for embedded programming and for different applications.

Module-1

Basic Structure of Computers: Functional Units, Basic Operational Concepts, Bus structure, Performance – Processor Clock, Basic Performance Equation, Clock Rate, Performance Measurement.

Machine Instructions and Programs: Memory Location and Addresses, Memory Operations, Instruction and Instruction sequencing, Addressing Modes, Assembler directives

Text book-1: 1.2, 1.3, 1.4, 1.6, 2.2, 2.3, 2.4, 2.5,2.6.1

Number of Hours: 8

Module-2

Input/output Organization: Accessing I/O Devices, Interrupts – Interrupt Hardware, Enabling and Disabling Interrupts, Handling Multiple Devices

Direct Memory Access: Bus Arbitration, Speed, size and Cost of memory systems. Cache Memories – Mapping Functions.

Text book-1: 4.1, 4.2,4.2.1, 4.2.2, 4.2.3, 4.4, 5.4, 5.5.1

Number of Hours: 8

Module-3

Basic Processing Unit: Some Fundamental Concepts: Register Transfers, Performing ALU operations, fetching a word from Memory, Storing a word in memory. Execution of a Complete Instruction.

Pipelining: Basic concepts, Role of Cache memory, Pipeline Performance.

Text book-1: 7.1, 7.2, 8.1

Number of Hours: 8

Module-4

ARM Embedded Systems:

Introduction, RISC design philosophy, ARM design philosophy, Embedded system hardware – AMBA bus protocol, ARM bus technology, Memory, Peripherals, Embedded system software – Initialization (BOOT) code, Operating System, Applications.

ARM Processor Fundamentals, ARM core dataflow model, registers, current program status register, Pipeline, Exceptions, Interrupts and Vector Table, Core extensions.

Text book-2: 1.1to 1.5, 2.1 to 2.5

Number of Hours:10

Module-5

Introduction to the ARM Instruction set:

Introduction, Data processing instructions, Load – Store instruction, Software interrupt instructions, Program status register instructions, Loading constants, ARMv5E extensions, Conditional Execution.

Text book-2: 3.1 to 3.9

Number of Hours:8

Suggested Learning Resources: (Text Book/ Reference Book/ Manuals):

Text books:

1. **Carl Hamacher, ZvonkoVranesic, SafwatZaky, Computer Organization, 5 th Edition, Tata McGraw Hill.**

2. **Andrew N Sloss, Dominic System and Chris Wright, "ARM System Developers Guide", Elsevier, Morgan Kaufman publisher, 1st Edition, 2008.**

Reference Books:

1. **Computer Organization and Architecture, William Stallings, 9th Edition, Pearson.**
2. **David A. Patterson, John L. Hennessy: Computer Organization and Design – The Hardware / Software Interface ARM Edition, 4th Edition, Elsevier, 2009.**

Web links and Video Lectures (e-Resources):

1. **https://nptel.ac.in/courses/106106092**
2. **https://nptel.ac.in/courses/106106166**
3. **https://nptel.ac.in/courses/106103180**
4. **https://nptel.ac.in/courses/108105102**

Teaching-Learning Process (Innovative Delivery Methods):

The following are sample strategies that educators may adopt to enhance the effectiveness of the teaching-learning process and facilitate the achievement of course outcomes.

1. **Concept Visualization and Demonstration:** Use processor simulators, ARM development environments, and visual demonstrations to illustrate instruction execution, addressing modes, pipelining, cache memory operations, interrupts, and processor architecture.
2. **Hands-on Programming Activities:** Conduct ARM assembly language programming exercises and embedded system application demonstrations to reinforce instruction set concepts, processor fundamentals, and embedded software development.
3. **Application-Oriented Learning:** Incorporate case studies and real-world examples from computer systems and embedded applications, such as IoT devices, consumer electronics, and industrial controllers, to connect theoretical concepts with practical implementations.

Design for Test Laboratory		Scheme	2025
Course Code	1BVLL405	Semester	III
Teaching Hours/Week (L:T:P)	0:0:2	CIE Marks	50
Total Hours of Pedagogy L:T:P:SL/TW	0:0:28:2	SEE Marks	50
Credits	1	Total Marks	100
Examination type (SEE)	**Practical**	Exam Hours	3

Course Outcome (Course Skill Set)

At the end of the course, the student will be able to:

1. Demonstrate the use of VLSI testing and DFT tools to model faults, perform fault simulation, and evaluate fault coverage in combinational circuits.
2. Generate test vectors for combinational circuits using path sensitization, D-Algorithm, and Boolean difference methods.
3. Analyze the testability of sequential circuits using time-frame expansion, state justification, state propagation, and scan-chain architectures.
4. Design and implement Design for Testability (DFT) techniques, including full scan design, boundary scan (JTAG), Built-In Self-Test (BIST) using LFSR and MISR, and basic memory testing concepts.

Note:

1. The laboratory syllabus consists of PART-A and PART-B. While PART-A has 8 conventional experiments, PART-B has 4 typical open-ended experiments. The maximum marks for the laboratory course are 100.
2. Both PART-A and PART-B are considered for CIE and SEE.
3. Students have answer 1(one) question from PART-A and 1(one) question from PART-B.
   a. The questions set for SEE shall be from among the experiments under PART-A. It is evaluated for **70 marks** out of the maximum 100 marks.
   b. The open-ended question set for SEE shall be any other open-ended question and not selected from the experiments under PART-A. It shall be evaluated for **30 marks.**
4. For Continuous Internal Evaluation (CIE) during the semester, classwork shall typically include open-ended questions from **Part-B**, along with other similar questions designed to enhance the students' skills.

PART – A
FIXED SET OF EXPERIMENTS

1. Introduction to VLSI testing concepts and DFT tools. Demonstration of simulation environment using open source /free ware / Tessent/ Modus / any other commercial tools.
2. Modeling stuck-at faults in simple combinational circuits (AND/OR networks).
3. Fault simulation and fault coverage calculation for combinational circuits.
4. Implementation of path sensitization method for generating test vectors.
5. Test generation using D-Algorithm (ATPG concept demonstration).
6. Test generation using Boolean difference method.
7. Parallel and deductive fault simulation techniques.
8. Testing of sequential circuits using time-frame expansion concept.
9. Sequential circuit testing – state justification and propagation analysis.
10. Implementation of scan chain architecture in a simple digital circuit. Demonstrate the scan working within open source /free ware / Tessent/Modus/ any other commercial tools.

PART – B

OPEN ENDED EXPERIMENTS
Open-ended experiments are a type of laboratory activity where the outcome is not predetermined and students are given the freedom to explore, design, and conduct the experiment based on the problem statements as per the concepts defined by the course coordinator. It encourages creativity, critical thinking, and inquiry-based learning.
1. Study and demonstration of boundary scan (IEEE 1149.1 – JTAG) architecture. Insert Boundaryscan and TAP for a design netlist using BoundaryScan and verify mandatory instructions over simulations. 2. Explain any type of March algorithm. Implement the March algorithm by inserting BIST in a design netlist using Memory BIST Tool. Generate Memory BIST patterns and simulate.. 3. Execute scan chain implementation for an 8-bit counter design in netlist. Execute ATPG on the scan inserted design and verify the ATPG patterns in Questa. Estimate coverage for Stuck and delay test.
Above Experiments Can be done using any tool: **Open source / Free ware / Tessent/ Modus / any other commercial tools.**
Suggested Learning Resources: (Text Book/ Reference Book/ Manuals): **Textbooks:** 1. Digital Systems Testing and Testable Design — Miron Abramovici, Melvin A. Breuer, Arthur D. Friedman 2. Digital System Test and Testable Design — Zainalabedin Navabi 3. Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits — Michael L. Bushnell and Vishwani D. Agrawal
Web links and Video Lectures (e-Resources): **1.** **https://www.youtube.com/watch?v=MgCFUO2BrkQ** **2.** **https://www.youtube.com/watch?v=nX0XCD0ggHs&list=PLvd8d-SyI7hjk_Ci0zpTqImAtpEjdK5JF**
Teaching-Learning Process (Innovative Delivery Methods): The following are sample strategies that educators may adopt to enhance the effectiveness of the teaching-learning process and facilitate the achievement of course outcomes. 1. While explaining each experiment, also focus on the application of that particular experiment in the electronics industry 2. In labs utilizing software programming, the emphasis must be on student understanding of the logic (e.g. pseudo-code) of the code, which libraries are required, which important functions calls need to be made and expected output. Faculty should not penalize students for making syntax errors in codes in the write up – however students must be able to debug the errors during program execution 3. Students should not memorize pin diagrams, these must be provided to the student during CIE and SEE 4. For record writing, faculty should ensure students write the main objective, design and procedure in their own words – and do not copy from manuals/online. Also, record writing should involve higher Blooms levels and not just Remember and Understand levels.

Python for Measurement & Data Analysis

Course Code	**1BVLL406A**	Scheme	2025
Type of Course	Ability Enhancement Course (Laboratory)	Semester	IV
Teaching Hours/Week (L:T:P)	0:0:1	CIE Marks	50
Total Hours of Pedagogy L:T:P:SL:TW	0:0:28:02	SEE Marks	50
Credits	01	Total Marks	100
Type of Examination	Practical	Exam Hours	3

Course outcome (Course Skill Set)

At the end of the course, the student will be able to:

1. Write basic Python programs for numerical calculations.
2. Use Python libraries for handling experimental data.
3. Visualize measurement data using graphs and plots.
4. Perform simple statistical and signal analysis on measurement datasets.

SET OF EXPERIMENTS

1. Introduction to Python environment and basic commands
2. Numerical computation using Python
3. Working with lists and arrays using NumPy
4. Matrix operations using NumPy
5. Reading measurement data from CSV file
6. Data manipulation using Pandas
7. Plotting experimental data using Matplotlib
8. Plotting multiple signals
9. Scatter plot for sensor measurements
10. Statistical analysis of measurement data
11. Histogram of measurement errors
12. Correlation analysis between variables
13. Simple signal analysis using Python
14. Mini project: Measurement data analysis and visualization....

Suggested Learning Resources: (Text Book/ Reference Book/ Manuals):

Textbooks:

1. W. McKinney, Python for Data Analysis. Sebastopol, CA, USA: O'Reilly Media 2012.
2. Q. Kong, T. Siauw, and A. Bayen, Python Programming and Numerical Methods: A Guide for Engineers and Scientists. Cambridge, MA, USA: Academic Press, 2020.

Web links and Video Lectures (e-Resources):

1. Complete Python for Data Science Course
   https://glasp.co/youtube/p/python-for-data-science-course-for-beginners-learn-python-pandas-numpy-matplotlib?utm_source=chatgpt.com
2. Data Analysis with Python Full Course
   https://www.youtube.com/watch?v=r-uOLxNrNk8
3. NumPy Full Tutorial

https://www.datakwery.com/freecodecamp/numpy/?utm_source=chatgpt.com
Teaching-Learning Process (Innovative Delivery Methods): The following are sample strategies that educators may adopt to enhance the effectiveness of the teaching-learning process and facilitate the achievement of course outcomes. 1. Hands-on Experiential Learning through Python-based numerical computing and data analysis. 2. Data-Driven Problem-Based Learning using real-world measurement and sensor datasets. 3. Visualization-Based Learning through graphical representation and interpretation of data. 4. Application-Based Learning through mini projects involving data analysis and visualization.

SPICE Programming for Electronic Circuits			
Course Code	**1BVLL406B**	Scheme	2025
Type of Course	Ability Enhancement Course (Laboratory)	Semester	IV
Teaching Hours/Week (L:T:P)	0:0:1	CIE Marks	50
Total Hours of Pedagogy L:T:P:SL/TW	0:0:28:02	SEE Marks	50
Credits	01	Total Marks	100
Type of Examination	Practical	Exam Hours	03

Course Outcome (Course Skill Set)

At the end of the course, the student will be able to:

1. Understand the fundamentals of the SPICE simulation environment and circuit modeling.
2. Develop and execute SPICE netlists for basic electronic circuits.
3. Perform DC, AC, and transient analyses using SPICE simulation.
4. Analyze the behavior and performance of analog and digital electronic circuits through simulation.
5. Simulate and characterize MOSFET and CMOS-based circuits for VLSI applications.

SET OF EXPERIMENTS using

Simulation Program with Integrated Circuit Emphasis (SPICE)

1. Familiarization with the LTspice/Ngspice environment and basic SPICE commands. Develop a SPICE netlist for a resistive network and perform DC sweep analysis and measure current through all elements voltage across all nodes.
2. Develop a SPICE netlist for resistor networks and verify circuit behavior through simulation. Validate Ohm's Law using simulation results.
3. Develop a SPICE netlists and analyze the transient response of an RC low pass and RC high pass circuits.
4. Develop a SPICE netlists and analyze the transient response of an RL low pass and RL high pass circuits.
5. Develop a SPICE netlists and perform AC analysis of an RL low pass and RL high pass circuits.
6. Develop a SPICE netlists and perform AC analysis of an RC low-pass filter with and without parasitic inductance.
7. Develop a SPICE netlist and perform AC analysis of an RC high-pass filter with and without parasitic inductance.
8. Develop a SPICE netlists and simulate a diode rectifier circuit and clipping circuits.
9. Develop a SPICE netlist and perform AC analysis of a RLC circuit.
10. Develop a SPICE netlist and study the frequency response and Bode plot of a circuit. Correlate the observed peak impedance characteristics with transient analysis results.

MOSFET-Based Experiments

11. Develop a SPICE netlist and simulate the drain characteristics (ID–VDS) of a MOSFET. Analyze the effect of gate voltage on device operation.
12. Develop a SPICE netlist and simulate the transfer characteristics (ID–VGS) of a MOSFET. Determine key device parameters from the simulation results.
13. Develop a SPICE netlist and simulate a common-source MOSFET amplifier. Analyze voltage gain and frequency response.
14. Develop a SPICE netlist and simulate a MOSFET inverter. Analyze its switching characteristics and transient response.
15. Develop a SPICE netlist and simulate a CMOS inverter. Plot and analyze its DC transfer characteristics (VTC).
16. Develop a SPICE netlist for a buffer by creating inverter sub-circuit.

Mini Project (Recommended)

Design, write SPICE netlist, simulate and analyze one of the following circuits:

- Implement 2-stage CMOS domino logic and measure the delay.

- Implement NMOS current mirror circuit for 1:1 and 1:2 scaling.
- Implement NMOS Opamp with unity gain (Voltage Follower) and gain-2.
- Implement CMOS high to low level shifter cell.
- Impedance profile of a simple power delivery network (frequency response)

Suggested Learning Resources: (Textbook/ Reference Book/ Manuals):

Textbooks:

1. SPICE for Circuits and Electronics Using PSpice, M. H. Rashid, SPICE for Circuits and Electronics Using PSpice. Upper Saddle River, NJ, USA: Pearson Education, 2004.
2. The SPICE Book, A. Vladimirescu, The SPICE Book. New York, NY, USA: John Wiley & Sons, 1994.

Reference books / Manuals:

1. **Purdue University, SPICE user manual:** **https://www.physics.purdue.edu/~jones105/phys536_Spring2008/Spice3F4_Manual.pdf**
2. **HSPICE® User Guide: Simulation and Analysis -** **https://cseweb.ucsd.edu/classes/wi10/cse241a/assign/hspice_sa.pdf**

Web links and Video Lectures (e-Resources):

- **IITR lecture – "Introduction to spice":**
  - **https://www.youtube.com/watch?v=KfBtduxuxCw**
- **IITR lecture – "SPICE Simulation":**
  - **https://www.youtube.com/watch?v=Z6Cfbs0ODpg**
  - **https://www.youtube.com/watch?v=tI5GLv1ipKw**

Teaching-Learning Process (Innovative Delivery Methods):

The following are sample strategies that educators may adopt to enhance the effectiveness of the teaching-learning process and facilitate the achievement of course outcomes.

1) **Hands-on Simulation-Based Learning:**
   Conduct guided laboratory sessions where students develop SPICE netlists, perform simulations, and analyze circuit behavior using LTspice, Ngspice, or equivalent tools. Encourage students to compare simulation results with theoretical calculations and expected circuit responses.
2) **Mini-Project and Problem-Based Learning (PBL):**
   Assign real-world circuit design problems and VLSI-oriented mini-projects involving MOSFETs, CMOS circuits, current mirrors, level shifters, and domino logic. Students shall design, simulate, validate, and present their solutions, fostering self-learning, critical thinking, and industry-relevant design skills.

Recommended Tools:

Free circuit simulation tools such as **LTspice and Ngspice**, or commercial VLSI ECAD software packages such as Siemens, Cadence, Altium etc..

RTL to GDSII Flow			
Course Code	**1BVLL406C**	Scheme	2025
Type of Course	Ability Enhancement Course (Laboratory)	Semester	IV
Teaching Hours/Week (L:T:P)	0:0:2	CIE Marks	50
Total Hours of Pedagogy L:T:P:SL:TW	0:0:28:02	SEE Marks	50
Credits	01	Total Marks	100
Type of Examination	Practical	Exam Hours	3

Course outcome (Course Skill Set)

At the end of the course, the student will be able to:

1. Explain the stages of the RTL-to-GDSII design flow.
2. Develop and simulate simple RTL designs using Verilog.
3. Perform logic synthesis and timing analysis using EDA tools.
4. Understand physical design stages including floorplanning, placement, routing, and verification.

SET OF EXPERIMENTS

1. Introduction to RTL-to-GDSII design flow and EDA tools
2. Writing Verilog RTL for basic logic gates
3. RTL design of combinational circuits (adder, multiplexer)
4. Functional simulation and waveform analysis
5. RTL design of sequential circuits (flip-flops)
6. Simulation of sequential circuits
7. RTL design of a 4-bit counter
8. Logic synthesis of RTL design
9. Analysis of synthesized netlist and reports
10. Timing analysis of synthesized design
11. Introduction to floorplanning
12. Placement and routing concepts
13. Clock tree synthesis overview
14. Physical verification concepts (DRC/LVS)
15. Final RTL-to-GDSII design flow demonstration for any simple experiment

Suggested Learning Resources: (Text Book/ Reference Book/ Manuals):

Textbook:

1. S. Saurabh, Introduction to VLSI Design Flow. Cambridge, U.K.: Cambridge University Press, 2023.

Web links and Video Lectures (e-Resources):

1. NPTEL RTL to GDS Flow Course
   https://nptel.ac.in/courses/108106191

Teaching-Learning Process (Innovative Delivery Methods):

The following are sample strategies that educators may adopt to enhance the effectiveness of the teaching-learning process and facilitate the achievement of course outcomes.

1. Hands-on Tool-Based Learning using EDA tools for RTL-to-GDSII design flow.
2. Project-Based Learning through end-to-end digital IC design and implementation.

3. Visualization and Analysis-Based Learning using simulation, synthesis, timing, and layout reports.
4. Collaborative Learning through design reviews, technical discussions, and team-based projects.

Recommended Tools:
Any freeware such as **OpenLane**, **or** any commercial VLSI EDA software (e.g. Siemens, Cadence, Altium etc.).

OpenLane Features

- Fully automated RTL-to-GDSII design flow.
- Integrates synthesis, floorplanning, placement, clock tree synthesis (CTS), routing, and signoff verification.
- Based on the open-source **SkyWater SKY130 Process Design Kit (PDK)**.
- Supports end-to-end ASIC design implementation.
- Suitable for teaching **VLSI Physical Design**, **ASIC Design Flow**, and **Design Automation** concepts.
- Integrates widely used open-source tools such as Yosys, OpenROAD, Magic, Netgen, and KLayout.

Power Electronics			
Course Code	**1BVLL406D**	Scheme	2025
Type of Course	Ability Enhancement Course (Laboratory)	Semester	IV
Teaching Hours/Week (L:T:P)	0:0:1	CIE Marks	50
Total Hours of Pedagogy L:T:P:SL:TW	0:0:28:02	SEE Marks	50
Credits	01	Total Marks	100
Type of Examination	Practical	Exam Hours	03

Course outcome (Course Skill Set)

At the end of the course, the student will be able to:

1. Identify and test power semiconductor devices.
2. Analyze the operation of controlled and uncontrolled rectifiers.
3. Understand the working of DC–DC converters and inverters.
4. Interpret voltage and current waveforms in power electronic circuits.

SET OF EXPERIMENTS

1. Study and identification of power semiconductor devices
2. V–I characteristics of power diode
3. V–I characteristics of SCR
4. Half-wave rectifier with resistive load
5. Full-wave rectifier with resistive load
6. Controlled rectifier using SCR
7. DC chopper circuit demonstration
8. Step-down DC–DC converter experiment
9. Step-up DC–DC converter experiment
10. MOSFET switching characteristics
11. Single-phase inverter circuit
12. Measurement of inverter output waveform
13. PWM control of power electronic circuit

Suggested Learning Resources: (Text Book/ Reference Book/ Manuals):

Textbooks:

1. Power Electronics: Circuits, Devices and Applications, M. H. Rashid, Power Electronics: Circuits, Devices and Applications, 4th ed. Noida, India: Pearson Education, 2014.
2. Power Electronics, P. S. Bimbhra, Power Electronics, 5th ed. New Delhi, India: Khanna Publishers, 2012.

Web links and Video Lectures (e-Resources):

https://www.youtube.com/watch?v=jydMBLSh7iI&list=PLSnw1KE0TFkVu05Ws0Ax143gZYmxPMCoY

Teaching-Learning Process (Innovative Delivery Methods):
The following are sample strategies that educators may adopt to enhance the effectiveness of the teaching-learning process and facilitate the achievement of course outcomes.

1. Experiential Learning through hands-on experimentation with power electronic circuits.
2. Simulation-Assisted Learning for analysis and validation of circuit performance.
3. Problem-Based Learning through parameter variation and performance evaluation.
4. Application-Oriented Learning through mini projects involving power conversion and control systems.

BIOLOGY FOR ELECTRICAL AND ELECTRONICS ENGINEERS		Semester	IV
Course Code	**1BEC407**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	2:0:0:2	SEE Marks	50
Total Hours of Pedagogy	28	Total Marks	100
Credits	02	Exam Hours	3
Examination type (SEE)	Theory		

Course objectives:

- Introduce biological concepts relevant to electrical/electronic systems.
- Apply biodesign principles to sensors, circuits, and biomedical devices.
- Explore biomimetic for signal processing, control, and energy systems.
- Motivate interdisciplinary innovation between biology and electronics

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Explanation via real life problem, situation modelling, and deliberation of solutions, hands-on sessions, reflective and questioning /inquiry-based teaching.
2. Instructions with interactions in classroom lectures (physical/hybrid).
3. Use of ICT tools, including YouTube videos, related MOOCs, AR/VR/MR tools.
4. Flipped classroom sessions (~10% of the classes).
5. Industrial visits, Guests talks and competitions for learning beyond the syllabus.
6. Students' participation through audio-video based content creation for the syllabus (as assignments).
7. Use of gamification tools (in both physical/hybrid classes) for creative learning outcomes.
8. Students' seminars (in solo or group) /oral presentations.

Module-1 (5 Hours)

INTRODUCTION TO BIOLOGY:

The cell(as an information-processing unit): the basic unit of life, Structure and functions of a cell. The Plant Cell and animal cell, Prokaryotic and Eukaryotic cell, Stem cells (inspiration for regenerative bioelectronics) and their application. Importance of special biomolecules: Enzymes, vitamins and hormones.(Classification with one example each,Properties and functions)

Module-2(5 Hours)

BIOMOLECULES AND THEIR APPLICATIONS (QUALITATIVE):

DNA/RNA for bio-computing and molecular electronics, Forensics – DNA fingerprinting, lipids (biodiesel, cleaning agents/detergents), Enzymes (glucose-oxidase in biosensors, lignolytic enzyme in bio-bleaching).Human Blood substitutes - hemoglobin-based oxygen carriers (HBOCs) and perflourocarbons (PFCs).

Module-3(8 Hours)

HUMAN ORGAN SYSTEMS AND BIO DESIGNS (QUALITATIVE):

Brain as a CPU system (architecture, CNS and Peripheral Nervous System, signal transmission, EEG, Robotic arms for prosthetics. Engineering solutions for Parkinson's disease).Eye as a Camera system (architecture of rod and cone cells, optical corrections, cataract, lens materials, bionic eye). Heart as a pump system (architecture, electrical signalling - ECG monitoring and heart related issues, reasons for blockages of blood vessels, design of stents, pace makers, defibrillators). Lungs as purification system (architecture, gas exchange mechanisms, spirometry, abnormal lung physiology - COPD, Ventilators, Heart-lung machine). Kidney as a filtration system (architecture, mechanism of filtration, CKD, dialysis systems).

Module-4 (5 Hours)
NATURE-BIOINSPIRED MATERIALS AND MECHANISMS (QUALITATIVE): Echolocation (ultrasonography, sonars), Photosynthesis (photovoltaic cells, bionic leaf). Bird flying (GPS and aircrafts), Lotus leaf effect (Super hydrophobic and self-cleaning surfaces), Plant burrs (Velcro), Shark skin (Friction reducing swim suits), Kingfisher beak (Bullet train).
Module-5(5 Hours)
TRENDSBIOENGINEERING (QUALITATIVE):
Bioprinting techniques and materials, 3D printing of ear, bone and skin. 3D printed foods. Electrical tongue and electrical nose in food science, DNA origami and Biocomputing, Bioimaging and Artificial Intelligence for disease diagnosis. Bioremediation and Bio mining.Medical imaging technologies—X-ray, CT, MRI and Ultrasound (overview);

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

1. Elucidate the basic biological concepts via relevant industrial applications and case studies.
2. Evaluate the principles of design and development, for exploring novel bioengineering projects.
3. Corroborate the concepts of biomimetics for specific requirements.
4. Think critically towards exploring innovative biobased solutions for socially relevant problems.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25 marks.
- The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.
- For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 2 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

Text Book: Text Book: Engineering with Biology- Fundamentals and Applications, 2nd Edition, S. Fatima, R. S. Deshpande, M. Ziaullah, Mahantesh Mattada, Santosh Nejakar and Sadashiv Halbhavi, Najekar Publications, 2026

Suggested Learning Resources:

Books

- Biology for Engineers, Rajendra Singh C and Rathnakar Rao N, Rajendra Singh C and Rathnakar Rao N Publishing, Bengaluru, 2023.
- Human Physiology, Stuart Fox, Krista Rompolski, McGraw-Hill eBook. 16th Edition, 2022
- Biology for Engineers, Thyagarajan S., Selvamurugan N., Rajesh M.P., Nazeer R.A., Thilagaraj W., Barathi S., and Jaganthan M.K., Tata McGraw-Hill, New Delhi, 2012.
- Biology for Engineers, Arthur T. Johnson, CRC Press, Taylor and Francis, 2011 Biomedical Instrumentation, Leslie Cromwell, Prentice Hall 2011.
- Biology for Engineers, Sohini Singh and Tanu Allen, Vayu Education of India, New Delhi, 2014.
- Biomimetics: Nature-Based Innovation, Yoseph Bar-Cohen, 1st edition, 2012, CRC Press.
- Bio-Inspired Artificial Intelligence: Theories, Methods and Technologies, D. Floreano and C. Mattiussi, MIT Press, 2008.
- Bioremediation of heavy metals: bacterial participation, by C R Sunilkumar, N GeethaA C Udayashankar Lambert Academic Publishing, 2019.
- 3D Bioprinting: Fundamentals, Principles and Applications by Ibrahim Ozbolat, Academic Press, 2016.
- Electronic Noses and Tongues in Food Science, Maria Rodriguez Mende, Academic Press, 2016

Web links and Video Lectures (e-Resources):

- https://nptel.ac.in/courses/121106008
- https://freevideolectures.com/course/4877/nptel-biology-engineers-other-non-biologists
- https://ocw.mit.edu/courses/20-020-introduction-to-biological-engineering-design-spring-2009
- https://ocw.mit.edu/courses/20-010j-introduction-to-bioengineering-be-010j-spring-2006 https://www.coursera.org/courses?query=biology
- https://onlinecourses.nptel.ac.in/noc19_ge31/preview
- https://www.classcentral.com/subject/biology
- https://www.futurelearn.com/courses/biology-basic-concepts

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Group Discussion of Case studies

- Model Making and seminar/poster presentations
- Design of novel device/equipment like Cellulose-based water filters, Filtration system

ENVIRONMENTALSCIENCEPROJECT			
Course Code	**1BEP408**	Scheme	**2025**
TypeofCourse	SocietalDevelopmentCourse(SDC)	Semester	IV
TeachingHours/Week(L:T:P)	30(0:0:0)	CIEMarks	50
TotalHoursofPedagogyper SemesterCI(L/T):LI(P):TW&SL	30(0:0:0:30)	SEEMarks	50
Credits	**1**	TotalMarks	100
Examinationtype (SEE)	**Theory**	ExamHours	03

Course Objectives:

The Environmental Science Project is a practical, applied-learning course that builds students' environmental awareness and responsibility. It focuses on real issues such as climate change, pollution, biodiversity, resource use, soil erosion, and thermal comfort, using field surveys, case studies, data collection, audits, and analysis to develop feasible and sustainable solutions. Students may work individually or in groups of up to four, including interdisciplinary topics, and assessment is based on the prescribed rubrics.

Courseoutcome (CourseSkillSet):

Attheendofthecourse,thestudentwillbeableto:

1. **CO1 (L2 – Understand):** Identify and analyse environmental problems through field interaction and technical assessment.
2. **CO2 (L3 – Apply):** Develop skills in project planning, field survey, data collection, implementation, documentation and reporting.
3. **CO3 (L4 – Analyze):** Formulate feasible environmental problem statements and solutions considering practical constraints and sustainability aspects.
4. **CO4 (L3 – Apply):** Apply principles of environmental responsibility, ethics and societal welfare in engineering practice through community-oriented interventions.
5. **CO5 (L4 – Analyze):** Exhibit multidisciplinary learning and problem-solving ability based on collected data, user feedback and baseline conditions.
6. **CO6 (L5 – Evaluate):** Demonstrate teamwork and communication skills while interacting with technical and non-technical stakeholders and reflect on project impact on society.

Restrictionsandprofessionalconduct:

Environmental Science Projects should be academic, socially responsible, technically focused, and politically neutral. Students and faculty must maintain professionalism, ethical conduct, and respect while working with communities and stakeholders, and avoid any political, ideological, commercial, or disruptive activities. Projects should also consider practical constraints such as cost, resources, safety, environmental impact, and stakeholder cooperation.

SET OF PROJECT ACTIVITIES (TW/SL = 30 HOURS)

Methods for project identification:

Students may identify the project topic using one or more of the following methods: interaction with local rural or urban stakeholders such as local leaders, corporation/municipality personnel, NGOs, panchayat representatives, etc.; review of issues highlighted in print and electronic media, and social networks; and, after selecting a broad topic, collect data, conduct a feasibility survey, estimate timelines and resources, approximate expenditure, and define the problem statement and objectives clearly.

List of Project Topics and Engineering Outcomes:

The following structured sequence of activities is to be carried out during the semester:

Sl. No.	Project title	Measurable engineering outcome	Mapped POs	SDGs
1	Rural and urban water conservation and management systems	Prepare a site-specific water-saving plan, estimate water demand–supply gap, and propose a feasible conservation intervention with quantified savings.	PO1, PO2, PO3, PO4, PO10, PO11	SDG 6, SDG 11, SDG 12
2	Waste management and recycling	Conduct waste audit, classify waste streams, and design a segregation/recycling workflow with measurable reduction in mixed waste.	PO2, PO3, PO4, PO6, PO8, PO10	SDG 11, SDG 12, SDG 13
3	Afforestation	Identify a degraded area, prepare plantation layout, and demonstrate survival-rate	PO2, PO3, PO4, PO6, PO7,	SDG 11, SDG 13,

		tracking and maintenance schedule for saplings.	PO11	SDG 15
4	Biogas generation and power generation	Estimate organic waste availability, size a small biogas system, and document expected gas output or energy yield.	PO1, PO2, PO3, PO4, PO5, PO10	SDG 7, SDG 11, SDG 12
5	DPR for solar power rural plant	Prepare a DPR with load assessment, panel sizing, cost estimate, and projected energy generation and payback.	PO1, PO2, PO3, PO4, PO5, PO10	SDG 7, SDG 9, SDG 11
6	DPR for electrification of village/tribal community	Map unserved/underserved households, propose electrification layout, and estimate coverage, losses, and implementation cost.	PO1, PO2, PO3, PO4, PO10, PO11	SDG 7, SDG 9, SDG 10
7	DPR for rural drainage system	Survey drainage bottlenecks, develop a drainage layout, and estimate runoff handling capacity and flood-risk reduction.	PO1, PO2, PO3, PO4, PO6, PO10	SDG 6, SDG 9, SDG 11
8	Sustainability and environmental health projects	Assess local environmental health issues and propose interventions with measurable improvement in hygiene, safety, or resource use.	PO2, PO3, PO4, PO6, PO7, PO8	SDG 3, SDG 6, SDG 11, SDG 12
9	Plastic free campaigns	Measure plastic usage before and after awareness intervention and report percentage reduction or behavioural change.	PO2, PO3, PO6, PO7, PO8, PO10	SDG 11, SDG 12, SDG 13
10	Health and nutrition awareness	Conduct baseline and post-program awareness survey and daocument improvement in awareness score or adoption of healthier practices.	PO2, PO6, PO7, PO8, PO9, PO10	SDG 2, SDG 3, SDG 11
11	Societal projects involving health wellness	Identify a community health need and develop an awareness/service module with measurable participation and feedback outcomes.	PO2, PO3, PO6, PO8, PO9, PO10	SDG 3, SDG 11, SDG 17
12	Air quality monitoring system	Collect air-quality data, compare with reference limits, and present trends along with possible mitigation suggestions.	PO2, PO3, PO4, PO5, PO6, PO10	SDG 3, SDG 11, SDG 13
13	Plastic waste reduction campaign	Track collection, segregation, and replacement actions, and quantify reduction in plastic waste generation or littering.	PO2, PO3, PO6, PO7, PO8, PO10	SDG 11, SDG 12, SDG 13
14	Urban greening projects	Prepare greening plan, identify planting locations, and assess environmental benefits such as shade, aesthetics, or heat mitigation.	PO2, PO3, PO4, PO6, PO7, PO11	SDG 11, SDG 13, SDG 15
15	Smart agriculture solution	Design a low-cost monitoring or irrigation support solution and estimate improvement in water use efficiency or crop support.	PO1, PO2, PO3, PO4, PO5, PO10	SDG 2, SDG 6, SDG 9
16	Smart irrigation system	Estimate crop water requirement, propose control logic, and quantify water savings compared with conventional irrigation.	PO1, PO2, PO3, PO4, PO5, PO10	SDG 2, SDG 6, SDG 12
17	Food security initiatives / cold storage system	Estimate storage need, design a simple cold-chain concept, and document reduction in	PO1, PO2, PO3, PO4, PO5,	SDG 2, SDG 9, SDG 12

		spoilage or wastage.	PO10	

Suggested Learning Resources

Particulars	Titles and Publishers
Textbooks	1. Phadke, N. D., *Community Engagement and Social Innovation*, Oxford University Press, New Delhi. 2. Garg, N. R., *Project-Based Learning in Engineering Education*, Pearson India Education Services, Noida. 3. Gupta, A. and P. Singh, *Service Learning and Community Projects*, McGraw-Hill Education (India), New Delhi. 4. Wilson, G., *Practical Guide to Community Development Projects*, Routledge, London.
Reference books	1. NPTEL courses on Project-Based Learning and Social Innovation. 2. SWAYAM courses on community engagement and sustainability. 3. UN Sustainable Development Goals portal. 4. MyGov India and local civic body portals for community initiatives. 5. YouTube resources on design thinking, social innovation, and community service learning. 6. NGO and government field-action case studies related to sanitation, water, health, education, and environment.
Web links and Video Lectures (e-Resources)	1. NPTEL courses on Engineering Geology. 2. NPTEL courses on Soil Mechanics and Foundation Engineering. 3. Virtual Labs – Geotechnical Engineering Virtual Lab. 4. Geological Survey of India. 5. YouTube channels on civil engineering experiments. 6. American Society of Civil Engineers (ASCE) – Geotechnical resources and standards.

Teaching Learning Process:

The suggested TLP for Community / Societal Project is as follows;

Week / Phase	**Teaching–Learning Activity**	**Faculty Role**	**Student Activity**	**Output / Evidence**
1	Course introduction, objectives, ethics, conduct, and assessment briefing	Explain course scope, rules, rubrics, and expected deliverables	Understand course requirements and form teams	Team list, course plan
2	Community problem identification and topic selection	Guide topic framing and feasibility	Identify local issues through discussion and observation	Shortlisted project topic
3	Stakeholder interaction and preliminary survey	Demonstrate survey methods and stakeholder engagement	Collect initial data from community/users	Survey notes, interview record
4	Problem statement and objective formulation	Review and refine problem statement	Prepare problem statement, scope, and objectives	Approved problem statement
5	Literature/case study review and baseline analysis	Suggest relevant references and examples	Study existing solutions and compare approaches	Baseline analysis summary
6	Project planning and role assignment	Help teams organize tasks, timeline, and	Plan activities, divide roles, and prepare	Work plan / Gantt chart

		responsibilities	schedule	
7	Feasibility analysis and solution brainstorming	Check technical feasibility and practicality	Generate possible engineering solutions	Solution alternatives sheet
8	Selection of final solution and design approach	Review final concept and design logic	Finalize concept, methods, and expected outcome	Concept note / design outline
9	Data processing / calculations / sizing / mapping	Support computations and technical review	Analyze data, perform calculations, prepare maps/charts	Technical analysis sheet
10	Prototype / model / audit / DPR / app development	Monitor progress and correct technical issues	Develop the selected output	Working model / draft DPR / map / app
11	Testing, refinement, and implementation planning	Evaluate technical correctness and improvements	Test prototype or validate proposal with users	Test results / revised output
12	Field implementation / demonstration / awareness activity	Facilitate community interaction and documentation	Conduct implementation or demonstration	Photos, attendance, implementation record
13	Documentation of outcomes, feedback, and impact	Review report structure and completeness	Compile findings, stakeholder feedback, and observations	Draft report
14	Presentation preparation and viva practice	Conduct mock presentation and feedback	Prepare slides/poster and rehearse	Presentation deck
15	Final presentation, submission, and reflection	Evaluate performance using rubrics	Present project, submit report, reflect on learning	Final report, presentation, viva

Assessment structure:

A. Continuous Internal Evaluation (CIE) – 50 marks

- Students, in batches of 3–4, shall undertake at least one project (or a combination of two related activities) aiming, as far as possible, at a logical implemented or implementable outcome.
- CIE will be conducted by a departmental committee (HoD/nominee, guide and one senior faculty) using the following rubrics totalling 50 marks:

CIE pass requirement:

A student shall secure a minimum of 20 marks out of 50 in CIE to become eligible to appear for SEE.

- Students who fail to earn the required CIE marks may be given additional opportunities before closure of the semester; no re-doing of CIE is permitted after the end of the semester.

B. Semester End Examination (SEE) – 100 marks (scaled to 50)

- Examination duration: 2 hours.
- Maximum examination marks: 100 (entered as 100 in the VTU portal; the ITI-SMU module automatically scales 100 → 50 for result processing).
- The SEE shall be conducted batch-wise by a committee of three faculty: project guide, one faculty from the same department and one from a different department.

SEE pass requirement and overall passing rule:

- For a pass in SEE, a student shall secure minimum 35 marks out of 100.
- For declaration of a pass grade, the sum of CIE marks (out of 50) and scaled SEE marks (out of 50) shall be ≥ 40; otherwise, the student is awarded grade F (Fail).

CIE Rubric — Continuous Internal Evaluation (Total 50 marks):

Criterion	Weight (marks)	Excellent (Full marks)	Good	Fair	Needs Improvement
Problem identification & relevance to society/environment	8	Problem clearly identified with strong evidence of relevance and well-defined scope.	Relevant problem with clear scope and adequate evidence.	Problem defined but justification is weak.	Problem unclear or not relevant.
Formation of problem statement; engineering approach, innovation & feasibility	10	Precise statement; sound, innovative, feasible approach.	Adequate statement; feasible with minor gaps.	Partial statement; marginal feasibility.	Missing or infeasible.
Interaction with stakeholders; data collection, analysis & interpretation	8	Thorough engagement; comprehensive data and well-interpreted analysis.	Good engagement; adequate data and analysis.	Limited engagement; incomplete data and superficial analysis.	Little or no stakeholder contact; no data/analysis.
Project documentation; clarity, organization & problem-solving demonstrated	10	Complete, well-organized, analytical, and strong problem-solving.	Complete and clear with some analytical content.	Basic with omissions; problem-solving limited.	Missing/poorly organized; no clear problem-solving.
Communication & presentation skills	6	Confident, structured, and answers queries fully; visuals effective.	Clear and satisfactory; responds to most queries.	Acceptable but lacks clarity or confidence; weak responses.	Poor or absent; unable to respond.
Contribution & benefit to society (impact, sustainability)	8	Clear, demonstrable societal benefit and realistic sustainability path.	Benefit plausible; sustainability considered with minor gaps.	Limited or unclear benefit; sustainability weak.	No evident benefit or sustainability.

Notes for CIE rubric:

- Minimum CIE pass requirement: 20/50 to be eligible for SEE. [Use departmental committee (HoD/guide + senior faculty) to apply the rubric and record marks.]

SEE Rubric — Semester End Examination (Enter marks out of 100; scaled to 50 later):

Criterion	Weight (marks)	Excellent (Full marks)	Good	Fair	Needs Improvement
Problem identification & relevance to society/environment	16	Clearly articulated with strong evidence and context.	Clear with reasonable evidence.	Problem stated but evidence/context weak.	Poorly defined or irrelevant.
Formation of	20	Precise;	Technically	Basic; limited	No viable

problem statement; engineering approach, innovation & feasibility		demonstrates engineering depth, novelty and feasibility.	sound and feasible with minor limitations.	technical depth or feasibility concerns.	engineering approach or infeasible plan.
Interaction with stakeholders; data collection, analysis & interpretation	16	Excellent engagement; rigorous data collection and insightful analysis.	Good engagement and acceptable analysis.	Superficial data collection and limited analysis.	Inadequate or no data; poor analysis.
Project documentation; clarity, technical rigor & problem-solving demonstrated	20	Comprehensive, technically rigorous, and systematic.	Complete and technically correct with minor gaps.	Lacks technical depth or has notable omissions.	Missing key elements or technically incorrect.
Communication, presentation & viva-voce responses	12	Presents expertly, defends work persuasively and answers all queries correctly.	Good presentation and satisfactory answers to most queries.	Adequate but fails to answer some technical questions.	Poor presentation and unable to defend work.
Contribution & benefit to society; impact assessment & sustainability	16	Clear, evidence-based impact assessment with scaling recommendations.	Reasonable impact discussion and sustainability considerations.	Limited evaluation of impact or sustainability.	No coherent assessment of impact or sustainability.

SEE pass rule:

- Student must secure at least 35/100 in SEE itself to be eligible for pass consideration.
- Final passing is based on CIE (out of 50) + SEE (scaled to 50) >= 40. Otherwise, grade F (Fail) is awarded.

Suggested implementation notes (for BoS / exam committees):

- Use numerical scores from the rubric and keep brief evaluator comments for each criterion.
- For team projects: record individual contribution within the documentation and adjust individual marks using a peer-evaluation sheet or guide's assessment.
- Maintain evidence (field notes, photos, questionnaires, DPRs, reports) as annexures for SEE moderation.
- Use standardized score sheet (spreadsheet) mapping rubric items to columns for easy aggregation and archival.

- Awareness Campaign on Single-Use Plastic and E-Waste Management

SuggestedLearningResources:

TextBooks:

1. BennyJoseph,*EnvironmentalStudies*,TataMcGraw-Hill,2ndEdition.
2. R.Rajagopalan,*EnvironmentalStudies:FromCrisistoCure*,OxfordUniversityPress,2005.
3. ErachBharucha,*TextbookofEnvironmentalStudies*,UniversityPress,latesteditionasavailablein library.
4. M.P.PooniaandS.C.Sharma,*EnvironmentalStudies*,VikasPublishingHouse,latesteditionasavailable

ReferenceBooks:

1. R.Sivakumar,PrinciplesofEnvironmentalScienceandEngineering,CengageLearning,2ndEdition.
2. G.TylerMillerJr.,EnvironmentalScience:WorkingwiththeEarth,ThomsonBrooks/Cole,11thEdition.
3. PratibhaSingh,AnoopSingh,andPiyushMalaviya,TextBookofEnvironmentalandEcology,AcmeLearnin 1stEdition.
4. S.M.Prakash,EnvironmentalStudies,ElitePublishingHouse,Mangalore,3rdEdition,2018.

WeblinksandVideoLectures(e-Resources):

1. VTUe-LearningCentre:http://elearning.vtu.ac.in
2. VTUe-Resources/e-Content:http://elearning.vtu.ac.in/e-Res.php
3. VTUe-ShikshanaLectureVideos:http://elearning.vtu.ac.in/esk3.php
4. VTUConsortiumDigitalResources:https://access.vtuconsortium.com/msec
5. VTUe-LearningCentre:http://elearning.vtu.ac.in
6. VTUe-Resources/e-Content:http://elearning.vtu.ac.in/e-Res.php
7. VTUe-ShikshanaLectureVideos:http://elearning.vtu.ac.in/esk3.php
8. VTUConsortiumDigitalResources:https://access.vtuconsortium.com/msec

AssessmentStructure:

ContinuousInternalEvaluation(CIE)shallbeconductedbytheDepartmentalProjectReviewCommitteeconsisting of a Senior Professor, the Project Guide, and one additional faculty member nominated by the Head of the Department.SemesterEndEvaluation(SEE)shallbeconductedbyuniversity-appointedexaminers.Theevaluation shall be basedonrubrics designedtoassess the attainmentofNBA-defined graduate attributes,includingproblem analysis, investigation, design of solutions, communication, teamwork, and professionalism.

TheweightageofmarksforCIEandSEEis50% each.

Pass Criteria:A candidate shall secure a minimum of 40% of the total marks prescribed for Project Work, subject to the required minimum in Continuous Internal Evaluation and Semester End Evaluation as per VTU regulations.

Sample Rubrics for Campus water-quality and development of a water-conservation plan.

Criterion	Weight (%)	4 - Excellent	3 - Good	2 - Satisfactory	1 - Needs improvement
Problem definition and campus context	10	Clearly defines campus water issue, boundaries, water sources, and purpose.	Defines issue and context with minor gaps.	Basic problem stated, but scope is incomplete.	Vague or incorrect problem definition.
Water-quality data collection	15	Uses appropriate sampling points, methods, and frequency; data are well documented.	Methods are mostly appropriate with minor omissions.	Limited methods or incomplete documentation.	Weak or unclear data collection.
Water-quality parameters and analysis	20	Correctly analyzes key physical, chemical, and	Analyzes most parameters correctly with	Some parameters analyzed, but	Minimal or incorrect analysis.

Criterion	Weight (%)	4 - Excellent	3 - Good	2 - Satisfactory	1 - Needs improvement
		microbiological parameters and interprets results.	minor interpretation gaps.	interpretation is weak.	
Evidence and standards comparison	15	Compares results against relevant standards/guidelines and draws valid conclusions.	Compares most results with reasonable conclusions.	Comparison is partial or uneven.	No meaningful comparison with standards.
Diagnosis of issues and causes	10	Identifies likely causes of poor quality or water loss using evidence.	Identifies main causes with some support.	Causes are mentioned, but weakly supported.	Causes are speculative or absent.
Conservation plan objectives and measures	15	Plan includes clear goals, realistic measures, prioritization, and campus suitability.	Plan is relevant and mostly realistic.	Plan has some useful measures but limited prioritization.	Plan is generic or impractical.
Feasibility and implementation	10	Addresses resources, responsibilities, timeline, and implementation steps clearly.	Covers most implementation aspects.	Implementation is partial or underdeveloped.	Little or no implementation planning.
Cost, savings, and sustainability	5	Provides reasonable cost-benefit thinking and expected savings.	Includes some cost or savings discussion.	Limited financial/savings analysis.	No cost or savings consideration.
Presentation and documentation	0–10	Clear structure, tables/figures, references, and professional report quality.	Well organized with minor issues.	Acceptable but uneven formatting or writing.	Poorly organized and difficult to follow.

Design for Test

Course Code	1BVL409	Scheme	2025
Type of Course	PCC	Semester	IV
Teaching Hours/Week (L:T:P:S)	3:0:0	CIE Marks	50
Total Hours of Pedagogy (Theory and Lab Hours)	42: 0 :0 :48	SEE Marks	50
Credits	3	Total Marks	100
Examination type (SEE)	Theory	Exam Hours	3

Course outcome (Course Skill Set)

At the end of the course, the student will be able to:

1. Understand the importance of testing in VLSI circuits.
2. Analyze fault models and test generation techniques.
3. Apply Design for Testability (DFT) techniques such as scan design and Built-In Self-Test (BIST).
4. Understand modern testing challenges in deep-submicron VLSI circuits.
5. Analyze and evaluate the testability of digital VLSI circuits by applying fault modeling, ATPG, fault simulation, and scan-based Design for Testability (DFT) techniques

Module-1

INTRODUCTION: Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends Affecting Testing, Electrical Parametric Testing

VLSI TESTING PROCESS ANDTEST EQUIPMENT: How to Test Chips, Types of Testing, Automatic Test Equipment.

FAULT MODELING: Defects, Errors, and Faults, Functional Versus Structural Testing, Levels of Fault Models, A Glossary of Fault Models, Single Stuck-at Fault.

Textbook 1: Chapter 1, Chapter 2and Chapter 4

Number of Hours: 08

Module-2

LOGIC AND FAULT SIMULATION: Simulation for Design Verification, Simulation for Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-Value Simulation, Algorithms for Fault Simulation, Statistical Methods for Fault Simulation

TESTABILITY MEASURES: SCOAP Controllability and Observability, High-Level Testability Measures

Textbook 1: Chapter 5 and Chapter 6

Number of Hours: 08

Module-3

COMBINATIONAL CIRCUIT TEST GENERATION: Algorithms and Representations, Redundancy Identification (RID), Testing as a Global Problem, Significant Combinational ATPG Algorithms, Test Generation Systems, Test Compaction

SEQUENTIAL CIRCUIT TEST GENERATION: ATPG for Single-Clock Synchronous Circuits, Time-Frame Expansion Method, Simulation-Based Sequential Circuit ATPG

Textbook 1: Chapter 7 and Chapter 8

Number of Hours: 08

Module-4

MEMORY TEST: Memory Density and Defect Trends, Faults, Memory Test Levels, March Test Notation, Fault Modeling, Memory Testing

DIGITAL DFT AND SCAN DESIGN: Ad-Hoc DFT Methods, Partial-Scan Design, Variations of Scan

Textbook 1: Chapter 9 and Chapter 14

	Number of Hours: 09
	Module-5
	Built-In Self-Test (BIST) and Memory Testing: Built-In Self-Test architecture, Test pattern generation using LFSR, Signature analysis and MISR, Logic BIST, Memory testing and memory fault models, March tests for memory testing, Introduction to low-power testing and modern DFT trends Textbook 1: Chapter 15 Number of Hours: 09

Suggested Learning Resources: (Text Book/ Reference Book/ Manuals):

Textbooks:

1. M. L. Bushnell and V. D. Agrawal, Essentials of Electronic Testing for Digital, Memory and Mixed-SignalVLSI Circuits. Boston, MA, USA: Kluwer Academic Publishers, 2002.

Reference books / Manuals:

1. M. Abramovici, M. A. Breuer, and A. D. Friedman, Digital Systems Testing and Testable Design. New York, NY, USA: Computer Science Press, 1990.
2. Z. Navabi, Digital System Test and Testable Design: Using HDL Models and Architectures. Boston, MA, USA: Kluwer Academic Publishers, 1998.
1. L.-T. Wang, C.-W. Wu, and X. Wen, VLSI Test Principles and Architectures: Design for Testability. Burlington, MA, USA: Morgan Kaufmann, 2006.

Web links and Video Lectures (e-Resources):
https://nptel.ac.in/courses/106103116

Teaching-Learning Process (Innovative Delivery Methods):
The following are sample strategies that educators may adopt to enhance the effectiveness of the teaching-learning process and facilitate the achievement of course outcomes.

1. Case Study-Based Learning using real-world VLSI testing and DFT applications.
2. Problem-Based Learning for fault modeling, ATPG, and fault simulation techniques.
3. Simulation and Tool-Assisted Learning for visualization of testing and scan design concepts.
4. Collaborative Learning through technical seminars, group discussions, and literature reviews.

Assessment Structure for PCC Courses

Assessment Structure:
The assessment in each PCC course is divided equally between Continuous Internal Evaluation (CIE) and the Semester End Examination (SEE), with each carrying 50% weightage.

- To qualify and become eligible to appear for SEE, in the **CIE**, a student must score at least **40% of 50 marks**, i.e., **20 marks**.
- To pass the **SEE**, a student must score at least **35% of 50 marks**, i.e., **18 marks**.
- Notwithstanding the above, a student is considered to have **passed the course,** provided the combined total of **CIE and SEE** is at least **40 out of 100 marks**.

Continuous Comprehensive Assessments (CCA)+ Internal Assessment Test (IA) = Continuous Internal Evaluation CIE [25+25=50 marks].
A minimum of two Internal Assessment Tests(IA) shall be conducted, carrying a total of 25 marks.
In addition, Continuous Comprehensive Assessment (CCA) shall be conducted for a total of 25 marks.
It is recommended to include a maximum of two learning activities as part of the CCA to foster the holistic development of students. The suggested activities shall be

Sl. No.	Name of the Learning activity	Maximum Marks
1	Group seminar	15
2	Assignment (at RBL3, RBL4, or RBL5 levels)	10

Rubrics for assessment of these learning activities are provide in the Rubrics Section.

Suggested Learning Activities may include (but are not limited to):

- Course Project
- Case Study Presentation
- Programming Assignment
- Tool/Software Exploration
- Literature Review
- Open Book Test (preferably at RBL4 and RBL5 levels)
- GATE-based Aptitude Test
- Assignment (at RBL3, RBL4, or RBL5 levels)
- Any other relevant and innovative academic activity
- Use of MOOCs and Online Platforms

Suggested Innovative Delivery Methods may include (but are not limited to):

- Flipped Classroom
- Problem-Based Learning (PBL)
- Case-Based Teaching
- Simulation and Virtual Labs
- Partial Delivery of course by Industry expert/ industrial visits
- ICT-Enabled Teaching
- Role Playing

Term Work (TW) and Self Learning (SL) components in Number of Hours per semester		
Term work (includes assignments, seminars, micro projects, industrial visits, any other student activities etc.)		
Sl. No.	**Term Work (TW) Activity**	**Number of Hours / Semester**
1	Group seminar	24
2	Assignment	24
OR SL: Self Learning, MOOCs, spoken tutorials, online educational resources etc.		
Sl. No.	**Self-Learning (SL) Activity**	**Number of Hours / Semester**
1	NPTEL/MooCs course on Analog Electronics and Linear Integrated Circuits (faculty have to verify the dates that the NPTEL course is being offered)	48

Continuous Internal Evaluation (CIE)

(i) The CIE marks shall be decided based on internal tests and other outcome-based activities. The continuous internal evaluation shall be carried out by the teacher handling the course.
(ii) Out of 50 marks earmarked for CIE, 25 marks shall be assigned for internal tests. The first test shall be conducted after completing two modules of the syllabus and the second one after completing the remaining three modules.
(iii) The remaining 25 marks shall be assigned for Continuous Course Assessment (CCA), conducted as per the rubrics listed in the assessment section of the respective syllabus.
(iv) A student shall obtain a minimum of 40% marks or 20 out of 50 marks allotted to CIE to become eligible to appear for the SEE.

Passing requirement in SEE

For a pass in the Semester End Examination (SEE), a student shall secure a minimum of 35 marks out of 100.
For the declaration of a pass grade, the sum of the Continuous Internal Evaluation (CIE) marks (out of 50) marks and the SEE marks scaled down to 50 shall be greater than or equal to 40 marks.
If the total (CIE + SEE) is less than 40 marks, the student shall be awarded the grade 'F' (Fail).

Assessment Structure for IPCC Courses

Assessment Structure:

The assessment for each course is equally divided between Continuous Internal Evaluation (CIE) and the Semester End Examination (SEE), with each component carrying **50% weightage** (i.e., 50 marks each).
The CIE Theory component will be **25 marks** and CIE Practical component will be **25 marks**.

Questions from the practical component of the IPCC subject shall not appear in the theory SEE component.

CIE Theory component: It consists of IA tests for 25 marks. The CIE Practical component for continuous assessments will be for 15 marks through rubrics and for lab tests will be for 10 marks.

- To qualify and become eligible to appear for SEE, in the **CIE theory component**, a student must score at least **40% of 25 marks**, i.e., **10 marks**.
- To qualify and become eligible to appear for SEE, in the **CIE Practical component**, a student must secure **a minimum of 40% of 25 marks**, i.e., **10 marks**.
- To pass the **SEE**, a student must secure **a minimum of 35% of 50 marks**, i.e., **18 marks**.
- A student is deemed to have **successfully completed the course** if the **combined total of CIE and SEE is at least 40 out of 100 marks**.

CIE Practical Component:
The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report using a defined set of rubrics. Each experiment report can be evaluated for 30 marks. The summation of all the experiments marks to be scaled down to 15 marks.

The laboratory test (duration 03 hours) at the end of the last week of the semester /after completion of all the experiments (whichever is early) shall be conducted for 50 marks and scaled down to 10 marks. For laboratory test, the student is required to conduct one experiment each from both Part A and Part B.

Continuous Internal Evaluation (CIE)

(i)Theory component
The CIE marks of 25 shall be earmarked for two tests.
The first test shall be conducted after completing two modules of the syllabus and the second one after completing the rest three modules.
Each test shall be conducted for 25 marks. The average of the two tests scaled down to 25 marks shall constitute the test marks for a maximum of 25 marks.

(ii) Laboratory component
Out of 25 marks, 15 marks shall be assigned for assessment as per the rubrics listed. The remaining 10 marks shall be based on the practical test conducted by two Internal examiners appointed by the HoD. The allotment of marks shall be as per the rubrics defined.

(i) To qualify and become eligible to appear for the SEE of the IC/IPCC, a student shall secure at least 40 % of 25 marks, i.e., 10 marks, in the CIE theory component, and at least 40 % of 25 marks, i.e., 10 marks in the CIE Practical component.

Table – IPCCs Distribution of marks		
Component	**Description**	**Marks**
Allotment of marks for regular class work		
Ability in Conducting Experiments	Initiative, skill, safety practices, teamwork, and independent handling of equipment during regular lab sessions.	5 marks
Laboratory Record / Journal	Regular and neat maintenance of lab record, accuracy of results, and timely submission.	10 marks
	Subtotal	**15**
Allotment of marks for CIE practical test		
Laboratory Test / Experiment Performance	Ability to set up apparatus, follow procedure, take observations, and obtain correct results in the test experiment.	5 marks
Viva-Voce	Understanding of theory, concepts, and experimental procedure; ability to explain results and answer related questions.	5 marks
	Subtotal	**10**
	Total	**25**

Passing Requirements for SEE

For a pass in the Semester End Examination (SEE), a student shall secure a minimum of 35 marks out of 100. For the declaration of a pass grade, the sum of the Continuous Internal Evaluation (CIE) marks (out of 50) marks and the SEE marks scaled down to 50 shall be greater than or equal to 40 marks.
If the total (CIE + SEE) is less than 40 marks, the student shall be awarded the grade 'F' (Fail).

Assessment Structure for PCC-Lab and AEC Lab Courses

Assessment Structure:
The assessment for each course is equally divided between Continuous Internal Evaluation (CIE) and the Semester End Examination (SEE), with each component carrying **50% weightage** (i.e., 50 marks each).

The CIE marks awarded shall be based on the continuous evaluation of the laboratory report using a defined set of rubrics. Each experiment report can be evaluated for 30 marks. Total marks for the all report shall be scaled down to 30 marks. The laboratory test (duration 03 hours) at the end of the last week of the semester /after completion of all the experiments (whichever is early) shall be conducted for 50 marks and Marks scored shall be scaled down to 20 marks. Final average of marks for report and test shall be out of 50 marks.
For both CIE and SEE, the student is required to conduct one experiment each from both Part A and Part B.

- To qualify and become eligible to appear for SEE, in the **CIE component**, a student must secure **a minimum of 40% of 50 marks**, i.e., **20 marks**.
- To pass the **SEE component**, a student must secure **a minimum of 35% of 50 marks**, i.e., **18 marks**.
- A student is deemed to have **successfully completed the course** if the **combined total of CIE and SEE is at least 40 out of 100 marks**

Term Work (TW) and Self Learning (SL) components in Number of Hours per semester (2) **Faculty are suggested to offer only TW and not SL.**	
Suggested Term Work (TW) Activity	**Number of Hours / Semester**
New Experiment to practice on their own	2
OR	
Practice some of the regular experiments with different design requirements on their own	2

Suggested Rubrics for PCC Courses

Note: the rubrics provided below are a reference and can be modified as required.

Rubrics for Learning Activity1: Group seminar (at RBL3, RBL4, or RBL5 levels)

	Superior (5)	**Good (4)**	**Fair (3)**	**Needs Improvement (2)**	**Unacceptable (1)**
Subject Knowledge (CO/PO Mapping)	Demonstrates deep knowledge of the subject with clear explanation.	Demonstrates adequate knowledge of most topics with clear explanation.	Demonstrates only basic concepts with Superficial knowledge of topic.	Does not have clear understanding of the topic and lacks grasp of information.	No explanation.
Communication Skills (CO/PO Mapping)	Clearly audible by the entire audience.	Audible by most of the audience.	Audience has difficulty to hear and follow the presentation.	Minimal command on vocabulary with inaccurate pronunciation.	Communication characterized by minimal degree of grammatical accuracy with frequent errors.
Viva Voce (CO/PO Mapping)	Able to understand and answer all the questions confidently with relevant explanation.	Able to understand and answer some of the questions with relevant explanation.	Able to answer and explain few questions with less relevance.	Unable to answer most of the questions.	No proper answer.

Rubrics for Learning Activity2: Assignment (at RBL3, RBL4, or RBL5 levels)

	Superior (5)	**Good (4)**	**Fair (3)**	**Needs Improvement (2)**	**Unacceptable (1)**
Problem understanding (CO/PO Mapping)	Demonstrates complete understanding of the question and assumptions.	Demonstrates good understanding with only minor omissions.	Demonstrates partial understanding with only some unclear assumptions.	Shows limited understanding of the questions.	Weak understanding of the question.
Correct application of	Applies all relevant	Applies most of the	Applies a few relevant	Frequent incorrect	Major errors in application of

theory and correctness of solution (CO/PO Mapping)	engineering principles, laws, and analytical methods correctly.	relevant engineering principles, laws, and analytical methods correctly.	engineering principles, laws, and analytical methods correctly	application of engineering principles and analytical methods.	engineering principles and analytical methods.

Suggested Rubrics for IPCC courses

Rubrics for CIE Lab test (50marks – later scaled down to 10marks):

Performance Indicators	Excellent	Very Good	Good	Satisfactory
Fundamental Knowledge (10) (PO1)	The student has in depth knowledge of the topics related to the course (9-10)	Student has good knowledge of some of the topics related to course (7-9)	Student is capable of narrating the answer but not capable to show in depth knowledge (6-7)	Student has not understood the concepts clearly (5-6)
Design Of Experiment (15) (PO2, PO3, PO5)	Student is capable of discussing more than one design for his/her problem statement and capable of proving the best suitable design with proper reason (14-15)	Student is capable of discussing few designs for his/her problem statement but not capable of selecting best (12-14)	Student is capable of discussing single design with its merits and de-merits (10-12)	Student is capable of explaining the design (9-10)
Implementation with appropriate HW/SW (15) (PO3 , PO4, PO5, PO8)	Student is capable of implementing the design with best suitable algorithm/HW considering optimal solution explanation. (14-15)	Student is capable of implementing the design with best suitable algorithm/HW and should be capable of explaining it (12-14)	Student is capable of implementing the algorithm/HW with some explanation. (10-12)	Student is just capable of implementing the algorithm/HW , and unsatisfactory explanation. (8-10)
Result &Analysis (10) (PO4, PO5, PO9)	Student is able to run the program on various cases and compare the result with proper analysis. (10)	Student will be able to run the program for most of the cases and provide proper analysis. (7-9)	Student will be able to run the code for few cases and provide analysis for a few cases. (5-7)	Student will be able to run the program for a simple case but not able to analyze the output. (3-5)

Rubrics for CIE – Continuous assessment (30marks – later scaled to 15 marks):

	Superior	**Good**	**Needs Significant Improvement**
Fundamental Knowledge about each experiment (6) (PO1)	The student has in depth knowledge of the topics (4-6)	Student has good knowledge of some of the topics (4)	Student has not understood the concepts clearly (2)
Design Of Experiment (8) (PO2, PO3, PO5)	Student capable of discussing more than one design for problem statement and capable of proving the best suitable design with proper reason (6-8)	Student capable of discussing few designs for problem statement , not capable of selecting best design (6)	Student struggles to explain the design (2-4)
Implementation (10) (PO3, PO4, PO5, PO8)	Student capable of implementing the design (either alone or in a team) with best suitable algorithm considering optimal solution. (8-10)	Student capable of implementing design (either alone or in a team) with best suitable algorithm and capable of explaining it (8)	Student struggle to implement the design (either alone or in a team) . (2-8)
Quality of Record and Observation write up (6) (PO8,PO5,PO9)	Lab record & observation book are well-organized, with clear sections (4-6)	Lab record/ observation book are organized,, but some sections are not well-defined. (4)	The lab record/ observation book poorly organized, with missing or unclear sections. (2-4)

Note: Term Work and Self Learning components are not included in the assessment. IPCC already has theory and lab assessment in CIE, including a TW/SL component may cause burden on students. Faculty may give 50 hours of SL, however this may not be included for assessment.

Suggested Rubrics for PCC-Lab and AEC Lab Courses

Rubrics for CIE – Continuous Lab assessment (30 marks):

	Superior	**Good**	**Fair**	**Needs Improvement**	**Unacceptable**
Fundamental Knowledge about each experiment (4) (PO1)	The student has in depth knowledge of the topics (4)	Student has good knowledge of some of the topics (3)	Student is capable of narrating the answer but not capable to show in depth knowledge (2)	Student has not understood the concepts clearly (1-2)	Student barely has fundamental knowledge (1)
Design Of Experiment (5) (PO2, PO3, PO5)	Student is capable of discussing more than one design for his/her problem statement and capable of proving the best suitable design with proper reason (5)	Student is capable of discussing few designs for his/her problem statement but not capable of selecting best (4-5)	Student is capable of discussing single design with its merits and de-merits (3-4)	Student struggles to explain the design (2-3)	Student has very weak understanding of the design (1-2)
Implementation (8) (PO3, PO4, PO5, PO8)	Student is capable of implementing the design with best suitable algorithm considering optimal solution. (7-8)	Student is capable of implementing the design with best suitable algorithm and should be capable of explaining it (5-6)	Student is capable of implementing the design with proper explanation. (3-4)	Student is capable of implementing the design. (1-2)	Implementation has major errors (1)
Result &Analysis (5) (PO4, PO5, PO9)	Student is able to execute the program/experiment on various cases and compare the result with proper analysis. (4-5)	Student will be able to execute the program/experiment for all the cases. (3-4)	Student will be able to execute the program/experiment for few cases and analyze the output. (2-3)	Student will be able to execute the program/experiment but not able to analyze the output. (1-2)	Program/Experiment execution has important errors and student is incapable to explaining any of them (1)
Quality of Record and	The lab record & observation book	The lab record	The lab record & observation	The lab record	Student has not submitted lab

Observation write up (8) (PO8,PO9)	are well-organized, with clear sections (e.g., Introduction, Method, Results, Conclusion). l (7-8)	&observation book are organized, with clear sections, but some sections are not well-defined. (5-6)	book lack clear organization or structure. Some sections are unclear or incomplete. (3-4)	&observation book are poorly organized, with missing or unclear sections. (1-2)	record or observation book (0)

Rubrics for CIE Lab Test (50 marks, later scaled to 20 marks) and SEE:

Performance Indicators	Excellent	Very Good	Good	Satisfactory
Fundamental Knowledge (5) (PO1)	The student has in depth knowledge of the topics related to the course (4)	Student has good knowledge of some of the topics related to course (3)	Student is capable of narrating the answer but not capable to show in depth knowledge (2)	Student has not understood the concepts clearly (1)
Design Of Experiment (5) (PO2, PO3, PO5)	Student is capable of discussing more than one design for his/her problem statement and capable of proving the best suitable design with proper reason (5)	Student is capable of discussing few designs for his/her problem statement but not capable of selecting best (4)	Student is capable of discussing single design with its merits and de-merits (3)	Student is capable of explaining the design (1-2)
Implementation with appropriate HW/SW (5) (PO3 , PO4, PO5, PO8)	Student is capable of implementing the design with best suitable algorithm/HW considering optimal solution explanation. (7-8)	Student is capable of implementing the design with best suitable algorithm/HW and should be capable of explaining it (5-6)	Student is capable of implementing the algorithm/HW with some explanation. (3-4)	Student is just capable of implementing the algorithm/HW, and unsatisfactory explanation. (1-2)
Result &Analysis (5) (PO4, PO5, PO9)	Student is able to run the program on various cases and compare the result with proper analysis. (5)	Student will be able to run the program for most of the cases and provide proper analysis. (4)	Student will be able to run the code for few cases and provide analysis for a few cases. (3)	Student will be able to run the program for a simple case but not able to analyze the output. (1-2)