6th Semester BE (CBCS) Open Electives Model Question Papers

15EC661

Visvesvaraya Technological University, Belagavi

MODEL QUESTION PAPER

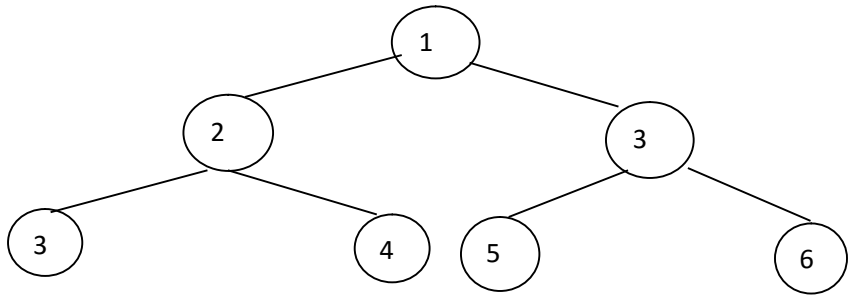
6th Semester, B.E (CBCS) – Open Elective

Course: 15EC661- DATA STRUCTURE USING C++

Time: 3 Hours **Max. Marks: 80**

Note: (i) Answer Five full questions selecting any one full question from each Module.
(ii) Question on a topic of a Module may appear in either its 1st or/and 2nd question.

		Module-1	Marks
1	a	Discuss template functions in C++. Write template function to swap two parameters with arguments being two integers or two float values	5
	b	Explain how "**new**" operator is used for dynamic memory allocation in C++. Write a function to allocate memory dynamically to a two dimensional array.	5
	c	Briefly explain Recursion. Write recursive function in C++ to find factorial of a number	6
		OR	
2	a	Write ADT specification for Linear Lists.	7
	b	Write a C++ program to insert a given element at the indexth position.	6
	c	Write destructors for chain.	3
		Module-2	
3	a	Write a C++ program to add two matrices.	6
	b	Explain how parenthesis matching is carried out using stacks. Write C++function for the same.	10
		OR	
4	a	Write a C++ program to transpose a given Sparse matrix.	10
	b	Write C++ abstract class for Stacks.	6
		Module-3	
5	a	What is the advantage of circular queue over simple queue? With neat diagrams explain how array length can be doubled in a circular queue	9
	b	Explain how overflow condition is eliminated using hashing with chains. Compare with the Linear probing method.	7
		OR	
6	a	Discuss problem description and solution strategy for rail road car rearrangement	8
	b	Write short notes on Hashing	8
		Module-4	

7	a	Draw the binary expression trees corresponding to each of the following expressions. 1. ((-A)+(X+Y))/((+B)*(C*A)) 2. (A+B)/(C-D)+E+G*H/A	6
	b	Write functions for 1. Pre-order traversal of a Binary tree 2. Determining height of the binary tree	10
		OR	
8	a	Write short notes on Linked representation of binary trees	10
	b	Write preorder, inorder and postorder traversals for the tree given below.  	6
		Module-5	
9	a	Explain the operations -- insertion and deletion for Max Heaps	8
	b	Write a function to search for an element in Binary Search Trees.	8
		OR	
10	a	Write a function for Heap-Sort and explain Heap-Sort with neat diagrams.	10
	b	Discuss Binary Search Trees with duplicates	6

Note: In the updated syllabus, the publisher of the prescribed text book has been changed to 'Universities Press', instead of 'Mc. Graw Hill.'

Visvesvaraya Technological University, Belagavi

MODEL QUESTION PAPER

6th Semester, B.E (CBCS) - Open Elective

Course: 15EC662–POWER ELECTRONICS

Time: 3 Hours **Max Marks: 80**

Note: (i) Answer Five full questions selecting any one full question from each Module.
(ii) Question on a topic of a Module may appear in either its 1st or 2nd question.

		Module 1	
1	(a)	Draw the circuit diagram, and control characteristics of GTO,MCT and TRAIC.	6
	(b)	What is a converter? How are power converters classified? Explain briefly.	6
	(c)	With the help of relevant equations and waveforms explain steady state characteristics of power BJT.	4
		OR	
2	(a)	Explain the switching characteristics of power MOSFET with neat diagram.	6
	(b)	What is an IGBT? Compare IGBT with BJT and MOSFET.	6
	(c)	Give the definition of power electronics. Explain the relationship of power electronics to power electronics and control. Mention two applications of power electronics.	4
		Module 2	
3	(a)	Explain the turn–on mechanism of a thyristor using two transistor analogy and derive an expression for the anode current in terms of transistor parameters.	8
	(b)	Explain different operation regions of SCR gate characteristics.	4
	(c)	Explain dynamic switching characteristics of SCR.	4
		OR	
4	(a)	With a circuit diagram and waveform explain RC-triggering circuit.	5
	(b)	Differentiate natural and forced commutation? Briefly explain different types of forced commutation.	6
	(c)	Sketch the V-I characteristics of an SCR and explain a) Latching current b) Holding current c) Break over voltage.	5
		Module 3	
5	(a)	With a neat diagram and waveform, explain the principle of single phase full converter with a purely resistive load. Derive the expression for output voltage and RMS output voltage.	6
	(b)	What are the advantages of single phase dual convertor operation with circulating current?	5
	(c)	For a single phase fully has RL load having L=6.5 mH,R=0.5 ohms and E=10v. The input voltage is Vs= 120v(rms) at 60Hz. Dertermine a)load current at wt=α=60^o, b) average thyristor current I_A c)rms thyristor current I_R d)rms output current I_{rms} e) average output current $I_{dc.}$	5
		OR	

6	(a)	Explain the operation of single phase AC voltage controllerfor inductive load with the help of circuit diagram and waveform.	6
	(b)	Derive an expression for the rms value of the output voltage of the bidirectional AC voltage controller, employing ON-OFF control.	6
	(b)	A single–phase half wave AC voltage controller has a resistive load of R= 5Ω and input voltage Vs=120v,60Hz. The delay angle of thyristor is $\alpha = \pi/3$. Find the i) RMS value of output voltage ii) input power factor iii) average input current.	4
Module 4			
7	(a)	With relevant equations and waveform explain step-down convertor with R-L load.	6
	(b)	Explain step –up converter with resistive load.	5
	(c)	The Buck Regulator has an input voltage of V_S= 12v. The required average output voltage is V_a= 5v at R= 500 Ω and the peak to peak output ripple voltage is 20mv. The switching frequency is 25kHz. If the peak to peak ripple current of the inductor is limited to 0.8A. Determine a) Duty cycle k b) filter inductance L and capacitance c) critical values of L and C.	5
OR			
8	(a)	Briefly explain how DC convertors are classified depending on the directions of current and voltage flows.	6
	(b)	With circuit diagram and waveform explain Buck Regulator.	5
	(c)	A boost regulator has an input voltage of Vs=5v. The average ouput voltage Va=15v and the average load current Ia= 0.5 A. The switching frequency is 25kHz.If L= 150µH and C=220 µF, determine duty cycle, ripple current of inductor, peak current of inductor, ripple voltage of filter capacitor and critical values of L and C.	5
Module 5			
9	(a)	Explain the performance parameters of inverters.	4
	(b)	Explain single phase full-bridge inverter with necessary circuit diagram and waveforms. Derive the equation for RMS output voltage.	6
	(c)	Explain the working of transistorized current source inverter.	6
OR			
10	(a)	Explain principle of working of variable DC link inverter. Also mention advantages and disadvantages.	6
	(c)	Explain operation of single phase half-bridge inverter and derive the output voltage equation of the inverter.	6
	(b)	The single phase full bridge inverter has a resistive load of R=24 ohms and the DC input voltage of Vs= 48 v. Determine i) RMS output voltage at the fundamental frequency. ii) Output power iii) Peak and average currents of each transistor.	4

15EC663

Visvesvaraya Technological University, Belagavi

MODEL QUESTION PAPER

6th Semester, B.E (CBCS) – Open Elective

Course: 15EC663 – DIGITAL SYSTEM DESIGN USING VERILOG

Time: 3 Hours **Max. Marks: 80**

Note: (i) Answer Five full questions selecting any one full question from each Module.
(ii) Question on a topic of a Module may appear in either its 1st or/and 2nd question.

		Module-1	**Marks**
1	a	What is Digital system? Explain how the Digital circuits are evolved over the times.	5
	b	Define the terms setup time, hold time and clock-to-output time of a flip-flop and what are the constraints imposed by these parameters on the circuit operations?	5
	c	Develop a Verilog model for a 7-segment decoder. Include an additional input, blank, that overrides the BCD input and causes all segments not to be lit.	6
		OR	
2	a	Develop a test bench model for the 3:8 decoder.	6
	b	With an example show the distinction between a Moore and Mealy finite-state machine and also draw the corresponding state transition diagram	10
		Module-2	
3	a	Explain Bidirectional tristate data connections . Design a 64K× 8-bit composite memory using four 16K × 8-bit components using Bidirectional tristate data connections.	8
	b	Develop a Verilog model of the FIFO, which can store up to 256 data items of 16 bits each using 256×16 bit dual port SSRAM for the data storage. The FIFO should provide status outputs *empty* and *full* to indicate the empty and full status of FIFO and FIFO will not be read when it is empty nor be written when it is full and that the write and the read port share a common clock.	8
		OR	
4	a	Design a circuit that computes the function $y=c_i \times x^2$, where x is a binary-coded input value and c_i is a coefficient stored in a flow-through SSRAM. x, c_i and y are all signed fixed-point values with 8 pre binary-point and 12 post-binary-point bits. The index i is also an input to the circuit, encoded as a 12-bit unsigned integer. Values for x and i arrive at the input during the cycle when a control input, start, is 1. The circuit should minimize area by using single multiplier to multiply c_i by x and then by x again.	8
	b	What is a common cause of soft errors in DRAMs? Compute the 12-bit ECC word corresponding to the 8-bit data word 01100001.	8
		Module-3	
	a	Explain different types of PCB design. How fast does a signal change propagate along a typical PCB trace?	8

5	b	Explain the concept differential signaling .How does differential signaling improve noise immunity?	8
		OR	
6	a	Explain signal integrity interconnection issue in PCB design.	6
	b	What is the benefit of allowing a PLD in a system to be reprogrammed?	5
	c	What distinguishes a platform FPGA from a simple FPGA?	5
		Module-4	
7	a	Explain Digital-to-Analog Converters using R/2R ladder DAC.	6
	b	Write a Verilog assignment that represents a tri-state bus driver for an 8-bit bus.	6
	c	How does the processor determine where to resume program execution on completion of handling an interrupt?	4
		OR	
8	a	Explain any four serial interface standards.	8
	b	Design and develop the Verilog code for an input controller that has 8-bit binary-coded input from a sensor. The value can be read from an 8-bit input register. The controller should interrupt the embedded Gumnut core when the input value changes. The controller is the only interrupt source in the system.	8
		Module-5	
9	a	Explain the design flow of hardware/software co-design.	10
	b	What aspects of the design flow does a verification plan cover?	6
		OR	
10	a	Explain Built-in self test (BIST) techniques.	8
	b	Explain the terms scan design and boundary scan	8