

Visvesvaraya Technological University, Belagavi

MODEL QUESTION PAPER

3rd Semester, B.E (CBCS 2017-18 Scheme) EC/TC

Course: 17EC34- Digital Electronics, **Set no. 1**

Time: 3 Hours

Max. Marks: 100

**Note: (i) Answer Five full questions selecting any one full question from each Module.
(ii) Question on a topic of a Module may appear in either its 1st or/and 2nd question.**

Module-1

- 1 a. Design a combinational logic circuit which takes two, 2-bit binary numbers as its input and generates an output equal to 1, when the sum of the two number is odd. **(06 Marks)**
b. Convert the given boolean function into
i) $f(a,b,c) = (a+b)(b+c)$ minterm canonical form
ii) $f(a,b,c) = a+ac(b+c)$ maxterm canonical form **(06 Marks)**
c. Find all the prime implicants and essential prime implicants for the given function using k-map method. $f(a,b,c,d) = \sum m(0,3,6,7,8,9,10) + dc(2,5,11,12,15)$ **(08 Marks)**

OR

- 2 a. Define the following terms:
Minterm, Maxterm, CSOP, CPOS, POS. **(05 Marks)**
b. Simplify the given function using K-map method.
 $f(a,b,c,d,e) = \sum m(3,7,11,12,13,14,15,16,18) + dc((24,25,26,27,28,29,30,31)$ **(05 Marks)**
c. Find the prime implicants and essential prime implicants using Quine-McCusky method and verify the result using k-map.
 $F(a,b,c,d) = \sum m(7,9,12,13,14,15) + dc(4,11)$ **(10 Marks)**

Module-2

- 3 a. What is magnitude comparator? Design a two bit digital comparator by writing TT, relevant expression and logic diagram. **(10 Marks)**
b. Implement the following functions using 3:8 decoder(IC-74138)
i) $f_1(a,b,c,d) = \pi M(2,4,5,7,9,10,13,14)$
ii) $f_2(a,b,c,d) = \sum m(1,3,5,8,12,14,15)$ **(10 Marks)**

OR

- 4 a. Explain Carry look ahead adder with neat diagram and relevant expressions. And also briefly explain how it is better than parallel adder. **(10 Marks)**
b. Implement $f(a,b,c,d) = \sum m(0,1,5,6,10,12,14,15)$ using
i) 8:1 MUX with a,b,c as select lines.
ii) 4:1 MUX with a, b as select lines. **(10 Marks)**

Module-3

- 5 a. What is flip-flop. Discuss working principle of SR flip-flop with its TT. Also highlight role of SR latch in switch debouncer circuit. **(10 Marks)**

b. What is significance of edge triggering? Explain working of negative edge triggered D flip-flop with their functional table and waveforms. **(10 Marks)**

1 Of 2

OR

6 a. Explain the working of Master-Slave JK flip-flop with functional table and timing diagram. Show how race around condition is overcome. **(12 Marks)**

b. Obtain characteristic equation for the following flip-flops.

i) JK f/f ii) SR f/f

(08 Marks)

Module-4

7 a. Explain Universal Shift Register with the help of logic diagram, mode control table and symbol. **(10 Marks)**

b. Explain the working of 4-bit Johnson counter using positive edge triggered D flip-flop, also draw the timing diagram. What is the modulus of this counter? **(10 Marks)**

OR

8 a. Design a Synchronous Mod-6 counter using JK flip-flop. **(10 Marks)**

b. Explain the working of 4-bit binary ripple up counter using negative edge triggered flip-flop. Also draw the timing diagram. **(10 Marks)**

Module-5

9 a. Explain Mealy and Moore models of clocked synchronous sequential circuits with necessary block diagrams. **(10 Marks)**

b. Design a cyclic Mod-8 synchronous binary counter using JK flip-flop. Give state diagram, transition table and excitation table. **(10 Marks)**

OR

10 a. Construct mealy state diagram that will detect input sequence 10110, when input pattern is detected, z is asserted high. Give state diagram for each state. **(10 Marks)**

b. Analyze the following sequential circuit shown in Fig Q10(b), and obtain

i) Flip-flop input and output equation

ii) Transition equation

iii) Transition table

iv) State table

v) Draw the state diagram.

(10 Marks)

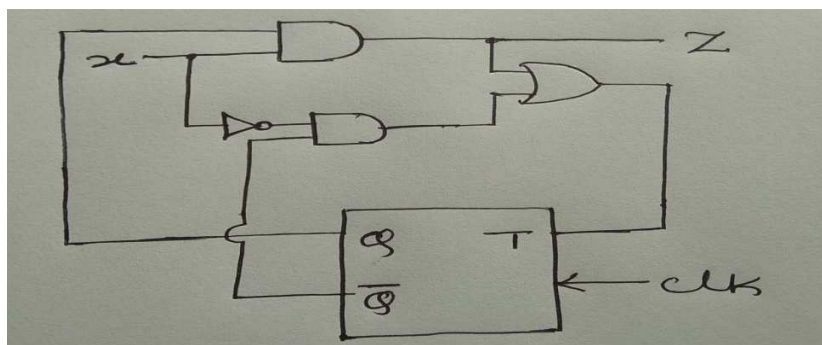


Fig Q10(b)