Model Question Paper

Third Semester B.E. (CBCS) Examination
Digital System Design(17EE35)

Time: 3 Hrs Max.Marks: 100

Note: Answer any FIVE full questions, choosing at least ONE question from each module

Module-I

1. a. Explain canonical minterm & canonical maxterm form with example. **(06 Marks)**
   b. Reduce the following function using K-map technique and implement using basic gates.
      i) $F(a,b,c,d) = \Sigma m(0,2,5,7,8,10,13,15) + \Sigma d(1,4,11,14)$
      ii) $F(a,b,c,d) = \Pi(4,5,6,7,8,12,13) + \Pi d(1,15)$ **(08 Marks)**
   c. Design a combinational logic circuit with three input variables that will produce logic 1 output when more than one input variables are logic 1. **(06 Marks)**

2. a. Find the reduced POS form of the following equation & also implement using NAND logic. $F(a,b,c,d) = \Sigma m(4,6,8,9,10,12,13,14) + \Sigma d(0,2,5)$ **(08 Marks)**
   b. Find all prime implicants of the function using a Quine-McCluskey method. $F(a,b,c,d) = \Sigma m(1,2,3,5,9,12,14,15) + \Sigma d(4,8,11)$ **(12 Marks)**

Module-II

3. a. Implement the following multiple output function using one 74138 & external gates. $F1(a,b,c) = \Sigma m(1,4,5,7)$ & $F2(a,b,c) = \Pi M(2,3,6,7)$ **(06 Marks)**
   b. Write the compressed truth table for a 4 to 2 line priority encoder with a valid output where the highest priority is given to highest bit position and simplify the same using K-map. Design the logic circuit as well. **(07 Marks)**
   c. Design a full adder by constructing the truth table and simplify the output equations. **(07 Marks)**

4. a. Design one-bit comparator circuit, represent truth table, k-maps and logic diagram. **(06 Marks)**
   b. Implement 4-bit parallel adder/subtractor using 4-full adders blocks. Explain its operation, if Cin = 0 the circuit should act as adder and if Cin = 1 the circuit act as subtractor. **(08 Marks)**
   c. Implement the function using 8:1 MUX, $F(a,b,c,d) = \Sigma m(0,1,3,4,7,10,11,14,15)$ **(06 Marks)**

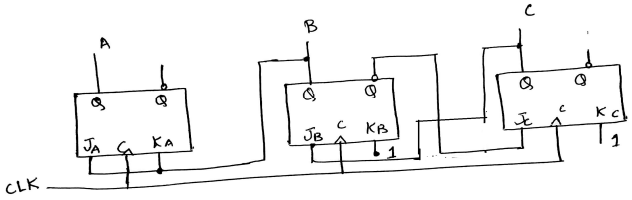
Module-III

5. a. With logic diagram and truth table explain the operation of a SR latch. **(06 Marks)**
   b. Explain the working of a master-slave JK flip-flop with the help of logic diagram, function table, logic symbol and timing diagram. **(08 Marks)**
   c. With a neat logic diagram, explain the operation of the 4-bit SISO unidirectional shift resister. **(06 Marks)**

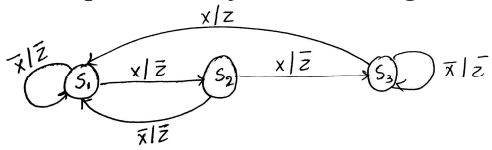
6. a. Obtain the characteristic equation for D and T flip-flop. **(04 Marks)**
   b. Explain the working principle of four bit binary ripple counter, with the help of logic diagram and timing diagram . **(06 Marks)**
   c. Design a synchronous counter Mod-6 Using clocked D flip-flops. **(10 Marks)**

Module-IV

7. a. Design a synchronous counter to sequence 0,1,4,6,7,5,0…. Using clocked D flip-flops. **(10 Marks)**
   b. Analyze the following synchronous sequential circuit. **(10 Marks)**



8. a. Explain Mealy and Moore model with neat block diagram. **(08 Marks)**
   b. Realize the system represented by the following state diagram using D flip-flop.



(12 Marks)

Module-V

9. a. Explain brief history of HDL and Structure of HDL module. **(08 Marks)**
   b. List the various styles/types of descriptions. Explain VHDL Behavioral description with example code. **(12 Marks)**

10. a. Mention types of VHDL operators. Explain in detail any one operator. **(06 Marks)**
    b. Compare VHDL and verilog. **(08 Marks)**
    c. Explain the signal declaration and signal assignment statements with relevant example **(06 Marks)**