CBCS Scheme

USN | | | | | | | | | | |

17EE35

Third Semester B.E. Degree Examination : Model Question Paper

DIGITAL SYSTEM DESIGN

Time: 3 hrs. Max. marks: 100

Note: Answer any FIVE full questions, choosing one full question from each module.

Module-1

1 a. Minimize the following expression in SOP form using K-Map

(i) $f(P,Q,R,S) = \Sigma m(0,1,4,8,9,10)$+**d(2,11)**

(ii) f(a,b,c,d)=Σm(1,2,3,5,6,7,11,12,13,14,15) draw the logic diagram using AOI logic (08 Marks)

b. What are prime implicant and essential prime implicant? simplify the Boolean function using K-Map and identify them f(a,b,c,d)=Σm(0,1,2,5,6,7,8,9,10,13,14,15) (06 Marks)

c. Design a combinational logic circuit to check for even parity of three bits (06 Marks)

OR

2 a. Minimize the following expression in POS form using K-Map

(i) $f(A,B,C,D) = \Pi M(0,2,3,8,9,12,13,15)$

(ii) f(A,B,C,D)=ΣM(1,3,7,11,15)+Σd(0,2,5) (06 Marks)

b. Simplify the Boolean expression using K-Map

f(A,B,C,D,E)=Σm(0,2,4,6,8,16,18,20,22,24,26,28,30)+d(3,7,11,15,19,23,27,31) (06 Marks)

c. Using Quine McCluskey method & PI reduction table, determine the minimal SOP expression for the following using decimal notation f=Σm(1,4,7,9,12,14)+Σdc(2,13) (08 Marks)

Module-2

3 a. Construct an 16:1 MUX using 4:1 and 2:1 multiplexers and hence analyze using truth table (08 Marks)

b. Using active high output 3:8 line decoder, implement the following functions

f1(A,B,C,D)=Σm(0,1,2,5,7,11,15)

f2(A,B,C,D)=Πm(1,3,4,11,13,14) (06 Marks)

c. Design a carry look ahead 4-bit parallel adder. Show that the time for addition is independent of the length of operands (06 Marks)

OR

4 a. Write the compressed truth table for a 4 to 2 line priority encoder with a valid output and simplify the same using K-Map. Design the logic circuit for the same. (08 Marks)

b. With the aid of block diagram clearly distinguish between a decoder and encoder (04 Marks)

c. With the help of truth table and simplification using K-Map, design a 2 bit comparator using basic gates (08 Marks)

Module-3

5. a. Compare between Combinational and Sequential circuits (04 Marks)

b. With the help of logic diagram, explain working of Master slave JK Flip-Flop along with waveforms. Explain race around condition. How is it eliminated? (08 Marks)

c. With the help of logic diagram, explain the 4 bit universal shift register using D flip-flops and 4:1 MUX (08 Marks)

OR

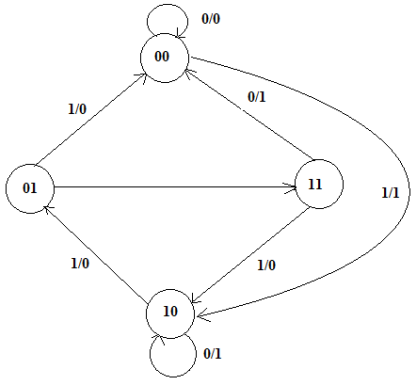
6 a. Write the truth table of the SR, JK, D & T flip-flops (08 Marks)

b Design a Mod 6 synchronous counter using D flip-flop and T flip-flop. (12 Marks)

Module-4

7 a. Explain Mealy and Moore model of a clocked synchronous sequential network. (06 Marks)

b. Construct a sequential logic circuit with single input and single output by obtaining the state and excitation table for the given state diagram using JK FF (08 Marks)



c. Construct a state diagram for synchronous decade UP/DOWN counter. The mode control; 'M' decides the pattern of counting operation. When M=0 Counter counts UP and when M=1, counter counts DOWN. When counter reaches terminal count Y=1 (for UP count) and Z=1 (for DOWN count). Label the state diagram in M/YZ mode. (06 Marks)

OR

8 a. Define state, present state, state diagram and state table (06 Marks)

b. Construct Moore and Mealy state diagram that will detect input sequence 10110, when input pattern is detected, z is asserted high. Give state diagram for each state. (08 Marks)

c. Design a synchronous counter using JK flip-flops to count the sequence 0,1,2,4,5,6,0,1,2 use static diagram and state table (06 Marks)

Module-5

9 a. Explain the various data types available in VHDL (06 Marks)

b. Write VHDL code for 2x1Multiplexer. (06 Marks)

c. Tabulate Rotate operators used in HDL with example operand A=1110 (08 Marks)

OR

10 a. Explain different logical operators used in HDLs (08 Marks)

b. Explain the behavioral type with half adder example in VHDL. (06 Marks)

c. Compare VHDL with Verilog (06 Marks)

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