Model Question Paper-1/2 with effect from 2022-23 (CBCS Scheme)

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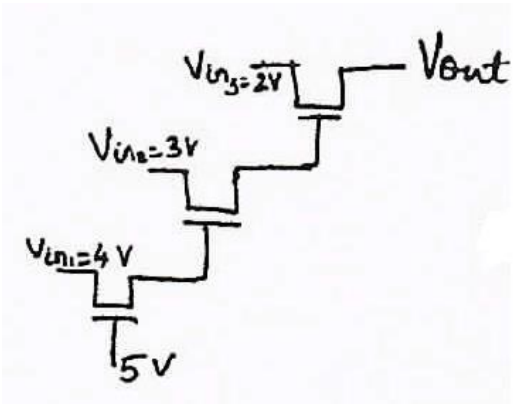
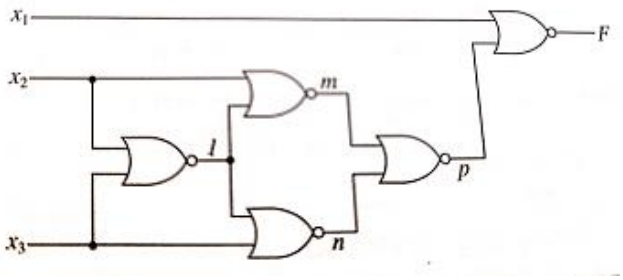
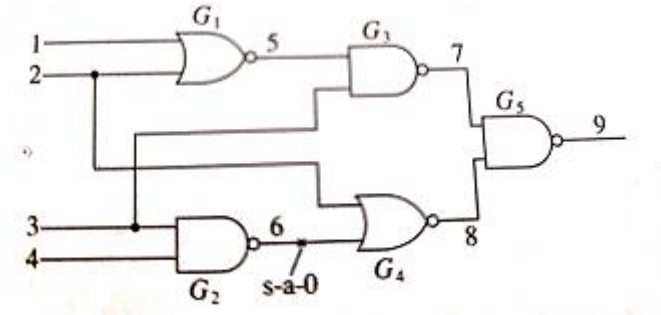
Sixth Semester B.E. Degree Examination

VLSI Design and Testing (21EC63)

TIME: 03 Hours **Max. Marks: 100**

Note: 01. Answer any **FIVE** full questions, choosing at least **ONE** question from each **MODULE**.

		Module -1	*Bloom's Taxonomy Level	Marks
Q.01	a	With necessary circuit diagram explain the operation of tristate inverter. Also realize 2:1 mux using tristate inverter.	L3	08
	b	Realize the CMOS gate for the following function $Y = \overline{A(B + C) + DE}$	L3	05
	c	Implement a D flipflop using transmission gate and explain its operation with necessary timing diagram	L3	07
		OR		
Q.02	a	Draw the circuit diagram of a CMOS inverter and with the help of its transfer characteristics, explain various regions of operation and derive the V_{out} equation for Region C.	L3	10
	b	Derive the equation for drain current of a MOSFET in non-saturated and saturated region of operation.	L3	06
	c	Compute the output voltage V_{out} in the pass transistor circuit shown in Fig.1  Fig.1	L3	04
		Module-2		
Q. 03	a	Explain the various steps in CMOS n-well process with necessary diagrams.	L3	10
	b	With neat diagrams, explain the lambda design rules for wires, contact cuts and Transistors.	L3	06
	c	Draw the stick diagram for the function $Y = \overline{ABC + D}$	L3	04
		OR		
Q.04	a	Construct necessary equivalent circuits using RC delay model to compute the propagation delay of 3-input NAND Gate.	L3	10
	b	Make use of necessary waveforms to define the following terms (i) Propagation delay (ii) Contamination delay (iii)Rise time (iv) Fall time (v) Edge rate.	L3	06
	c	Make use of necessary circuit diagrams to compute logical effort of the following gates. (i)2-input NOR gate and (ii)3-input NAND Gate.	L3	04
		Module-3		

Q. 05	a	Make use of necessary circuit diagram explain the operation of three transistor DRAM cell.	L3	10
	b	Explain the operation of full CMOS SRAM cell with necessary topology.	L3	10
		OR		
Q. 06	a	Explain the operation of 4*4 NAND based ROM array with necessary circuit diagram.	L3	08
	b	With necessary circuit diagram explain the operation of NOR flash memory cell with bias conditions.	L3	08
	c	Explain the hysteresis characteristics of ferroelectric capacitor with necessary diagram.	L3	04
		Module-4		
Q. 07	a	Differentiate between fault and failure with an example. Explain different types of stuck at faults with example.	L3	05
	b	For the circuit shown in Fig.2 using Boolean difference (i) detect s@0 and s@1 at x2, (ii) determine partial Boolean difference for x2-l-n-p-F.  Fig.2	L4	10
	c	. Explain stuck open faults in CMOS circuits with an example.	L3	05
		OR		
Q. 08	a	What is fault diagnosis? Explain one dimensional path sensitization technique for combinational circuits with an example.	L3	08
	b	Find the test pattern for line 6 s@0 for the circuit shown in Fig.3 using D Algorithm.  Fig.3	L4	12
		Module-5		
Q. 09	a	For the state table shown in Table.1 find (i)Response for 101 sequence, (ii) Homing tree, (iii) Distinguishing tree.	L4	10

Present state	Input $x = 0$	Input $x = 1$
A	B,0	D,0
B	A,0	B,0
C	D,1	A,0
D	D,1	C,0

Table 1

	b	Explain the various phases involved in checking experiment based on sequential circuit structure.	L3	05

	c	Explain the process of testing sequential circuit as iterative combinational circuits.	L3	05
		OR		
Q. 10	a	Define the terms controllability and observability with an example.	L3	06
	b	With a neat logic diagram, explain clocked hazard free latches used in LSSD Technique.	L3	08
	c	Explain any two Adhoc design rules for improving testability.	L3	06