Model Question Paper-1/2 with effect from 2021(CBCS Scheme)

USN | | | | | | | | | | |

7th Semester B.E. Degree Examination

ADVANCED VLSI

TIME: 03 Hours **Max. Marks: 100**

Note: 01. Answer any **FIVE** full questions, choosing at least **ONE** question from each **MODULE**.
02.

		Module -1	*Bloom's Taxonomy Level	COs	Marks
Q.01	a	Differentiate between Full custom, Semi-custom, and Programmable ASICs. Explain their applications.	L2	CO2	6M
	b	Illustrate the design flow of ASIC with a suitable diagram.	L2	CO1	7M
	c	Explain the significance of Booth encoding in multipliers using an example.	L2	CO2	7M
		OR			
Q.02	a	Discuss the importance of data path logic cells in CMOS design.	L2	CO2	6M
	b	Discuss the working principle of carry-skip, carry-select, carry-save, and Carry Bypass adders with necessary diagrams	L2	CO2	7M
	c	What is the role of I/O cells in ASIC design? Explain with an example.	L1	CO2	7M
		Module-2			
Q. 03	a	What are the goals and objectives of floor planning? Describe the steps involved in power planning during floor planning.	L1	CO3	7M
	b	Explain the Min-cut placement algorithm with an example.	L2	CO3	6M
	c	Explain the channel definition process in floor planning and its importance.	L2	CO3	7M
		OR			
Q.04	a	What are the goals and objectives of global routing in physical design? Explain global routing methods with examples.	L1	CO3	7M
	b	Explain the iterative placement improvement technique and its relevance in physical design.	L2	CO3	6M
	c	Explain how partitioning and back annotation are used in floor planning to improve timing and reduce delays.	L2	CO4	7M
		Module-3			
Q. 05	a	Explain the verification process in VLSI design. Discuss the role of functional coverage in enhancing the verification process.	L2	CO5	6M
	b	Discuss the role of constrained random stimulus in design verification.	L2	CO5	7M
	c	Explain the use of associative arrays and queues in System Verilog with examples.	L2	CO5	7M
		OR			
Q. 06	a	Write and explain a SystemVerilog code snippet using associative arrays.	L3	CO5	7M
	b	How are fixed arrays and dynamic arrays different in System Verilog? Provide examples.	L1	CO5	6M
	c	Describe the purpose of typedef and user-defined structures in System Verilog.	L2	CO5	7M

Module-4					
Q. 07	a	Differentiate between tasks and functions in System Verilog. Provide suitable examples.	L2	CO5	7M
	b	Describe the significance of separating the testbench and design in verification.	L2	CO5	6M
	c	Write and explain a SystemVerilog code that integrates an interface with assertions to validate a basic logic circuit.	L3	CO5	7M
OR					
Q. 08	a	Explain the purpose and structure of interface constructs in System Verilog.	L2	CO5	7M
	b	Discuss stimulus timing and its importance in System Verilog testbenches.	L2	CO5	6M
	c	Discuss the role of assertions in SystemVerilog. Provide examples of immediate and concurrent assertions.	L2	CO5	7M
Module-5					
Q. 09	a	What is randomization in SystemVerilog? Explain how random number generators can be used for generating constrained inputs.	L1	CO5	10M
	b	Illustrate the use of a cover group with a practical example. Explain how cross-coverage enhances the verification process.	L2	CO5	10M
OR					
Q. 10	a	Explain the strategies for improving functional coverage during simulation.	L2	CO5	6M
	b	Explain how automated bin creation in SystemVerilog enhances the efficiency and accuracy of functional coverage analysis.	L2	CO5	10M
	c	Explain coverage types with necessary example	L2	CO5	4M

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Subject Title Advanced VLSI

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Note: 01. 02. Answer any **FIVE** full questions, choosing at least **ONE** question from each **MODULE**.
03.
04.

		Module -1	*Bloom's Taxonomy Level	COs	Marks
Q.01	a	With a neat diagram, explain ASIC design flow	L2	CO1	7
	b	Explain Booth multiplier encoding by considering unsigned number as one of the example	L2	CO1	5
	c	Explain the following with relevant diagram a. Standard Cell based ASIC b. Gate array based ASIC	L2	CO1	8
		OR			
Q.02	a	Explain the working of a. Carry skip and b. Carry bypass adders with necessary diagrams	L2	CO1	7
	b	Define data path and explain any 8 data path elements with neat diagram	L2	CO1	8
	c	Explain I/O cells with neat diagram.	L2	CO1	5
		Module-2			
Q. 03	a	Explain about the following: Goals and objectives of 1.Floor planning 2. Placement and 3. Routing	L2	CO2 & CO3	8
	b	Explain the global routing methods in an ASIC physical design	L2	CO2 & CO3	7
	c	Explain the following in ASIC floor plan 1. Clock planning 2. Power planning in brief	L2	CO2 & CO3	5
		OR			
Q.04	a	Explain the following placement algorithms: 1. Min-cut placement 2. Iterative placement improvement	L2	CO2 & CO3	8
	b	Explain global routing between blocks with neat diagram	L2	CO2 & CO3	7
	c	Explain the concept of measurement of delay in floor planning	L2	CO2 & CO3	5
		Module-3			
Q. 05	a	Explain the verification process of system verilog	L2	CO5	7
	b	Explain the different types of array methods used in unpacked arrays	L2	CO5	8
	c	Write a short note on built in data types of system verilog with examples	L2	CO5	5

		OR			
Q. 06	a	Explain the factors in randomizing the stimulus to design	L2	CO5	8
	b	Explain the various test bench components	L2	CO5	7
	c	Explain the constants and strings in system verilog with examples	L2	CO5	5
		Module-4			
Q. 07	a	Explain tasks and void functions with examples	L2	CO4	7
	b	Explain with examples the various system verilog assertions	L2	CO4	8
	c	Explain the 1.Returning of array from a function 2. Passing an array to a function in system verilog	L2	CO4	5
		OR			
Q. 08	a	Explain the routine arguments with necessary examples	L2	CO4	8
	b	Explain the concept of separating the test bench and design in system verilog with an example	L2	CO4	7
	c	Write a short note on procedural statements in system verilog	L2	CO4	5
		Module-5			
Q. 09	a	Write about the common randomization problems in system verilog	L2	CO4	7
	b	List the various coverage types in system verilog and explain them	L2	CO4	8
	c	Write a short note on measuring coverage statistics during simulation	L2	CO4	5
		OR			
Q. 10	a	Explain about the various random number generators in system verilog	L2	CO4	8
	b	Which are the various functional coverage strategies? Explain them in detail	L2	CO4	7
	c	List the various random number functions and explain them in brief.	L2	CO4	5

*Bloom's Taxonomy Level: Indicate as L1, L2, L3, L4, etc. It is also desirable to indicate the COs and POs to be attained by every bit of questions.