Model Question Paper-1/2 with effect from 2021(CBCS Scheme)

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7th Semester B.E. Degree Examination

Subject Title DSP Algorithms and Architecture

TIME: 03 Hours **Max. Marks: 100**

Note: 01. 02. Answer any **FIVE** full questions, choosing at least **ONE** question from each **MODULE**.
03.
04.

		Module -1	*Bloom's Taxonomy Level	COs	Marks
Q.01	a	For the FIR filter y(n)= 0.5 x(n)+ 0.5 x(n-1). Determine i) System Function ii) Magnitude and phase function iii) Step response iv) Group Delay.	L3	1	8
	b	Explain IIR filter design	L3	1	6
	c	Describe the major feature of programmable DSP	L1	1	6
		OR			
Q.02	a	Obtain the transfer function of the IIR filter whose difference equation is given y[n] = 0.9 y(n-1) +0.1 x(n)	L3	1	8
	b	Define decimation and interpolation process. Explain them using block diagrams and equations with a neat diagram	L3	1	6
	c	Explain FIR filter with its design	L2	1	6
		Module-2			
Q. 03	a	Investigate the basic features that should be provided in the DSP architecture to be used to implement the following Nth order FIR y[n]= Σ h(i) x(n-i), where n =0,1,2	L3	2	8
	b	Explain Barun and Baugh Wooley multiplier for unsigned and signed numbers. Show the multiplication operation for 4x4 unsigned multiplication.	L2	2	9
	c	To find the sum of 64, 16 bit numbers. How many bits should the accumulator have so that the sum can be computed without the occurrence of overflow error or loss of accuracy?	L3	2	3
		OR			
Q.04	a	Explain the implementation of 8 Tap FIR filter y[n]= Σ h(i) x(n-i) using parallelism and pipelining .	L2	2	9
	b	Draw the schematic diagram of the saturation logic and explain the same.	L2	2	8
	c	A barrel shifter is to be designed with 16 inputs for left shifts from 0 to 15 bits. How many control lines are required to implement the shifter.	L3	2	3
		Module-3			
Q. 05	a	Describe the multiplier/adder unit of TMS320c54xx processor with a neat block diagram.	L2	2	7
	b	Describe any Four data addressing modes of TMS320c54xx processor.	L2	2	8
	c	Compare architectural features of TMS320C25 and DSP6000 fixed	L2	2	5

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		point digital signal processors.			
		OR			
Q. 06	a	Describe the accumulator unit of TMS320c54xx processor with a neat block diagram.	L2	2	7
	b	Describe Host Port interface and explain its signals.	L2	2	8
	c	Explain the functional building block of TMS320c54xx processor	L2	2	5
		Module-4			
Q. 07	a	Determine the number of stages and number of butterflies in each stage and the total number of butterflies needed for the entire computation of 512 point FFT	L3	3	7
	b	Explain with the help of a block diagram and mathematical equations the implementation of a second order IIR filter. No program code is required.	L2	3	8
	c	Briefly explain IIR filters.	L2	3	5
		OR			
Q. 08	a	Explain, how scaling prevents overflow conditions in the butterfly computation.	L2	3	7
	b	Write the assembly language program for TMS320C54XX processor to implement an FIR filter.	L3	3	8
	c	Write a subroutine program to find the spectrum of the transformed data using TMS320C54XX DSP.	L3	3	5
		Module-5			
Q. 09	a	Explain with a neat diagram, the synchronous serial interface between the C54xx and a CODEC device.	L2	4	10
	b	Explain the memory interface block diagram for the TMS 320 C54xx processor.	L2	4	5
	c	Design a data memory system with address range 000800h – 000fffh for a c5416 processor using 2kx8 SRAM memory chips.	L3	4	5
		OR			
Q. 10	a	Explain the operation of pulse position modulation (PPM) to encode two biomedical signals.	L2	4	10
	b	Explain an interface between an A/D converter and the TMS320C54XX processor in the programmed I/O mode.	L2	4	5
	c	With the help of block diagram explain JPEG algorithm.	L2	4	5

*Bloom's Taxonomy Level: Indicate as L1, L2, L3, L4, etc. It is also desirable to indicate the COs and POs to be attained by every bit of questions.

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03.
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		Module -1	*Bloom's Taxonomy Level	COs	Marks
Q.01	a	For the FIR filter y(n)= 0.5 x(n)+ 0.5 x(n-1). Determine i) System Function ii) Magnitude and phase function iii) Step response iv) Group Delay.	L3	1	8
	b	Explain the sampling process.	L1	1	6
	c	Describe the major feature of programmable DSP	L1	1	6
		OR			
Q.02	a	Explain the operation used in DSP to increase the sampling rate. The sequence x(n)=[0,2,4,6,8] is interpolated using interpolation sequence b_k =[1/2,1,1/2] and the interpolation factor is 2.find the interpolated sequence y(m).	L3	1	8
	b	Define decimation and interpolation process. Explain them using block diagrams and equations with a neat diagram	L2	1	6
	c	Explain FIR filter with its design	L2	1	6
		Module-2			
Q. 03	a	Investigate the basic features that should be provided in the DSP architecture to be used to implement the following Nth order FIR y[n]= Σ h(i) x(n-i), where n =0,1,2	L3	2	8
	b	Explain briefly about MAC unit.	L2	2	9
	c	To find the sum of 64, 16 bit numbers. How many bits should the accumulator have so that the sum can be computed without the occurrence of overflow error or loss of accuracy?	L3	2	3
		OR			
Q.04	a	Explain the implementation of 8 Tap FIR filter y[n]= Σ h(i) x(n-i) using parallelism and pipelining .	L3	2	9
	b	Explain circular and bit reversed addressing mode.	L2	2	8
	c	A DSP has a circular buffer with the start and end addresses are 0200h and 020F h respectively. What would be the new value of the address pointer of the buffer, if in the course of address computation if get updated to i) 0212 h ii) 01FCh	L3	2	3
		Module-3			
Q. 05	a	Describe the functioning of barrel shifter in TMS320C54XX processor.	L2	2	7
	b	Explain PMST register.	L2	2	8
	c	Compare architectural features of TMS320C25 and DSP6000 fixed	L2	2	5

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		point digital signal processors.			
		OR			
Q. 06	a	Explain the operation of serial I/O ports and hardware timer of TMS320C54XX on chip peripherals.	L2	2	7
	b	Describe Host Port interface and explain its signals.	L2	2	8
	c	Explain the different types of interrupts in TMS320C54xx processors.	L2	2	5
		Module-4			
Q. 07	a	What is an interpolation filter? Explain the implementation of digital interpolation using FIR filter and poly phase sub filter.	L2	3	7
	b	Write the assembly language program for TMS320C54XX processor to implement an FIR filter.	L3	3	8
	c	Describe the importance of Q notation in DSP algorithm implementation with examples.	L2	3	5
		OR			
Q. 08	a	How many add/subtract and multiply operations are needed to compute the butterfly structure?	L3	3	7
	b	Derive the equation to implement a butterfly structure in DIT FFT algorithm.	L2	3	8
	c	Write a subroutine program to find the spectrum of the transformed data using TMS320C54xx DSP.	L3	3	5
		Module-5			
Q. 09	a	Explain with a neat diagram, the memory interface for read-read-write sequence of operation. Explain the purpose of each signal involved.	L2	4	10
	b	How interrupts are handled by C54xx DSP processor.	L2	4	5
	c	Design a data memory system with address range 000800h – 000fffh for a c5416 processor using 2kx8 SRAM memory chips.	L2	4	5
		OR			
Q. 10	a	Explain with neat diagram, the synchronous serial interface between the C54xx and a CODEC device.	L2	4	10
	b	Explain an interface between an A/D converter and the TMS320C54XX processor in the programmed I/O mode.	L2	4	5
	c	With the help of block diagram explain JPEG algorithm.	L2	4	5

*Bloom's Taxonomy Level: Indicate as L1, L2, L3, L4, etc. It is also desirable to indicate the COs and POs to be attained by every bit of questions.

With the help of the implementation structure, explain the FFT algorithm for DIT-FFT computation on TMS320C54XX processors. Use ¼ as a scale factor for all butterflies.