21EC733 Model Question Paper-1/2 with effect from 2021(CBCS Scheme) USN 7th Semester B.E. Degree Examination

Subject Title DSP Algorithms and Architecture

TIME: 03 Hours

Max. Marks: 100

02. Answer any FIVE full questions, choosing at least ONE question from each 01. Note: MODULE. 03.

04.

Function ii) Magnitude and phase function iii) Step response iv) Group Delay.L.31bExplain IIR filter designL.310cDescribe the major feature of programmable DSPL.1100.02aObtain the transfer function of the IIR filter whose difference equation is given $y[n] = 0.9 y(n-1) + 0.1 x(n)$ 110bDefine decimation and interpolation process. Explain them using block diagrams and equations with a neat diagram1.310cExplain FIR filter with its designL.210Q.03aInvestigate the basic features that should be provided in the DSP architecture to be used to implement the following Nth order FIR y[n] = $\Sigma(i) x(n-i)$, where $n = 0, 1, 2$ 122bExplain Barun and Baugh Wooley multiplier for unsigned and signed multiplication.L.2222cTo find the sum of 64, 16 bit numbers. How many bits should the accumulator have so that the sum can be computed without the occurrence of overflow error or loss of accuracy?1222Q.04aExplain the implementation of 8 Tap FIR filter y[n] = Σ h(i) x(n-i) using parallelism and pipelining.228cA barrel shifter is to be designed with 16 inputs for left shifts from 0 to 15L.322cA barrel shifter is to be designed with 16 inputs for left shifts from 0 to 15L.323dDescribe any control lines are required to implement the shifter.122cA barrel shifter			Module -1	*Bloom's Taxonomy Level	COs	Marks
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Describe the major feature of programmable DSPImage: Normal State Stat		b	Explain IIR filter design		-	6
Q.02aORImage: Constraint of the Constrai		с	Describe the major feature of programmable DSP	L1	1	6
Q.02aObtain the transfer function of the IIR filter whose difference equation is given $y[n] = 0.9 y(n-1) + 0.1 x(n)$ L318bDefine decimation and interpolation process. Explain them using block diagrams and equations with a neat diagramL316cExplain FIR filter with its designL216Q.03aInvestigate the basic features that should be provided in the DSP architecture to be used to implement the following Nth order FIR $y[n] = \Sigma h(i) x(n-i)$, where $n = 0, 1, 2$ L322bExplain Barun and Baugh Wooley multiplier for unsigned and signed multiplication.L222cTo find the sum of 64, 16 bit numbers. How many bits should the accumulator have so that the sum can be computed without the occurrence of overflow error or loss of accuracy?L222Q.04aExplain the implementation of 8 Tap FIR filter $y[n] = \Sigma h(i) x(n-i)$ using parallelism and pipelining .L222bDraw the schematic diagram of the saturation logic and explain the a neat block diagram.L222cA barrel shifter is to be designed with 16 inputs for left shifts from 0 to 15L322cA barrel shifter is to be designed with 0 TMS320c54xx processor with a neat block diagram.22bDescribe the multiplic/adder unit of TMS320c54xx processor with a neat block diagram.22						
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processor.	Q. 03	а	1 1	L2	2	/
		b	Describe any Four data addressing modes of TMS320c54xx	L2	2	8
C Compare architectural features of TMS320C25 and DSP6000 fixed		с		L2	2	5

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		point digital signal processors.			
		OR			
Q. 06	a	Describe the accumulator unit of TMS320c54xx processor with a neat block diagram.	L2	2	7
	b	Describe Host Port interface and explain its signals.	L2	2	8
	с	Explain the functional building block of TMS320c54xx processor	L2	2	5
		Module-4			
Q. 07	a	Determine the number of stages and number of butterflies in each stage and the total number of butterflies needed for the entire computation of 512 point FFT	L3	3	7
	b	Explain with the help of a block diagram and mathematical equations the implementation of a second order IIR filter. No program code is required.	L2	3	8
	c	Briefly explain IIR filters.	L2	3	5
		OR			
Q. 08	a	Explain, how scaling prevents overflow conditions in the butterfly computation.	L2	3	7
	b	Write the assembly language program for TMS320C54XX processor to implement an FIR filter.	L3	3	8
	c	Write a subroutine program to find the spectrum of the transformed data using TMS320C54XX DSP.	L3	3	5
		Module-5			
Q. 09	a	Explain with a neat diagram, the synchronous serial interface between the C54xx and a CODEC device.	L2	4	10
	b	Explain the memory interface block diagram for the TMS 320 C54xx processor.	L2	4	5
	c	Design a data memory system with address range 000800h – 000fffh for a c5416 processor using 2kx8 SRAM memory chips.	L3	4	5
		OR			
Q. 10	a	Explain the operation of pulse position modulation (PPM) to encode two biomedical signals.	L2	4	10
	b	Explain an interface between an A/D converter and the TMS320C54XX processor in the programmed I/O mode.	L2	4	5
	с	With the help of block diagram explain JPEG algorithm.	L2	4	5

*Bloom's Taxonomy Level: Indicate as L1, L2, L3, L4, etc. It is also desirable to indicate the COs and POs to be attained by every bit of questions.

21EC733 Model Question Paper-1/2 with effect from 2021(CBCS Scheme) USN 7th Semester B.E. Degree Examination

Subject Title DSP Algorithms and Architecture

TIME: 03 Hours

Max. Marks: 100

Note: 01. 02. Answer any **FIVE** full questions, choosing at least **ONE** question from each **MODULE**. 03.

04.

		Module -1	*Bloom's Taxonomy Level	COs	Marks
Q.01	а	For the FIR filter y(n)= 0.5 x(n)+ 0.5 x(n-1). Determine i) System	L3	1	8
		Function ii) Magnitude and phase function iii) Step response iv)			
		Group Delay.			
	b	Explain the sampling process.	L1	1	6
	с		L1	1	6
		Describe the major feature of programmable DSP			
0.02		OR	L3	1	8
Q.02	а	Explain the operation used in DSP to increase the sampling rate.	L3	1	8
		The sequence $x(n)=[0,2,4,6,8]$ is interpolated using interpolation			
		sequence $b_k = [1/2, 1, 1/2]$ and the interpolation factor is 2.find the			
	b	interpolated sequence y(m).	L2	1	6
	D	Define decimation and interpolation process. Explain them using	L2	1	0
		block diagrams and equations with a neat diagram	L2	1	6
	c	Explain FIR filter with its design	L2	1	6
Q. 03	0	Module-2	L3	2	8
Q. 03	а	Investigate the basic features that should be provided in the DSP	L3	2	0
		architecture to be used to implement the following Nth order FIR $u = 5 h(i) u(n - 1)$, where $n = 0, 1, 2$.			
	h	$y[n] = \Sigma h(i) x(n-i)$, where n =0,1,2	L2	2	9
	b	Explain briefly about MAC unit.		2	3
	с	To find the sum of 64, 16 bit numbers. How many bits should the accumulator have so that the sum can be computed without the occurrence	L3	2	3
		of overflow error or loss of accuracy?			
		OR			
Q.04	а	Explain the implementation of 8 Tap FIR filter $y[n] = \Sigma h(i) x(n-i)$ using	L3	2	9
		parallelism and pipelining .			
	b	Explain circular and bit reversed addressing mode.	L2	2	8
	с	A DSP has a circular buffer with the start and end addresses are 0200h and	L3	2	3
		020F h respectively. What would be the new value of the address pointer			
		of the buffer, if in the course of address computation if get updated to i)			
		0212 h ii) 01FCh			
Q. 05	а	Module-3	L2	2	7
Q. 05	a	Describe the functioning of barrel shifter in TMS320C54XX		2	/
		processor.			
	b	Explain PMST register.	L2	2	8
	c	Compare architectural features of TMS320C25 and DSP6000 fixed	L2	2	5

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					0.00
		point digital signal processors.			
		OR			
Q. 06	a	Explain the operation of serial I/O ports and hardware timer of	L2	2	7
		TMS320C54XX on chip peripherals.			
	b	Describe Host Port interface and explain its signals.	L2	2	8
	с	Explain the different types of interrupts in TMS320C54xx processors.	L2	2	5
		Module-4			
Q. 07	а	What is an interpolation filter? Explain the implementation of	L2	3	7
		digital interpolation using FIR filter and poly phase sub filter.			
	b	Write the assembly language program for TMS320C54XX processor	L3	3	8
		to implement an FIR filter.			
	c	Describe the importance of Q notation in DSP algorithm	L2	3	5
		implementation with examples.			
		OR			
Q. 08	a	How many add/subtract and multiply operations are needed to	L3	3	7
		compute the butterfly structure?			
	b	Derive the equation to implement a butterfly structure in DIT FFT	L2	3	8
		algorithm.			
	с	Write a subroutine program to find the spectrum of the	L3	3	5
		transformed data using TMS320C54xx DSP.			
		Module-5			
Q. 09	a	Explain with a neat diagram, the memory interface for read-read-	L2	4	10
		write sequence of operation. Explain the purpose of each signal			
		involved.			
	b	How interrupts are handled by C54xx DSP processor.	L2	4	5
	с	Design a data memory system with address range 000800h -	L2	4	5
		000fffh for a c5416 processor using 2kx8 SRAM memory chips.			
		OR			
Q. 10	a	Explain with neat diagram, the synchronous serial interface	L2	4	10
		between the C54xx and a CODEC device.			
	b	Explain an interface between an A/D converter and the	L2	4	5
		TMS320C54XX processor in the programmed I/O mode.			
	с	With the help of block diagram explain JPEG algorithm.	L2	4	5

*Bloom's Taxonomy Level: Indicate as L1, L2, L3, L4, etc. It is also desirable to indicate the COs and POs to be attained by every bit of questions.

With the help of the implementation structure, explain the FFT algorithm for DIT-FFT computation on TMS320C54XX processors. Use ¼ as a scale factor for all butterflies.