Model Question Paper-1/2 with effect from 2021(CBCS Scheme)

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7th Semester B.E. Degree Examination

VLSI CIRCUITS AND SYSTEMS

TIME: 03 Hours **Max. Marks: 100**

Note: 01. Answer any **FIVE** full questions, choosing at least **ONE** question from each **MODULE**.

		Module -1	*Bloom's Taxonomy Level	COs	Marks
Q.01	a	Define Moore's law and explain its implication on IC industry in terms of cost, feature size and performance.	L2	1	8
	b	What are stick diagrams in VLSI design? Create a stick diagram for a simple inverter and three input NAND	L3	1	7
	c	Sketch complementary CMOS gate for function Y= $\overline{(A + B + C) \cdot D)}$	L2	1	5
		OR			
Q.02	a	Discuss the different masks in an inverter with a neat schematic.	L2	1	8
	b	Draw the schematic of a 3-input and 2 input NAND gate using CMOS technology and explain its operation with the help of a truth table	L2	1	7
	c	Explain pass transistors in CMOS logic circuits	L2	1	5
		Module-2			
Q. 03	a	Illustrate the structure and operation of an nMOS transistor in accumulation, depletion, and inversion modes with relevant diagrams.	L2	2	10
	b	With a neat circuit diagram explain the tri state inverter	L2	2	5
	c	Illustrate layout design rules for Contacts with neat diagram.	L2	2	5
		OR			
Q.04	a	Derive the MOSFET current equation in linear and saturation regions for drain current (Ids)and explain how it varies with Vgs and Vds.	L3	2	10
	b	Briefly explain the process of lithography	L2	2	5
	c	Explain how the beta ratio (βp/βn) affect the threshold voltage and output of skewed inverters	L2	2	5
		Module-3			
Q. 05	a	Explain Conventional CMOS Flip Flops with a neat diagram	L2	3	8
	b	Design and explain a circuit to compute F=AB+CD using NANDs and NORs by bubble pushing	L3	3	7
	c	With a neat diagram explain the concept of footed and unfooted dynamic gates	L2	3	5
		OR			
Q. 06	a	With a neat diagram explain Resettable Flipflops with Asynchronous reset.	L2	3	8
	b	Explain how enabling is performed with a multiplexer and clock gating in enabled latches and flipflops	L2	3	7
	c	Write a note on conventional keepers	L1	3	5

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Module-4					
Q. 07	a	Discuss the working of carry ripple adder with neat diagrams	L2	4	8
	b	With a neat diagram explain 1-Transistor dynamic RAM cell	L2	4	7
	c	Briefly describe how multiple inputs are added in adder circuits	L2	4	5
OR					
Q. 08	a	Describe the working of a 6-transistor (6T) SRAM memory cell with a neat diagram, including the function of sense amplifier	L2	4	8
	b	Explain how Manchester carry chains are built using multiple stages with a neat diagram	L2	4	7
	c	Draw the diagram of decoder using pseudo nMOS NOR gate and inverters	L1	4	5
Module-5					
Q. 09	a	Draw Gajski-Kuhn Y chart describing relationship between various domain and levels of abstraction.	L1	5	10
	b	Explain various Logic Verification Principles.	L2	5	5
	c	Write a note on LFSR used in BIST.	L1	5	5
OR					
Q. 10	a	Explain Hierarchy, regularity, locality, and Modularity in structured Design Techniques.	L2	5	10
	b	Briefly explain the concept of stuck at faults used in CMOS.	L2	5	5
	c	Explain Ad hoc testing approach in detail.	L2	5	5

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Note: Answer any **FIVE** full questions, choosing at least **ONE** question from each **MODULE**.

		Module -1	*Bloom's Taxonomy Level	COs	Marks
Q.01	a	Describe the step-by-step process of fabricating a CMOS transistor.	L2	1	8
	b	With a neat diagram illustrate the concept of CMOS logic and describe the working of a CMOS inverter.	L2	1	7
	c	Explain transmission gates in CMOS logic circuits?	L2	1	5
		OR			
Q.02	a	What is lambda-based design rules and explain in detail with neat diagrams	L2	1	8
	b	Draw the schematic of a 3-input and 2 input NOR gate using CMOS technology and explain its operation with the help of a truth table	L1	1	7
	c	Sketch a stick diagram for a CMOS gate computing Y = (A + B + C) · D)' and estimate cell width and height.	L3	1	5
		Module-2			
Q. 03	a	Explain the operation of nMOS transistor in cut off, linear and saturation region. Illustrate with relevant diagrams.	L2	2	10
	b	Illustrate layout design rules for transistors with neat diagram.	L2	2	5
	c	Explain the process of enabling in latches and flip-flops using multiplexers and clock gating.	L2	2	5
		OR			
Q.04	a	Explain the concept of noise margin in CMOS circuits with a neat diagram.	L2	2	10
	b	Sketch the pseudo- nmos Inverter circuit transfer characteristics	L3	2	5
	c	Explore the common approaches used in oxidation of silicon	L2	2	5
		Module-3			
Q. 05	a	With a neat diagram explain Resettable Flipflops with synchronous reset	L2	3	8
	b	With a neat diagram explain the operation of differential sense amplifier flip flop	L2	3	7
	c	Write a note on monotonicity problem	L1	3	5
		OR			
Q. 06	a	Expalin true single phase clocked flipflops and latches with a neat diagram.	L2	3	8
	b	With a neat diagram explain AND/NAND gate and XOR/XNOR dual rail domino logic.	L2	3	7
	c	Illustrate with a neat diagram the concept of conventional keepers	L2	3	5

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Module-4					
Q. 07	a	With a neat circuit diagram and waveforms explain the read operation of SRAM cell.	L2	4	10
	b	With a neat block diagram explain 4 bits carry look ahead adder circuit.	L2	4	5
	c	Write a note on one zero detectors	L1	4	5
OR					
Q. 08	a	With a neat diagram and expressions illustrate the working of Manchester valency 4 carry chain adder	L2	4	10
	b	How do adders handle subtraction operations? Illustrate with neat diagram	L2	4	5
	c	Construct a 4x6 ROM using Pseudo nMOS logic, including an example to illustrate the design.	L3	4	5
Module-5					
Q. 09	a	Explain 3-bit BILBO with a neat diagram.	L2	5	8
	b	With a neat diagram illustrate the functional equivalence at various levels of abstraction with a neat diagram in logic verification	L2	5	7
	c	Write a note on a. Hierarchy b. Modularity	L1	5	5
OR					
Q. 10	a	Describe the use of scan registers in modern scan techniques with the help of a neat diagram.	L2	5	8
	b	Discuss controllability and observability	L2	5	7
	c	Write a brief note on CFSR used in BIST	L1	5	5