Model Question Paper-I with effect from 2023-24 (CBCS Scheme)

USN | | | | | | | | | | |

Third Semester B.E. Degree Examination

Digital Design and Computer Organization

TIME: 03 Hours **Max. Marks: 100**

Note: 01. Answer any **FIVE** full questions, choosing at least **ONE** question from each **MODULE**.

		Module -1	*Bloom's Taxonomy Level	Marks
Q.01	a	Demonstrate the nonassociativity of the NOR gate	L2	5
	b	Design a car safety alarm circuit diagram. The system considers four inputs: door (D), key (K), seat pressure (P) and seat belt (B). The input is considered HIGH (1) if the door is closed, the key is in, the driver is on the seat, or the seat belt is fastened. The alarm (A) should sound with two conditions as stated below: The door is not closed, and the key is in. The door is closed, the key is in the driver's seat, and the seat belt is not closed. (a) Construct a truth table for the system based on input arrangement D, K, P, B with A as an output (b)Design a Karnaugh map to verify the simplified expression (c) Draw the simplified circuit using NOR gates only	L3	8
	c	With an example explain the working of Test Bench in Verilog.	L2	7
		OR		
Q.02	a	Demonstrate the positive and negative logic signal	L2	5
	b	A digital system is to be designed in which the month of the year is given as I/P in four-bit form. The month of January is represented as '0000', February as "0001" and so on. The output of the system should correspond to the input of the month containing 31 days, or otherwise, it is '0'. Consider the excess number in the I/P beyond 1011' as don't care condition: (i) Write truth table, SOP Em and POSIIM form (ii) Simplify for SOP using K-map (iii) Realize using basic gates	L3	8
	c	What is User-Defined Primitives in Verilog? What are the general rules for UDP? Explain with an example HDL for user defined primitive. Draw the Schematic for the Circuit with UDP_02467	L2	7
		Module-2		
Q. 03	a	Differentiate Latches and Flip-Flops.	L2	5
	b	Explain the working of Four-bit adders using 4-full Adders.	L3	8
	c	Implement Y (A, B, C, D) = ∑m (0, 1, 6, 7, 8, 9, 10, 11, 12, 14) using 16-to-1 multiplexer and 8-to-1 multiplexer.	L3	7
		OR		
Q.04	a	Explain different modeling styles used to write the code in VERILOG with an example.	L2	5
	b	Design a BCD-to-excess-3 code converter.	L3	8

	c	Define decoder. Describe the working principle of a 3:8 decoder. Draw the logic diagram of the 3:8 decoder with enabled input. Realize the following Boolean expressions using a 3:8 decoder and multi-input OR gates: F1(A, B, C) = ∑ m(1, 3, 7) F2(A, B, C) = ∑m(2, 3, 5).	L3	7
Module-3				
Q. 05	a	Write one address, two address, and three address instructions to carry out C← [A] + [B].	L3	5
	b	Explain the basic operation concepts of the computer with a neat diagram.	L2	8
	c	Explain a) Processor Clock, b) Basic performance equation, c) Clock rate d) Performance measurement	L2	7
OR				
Q. 06	a	Write ALP of adding a list of n numbers using indirect addressing mode	L3	5
	b	What is an addressing mode? Explain the different addressing modes. With an example for each.	L2	8
	c	Explain the following: (i) Byte addressability (ii) Big-endian assignment (i) Little-endian assignment.	L2	7
Module-4				
Q. 07	a	Draw a neat block diagram of memory hierarchy in a computer system. Discuss the variation of size, speed and cost per bit in the hierarchy.	L2	10
	b	What is DMA Bus arbitration? Explain different bus arbitration techniques.	L2	10
OR				
Q. 08	a	With neat sketches, explain various methods for handling multiple interrupt requests raised by multiple devices.	L2	10
	b	What is cache memory? Explain the different mapping functions used in cache memory.	L2	10
Module-5				
Q. 09	a	Explain the single-bus organization of computers and fundamental concepts with a neat diagram.	L2	10
	b	Write and explain the control sequence for execution of the instruction Add(R3), R1	L3	10
OR				
Q. 10	a	Explain with an example the different types of hazards that occur during pipelining.	L2	10
	b	Write and explain the control sequence for the execution of an unconditional branch instruction.	L3	10

*Bloom's Taxonomy Level: Indicate as L1, L2, L3, L4, etc. It is also desirable to indicate the COs and POs to be attained by every bit of question.