

Model Question Paper-1 with effect from 2022-23 (2022 Scheme)

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Sixth Semester B.E. Degree Examination VLSI DESIGN AND TESTING

TIME: 03 Hours

Max. Marks: 100

Note: 01. Answer any **FIVE** full questions, choosing at least **ONE** question from each **MODULE**.

Module -1			*Bloom's Taxonomy Level	COs	Marks
Q.01	a	Discuss the various types of MOSFETs, their symbolic representations, and physical structures, with neat diagrams.	L2	CO1	08
	b	Describe how a MOSFET acts as a switch	L2	CO1	06
	c	Draw the schematic diagram of a 2-input NAND gate using CMOS Logic and explain its operation.	L3	CO1	06
OR					
Q.02	a	Using CMOS Logic draw the schematic diagrams for the following Boolean logic expressions: i. $Y = \overline{(ABC+D)} E$ ii. $Y = \overline{(A+B)C} + D$ iii. $Y = \overline{(AB + C)DE}$	L3	CO1	10
	b	Discuss the following types of design representation with examples: i) Structural representation ii) Physical representation	L2	CO1	10
Module-2					
Q. 03	a	Derive the drain current equations for a MOSFET in the linear (non-saturated) and saturation regions.	L2	CO2	10
	b	What is the threshold voltage? What are the parameters on which the threshold voltage depends?	L2	CO2	05
	c	Explain the noise margin in a CMOS inverter.	L2	CO2	05
OR					
Q.04	a	Derive the DC characteristics of a CMOS inverter and obtain the relationship for the output voltage in different regions of the DC transfer characteristics.	L2	CO2	12
	c	Explain the noise margin in a CMOS inverter with neat sketches.	L2	CO2	08
Module-3					
Q. 05	a	Describe the following processing methods with neat sketches: i) Wafer processing using the Czochralski method	L2	CO3	10

		ii) Selective diffusion process			
	b	What is the purpose of layout design rules? What are the key constraints of layout design rules?	L2	CO3	06
	c	Explain the static and dynamic power dissipation in a CMOS gate.	L2	CO3	04
OR					
Q. 06	a	Explain the switching characteristics of a CMOS gate with the determination of the following switching times: i) Rise time ii) Fall time iii) Delay time	L2	CO3	12
	b	Describe the following with relevant equations: i) Charge sharing ii) Yield	L2	CO3	08
Module-4					
Q. 07	a	Draw the schematic diagram of the Boolean function $Y = (A + B)C + DE$ using pseudo NMOS logic and explain its operation. Also discuss the advantages and disadvantages of this logic.	L3	CO4	08
	b	Describe the operation of C ² MOS logic.	L2	CO4	06
	c	Draw the schematic diagram of a 4:1 multiplexer using NMOS and CMOS implementation of pass transistor logic.	L3	CO4	06
OR					
Q. 08	a	Draw the schematic structure and the graphical representation of the function $Y = \overline{(A + B) + CD}$ using CMOS logic. Also, draw the layout for the same using the Euler path method.	L3	CO4	08
	b	Differentiate between two-phase dynamic logic and four-phase dynamic logic.	L2	CO4	04
	c	Describe the operation of CVS Logic.	L2	CO4	06
Module-5					
Q. 09	a	Describe the behavior of a two-inverter basic bi-stable element.	L2	CO5	10
	b	Explain the operation of a NOR-based SR latch circuit and define the related lumped load capacitances at the output node.	L2	CO5	10
OR					
Q. 10	a	Explain any four techniques used for reducing the complexity of IC design in structured design strategies.	L2	CO5	10
	b	Write a short note on the following topics related to automated synthesis: i) Procedural module definition ii) Silicon compiler	L2	CO5	10