Model Question Paper-1/2 with effect from 2023-24 (CBCS Scheme)

USN | | | | | | | | | | |

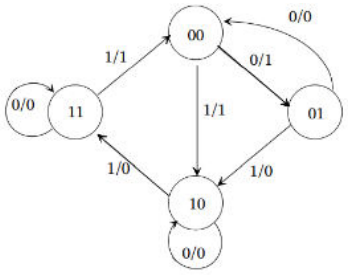
Third Semester B.E. Degree Examination

Subject Title: Digital Logic Circuits

Time :03 Hours **Max Marks:100**

Note: Answer any **FIVE** full questions, choosing at least **ONE** question from each **MODULE**.

		Module -1	RBL	COs	Mars	PO
Q.01	a	What do you mean by combinational logic? Write the logic truth table using 4 input variables & output is high when majority of inputs are high.	L1	01	06	1,2
	b	Place the following equations into the proper canonical Form. i. P=f(a,b,c)=ab'+ac'+bc ii.T=f(a,b,c)=(a+b')(b'+c).	L2	01	08	1,2
	c	Simplify the following expression using a 3 variable K Map. Q=f(a,b,c)=$\sum(1,2,3,6,7)$	L2	01	06	1,2
		OR				
Q.02	a	Simplify the following expression using a 4 variable K Map. P=f(r,s,t,u)=$\sum(1,3,4,6,9,11,12,14)$	L3	01	08	1,2
	b	Simplify using the Quine-McClusky minimization technique. F(A,B,C,D)=$\sum m(0,1,3,7,8,9,11,15)$.	L2	01	12	1,2
		Module-2				
Q. 03	a	Explain 74X138 3:8 decoder with a neat circuit diagram.	L1	02	06	
	b	Implement the following using 8:1 MUX with a,b,c as select lines. F(a,b,c,d)=$\sum(0,1,5,6,7,9,10,15)$	L3	02	06	2,3
	c	Design a 1 bit comparator using gates.	L3	02	08	1,2,3
		OR				
Q.04	a	Write a short note on look ahead carry generator.	L2	02	06	1,2
	b	Design a full adder using 4:1 MUX and also using basic gates.	L4	02	08	2,3,4
	c	Design a 2 bit comparator using gates.	L4	02	06	2,3
		Module-3				
Q. 05	a	With a neat diagram, explain the working of master-slave JK flip flop along with waveforms.	L2	02	10	1,2
	b	Explain switch debouncer using SR latch with waveforms	L3	02	10	1,2
		OR				
Q. 06	a	Differentiate between latches and flip flops. Derive the characteristic equation of SR,JK,D & T flip flop.	L2	02	10	1,2
	b	With a neat diagram explain the working of D & T flip flop	L1	03	10	1,2

		with input and output waveforms.				
		Module-4				
Q. 07	a	Explain the working of 4 bit binary ripple counter using positive edge triggered T flip flop.	L3	04	10	1,2
	b	With a neat diagram explain the operation of SISO,SIPO,PISO,PIPO	L1	04	10	1.2
		OR				
Q. 08	a	Describe the block diagram of MOD-7 Johnson counter & explain its operation.	L3	04	10	1,2,3
	b	Design a MOD5 synchronous binary counter using clocked JK flip flop.	L4	04	10	1,2,3, 4
		Module-5				
Q. 09	a	With a neat diagram, explain Moore & Mealy model in a sequential circuit analysis.	L2	05	08	1,2
	b	Design a sequential circuit using T flip flop as shown in Fig.Q 9(b).  Fig.Q 9(b).	L4	05	12	2,3,4
		OR				
Q. 10	a	Write a short note on i. ROM ii.EPROM	L1	05	10	1,2
	b	Design a synchronous counter using JK flip flop to count the following sequence: 7,4,3,1,6,0,7…..	L4	05	10	2,2,4

*Bloom's Taxonomy Level: Indicate as L1, L2, L3, L4, etc. It is also desirable to indicate the COs and POs to be attained by every bit of questions.