Fifth Semester B.E. / B. Arch. / MCA / M.Tech. Semester End Examination, MAR/APR. 2023-24 ANALOG ELECTRONIC CIRCUITS (Model Question Paper)

## Time: 3 Hours

Max. Marks: 100

| Instructions: | 1. | Answer any Five full questions choosing ONE from each unit. |
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|  |  | UNIT - I | L | CO | PO | M |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | a. | Explain the working of negative clamper circuit. Draw the required waveforms |  |  |  |  |
|  |  |  | (2) | (1) | (1) | (5) |
|  | b. | Design a fixed bias circuit for the following specifications:$V_{C C=}=12 \mathrm{~V}, I_{C}=3 \mathrm{~mA}, V_{C E=}=6 \mathrm{~V}, \beta=100$ |  |  |  |  |
|  |  |  | (2) | (1) | ( 1 ) | (5) |
|  | c. | For the voltage divider bias circuit, derive an expression for stability factor $S_{I c 0}$ and explain the variation of $S_{I C 0}$ for different cases. |  |  |  |  |
|  |  |  | (3) | (1) | (2) | (10) |
| 2 | a. | Explain the working of series clipping circuit to clip the input sinusoidal signal above reference level. Draw the waveforms and transfer characteristics. |  |  |  |  |
|  |  |  | ( 1) | (1) | ( 1 ) | ( 5) |
|  | b. | For the emitter stabilized bias circuit, calculate the location of operating point Q and the voltages $V_{B}, V_{C}, V_{B C}$ if $R_{C}=3.3 k \Omega, R_{B}=220 \mathrm{k} \Omega, R_{E}=1 \mathrm{k} \Omega, V_{C C}=10 \mathrm{~V}, \beta=150$. |  |  |  |  |
|  |  |  | (3) | (1) | ( 2 ) | ( 5) |
|  | c. | For the fixed bias circuit, derive an expression for stability factors $S_{I c o,} \quad S_{V B E}, S_{\beta}$ and also obtain the relation between (i) $S_{I c o,}$ and $S_{V B E}$, (ii) $S_{I c o,}$ and $S_{\beta}$. |  |  |  |  |
|  |  |  | (3) | ( 1 ) | (2) | ( 10) |
|  |  | UNIT - II | L | CO | PO | M |


| 3 | a. | Draw the hybrid parameter model for common base and common emitter modes along with the <br> suitable equations. |  |  |  |  |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- |
|  |  |  | (3) | (2) | ( 1) | ( 6) |


|  | b. | For the common collector amplifier, calculate current gain, input resistance, voltage gain and output impedance if $V_{C C}=10 \mathrm{~V}, R_{1}=6 \mathrm{k} \Omega, R_{2}=6 \mathrm{k} \Omega, R_{S}=600 \Omega, R_{E}=1 \mathrm{k} \Omega, R_{\mathrm{L}}=10 \mathrm{k} \Omega$. hparameters are $h_{o c}=\frac{25 \mu A}{V}, h_{r c}=1, h_{f c}=-101, h_{i c}=1.2 k \Omega$. Use exact $h$-parameter model. |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | (3) | ( 2 ) | (2) | (10) |
|  | c. | Compare common base, common collector and common emitter modes. |  |  |  |  |
|  |  |  | (1) | ( 2 ) | (1) | (4) |
| 4 | a. | Explain the effect of input RC network, output RC network and bypass network on the low frequency response of RC coupled amplifier. |  |  |  |  |
|  |  |  | (3) | (2) | (1) | (10) |

b. Using hybrid pi model, derive an expression for common emitter short circuit current gain and its variation on frequency. Also obtain expressions for $f_{\beta}$ and $f_{T}$.

|  | (4) | (2) | (2) | (10) |
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| UNIT - III | L | CO | PO | M |


$\mathbf{5}$ a. |  | For the Darlington connection, derive an expression for current gain and input resistance for first |
| :--- | :--- | :--- | :--- | and second stage. Also calculate overall current gain.

(3) (3) $^{(3)}$ (1)
(10)
b. For the two stage CE-CE , RC coupled amplifier, $R_{1}=220 k \Omega, R_{2}=22 k \Omega, R_{C}=3.3 k \Omega$. $R_{E}=$ $470 \Omega, R_{S}=600 \Omega, C_{E}=47 \mu F, C_{1}=C_{2}=0.1 \mu F$ for the first stage. For the second stage the component values are $R_{1}^{\prime}=33 k \Omega, R_{2}^{\prime}=3.3 k \Omega, R_{C}^{\prime}=4.7 k \Omega, R_{E}^{\prime}=330 \Omega, C_{E}^{\prime}=$ $10 \mu \mathrm{~F}, V_{C C}=10 \mathrm{~V}, h_{i e}=1.2 \mathrm{k} \Omega, h_{f e}=50$. Calculate the overall voltage gain taking source

|  |  | resistance into account, input resistance and output resistance. Draw the circuit diagram and use approximate hybrid model. |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | (4) | (3) | (2) | (10) |
| 6 | a. | Explain the features of following feedback amplifiers: <br> (i)Voltage series feedback amplifiers <br> (ii)Current shunt feedback amplifiers |  |  |  |  |
|  |  |  | (2) | (3) | (1) | (10) |
|  | b. | For the current series feedback amplifier, obtain an expression for input resistance with feedback and output resistance with feedback. |  |  |  |  |
|  |  |  | (2) | ( 3 ) | (1) | (10) |
|  |  | UNIT - IV | L | CO | PO | M |
| 7 | a. | Define total harmonic distortion in power amplifiers. Hence derive an expression for second harmonic distortion in Class-A power amplifier. |  |  |  |  |
|  |  |  | (2) | (4) | (1) | (10) |
|  | b. | Compare push-pull and complementary symmetry Class B power amplifiers. |  |  |  |  |
|  |  |  | (1) | (4) | (1) | (5) |
|  | c. | In class B push-pull amplifier, show that efficiency at maximum power dissipation is only $50 \%$. |  |  |  |  |
|  |  |  | (2) | (4) | (1) | (5) |
| 8 | a. | Explain Barkhausen criteria for sustained oscillations. |  |  |  |  |
|  |  |  | (2) | (4) | (1) | (5) |
|  | b. | For Wien bridge oscillator, derive an expression for frequency of oscillations. Also calculate the minimum value of $A$ and $\beta$. |  |  |  |  |
|  |  |  | (4) | (4) | (2) | (10) |
|  | c. | Calculate the frequency of oscillations in Colpitt's oscillator if $C_{1}=C_{2}=3 n F, L=200 \mu \mathrm{H}$. Draw the circuit diagram. |  |  |  |  |
|  |  |  | (3) | (4) | (2) | (5) |
|  |  | UNIT -V | L | CO | PO | M |
| 9 | a. | Compare BJT and FET on different parameters. |  |  |  |  |
|  |  |  | (2) | ( 5 ) | (1) | (5) |
|  | b. | Explain the construction of JFET and its characteristics. |  |  |  |  |
|  |  |  | (2) | (5) | (1) | (10) |
|  | c. | Explain the dc analysis and working of fixed bias circuit of JFET. |  |  |  |  |
|  |  |  | (2) | ( 5 ) | (1) | (5) |
| 10 | a. | Consider JFET in common source configuration working with self bias , bypassed source resistance mode. Obtain expressions for input impedance, output impedance and voltage gain. Draw the small signal model |  |  |  |  |
|  |  |  | (3) | ( 5 ) | ( 2) | (6) |
|  | b. | For the voltage divider bias circuit of JFET, $R_{1}=22 k \Omega, R_{2}=12 k \Omega, R_{D}=1 k \Omega, R_{S}=$ $2.2 k \Omega, V_{D D}=10 \mathrm{~V}, I_{D S S}=10 \mathrm{~mA}, V_{p}=-3 \mathrm{~V}$. Calculate the drain current, voltage between gate and source, voltage between drain and source, voltage at the gate and source. |  |  |  |  |
|  |  |  | (3) | (5) | (2) | (10) |
|  | c. | Compare D-MOSFET and E-MOSFET devices. |  |  |  |  |
|  |  |  | (2) | ( 5 ) | (1) | (4) |

