

Model Question Paper-1/2 with effect from 2022-23 (CBCS Scheme)

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Fifth Semester B.Tech. Degree Examination
Subject Title DIGITAL SYSTEM DESIGN USING VERILOG

TIME: 03 Hours

Max. Marks: 100

Note: 01. Answer any **FIVE** full questions, choosing at least **ONE** question from each **MODULE**.

Module -1			*Bloom's Taxonomy Level	COs	Marks
Q.01	a	Explain the design methodology flow for HDLs based ASICs	L1,L2,L3	C01	12
	b	Define Glitches and Hazards and explain the procedure to remove static hazard with the simulation result diagram	L1,L2,L3	C01	8
OR					
Q.02	a	Explain elimination of Static Hazards in Two-Level Circuits and Multilevel Circuits	L1,L2,L3	C01	12
	b	Write a Verilog code for 16 bit ripple carry adder using Concatenation with hierarchy design flow diagram	L1,L2,L3	C01	8
Module-2					
Q. 03	a	Write a Verilog code to address the problem of Propagation delay in continuous assignment statement	L1,L2,L3	C02	12
	b	Write a Verilog code Comparator (2bit)using Concatenation operator.	L1,L2,L3	C02	8
OR					
Q.04	a	Write a Verilog code for 4:1 Mux of 32 bit input using "case" statement .	L1,L2,L3	C02	8
	b	Write a Verilog code for 3:8 decoder using "case" statement .	L1,L2,L3	C02	12
Module-3					
Q. 05	a	Explain Algorithmic State Machine Charts for Behavioral Modeling,	L1,L2,L3	C03	8
	b	Write a Verilog code 4 Bit updown counter.	L1,L2,L3	C03	12
OR					
Q. 06	a	Write a Verilog code 4 bit universal Shift Registers,	L1,L2,L3	C03	12
	b	Explain Synthesis of Combinational Logic	L1,L2,L3	C03	8
Module-4					
Q. 07	a	Explain Mealy and Moore finite state machines with example	L1,L2,L3	CO4	12
	b	Explain State-Transition Graphs	L1,L2,L3	CO4	8
OR					
Q. 08	a	Explain Synthesis of Explicit State Machines.	L1,L2,L3	CO4	12
	b	Explain Synthesis of Implicit State Machines	L1,L2,L3	CO4	8
Module-5					
Q. 09	a	Explain Programmability of PLDs	L1,L2	CO5	12

	b	Explain Programmable Logic Devices	L1,L2	CO5	8
OR					
Q. 10	a	Explain Programmable Array Logic (PAL),	L1,L2	CO5	12
	b	Explain Complex PLDs (CPLDs)	L1,L2	CO5	8

*Bloom's Taxonomy Level: Indicate as L1, L2, L3, L4, etc. It is also desirable to indicate the COs and POs to be attained by every bit of questions.