Model Question Paper- I

Fifth Semester B.E Degree

Course Title: Digital VLSI Design **Course Code:BVL503**

Duration: 03Hours Max.Marks:100

Note: Answer any FIVE full questions, choosing at least ONE question from each Unit.

Q.No.		Module-1	M
1.	a)	With neat diagram **explain** the MOS Transistor physical Structure?	6
	b)	With neat diagram **explain** the simple CMOS flip flop with 2 mux and 2 inverters.	8
	c)	**Differentiate** between CMOS and NMOS	6
		OR	
2.	a)	With neat diagram **explain** physical construction/ layout of CMOS flip-flop.	10
	b)	**Explain** how mos transistor can be used as switch?	10
		Module-2	
3.	a)	**Write** the CMOS inverter circuit and briefly **explain**. Write the CMOS VTC showing regions A,B,C,D,E. **Derive** the expressions for output voltage in region D	10
	b)	**Explain** Accumulation, Depletion, and Inversion modes in an mos structure	6
	c)	With the circuit diagram **explain** CMOS tristate inverter.	4
		OR	
4.	a)	**Explain** the n mos device behaviour under the inluence of different terminal voltages with neat diagram.	8
	b)	**Explain** the following i. channel length modulation ii. Noise margin iii. Body effect	12

		Module-3	
5.	a)	With a diagram **derive** an expression for sheet resistance. Also **write** the resistance of non-rectangular shapes	8
	b)	**Derive** an equation for resistance for rise and fall time w.r.t cmos inverter	8
	c)	**Explain** rise time, fall time, delay time with respect to switching characteristics for CMOS inverter.	4
		OR	
6.	a)	**Explain** how long wire is represented in terms of distributed RC section and estimate the propagation time With suitable equation	4
	b)	**Derive** an equation for static and dynamic power dissipation w.r.t cmos inverter	8
	c)	**Write** a short note on i. Diffusion capacitance **ii.** Routing capacitance	8
		Module-4	
7.	a)	**Realize** CMOS logic structure\ CMOS Complementary logic for Boolean expression $Z = \overline{AB + C(D + E)}$	6
	b)	**Explain** the C^2MOS [clocked CMOS logic] with an example	6
	c)	**Explain** the circuit of pass logic function unit of a) NMOS b) Full CMOS TG	8
		OR	
8.	a)	**Explain** Tri-state pad **and** Bi-directional with neat diagrams and truth table.	6
	b)	**Explain** the circuit of psudo NMOS logic by taking an example of the Boolean function $Y = \overline{AB + C(D + E)}$	6
	c)	**Explain** the dynamic version of CVSL with an example. Also realize 2 input AND/NAND using CVSL	8

		Module-5	
9.	a)	**Explain** the CMOS SR Latch circuit based on NOR 2 input gates.	6
	b)	**Explain** the working of CMOS implementation of D-latch with neat circuit and timing diagram showing setup and hold time.	8
	c)	**Explain** the static behavior of the 2-inverter basic bistable element with neat circuit, schematic and voltage transfer curve	6
		OR	
10.	a)	**Draw** the diagram of 4-bit x 4-bit NOR based ROM array. **Explain** its functioning.	6
	b)	With necessary circuit diagram **explain** the operation of 3-transistor DRAM cell with pull-up and read/write circuitry and waveforms.	10
	c)	**Explain** the operation of 1-transistor DRAM cell with its access lines	4