VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI
Scheme of Teaching and Examinations – 2020 - 21
Choice Based Credit System (CBCS) and Outcome Based Education(OBE)

Programme: M.TECH IN ELECTRONICS (ELD)

I SEMESTER

Sl. No	Course	Course Code	Course Title	Teaching Hours /Week		Examination				Credits
				Theory	Practical/ Field work/ Assignment	Duration in hours	CIE Marks	SEE Marks	Total Marks	
1	PCC	20ELD11	Advanced Engineering Mathematics	04	--	03	40	60	100	4
2	PCC	20ECS12	Advanced Digital Signal Processing	04	--	03	40	60	100	4
3	PCC	20EVE13	Advanced EmbeddedSystem	04	--	03	40	60	100	4
4	PCC	20ELD14	Digital Circuits and Logic Design	04	--	03	40	60	100	4
5	PCC	20EVE15	Digital VLSI Design	04	--	03	40	60	100	4
6	PCC	20ELDL16	Embedded Systems Lab	-	04	03	40	60	100	2
7	PCC	20RMI17	Research Methodology and IPR	02	--	03	40	60	100	2
			TOTAL	**22**	**04**	**21**	**280**	**420**	**700**	**24**

Note: PCC: Professional core.

Internship: All the students have to undergo mandatory internship of 6 weeks during the vacation of I and II semesters and /or II and III semesters. A University examination shall be conducted during III semester and the

prescribed credit shall be counted for the same semester. Internship shall be considered as a head of passing and shall be considered for the award of degree. Those, who do not take-up/complete the internship shall be declared as fail in internship course and have to complete the same during the subsequent University examination after satisfying the internship requirements.
Note: (i) Four credit courses are designed for 50 hours Teaching – Learning process. (ii) Three credit courses are designed for 40 hours Teaching – Learning process.

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II SEMESTER

Sl. No	Course	Course Code	Course Title	Teaching Hours /Week		Examination				Credits
				Theory	Practical/ Field work/ Assignment/ Project	Duration in hours	CIE Marks	SEE Marks	Total Marks	
1	PCC	20ELD21	Advanced Computer Architecture	04	--	03	40	60	100	4
2	PCC	20EVE22	Real Time Operating System	04	--	03	40	60	100	4
3	PCC	20ECS23	Error Control Coding	04	--	03	40	60	100	4
4	PEC	20XXX24X	Professional elective 1	04	--	03	40	60	100	4
5	PEC	20XXX25X	Professional elective 2	04	--	03	40	60	100	4
6	PCC	20ELDL26	Digital Circuits Simulation Lab	--	04	03	40	60	100	2
7	PCC	20ELD27	Technical Seminar	--	02	--	100	--	100	2
TOTAL				**20**	**06**	**20**	**340**	**360**	**700**	**24**

Note: PCC: Professional core, PEC: Professional Elective.

Professional Elective 1		Professional Elective 2	
Course Code under 20XXX24X	**Course title**	**Course Code under 20XXX25X**	**Course title**
20ECS241	Wireless Sensor Networks	20EIE251	Automotive Electronics
20EVE242	Nanoelectronics	20EVE252	SoC Design
20ECS243	Cryptography and Network Security (20EVE334)	20ELD253	Micro Electro Mechanical Systems
20ELD244	Reconfigurable Computing	20ELD254	Advanced Control System (20EIE15)

Note:

1. Technical Seminar: CIE marks shall be awarded by a committee comprising of HoD as Chairman, Guide/co-guide, if any, and a senior faculty of the department. Participation in the seminar by all postgraduate students of the same and other semesters of the programme shall be mandatory.

The CIE marks awarded for Technical Seminar, shall be based on the evaluation of Seminar Report, Presentation skill and Question and Answer session in the ratio 50:25:25.

2. Internship: All the students shall have to undergo mandatory internship of 6 weeks during the vacation of I and II semesters and /or II and III semesters. A University examination shall be conducted during III semester and the prescribed credit shall be counted in the same semester. Internship shall be considered as a head of passing and shall be considered for the award of degree. Those, who do not take-up/complete the internship shall be declared as fail in internship course and have to complete the same during the subsequent University examination after satisfying the internship requirements.

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Choice Based Credit System (CBCS) and Outcome Based Education(OBE)

Programme: M.TECH IN ELECTRONICS (ELD)

III SEMESTER

Sl. No	Course	Course Code	Course Title	Teaching Hours /Week		Examination				Credits
				Theory	Practical/ Field work/ Assignment	Duration in hours	CIE Marks	SEE Marks	Total Marks	
1	PCC	20ELD31	Synthesis and Optimization ofDigital Circuits	04	--	03	40	60	100	4
2	PEC	20XXX32X	Professional elective 3	04	--	03	40	60	100	3
3	PEC	20XXX33X	Professional elective 4	04	--	03	40	60	100	3
4	Project	20ELD34	Project Work phase -1	--	02	--	100	--	100	2
5	PCC	20ELD35	Mini-Project	--	02	--	100	--	100	2
6	Internship	20ELDI36	Internship	(Completed during the intervening vacation of I and II semesters and /or II and III semesters.)		03	40	60	100	6
TOTAL				**12**	**02**	**12**	**260**	**240**	**500**	**20**

Note: PCC: Professional core, PEC: Professional Elective.

Professional elective 3		Professional elective 4	
Course Code under 20XXX32X	**Course title**	**Course Code under 20XXX33X**	**Course title**
20ECS321	Advances in Image Processing	20EVE331	VLSI Design for Signal Processing
20EVE322	CMOS RF Circuits Design	20ESP332	Pattern Recognition & Machine Learning
20ELD323	Business Intelligence and its Applications	20ECS333	Internet of Things
20ECS324	RF MEMS	20ESP334	Communication System Design using DSP Algorithms

Note:

1. Project Phase-1: Students in consultation with the guide/co-guide if any, shall pursue literature survey and complete the preliminary requirements of selected Project work. Each student shall prepare relevant introductory project document, and present a seminar.

CIE marks shall be awarded by a committee comprising of HoD as Chairman, Guide/co-guide if any, and a senior faculty of the department. The CIE marks awarded for project work phase -1, shall be based on the evaluation of Project Report, Project Presentation skill and Question and Answer session in the ratio 50:25:25.

SEE (University examination) shall be as per the University norms.

2. Internship: Those, who have not pursued /completed the internship shall be declared as fail in internship course and have to complete the same during subsequent University examinations after satisfying the internship requirements. Internship SEE (University examination) shall be as per the University norms.

VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI
Scheme of Teaching and Examinations – 2020 - 21
Choice Based Credit System (CBCS) and Outcome Based Education(OBE)

Programme: M.TECH IN ELECTRONICS (ELD)

IV SEMESTER

Sl. No	Course	Course Code	Course Title	Teaching Hours /Week		Examination				Credits
				Theory	Practical/ Field work/ Assignment	Duration in hours	CIE Marks	SEE Marks Viva voce	Total Marks	
1	Project	20ELD41	Project work phase -2	--	04	03	40	60	100	20
			TOTAL	--	**04**	**03**	**40**	**60**	**100**	**20**

Note:

1. Project Phase-2:

CIE marks shall be awarded by a committee comprising of HoD as Chairman, Guide/co-guide, if any, and a Senior faculty of the department. The CIE marks awarded for project work phase -2, shall be based on the evaluation of Project Report subjected to plagiarism check, Project Presentation skill and Question and Answer session in the ratio 50:25:25.

SEE shall be at the end of IV semester. Project work evaluation and Viva-Voce examination (SEE), after satisfying the plagiarism check, shall be as per the University norms.

VISVESVARAYA TECHNOLOGICAL UNIVERSITY BELAGAVI

Scheme of Teaching and Examinations and Syllabus
M.Techin Electronics (ELD)
(Effective from Academic year 2020 - 21)

M.TECH IN ELECTRONICS (ELD)

Choice Based Credit System (CBCS) and Outcome Based Education (OBE)
(Effective from the academic year 2020-21)

SEMESTER -I

ADVANCED ENGINEERING MATHEMATICS

CourseCode	**20ELD11**	CIEMarks	40
Lecture Hours/Week	**04**	SEE Marks	60
Total Number of LectureHours	**50**	Exam Hours	03
Credits - 04			

Module-1

Linear Algebra-I
Introduction to vector spaces and sub-spaces, definitions, illustrative example. Linearly independent and dependent vectors- Basis-definition and problems. Linear transformations-definitions. Matrix form of linear transformations-Illustrative examples (Text Book1).

Module-2

Linear Algebra-II
Computation of eigen values and eigen vectors of real symmetric matrices-Given's method. Orthogonal vectors and orthogonal bases. Gram-Schmidt orthogonalization process (Text Book1).

Module-3

Calculus of Variations
Concept of functional- Eulers equation. Functional dependent on first and higher order derivatives, Functional on several dependent variables. Isoperimetric problems-variation problems with moving boundaries. (TextBook2).

Module-4

Probability Theory: Review of basic probability theory. Definitions of random variables and probability distributions, probability mass and density functions, expectation, moments, central moments, characteristic functions, probability generating and moment generating functions-illustrations. Poisson, Gaussian and Erlang distributions examples (Text Book 3).

Module-5

Engineering Applications on Random processes: Classification. Stationary, WSS and ergodic random process. Auto-correlation function - properties, Gaussian random process (Text Book 3).

Course outcomes:

At the end of the course the student will be able to:

1. Understand vector spaces, basis, linear transformations and the process of obtaining matrix of linear transformations arising in magnification and rotation of images.
2. Apply the technique of singular value decomposition for data compression, least square approximation in solving inconsistent linear systems.
3. Utilize the concepts of functional and their variations in the applications of communication systems, decision theory, synthesis and optimization of digital circuits.
4. Learn the idea of random variables (discrete/continuous) and probability distributions in analyzing the probability models arising in control systems and system communications.
5. Analyze random process through parameter-dependent variables in various random processes.

Question paper pattern:

The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.

- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

Textbooks:

1. 'Linear Algebra and its Applications', David C Lay, Steven R Lay and J J McDonald, Pearson Education Ltd., 5th Edition, 2015
2. 'Differential Equations and Calculus of Variations', Elsgolts L, MIR Publications, 3rd Edition, 1977
3. 'Probability, Statistics and Random Process', T Veerarajan, Tata Mc-Graw Hill Co., 3rd Edition, 2016

Reference Books:

1. 'Introduction to Linear Algebra', Gilbert Strang, Wellesley-Cambridge Press, 5th Edition, 2016
2. 'Schaum's Outlines of Theory and Problems of Matrix Operations', Richard Bronson, McGraw-Hill, 1988
3. 'Probability and Random Process with application to Signal Processing', Scott L Miller, Donald G Childers, Elsevier Academic Press, 2nd Edition, 2013

Advanced Digital Signal Processing

CourseCode	**20ECS12**	CIEMarks	40
Lecture Hours/Week	**04**	SEE Marks	60
Total Number of LectureHours	**50**	Exam Hours	03
Credits - 04			

Module-1

Multirate Digital Signal Processing: Introduction, decimation by a factor 'D', Interpolation by a factor 'I', sampling rate conversion by a factor 'I/D', Implementation of sampling rate conversion, Multistage implementation of sampling rate conversion, Applications of multirate signal processing, Digital filter banks, two channel quadrature mirror filter banks, M-channel QMF bank (Text 1).

Module-2

Linear prediction and Optimum Linear Filters: Random signals, Correlation Functions and Power Spectra, Innovations Representation of a Stationary Random Process. Forward and Backward Linear Prediction. Solution of the Normal Equations. The Levinson-Durbin Algorithm. Properties of the Linear Prediction-Error Filters (Text 1).

Module-3

Adaptive filters: Applications of Adaptive Filters-Adaptive Channel Equalization, Adaptive noise cancellation, Linear Predictive coding of Speech Signals, Adaptive direct form FIR filters-The LMS algorithm, Properties of LMS algorithm. Adaptive direct form filters- RLS algorithm (Text 1).

Module-4

Power Spectrum Estimation: Non parametric Methods for Power Spectrum Estimation - Bartlett Method, Welch Method, Blackman and Tukey Methods.
Parametric Methods for Power Spectrum Estimation: Relationship between the auto correlation and the model parameters, Yule and Walker methods for the AR Model Parameters, Burg Method for the AR Model parameters, Unconstrained least-squares method for the AR Model parameters, Sequential estimation methods for the AR Model parameters, ARMA Model for Power Spectrum Estimation (Text 1).

Module-5

WAVELET TRANSFORMS: The Age of Wavelets, The origin of Wavelets, Wavelets and other reality transforms, History of wavelets, Wavelets of the future.

Continuous Wavelet and Short Time Fourier Transform: Wavelet Transform, Mathematical preliminaries, Properties of wavelets.

Discrete Wavelet Transform: Haar scaling functions, Haar wavelet function, Daubechies Wavelets (Chapters 1, 3 & 4 of Text 2).

Course outcomes:

At the end of the course the student will be able to:

1. Design adaptive filters for a given application
2. Design multirate DSP Systems
3. Implement adaptive signal processing algorithm
4. Design active networks
5. Understand advanced signal processing techniques, including multi-rate processing and time-frequency analysis techniques

Question paper pattern:

The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.

- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

Textbooks:

1. 'Digital Signal Processing, Principles, Algorithms and Applications', John G. Proakis, Dimitris G.Manolakis, Pearson, Fourth edition, 2007
2. 'Insight into Wavelets- from Theory to Practice', K P Soman, Ramachandran, Resmi, PHI, Third Edition, 2010

Advanced Embedded System

CourseCode	**20EVE13**	CIEMarks	40
Lecture Hours/Week	**04**	SEE Marks	60
Total Number of LectureHours	**50**	Exam Hours	03
Credits - 04			

Module-1

Embedded System: Embedded vs General computing system, classification, application and purpose of ES. Core of an Embedded System, Memory, Sensors, Actuators, LED, Opto coupler, Communication Interface, Reset circuits, RTC, WDT, Characteristics and Quality Attributes of Embedded Systems (Text 1: Selected Topics from Ch -1, 2, 3).

Module-2

Hardware Software Co-Design, embedded firmware design approaches, computational models, embedded firmware development languages, Integration and testing of Embedded Hardware and firmware, Components in embedded system development environment (IDE), Files generated during compilation, simulators, emulators and debugging (Text 1: Selected Topics from Ch-7, 9, 12, 13).

Module-3

ARM-32 bit Microcontroller: Thumb-2 technology and applications of ARM, Architecture of ARM Cortex M3, Various Units in the architecture, General Purpose Registers, Special Registers, exceptions, interrupts, stack operation, reset sequence (Text 2: Ch 1, 2, 3).

Module-4

Instruction Sets: Assembly basics, Instruction list and description, useful instructions, Memory Systems, Memory maps, Cortex M3 implementation overview, pipeline and bus interface (Text 2: Ch-4, 5, 6).

Module-5

Exceptions, Nested Vector interrupt controller design, Systick Timer, Cortex-M3 Programming using assembly and C language, CMSIS (Text 2: Ch-7, 8, 10).

Course outcomes:

At the end of the course the student will be able to:

1. Understand the basic hardware components and their selection method based on the characteristics and attributes of an embedded system.
2. Explain the hardware software co-design and firmware design approaches.
3. Understand the suitability of the instruction sets of ARM processors to design of embedded systems.
4. Acquire the knowledge of the architectural features of ARM CORTEX M3, a 32-bit microcontroller including memory map, interrupts and exceptions.
5. Apply the knowledge gained for Programming ARM CORTEX M3 for different applications.

Question paper pattern:

The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.

- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

Students have to conduct the following experiments as a part of CIE marks along with other Activities:

ARM Cortex M3 Programs - Programming to be done using Keil uVision 4 and download the program on to a M3 evaluation board such as NXP LPC1768 or ATMEL ARM

a) Write an Assembly language program to calculate the sum and display the result for the addition of first ten numbers. SUM = 10+9+8+.....+1

b) Write an Assembly language program to store data in RAM

c) Write a C program to output the “Hello World” message using UART

d) Write a C program to operate a buzzer using Cortex M3

e) Write a C program to display the temperature sensed using Cortex M3.

f) Write a C program to control stepper motor using Cortex M3.

Textbooks:

1. 'Introduction to embedded systems', K. V. Shibu, TMH education Pvt. Ltd., 2009
2. 'The Definitive Guide to the ARM Cortex-M3', Joseph Yiu, Newnes, (Elsevier), 2nd edn, 2010.

Reference Book:

'Embedded systems - A contemporary design tool', James K. Peckol, John Wiley, 2008

Digital Circuits and Logic Design

CourseCode	**20ELD14**	CIEMarks	40
Lecture Hours/Week	**04**	SEE Marks	60
Total Number of LectureHours	**50**	Exam Hours	03
Credits - 04			

Module-1

Threshold Logic: Introductory Concepts, Synthesis of Threshold Networks, Capabilities, Minimization, and Transformation of Sequential Machines: The Finite- State Model, Further Definitions, Capabilities.

Module-2

Fault Detection by Path Sensitizing, Detection of Multiple Faults, Failure-Tolerant Design, Quadded Logic, ReliableDesign and Fault Diagnosis Hazards: Fault Detection inCombinational Circuits.

Module-3

Fault-Location Experiments, Boolean Differences, Limitations ofFinite – State Machines, State Equivalence and MachineMinimization, Simplification of Incompletely SpecifiedMachines.

Module-4

Structure of Sequential Machines: Introductory Example, State Assignments Using Partitions, The Lattice of closed Partitions,Reductions of the Output Dependency, Input Independenceand Autonomous Clocks, Covers and Generation of closedPartitions by state splitting, Information Flow in SequentialMachines, decompositions, Synthesis of Multiple Machines.

Module-5

State Identifications and Fault-Detection Experiments: HomingExperiments, Distinguishing Experiments, MachineIdentification, Fault Detection Experiments, Design ofDiagnosable Machines, Second Algorithm for the Design ofFault Detection Experiments, Fault-Detection.

Course outcomes:

At the end of the course the student will be able to:

1.Understand the concepts of sequential machines.
2. Design Sequential Machines/Circuits.
3. Analyze the faults in the design of circuits.
4.Apply fault detection experiments to sequential circuits.
5.Comprehend the structure of sequential machines.

Question paper pattern:

The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.

- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

Textbook:

'Switching and Finite Automata Theory', ZviKohavi, TMH,ISBN: 978_0_07_099387_7, 2nd Edition, 2008.

Reference Books:

1. 'Digital Circuits and logic Design', Charles Roth Jr., CengageLearning, 7th edition, 2014.
2. 'Fault Tolerant and Fault Testable Hardware Design',Parag K Lala,Prentice Hall Inc. 1985.
3. 'Introductory Theory of Computer', E. V. Krishnamurthy, MacmillanPress Ltd, 1983
4. 'Theory of computer science – Automata,Languages and Computation', Mishra & Chandrasekaran, 2nd Edition, PHI, 2004.

Digital VLSI Design

CourseCode	**20EVE15**	CIEMarks	40
Lecture Hours/Week	**04**	SEE Marks	60
Total Number of LectureHours	**50**	Exam Hours	03
Credits - 04			

Module-1

MOS Transistor: The Metal Oxide Semiconductor (MOS) Structure, The MOS System under External Bias, Structure and Operation of MOS Transistor, MOSFET Current-Voltage Characteristics, MOSFET Scaling and Small-Geometry Effects.

MOS Inverters-Static Characteristics: Introduction, Resistive-Load Inverter, Inverters with nType MOSFET Load.

Module-2

MOS Inverters-Static Characteristics: CMOS Inverter.

MOS Inverters: Switching Characteristics and Interconnect Effects: Introduction, Delay-Time Definition, Calculation of Delay Times, Inverter Design with Delay Constraints, Estimation of Interconnect Parasitics, Calculation of Interconnect Delay, Switching Power Dissipation of CMOS Inverters.

Module-3

Semiconductor Memories: Introduction, Dynamic Random Access Memory (DRAM), Static Random Access Memory (SRAM), Nonvolatile Memory, Flash Memory, Ferroelectric Random Access Memory (FRAM)

Module-4

Dynamic Logic Circuits: Introduction, Basic Principles of Pass Transistor Circuits, Voltage Bootstrapping, Synchronous Dynamic Circuit Techniques, Dynamic CMOS Circuit Techniques, High
Performance Dynamic CMOS circuits.

BiCMOS Logic Circuits: Introduction, Bipolar Junction Transistor (BJT): Structure and Operation, Dynamic Behavior of BJTs, Basic BiCMOS Circuits: Static Behavior, Switching Delay in BiCMOS Logic Circuits, BiCMOS Applications.

Module-5

Chip Input and Output (I/O) Circuits: Introduction, ESD Protection, Input Circuits, Output Circuits and L(di/dt) Noise, On-Chip Clock Generation and Distribution, Latch-Up and Its Prevention.

Design for Manufacturability: Introduction, Process Variations, Basic Concepts and Definitions, Design of Experiments and Performance Modeling.

Course outcomes:

At the end of the course the student will be able to:

1. Analyse issues of On-chip interconnect Modelling and Interconnect delay calculation.
2. Analyse the Switching Characteristics in Digital Integrated Circuits.
3. Use the Dynamic Logic circuits in state-of-the-art VLSI chips.
4. Study critical issues such as ESD protection, Clock distribution, Clock buffering, and Latch phenomenon
5. Use Bipolar and Bi-CMOS circuits in very high speed design.

Question paper pattern:

The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.

- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

Textbook:

'CMOS Digital Integrated Circuits: Analysis and Design', Sung Mo Kang & Yusuf Leblebici, Tata McGraw-Hill, Third Edition

Reference Books:

1. 'Principles of CMOS VLSI Design: A System Perspective', Neil Weste and K. Eshraghian, Pearson Education (Asia) Pvt. Ltd., Second Edition, 2000
2. 'Modern VLSI Design: System on Silicon', Wayne, Wolf, Prentice Hall PTR/ Pearson Education, Second Edition, 1998
3. 'Basic VLSI Design', Douglas A Pucknell& Kamran Eshraghian, PHI, 3rdEdition (original Edition 1994)

Embedded Systems Lab

CourseCode	**20ELDL16**	CIEMarks	40
Teaching Hours/Week	**04** (2 Hrs Tutorial + 2 Hrs Practical)	SEE Marks	60
		Exam Hours	03
Credits - 02			

Part A: EDA

Using Cadence OrCAD or OrCAD Lite or any EDA Tool, design and verify the following:

Sl.No	Experiments
1	3½ Digit Digital Voltmeter
2	Monolithic function Generator
3	Regulated Power supplies
4	Batch counter using TTL ICs
5	DAC and ADC
6	P, PI, PID and ON/OFF Controllers
7	Programmable Timers
8	Filters and Resonance Circuits

PART-B: ARM-CORTEX M3

[Programming to be done using Keil uVision 4 and download theprogram on to a M3 evaluation board such as NXP LPC1768 orATMEL ATSAM3U]

1	Write an Assembly language program to calculate 10+9+8+.....+1
2	Write an Assembly language program to link Multiple object files and link them together.
3	Write an Assembly language program to store data in RAM.
4	Write a C program to Output the "Hello World" message using UART.
5	Write a C program to Design a Stopwatch using interrupts.

6	Write an Exception vector table in C
7	Write an Assembly Language Program for locking a Mutex.
8	Write a SVC handler in C. Use the wrapper code to extract the correct stack frame starting location. The C handler can then use this to extract the stackedPC location and the stacked register values.

Course outcomes:

At the end of the course the student will be able to:

1. Understand the computer aided design tools for the electronic circuit designs.
2. Design and verify analogcircuits such as ADC, DAC, Controllers, etc. using simulation tools
3. Create and verify digital systems using Cadence OrCAD, OrCAD Lite or any EDA tool.
4. Develop assembly programs for different applications using ARM Cortex M3 and Keil uVision-4 tool.
5. Develop C Programs for different applications using ARM-Cortex M3 and Keil uVision-4 tool.

Conduct of Practical Examination:

1. All laboratory experiments are to be included for practical examination.
2. For examination, two questions using different tool to be set.
3. Students are allowed to pick one experiment from the lot.
4. Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.
5. Change of experiment is allowed only once and Marks allotted to the procedure part to be made zero.

Research Methodology and IPR

CourseCode	**20RMI17**	CIEMarks	40
Lecture Hours/Week	**02**	SEE Marks	60
		Exam Hours	03
Credits - 02			

Module-1

Research Methodology: Introduction, Meaning of Research, Objectives of Research, Motivation in Research, Types of Research, Research Approaches, Significance of Research, Research Methods versus Methodology, Research and Scientific Method, Importance of Knowing How Research is Done, Research Process, Criteria of Good Research, and Problems Encountered by Researchers in India.

Defining the Research Problem: Research Problem, Selecting the Problem, Necessity of Defining the Problem, Technique Involved in Defining a Problem, An Illustration.

Module-2

Reviewing the literature: Place of the literature review in research, Bringing clarity and focus to your research problem, Improving research methodology, Broadening knowledge base in research area, Enabling contextual findings, How to review the literature, searching the existing literature, reviewing the selected literature, Developing a theoretical framework, Developing a conceptual framework, Writing about the literature reviewed.

Research Design: Meaning of Research Design, Need for Research Design, Features of a Good Design, Important Concepts Relating to Research Design, Different Research Designs, Basic Principles of Experimental Designs, Important Experimental Designs.

Module-3

Design of Sampling: Introduction, Sample Design, Sampling and Non-sampling Errors, Sample Survey versus Census Survey, Types of Sampling Designs.

Measurement and Scaling: Qualitative and Quantitative Data, Classifications of Measurement Scales, Goodness of Measurement Scales, Sources of Error in Measurement Tools, Scaling, Scale Classification Bases, Scaling Technics, Multidimensional Scaling, Deciding the Scale.

Data Collection: Experimental and Surveys, Collection of Primary Data, Collection of Secondary Data, Selection of Appropriate Method for Data Collection, Case Study Method.

Module-4

Testing of Hypotheses: Hypothesis, Basic Concepts Concerning Testing of Hypotheses, Testing of Hypothesis, Test Statistics and Critical Region, Critical Value and Decision Rule, Procedure for Hypothesis Testing, Hypothesis Testing for Mean, Proportion, Variance, for Difference of Two Mean, for Difference of Two Proportions, for Difference of Two Variances, P-Value approach, Power of Test, Limitations of the Tests of Hypothesis.
Chi-square Test: Test of Difference of more than Two Proportions, Test of Independence of Attributes, Test of Goodness of Fit, Cautions in Using Chi Square Tests.

Module-5

Interpretation and Report Writing: Meaning of Interpretation, Technique of Interpretation, Precaution in Interpretation, Significance of Report Writing, Different Steps in Writing Report, Layout of the Research Report, Types of Reports, Oral Presentation, Mechanics of Writing a Research Report, Precautions for Writing Research Reports.
Intellectual Property: The Concept, Intellectual Property System in India, Development of TRIPS Complied Regime in India, Patents Act, 1970, Trade Mark Act, 1999,The Designs Act, 2000, The Geographical Indications of Goods (Registration and Protection) Act1999, Copyright Act,1957,The Protection of Plant Varieties and Farmers' Rights Act, 2001,The Semi-Conductor Integrated Circuits Layout Design Act, 2000, Trade Secrets, Utility Models, IPR and Biodiversity, The Convention on Biological Diversity (CBD) 1992, Competing Rationales for Protection of IPRs, Leading International Instruments Concerning IPR, World Intellectual Property Organisation (WIPO),WIPO and WTO, Paris Convention for the Protection of Industrial Property, National Treatment, Right of Priority, Common Rules, Patents, Marks, Industrial Designs, Trade Names, Indications of Source, Unfair Competition, Patent Cooperation Treaty (PCT), Advantages of PCT Filing, Berne Convention for the Protection of Literary and Artistic Works, Basic Principles, Duration of Protection, Trade Related Aspects of Intellectual Property Rights (TRIPS) Agreement, Covered under TRIPS Agreement, Features of the Agreement, Protection of Intellectual Property under TRIPS, Copyright and Related Rights, Trademarks, Geographical indications, Industrial Designs, Patents, Patentable Subject Matter, Rights Conferred, Exceptions, Term of protection, Conditions on Patent Applicants, Process Patents, Other Use without Authorization of the Right Holder, Layout-Designs of Integrated Circuits, Protection of Undisclosed Information, Enforcement of Intellectual Property Rights, UNSECO.

Course outcomes:

At the end of the course the student will be able to:

1. Discuss research methodology and the technique of defining a research problem
2. Explain the functions of the literature review in research, carrying out a literature search, developing theoretical and conceptual frameworks and writing a review.
3. Explain various research designs, sampling designs, measurement and scaling techniques and also different methods of data collections.
4. Explain several parametric tests of hypotheses, Chi-square test, art of interpretation and writing research reports
5. Discuss various forms of the intellectual property, its relevance and business impact in the changing global business environment and leading International Instruments concerning IPR.

Question paper pattern:

The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.

- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

Textbooks:

1. 'Research Methodology: Methods and Techniques', C.R. Kothari, Gaurav Garg, New Age International, 4th Edition, 2018
2. 'Research Methodology a step-by-step guide for beginners. (For the topic Reviewing the literature under module 2)', Ranjit Kumar, SAGE Publications, 3rd Edition, 2011
3. Study Material (For the topic Intellectual Property under module 5) Professional Programme Intellectual Property Rights, Law and Practice, The Institute of Company Secretaries of India, Statutory Body Under an Act of Parliament, September 2013.

Reference Books:

1. ‘Research Methods: the concise knowledge base’, Trochim, Atomic Dog Publishing, 2005
2. ‘Conducting Research Literature Reviews: From the Internet to Paper’, Fink A, Sage Publications, 2009

M.TECH IN DIGITAL ELECTRONICS / ELECTRONICS (ELD)

Choice Based Credit System (CBCS) and Outcome Based Education(OBE)
(Effective from the academic year 2020-21)

SEMESTER -II

Advanced Computer Architecture

CourseCode	**20ELD21**	CIEMarks	40
Lecture Hours/Week	**04**	SEE Marks	60
Total Number of LectureHours	**50**	Exam Hours	03
Credits - 04			

Module-1

Parallel Computer Models: The State of Computing, Multiprocessors and multicomputers, Multivector and SIMD computers.

Program and Network Properties: Conditions of parallelism, Program Partitioning & Scheduling, Program Flow Mechanisms.

Module-2

Principles of Scalable Performance: Performance Metrics and Measures, Parallel Processing Applications, Speedup Performance Laws, Scalability Analysis and Approaches.

Processors & Memory Hierarchy: Advanced processor technology, Super Scalars & Vector Processors, Memory Hierarchy Technology, Virtual Memory Technology.

Module-3

Bus, Cache and Shared Memory: Bus Systems, Cache Memory Organizations, Shared Memory Organizations, Sequential & Weak Consistency Model.

Pipelining & Superscalar Technologies: Linear Pipeline Processors, Nonlinear Pipeline Processors, Instruction Pipeline Design, Arithmetic Pipeline Design, Superscalar Pipeline Design.

Module-4

Multivector& SIMD Computers: Vector Processing principles, Multivector Multiprocessors, Compound Vector Processing, SIMD Computer Organization.

Scalable, Multithreaded and Data Flow Computers: Latency Hiding Techniques, Principles of Multithreading, Fine Grain Multi Computers, Scalable and Multithreaded Architectures, Data Flow and Hybrid Architectures.

Module-5

Parallel Models, Languages and Compilers: Parallel Programming Models, Parallel Languages & Compilers, Dependence Analysis and Data Arrays, Code Optimization and Scheduling, Loop Parallelization and Pipelining.
Parallel Program Development and Environments: Parallel Programming Environments, Synchronization and Multi Processor Modes, Shared Variable Program Structures.

Course outcomes:
At the end of the course the student will be able to:

1. Understand the basic concepts for parallel processing
2. Analyze program partitioning and flow mechanisms
3. Apply pipelining concept for the performance evaluation
4. Learn the advanced processor architectures for suitable applications
5. Understand parallel Programming

Question paper pattern:
The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.

- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

Textbook:

'Advanced Computer Architecture: Parallelism, Scalability, Programmability', Kai Hwang & Narendra Jotwani,McGraw Hill Education, ISBN:978-93-392-2092-1, 3rdEdition,2016

Reference Books:

1. 'Computer Architecture, Pipelined and Parallel Processor Design', M.J. Flynn, Narosa Publishing, 2002.
2. 'Parallel programming in C with MPI and OpenMP', Michael J Quinn, Tata McGraw Hill, 2013.
3. 'An Introduction to Parallel Computing: Design and Analysis of Algorithms', Ananth Grama, Pearson, 2nd Edition, 2004.

Real Time Operating System

CourseCode	**20EVE22**	CIEMarks	40
Lecture Hours/Week	**04**	SEE Marks	60
Total Number of LectureHours	**50**	Exam Hours	03
Credits - 04			

Module-1

Real-Time Systems and Resources: Brief history of Real Time Systems, A brief history of Embedded Systems. System Resources, Resource Analysis, Real-Time Service Utility, Scheduler concepts, Real-Time OS, State transition diagram and tables, Thread Safe Reentrant Functions (Text 1: Selected sections from Chap. 1, 2).

Module-2

Processing with Real Time Scheduling: Scheduler Concepts, Preemptive Fixed Priority Scheduling Policies with timing diagrams and problems and issues, Feasibility, Rate Monotonic least upper bound, Necessary and Sufficient feasibility, Deadline –Monotonic Policy, Dynamic priority policies, Alternative to RM policy (Text 1: Chap. 2,3,7).

Module-3

Memory and I/O: Worst case execution time, Intermediate I/O, Shared Memory, ECC Memory, Flash file systems. Multi-resource Services, Blocking, Deadlock and live lock, Critical sections to protect shared resources, Missed deadline, QoS, Reliability and Availability, Similarities and differences, Reliable software, Available software (Text 1: Selected topics from Chap. 4,5,6,7,11).

Module-4

Firmware Components: The 3 firmware components, RTOS system software mechanisms, Software application components. Debugging Components, Exceptions, assert, Checking return codes, Single-step debugging, Test access ports, Trace Ports (Text 1: Selected topics from Chap. 8,9).

Module-5

Process and Threads: Process and thread creations, Programs related to semaphores, message queue, shared buffer applications involving inter task/thread communication (Text 2: Chap. 11).

Course outcomes:

At the end of the course the student will be able to:

1. Develop programs for real time services, firmware and RTOS, using the fundamentals of Real Time Embedded System, real time service utilities, debugging methodologies and optimization techniques.
2. Select the appropriate system resources (CPU, I/O, Memory, Cache, ECC Memory, Microcontroller/ FPGA/ ASIC to improve the system performance.
3. Apply priority based static and dynamic real time scheduling techniques for the given specifications.
4. Analyze deadlock conditions, shared memory problem, critical section problem, missed deadlines, availability, reliability and QoS.
5. Develop programs for multithreaded applications using suitable techniques and data structure

Question paper pattern:

The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.

- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

Textbooks:

1. 'Real-Time Embedded Systems and Components', Sam Siewert, Cengage Learning, India Edition, 2007.
2. 'Embedded/Real Time Systems, Concepts, Design and Programming, Black Book', Dr. K.V.K.K Prasad, Dream Tech Press, New edition, 2010.

Reference Books:

1. 'Real Time System', James W S Liu, Pearson Education, 2008.
2. 'Programming for Embedded Systems', Dream Tech Software Team, John Wiley, India Pvt. Ltd., 2008.

Error Control Coding

CourseCode	**20ECS23**	CIEMarks	40
Lecture Hours/Week	**04**	SEE Marks	60
Total Number of LectureHours	**50**	Exam Hours	03
Credits - 04			

Module-1

Information theory: Introduction, Entropy, Source coding theorem, discrete memoryless channel, Mutual Information, Channel Capacity Channel coding theorem (Chap. 5 of Text 1).

Introduction to algebra: Groups, Fields, binary field arithmetic, Construction of Galois Fields GF (2^m) and its properties, (Only statements of theorems without proof) Computation using Galois field GF (2^m) arithmetic, Vector spaces and Matrices (Chap. 2 of Text 2).

Module-2

Linear block codes: Generator and parity check matrices, Encoding circuits, Syndrome and error detection, Minimum distance considerations, Error detecting and error correcting capabilities, Standard array and syndrome decoding, Single Parity Check Codes (SPC),Repetition codes, Self dual codes, Hamming codes, Reed-Muller codes. Product codes and Interleaved codes(Chap. 3 of Text 2).

Module-3

Cyclic codes: Introduction, Generator and parity check polynomials, Encoding of cyclic codes, Syndrome computing and error detection, Decoding of cyclic codes, Error trapping Decoding, Cyclic hamming codes, Shortened cyclic codes (Chap. 4 of Text2).

Module-4

BCH codes: Binary primitive BCH codes, Decoding procedures, Implementation of Galois field arithmetic. (6.1,6.2,6.7 of Text 2) Primitive BCH codes over GF (q),

Reed -Solomon codes (7.2,7.3 of Text 2).

Majority Logic decodable codes: One -step majority logic decoding, Multiple-step majority logic (8.1,8.4 of Text 2).

Module-5

Convolution codes: Encoding of convolutional codes: Systematic and Nonsystematic Convolutional Codes, Feedforward encoder inverse, A

catastrophic encoder, Structural properties of convolutional codes: state diagram, state table, state transition table, tree diagram, trellis diagram.
Viterbi algorithm, Sequential decoding: Log Likelihood Metric for Sequential Decoding (11.1,11.2, 12.1,13.1 of Text 2).

Course outcomes:
At the end of the course the student will be able to:
1. Understand the concept of the Entropy, information rate and capacity for the Discrete memoryless channel.
2. Apply modern algebra and probability theory for the coding.
3. Compare Block codes such as Linear Block Codes, Cyclic codes, etc. and Convolutional codes.
4. Detect and correct errors for different data communication and storage systems.
5. Analyze and implement different Block code encoders and decoders, and also convolutional encoders and decoders including soft and hard Viterbi algorithm.

Question paper pattern:
The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.
- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

Students have to conduct the following experiments as a part of CIE marks along with other Activities:
Software to be used: SCILAB/MATLAB

1. Simulate the BER performance of (7, 4) Hamming code on AWGN channel. Use QPSK modulation scheme. Channel decoding is to be performed through maximum-likelihood decoding. Plot the bit error rate versus SNR (dB), i.e. $P_{e,b}$ versus E_b/N_0.Consider binary input vector of size 5 lakh bits. Use the following parity check matrix for the (7, 4) Hamming code.

$$H = \begin{bmatrix} 1001110 \\ 0100111 \\ 0011101 \end{bmatrix}$$

Also find the coding gain.
(Refer: http://www.dsplog.com/2012/03/15/hamming-code-soft-hard-decode/)

2. Simulate the BER performance of (2, 1, 3) binary convolutional code with generator sequences $g^{(1)}$ =(1 0 1 1) and $g^{(2)}$ =(1 1 1 1) on AWGN channel. Use QPSK modulation scheme. Channel decoding is to be performed through Viterbi decoding. Plot the bit error rate versus SNR(dB), i.e. $P_{e,b}$ versus E_b/N_0.Consider binary input vector of size 3 lakh bits. Also find the coding gain.

3. Simulate the BER performance of rate 1/3 Turbo code. Turbo encoder uses two recursive systematic encoders with $G(D) = \left[1, \frac{1+D^4}{1+D+D^2+D^3+D^4}\right]$ and pseudo-random interleaver. Use QPSK modulation scheme. Channel decoding is to be performed through maximum a-posteriori (MAP) decoding algorithm. Plot the bit error rate versus SNR(dB), i.e. $P_{e,b}$ versus E_b/N_0.Consider binary input vector of size of around 3 lakh bits and the block length as 10384 bits. Also find the coding gain.

4. Use a MATLAB simulation to confirm that SOVA (Soft Output Viterbi Algorithm) is inferior to MAP decoding in terms of bit error performance, and give the reason why. Consider a rate ½ Turbo code punctured from the rate 1/3 Turbo code. The puncturing matrix is [1 0 ; 0 1] . Demonstrate the decoding process of the code. (Refer: Example 6.1 from 'A Practical Guide to Error-control Coding Using MATLAB', Yuan Jiang, ISBN: 9781608070886, Artech House Publishers, 2010)

Textbooks:

1. 'Digital Communication systems', Simon Haykin, Wiley India Private. Ltd, ISBN 978-81-265-4231-4, First edition, 2014
2. 'Error control coding', Shu Lin and Daniel J. Costello. Jr, Pearson, Prentice Hall, 2nd edition, 2004

Reference Books:

1. 'Theory and practice of error control codes', Blahut. R. E, Addison Wesley, 1984
2. 'Introduction to Error control coding', Salvatore Gravano, Oxford University Press, 2007
3. 'Digital Communications - Fundamentals and Applications', Bernard Sklar, Pearson Education (Asia) Pvt. Ltd., 2nd Edition, 2001

Professional Elective 1

Wireless Sensor Networks

CourseCode	**20ECS241**	CIEMarks	40
Lecture Hours/Week	**04**	SEE Marks	60
Total Number of LectureHours	**50**	Exam Hours	03
Credits - 04			

Module-1

Introduction: Sensor Mote Platforms, WSN Architecture and Protocol Stack (Chap. 1Text 1).
WSN Applications: Military Applications, Environmental Applications, Health Applications, Home Applications, Industrial Applications (Chap. 2 Text 1).

Module-2

Factors Influencing WSN Design: Hardware Constraints Fault Tolerance Scalability Production Costs WSN Topology, Transmission Media, Power Consumption (Chap. 3 Text 1).
Physical Layer: Physical Layer Technologies, Overview of RF Wireless Communication, Channel Coding (Error Control Coding), Modulation, Wireless Channel Effects, PHY Layer Standards (Chap. 4 of Text 1).

Module-3

Medium Access Control: Challenges for MAC, CSMA Mechanism, Contention-Based Medium Access, Reservation-Based Medium Access, Hybrid Medium Access (Chap. 5 of Text 1).
Network Layer: Challenges for Routing, Data-centric and Flat Architecture Protocols, Hierarchical Protocols, Geographical Routing Protocols (Chap. 7 of Text 1).

Module-4

Transport Layer: Challenges for Transport Layer, Reliable MultiSegment Transport (RMST) Protocol, Pump Slowly, Fetch Quickly (PSFQ) Protocol, Congestion Detection and Avoidance (CODA) Protocol, Event-to-Sink Reliable Transport (ESRT) Protocol, GARUDA (Chap. 8 Text 1).

Application Layer: Source Coding (Data Compression), Query Processing, Network Management (Chap. 9 Text 1).

Module-5

Time Synchronization: Challenges for Time Synchronization, Network Time Protocol, Timing-Sync Protocol for Sensor Networks (TPSN), Reference-Broadcast Synchronization (RBS), Adaptive Clock Synchronization (ACS) (Chap. 11 of Text1).

Localization; Challenges in Localization, Ranging Techniques, Range-Based Localization Protocols, Range-Free Localization Protocols. (Chap. 12 Text 1).

Course outcomes:

At the end of the course the student will be able to:

1. Acquire knowledge of characteristics of mobile/wireless communication channels
2. Apply statistical models of multipath fading
3. Understand the multiple radio access techniques, radio standards and communication protocols to be used for wireless sensor
4. Design wireless sensor network system for different applications under consideration.
5. Understand the hardware details of different types of sensors and select right type of sensor for various applications.

Question paper pattern:

The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.

- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

Textbooks:

1. 'Wireless Sensor Networks', Ian F. Akyildiz and Mehmet Can Vuran, John Wiley & Sons Ltd. ISBN 978-0-470-03601-3 (H/B), 2010
2. 'Wireless Sensor Networks:Signal Processing and Communications Perspectives', Ananthram Swami, et. al., John Wiley & Sons Ltd., ISBN 978-0470-03557-3, 2007

Nanoelectronics

CourseCode	**20EVE242**	CIEMarks	40
Lecture Hours/Week	**04**	SEE Marks	60
Total Number of LectureHours	**50**	Exam Hours	03
Credits - 04			

Module-1

Introduction: Overview of nanoscience and engineering. Development milestones in microfabrication and electronic industry. Moores' law and continued miniaturization, Classification of Nanostructures, Electronic properties of atoms and solids: Isolated atom, Bonding between atoms, Giant molecular solids, Free electron models and energy bands, crystalline solids, Periodicity of crystal lattices, Electronic conduction, effects of nanometer length scale, Fabrication methods: Top down processes, Bottom up processes methods for templating the growth of nanomaterials, ordering of nanosystems (Text 1).

Module-2

Characterization: Classification, Microscopic techniques, Field ion microscopy, scanning probe techniques, diffraction techniques: bulk and surface diffraction techniques, spectroscopy techniques: photon, radiofrequency, electron, surface analysis and dept profiling: electron, mass, Ion beam, Reflectometry, Techniques for property measurement: mechanical, electron, magnetic, thermal properties (Text1).

Module-3

Inorganic semiconductor nanostructures: overview of semiconductor physics. Quantum confinement in semiconductor nanostructures: quantum wells, quantum wires, quantum dots, super-lattices, band offsets, electronic density of states (Text1).
Carbon Nanostructures: Carbon molecules, Carbon Clusters, Carbon Nanotubes, application of Carbon Nanotubes (Text 2).

Module-4

Fabrication techniques: requirements of ideal semiconductor, epitaxial growth of quantum wells, lithography and etching, cleaved-edge over growth, growth of vicinal substrates, strain induced dots and wires, electrostatically induced dots and wires, Quantum well width fluctuations, thermally annealed quantum

wells, semiconductor nanocrystals, colloidal quantum dots, self-assembly techniques.

Physical processes: modulation doping, quantum hall effect, resonant tunneling, charging effects, ballistic carrier transport, Inter band absorption, intra band absorption, Light emission processes, phonon bottleneck, quantum confined stark effect, nonlinear effects, coherence and dephasing, characterization of semiconductor nanostructures: optical electrical and structural (Text1).

Module-5

Methods of measuring properties: atomic, crystallography, microscopy, spectroscopy (Text 2).

Applications: Injection lasers, quantum cascade lasers, single-photon sources, biological tagging, optical memories, coulomb blockade devices, photonic structures, QWIPs, NEMS, MEMS (Text1).

Course outcomes:

At the end of the course the student will be able to:

1. Know the principles behind Nanoscience engineering and Nanoelectronics.
2. Apply the knowledge to prepare and characterize nanomaterials.
3. Know the effect of particles size on mechanical, thermal, optical and electrical properties of nanomaterials.
4. Design the process flow required to fabricate state of the art transistor technology.
5. Analyze the requirements for new materials and device structure in the future technologies.

Question paper pattern:

The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.

- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

Textbooks:

1. 'Nanoscale Science and Technology', Ed Robert Kelsall, Ian Hamley, Mark Geoghegan, John Wiley, 2007
2. 'Introduction to Nanotechnology', Charles P Poole, Jr, Frank J Owens, John Wiley, Copyright 2006, Reprint 2011.

Reference Book:

'Hand Book of Nanoscience Engineering and Technology', Ed William A Goddard III, Donald W Brenner, Sergey E. Lyshevski, Gerald J Iafrate, CRC Press, 2003

Cryptography and Network Security

CourseCode	**20ECS243**	CIEMarks	40
Lecture Hours/Week	**04**	SEE Marks	60
Total Number of LectureHours	**50**	Exam Hours	03
Credits - 04			

Module-1

Foundations: Terminology, Steganography, substitution ciphers and transpositions ciphers, Simple XOR, One-Time Pads, Computer Algorithms (Text 2: Chapter 1: Section 1.1 to 1.6).
SYMMETRIC CIPHERS: Traditional Block Cipher structure, Data encryption standard (DES), The AES Cipher. (Text 1: Chapter 2: Section2.1, 2.2, Chapter 4).

Module-2

Introduction to modular arithmetic, Prime Numbers, Fermat's and Euler's theorem, primality testing, Chinese Remainder theorem, discrete logarithm. (Text 1: Chapter 7: Section 1, 2, 3, 4, 5).
Principles of Public-Key Cryptosystems, The RSA algorithm, Diffie - Hellman Key Exchange, Elliptic Curve Arithmetic, Elliptic Curve Cryptography (Text 1: Chapter 8, Chapter 9: Section 9.1, 9.3, 9.4).

Module-3

Pseudo-Random-Sequence Generators and Stream Ciphers: Linear Congruential Generators, Linear Feedback Shift Registers, Design and analysis of stream ciphers, Stream ciphers using LFSRs, A5, Hughes XPD/KPD, Nanoteq, Rambutan, Additive generators, Gifford, Algorithm M, PKZIP (Text 2: Chapter 16).

Module-4

One-Way Hash Functions: Background, Snefru, N-Hash, MD4, MD5, Secure Hash Algorithm [SHA], One way hash functions using symmetric block algorithms, Using public key algorithms, Choosing a one-way hash functions, Message Authentication Codes. Digital Signature Algorithm, Discrete Logarithm Signature Scheme (Text 2: Chapter 18: Section 18.1 to 18.5, 18.7, 18.11 to 18.14 and Chapter 20: Section 20.1, 20.4).

Module-5

E-mail Security: Pretty Good Privacy-S/MIME (Text 1: Chapter 17: Section 17.1, 17.2).
IP Security: IP Security Overview, IP Security Policy, Encapsulation Security Payload (ESP), Combining security Associations. (Text 1: Chapter 18: Section 18.1 to 18.4).
Web Security: Web Security Considerations, SSL (Text 1: Chapter 15: Section 15.1, 15.2).

Course outcomes:
At the end of the course the student will be able to:

1. Understand the basics of symmetric key and public key cryptography.
2. Use basic cryptographic algorithms to encrypt the data.
3. Generate some pseudorandom numbers required for cryptographic applications.
4. Provide authentication and protection for encrypted data.
5. Understand the techniques and features of Email, IP and Web security.

Question paper pattern:
The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.

- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

Textbooks:

1. 'Cryptography and Network Security Principles and Practice', William Stallings, Pearson Education Inc., ISBN: 978-93325-1877-3, 6th Edition, 2014
2. 'Applied Cryptography Protocols, Algorithms, and Source code in C', Bruce Schneier, Wiley Publications ISBN: 9971-51348-X, 2nd Edition

Reference Books:

1. 'Cryptography and Network Security', Behrouz A. Forouzan, TMH, 2007
2. 'Cryptography and Network Security', Atul Kahate, TMH, 2003

Reconfigurable Computing

CourseCode	**20ELD244**	CIEMarks	40
Lecture Hours/Week	**04**	SEE Marks	60
Total Number of LectureHours	**50**	Exam Hours	03
Credits - 04			

Module -1

Introduction: History, Reconfigurable vs Processor based system, RC Architecture.
Reconfigurable Logic Devices: Field Programmable Gate Array, Coarse Grained Reconfigurable Arrays.
Reconfigurable Computing System: Parallel Processing on Reconfigurable Computers, A survey of Reconfigurable Computing System (Text 1).

Module-2

Languages and Compilation: Design Cycle, Languages, HDL, High Level Compilation, Low level Design flow, Debugging Reconfigurable Computing Applications (Text 1).

Module -3

Implementation: Integration, FPGA Design flow, Logic Synthesis.
High Level Synthesis for Reconfigurable Devices: Modelling, Temporal Partitioning Algorithms (Text 2).

Module-4

Partial Reconfiguration Design: Partial Reconfiguration Design, Bitstream Manipulation with JBits, The modular Design flow, The Early Access Design Flow, Creating Partially Reconfigurable Designs, Partial Reconfiguration using Hansel-C Designs, Platform Design (Text 2).

Module -5

Signal Processing Applications: Reconfigurable computing for DSP, DSP application building blocks, Examples: Beamforming, Software Radio, Image and video processing, Local Neighbourhood functions, Convolution (Text 1).
System on a Programmable Chip: Introduction to SoPC, Adaptive Multiprocessing on Chip(Text 2).

Course Outcomes:

At the end of the course the student will be able to:

1. Understand the fundamental principles and practices in reconfigurable architecture.
2. Simulate and synthesize the reconfigurable computing architectures.
3. Understand the FPGA design principles, and logic synthesis
4. Integrate hardware and software technologies for reconfiguration computing focusing on partial reconfiguration design.
5. Design digital systems for a variety of applications on signal processing and system on chip configurations.

Question paper pattern:

The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.

- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

Text Books:

1. 'Reconfigurable Computing:Accelerating Computation with Field-Programmable Gate Arrays', M. Gokhale and P. Graham, Springer, ISBN: 978-0-387-26105-8, 2005.
2. 'Introduction to Reconfigurable Computing: Architectures, Algorithms and Applications', C. Bobda, Springer, ISBN: 978-1-4020-6088-5, 2007.

Reference Books:

1. 'Practical FPGA Programming in C', D. Pellerin and S. Thibault, Prentice-Hall, 2005.
2. 'FPGA Based System Design',W. Wolf, Prentice-Hall, 2004.
3. 'Rapid System Prototyping with FPGAs: Accelerating the Design Process', R. Cofer and B. Harding, Newnes, 2005.

Professional Elective 2

Automotive Electronics

CourseCode	**20EIE251**	CIEMarks	40
Lecture Hours/Week	**04**	SEE Marks	60
Total Number of LectureHours	**50**	Exam Hours	03
Credits - 04			

Module 1

Automotive Fundamentals, the Systems Approach to Control and Instrumentation: Use of Electronics in the Automobile, Antilock Brake Systems(ABS), Electronic steering control, Power steering, Tractioncontrol, Electronically controlled suspension (Chap.1 and2 of Text).

Module 2

Automotive instrumentation Control: Operational amplifiers, Digital circuits, Logic circuits, Microcomputer fundamentals, Microcomputer operations, Microprocessor architecture, digital to analog converter, analog to digital converter, Microcomputer applications in automotive systems, Instrumentation applications of microcomputers, Microcomputer in control systems (Chap.3 and 4 of Text).

Module 3

The basics of Electronic Engine control: Integrated body: Climate controls, Motivation for ElectronicEngine Control, Concept of An Electronic Engine Control System,Definition of General Terms, Definition of EnginePerformanceTerms, Electronic fuel control system, Engine control sequence,Electronic Ignition, Sensors and Actuators, Applications ofsensors and actuators, air flow rate sensor, Indirect measurementof mass air flow, Engine crankshaft angular position sensor,Automotive engine control actuators, Digital engine control,Engine speed sensor, Timing sensor for ignition and fuel delivery,Electronic ignition control systems, Safety systems, Interiorsafety, Lighting, Entertainment systems (Chap. 5 and 6 of Text).

Module 4

Vehicle Motion Control and Automotive diagnostics: Cruisecontrol system, Digital cruise control, Timing light, Engineanalyzer, On-board and off-board diagnostics, Expert systems.Stepper motor-based actuator, Cruise control electronics,Vacuum - antilock braking system, Electronic suspension system,

Electronic steering control, Computer-based instrumentationsystem, Sampling and Input\output signal conversion, Fuelquantity measurement, Coolant temperature measurement, Oilpressure measurement, Vehicle speed measurement, Displaydevices, Trip-Information-Computer, Occupant protectionsystems (Chap. 8 and 10 of Text).

Module 5

Future automotive electronic systems: Alternative Fuel Engines, Collision Wide Range Air/Fuel Sensor,Alternative Engine, Low Tire Pressure Warning System, Collisionavoidance Radar Warning Systems, Low Tire Pressure WarningSystem, Radio Navigation, Advance Driver information System.Alternative-Fuel Engines, Transmission Control, CollisionAvoidance Radar Warning System, Low Tire Pressure WarningSystem, Speech Synthesis Multiplexing in Automobiles, ControlSignal Multiplexing, Navigation Sensors, Radio Navigation, Signpost Navigation, Dead Reckoning Navigation Future Technology, Voice Recognition Cell Phone Dialing Advanced Driver informationSystem, Automatic Driving Control (Chap. 11 of Text).

Course Outcomes:

At the end of the course the student will be able to:

1. Implement various control requirements in the automotive system.
2. Comprehend dashboard electronics and engine system electronics.
3. Identify various physical parameters that are to be sensed and monitored for maintaining the stability of the vehicle under dynamicconditions.
4. Understand and implement the controls and actuator system pertainingto the comfort and safety of commuters.
5. Design sensor network for mechanical fault diagnostics in an automotive vehicle.

Question paper pattern:

The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.

- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.

- The students will have to answer five full questions, selecting one full question from each module.

Text Book:

'Understanding Automotive Electronics', William B. Ribbens,SAMS/Elsevier publishing, 6th Edition, 1997.

Reference Book:

'Automotive Electrics and Automotive Electronics-Systems and Components, Networking and Hybrid Drive', Robert Bosch Gmbh,Springer Verlag,5th Edition, 2007.

SoC Design

CourseCode	**20EVE252**	CIEMarks	40
Lecture Hours/Week	**04**	SEE Marks	60
Total Number of LectureHours	**50**	Exam Hours	03
Credits - 04			

Module-1

ARM Organization and Implementation: 3-stage pipeline ARM organization, 5-stage pipeline ARM organization, ARM instruction execution, ARM implementation, The ARM coprocessor interface.

The ARM Instruction Set: Introduction, Exceptions, Conditional execution, Branch and Branch with Link (B, BL), Branch, Branch with Link and eXchange (BX, BLX), Software Interrupt (SWI), Data processing instructions, Multiply instructions, Count leading zeros (CLZ - architecture v5T only), Single word and unsigned byte data transfer instruction, Half-word and signed byte data transfer instructions, Multiple register transfer instructions, Swap memory and register instructions (SWP), Status register to general register transfer instructions, General register to status register transfer instructions, Coprocessor instructions, Coprocessor data operations, Coprocessor data transfers, Coprocessor register transfers, Breakpoint instruction (BRK - architecture v5T only), Unused instruction space, Memory faults, ARM architecture variants.

Module 2

Architectural Support for High-Level Languages: Abstraction in software design, Data types, Floating-point data types, The ARM floating-point architecture, Expressions, Conditional statements, Loops, Functions and procedures, Use of memory, Run-time environment.

Architectural Support for System Development: The ARM memory interface, The Advanced Microcontroller Bus Architecture (AMBA), The ARM reference peripheral specification, Hardware system prototyping tools, The ARMulator, The JTAG boundary scan test architecture, The ARM debug architecture, Embedded Trace, Signal processing support.

Module 3

ARM Processor Cores: ARM7TDMI, ARM8, ARM9TDMI, ARM10TDMI, Discussion, Example and exercises.

Memory Hierarchy: Memory size and speed, On-chip memory, Caches, Cache design - an example, Memory management, Examples and exercises.

Module 4

Architectural Support for Operating Systems: An introduction to operating systems, The ARM system control coprocessor, CP15 protection unit registers, ARM protection unit, CP15 MMU registers, ARM MMU architecture, Synchronization, Context switching, Input/ Output, Example and exercises.
ARM CPU Cores: The ARM710T, ARM720T and ARM740T, The ARM810, The Strong ARM SA-110, The ARM920T and ARM940T, The ARM946E-S and ARM966E-S, The ARM1020E, Discussion, Example and exercises.

Module 5

Embedded ARM Applications: The VLSI Ruby II Advanced Communication Processor, The VLSI ISDN Subscriber Processor, The One C™VWS22100 GSM chip, The Ericsson-VLSI Bluetooth Baseband Controller, The ARM7500 and ARM7500FE, The ARM7100 364, The SA-1100 368, Examples and exercises.
The AMULET Asynchronous ARM Processors: Self-timed design 375, AMULET1 377, AMULET2 381, AMULET2e 384, AMULET3 387, The DRACO telecommunications controller 390, A self-timed future? 396, Example and exercises.

Course Outcomes:
At the end of the course the student will be able to:

1. Apply the 3- and 5-stage pipeline ARM processor cores and analyse the implementation issues.
2. Use the concepts and methodologies employed in designing a System- on-chip (SoC) based around a microprocessor core and in designing the microprocessor core itself.
3. Understand how SoCs and microprocessors are designed and used, and why a modern processor is designed the way that it is.
4. Use integrated ARM CPU cores (including StrongARM) that incorporate full support for memory management.
5. Analyze the requirements of a modern operating system and use the ARM architecture to address the same.

Question paper pattern:
The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.

- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.

- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

Text Book:

'ARM System-On-Chip Architecture', Steve Furber, Addison Wesley, 2nd edition.

Reference Books:

1. 'The Definitive Guide to the ARM Cortex-M3', Joseph Yiu, Newnes, (Elsevier), 2nd edition,2010.
2. 'On-Chip Communication Architectures: System on Chip Interconnect', Sudeep Pasricha and NikilDutt, Morgan Kaufmann Publishers, 2008.
3. 'Reuse Methodology Manual for System on Chip designs', Michael Keating, Pierre Bricaud, Kluwer Academic Publishers, 2nd edition, 2008.

Micro Electro Mechanical Systems

CourseCode	**20ELD253**	CIEMarks	40
Lecture Hours/Week	**04**	SEE Marks	60
Total Number of LectureHours	**50**	Exam Hours	03
Credits - 04			

Module 1

Overview of MEMS and Microsystems: MEMS and Microsystem, Typical MEMS and Microsystems Products, Evolution of Microfabrication, Microsystems and Microelectronics, Multidisciplinary Nature of Microsystems, Miniaturization. Applications and Markets.

Module 2

Working Principles of Microsystems: Introduction, Microsensors, Microactuation, MEMS with Microactuators, Microaccelerometers, Microfluidics.

Engineering Science for Microsystems Design and Fabrication: Introduction, Atomic Structure of Matters, Ions and Ionization, Molecular Theory of Matter and Inter-molecular Forces, Doping of Semiconductors, The Diffusion Process, Plasma Physics, Electrochemistry.

Module 3

Engineering Mechanics for Microsystems Design: Introduction, Static Bending of Thin Plates, Mechanical Vibration, Thermomechanics, Fracture Mechanics, Thin Film Mechanics, Overview on Finite Element Stress Analysis.

Module 4

Scaling Laws in Miniaturization:
Introduction, Scaling in Geometry, Scaling in Rigid-Body Dynamics, Scaling in Electrostatic Forces, Scaling of Electromagnetic Forces, Scaling in Electricity, Scaling in Fluid Mechanics, Scaling in Heat Transfer.

Module 5

Overview of Micro-manufacturing: Introduction, Bulk Micro-manufacturing, Surface Micromachining, The LIGA Process, Summary on Micromanufacturing.
Microsystem Design: Introduction, Design Considerations, Process Design, Mechanical Design, Using Finite Element Method.

Course Outcomes:

At the end of the course the student will be able to:

1. Understand the technologies related to Micro Electro Mechanical Systems.
2. Relate to the scaling laws in miniaturization.
3. Analyse the MEMS devices and develop suitable mathematical models
4. Understand the various application areas for MEMS devices
5. Describe the design and fabrication processes involved with MEMS devices.

Question paper pattern:

The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.

- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

Text Book:

'MEMS and Micro systems: Design, Manufacture and Nanoscale Engineering', Tai-Ran Hsu, John Wiley & Sons, ISBN: 978-0470-08301-7, 2nd Edition, 2008

Reference Books:

1. 'Micro and Nano Fabrication: Tools and Processes', Hans H. Gatzen, Volker Saile, Jurg Leuthold, Springer, 2015
2. 'Micro Electro Mechanical Systems (MEMS)', Dilip Kumar Bhattacharya, Brajesh Kumar Kaushik, Cengage Learning.

Advanced Control System

CourseCode	**20ELD254**	CIEMarks	40
Lecture Hours/Week	**04**	SEE Marks	60
Total Number of LectureHours	**50**	Exam Hours	03
Credits - 04			

Module 1

Digital Control Systems: Review of Difference equations, Z – transformsand Inverse Z transforms, The Z- transfer function(Pulse transfer function), The Z - Transform Analysis of Sampleddata Control Systems, The Z and S - domain relationship, Stabilityanalysis (Jury's Stability Test and Bilinear Transformation)(Text 1,Text 2).

Module 2

State Models & Solution of State equations: State models for Linear Continuous Time and Linear Discrete Time systems,Diagonalization, Solution of State Equations (for both Continuousand Discrete Time systems), Relevant problems(Text1).

Module 3

State Feedback Systems: Concepts of Controllability and Observability (for both Continuous and Discrete Time systems),Pole Placement by State Feedback (for both continuous anddiscrete Time systems), Observer System (Full order and Reducedorder observers for both Continuous and Discrete Time systems),Relevant problems(Text 1, Text 2).

Module 4

Regulators: Dead beat Control by State Feedback, Optimal control problems using State Variable approach, State regulator andOutput regulator, Concepts of Model Reference Adaptive Control(MRAC)(Text 1, Text 2).

Module 5

Nonlinear Control Systems: Behavior of Nonlinear Systems, Common Physical Nonlinearities, Describing Function Method,Stability Analysis by Describing Function Method, Phase PlaneMethod, Stability Analysis by Phase Plane Method (Text 1).

Course Outcomes:
At the end of the course the student will be able to:

1. Derive the pulse transfer function for various closed loop configurationsand understand the stability analysis of sampled data control systems.
2. Apply state space techniques to model linear continuous and discrete time systems, convert state space (SS) representations to transfer function (TF)representation and vice versa.
3. Apply controllability and observability tests.
4. Solve the optimal control problems using state variable approach andknowledge of adaptive control systems.
5. Understand the types of nonlinearities, characteristics of Nonlinear systems and the stability analysis of Nonlinear control systems.

Question paper pattern:

The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.

- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

Text Books:

1. 'Control Systems Engineering', IJ Nagrath& MGopal, New Age International Publishers, Fifth edition, 2007.
2. 'Discrete Time Control Systems', K Ogata, 2nd edition, PHI, 2009.

Reference Books:

1. 'Modern Control Engineering', K Ogata, PHI, 5th Edition, 2010.
2. 'Modern Control System Theory', M Gopal,New Age International, 2012.
3. 'Digital Control and State Variable methods', M Gopal, TataMcGrawHill, 4th edition, 2012.
4. 'Advanced Control Theory', A Nagoorkani, RBA publications, 2006.

Digital Circuits Simulation Lab

CourseCode	**20ELDL26**	CIEMarks	40
TeachingHours/Week	**04** (2 Hrs Tutorial + 2 Hrs Practical)	SEE Marks	60
		Exam Hours	03
Credits - 02			

Laboratory Experiments:

PART-A: Graphical Programming using LabVIEW.

Sl.No.	**Experiments**
1	Design of 4 bit Adders (CLA, CSA, CMA, Parallel adders)
2	Design of Binary Subtractors
3	Design of Encoder (8 x 3), Decoder(3 x 8)
4	Design of Multiplexer (8 x 1) and Demultiplexer (1 x 8)
5	Design of code converters & Comparator
6	Design of FF (SR, D, T, JK, and Master Slave with delays)
7	Design of registers using latches and flip-flops
8	Design of 8-bit Shift registers
9	Design of Asynchronous & Synchronous Counters

PART-B: Develop Verilog Program for design and testing the followingdigital circuits (for 4/8 bits) using FPGA/CPLD. Use logicanalyzer/Chipscope for the verification of results.

(Note: Programming can be done using any complier. Down load theprograms on FPGA/CPLD boards and performance testing may bedone using pattern generator (32 channels and logic analyzer)/Chipscope pro. Implementing the above designs onXilinx/Altera/Cypress/equivalent based FPGA/CPLD kits.)

Sl. No.	**Experiments**
1	Carry skip and carry look ahead adder
2	BCD adder and subtractor
3	Array Multiplication (signed and unsigned)
4	Booth multiplication (radix-4)
5	Magnitude comparator
6	LFSR

7	Parity generator
8	Universal Shift Register
9	Sequence generation (11101 say) using Mealy/Moore FSM

Course outcomes:

At the end of the course the student will be able to:

1. Simulate the digital circuits using graphical programming tool LabVIEW.
2. Build user friendly interfaces to interact with the digital circuits and to observe the outputs.
3. Develop Verilog Programs for Digital Circuit design simulation.
4. Implementdigital systems on FPGA/CPLD.
5. Test and validate digital systems using Logic analyzer/Chipscope.

Conduct of Practical Examination:

1. All laboratory experiments are to be included for practical examination.
2. For examination, one question each to be set from PART-A and PART-B.
3. Students are allowed to pick one experiment from the lot.
4. Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.
5. Change of experiment is allowed only once and Marks allotted to the procedure part to be made zero.

Technical Seminar

CourseCode	**20ELD27**	CIEMarks	100
Number of Contact Hours/Week	**02**	SEE Marks	-
		Exam Hours	-
Credits - 02			

Course objectives:
The objective of the seminar is to inculcate self-learning, face audience confidently, enhance communication skill, involve in group discussion and present and exchange ideas.

Each student, under the guidance of a Faculty, is required to

- Choose, preferably through peer reviewed journals, a recent topic of his/her interest relevant to the Course of Specialization.
- Carryout literature survey, organize the Course topics in a systematic order.
- Prepare the report with own sentences.
- Type the matter to acquaint with the use of Micro-soft equation and drawing tools or any such facilities.
- Present the seminar topic orally and/or through power point slides.
- Answer the queries and involve in debate/discussion.
- Submit two copies of the typed report with a list of references.

The participants shall take part in discussion to foster friendly and stimulating environment in which the students are motivated to reach high standards and become self-confident.

The CIE marks for the seminar shall be awarded (based on the relevance of the topic, presentation skill, participation in the question and answer session and quality of report) by the committee constituted for the purpose by the Head of the Department. The committee shall consist of three faculties from the department with the senior most acting as the Chairperson.

Marks distribution for CIE of the course 20ELD27 seminar:

Seminar Report: 50 marks
Presentation skill: 25 marks
Question and Answer:25 marks

M.TECH IN DIGITAL ELECTRONICS / ELECTRONICS (ELD)

Choice Based Credit System (CBCS) and Outcome Based Education(OBE)
(Effective from the academic year 2020-21)

SEMESTER -III

Synthesis and Optimization of Digital Circuits

CourseCode	**20ELD31**	CIEMarks	40
Lecture Hours/Week	**04**	SEE Marks	60
Total Number of LectureHours	**50**	Exam Hours	03
Credits - 04			

Module -1

Introduction to Synthesis and optimization: Design of Microelectronics circuits, Computer aided Synthesis and Optimization.

Hardware Modeling: HDLs for Synthesis, Abstract models, Compilation and Behavioral Optimization(Text1: Topics from Chap.1,3).

Module -2

Graph theory for CAD for VLSI: Graphs, Combinatorial Optimization, Graph Optimization problems and Algorithms, Boolean Algebra and Applications.

Architectural Synthesis and Optimization: Fundamental Architectural Synthesis problems, Area and Performance Estimation, Strategies for Architectural Optimization, Datapath Synthesis, Control Path Synthesis (Text1: Topics from Chap. 2,4).

Module -3

Two level Combinational Logic Optimization: Introduction, Logic Optimizations, Operations on Two level Logic Covers, Algorithms for Logic Minimization, Symbolic Minimization and Encoding Problems.

Multiple Level Combinational Logic Optimization: Introduction, Models and Transformations for Combinational Networks, The Algebraic Model, The Boolean Model (Text1: Chap. 7, 8).

Module -4

Sequential Logic Optimization: Introduction, Sequential Logic Optimization using State based Models, Sequential Logic Optimization using Network Models, Implicit FSM Traversal Methods, Testability concerns for Synchronous Circuits (Text 1: Chap. 9).

Module -5

Scheduling Algorithms: Introduction, A Model for Scheduling problems, Scheduling with Resource Constraints, Scheduling without Resource Constraints, Scheduling Algorithms for Extended Sequencing Models, Scheduling Pipelined Circuits.

Resource Sharing and Binding: Sharing and Binding for Resource dominated circuits, Sharing and Binding for General Circuits, Concurrent Binding and Scheduling(Text1: Chap. 5,6).

Course Outcomes:

At the end of the course the student will be able to:

1. Understand the process of synthesis and optimization in a top down approach for digital circuits models using HDLs.
2. Understand the terminologies of graph theory and its algorithms to optimize a Boolean equation.
3. Apply different two level and multilevel optimization algorithms for combinational circuits.
4. Apply the different sequential circuit optimization methods using state models and network models.
5. Apply different scheduling algorithms with resource binding and without resource binding for pipelined sequential circuits and extended sequencing models.

Question paper pattern:

The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.

- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

Text Book:

‘Synthesis and Optimization of Digital Circuits’, Giovanni De Micheli, Tata McGraw-Hill, ISBN: 9780070582781, 2003.

Reference Book:

‘Automatic Logic synthesis Techniques for Digital Systems’, Edwars M.D, Macmillan New Electronic Series, 1992.

Professional elective 3

Advances in Image Processing

CourseCode	**20ECS321**	CIEMarks	40
Lecture Hours/Week	**03**	SEE Marks	60
Total Number of LectureHours	**40**	Exam Hours	03
Credits - 03			

Module-1

The image, its representations and properties: Image representations a few concepts, Image digitization, Digital image properties, Color images.

Module-2

Image Pre-processing: Pixel brightness transformations, geometric transformations, local pre-processing.

Module-3

Segmentation: Thresholding; Edge-based segmentation – Edge image thresholding, Edge relaxation, Border tracing, Hough transforms; Region – based segmentation – Region merging, Region splitting, Splitting and merging, Watershed segmentation, Region growing post-processing.

Module-4

Shape representation and description: Region identification; Contour-based shape representation and description – Chain codes, Simple geometric border representation, Fourier transforms of boundaries, Boundary description using segment sequences, B-spline representation; Region-based shape representation and description – Simple scalar region descriptors, Moments, Convex hull.

Module-5

Mathematical Morphology: Basic morphological concepts, Four morphological principles, Binary dilation and erosion, Skeletons and object marking, Morphological segmentations and watersheds.

Course outcomes:

At the end of the course the student will be able to:

1. Understand the representation of the digital image and its properties.
2. Apply pre-processing techniques required to enhance the image for its further analysis.
3. Use segmentation techniques to select the region of interest in the image for analysis.

4. Represent the image based on its shape and edge information and also describe the objects present in the image based on its properties and structure.
5. Use morphological operations to simplify images, and quantify and preserve the main shape characteristics of the objects.

Question paper pattern:
The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.

- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

Text Book:

'Image Processing, Analysis, and Machine Vision', Milan Sonka, Vaclav Hlavac, Roger Boyle, Cengage Learning, ISBN: 978-81-315-1883-0, 2013

Reference Books:

1. 'Digital Image Processing for Medical Applications', Geoff Doughertry, Cambridge university Press, 2010.
2. 'Digital Image Processing', S Jayaraman, S Esakkirajan, T Veerakumar, Tata McGraw Hill, 2011.

CMOS RF Circuit Design

CourseCode	**20EVE322**	CIEMarks	40
Lecture Hours/Week	**03**	SEE Marks	60
Total Number of LectureHours	**40**	Exam Hours	03
Credits - 03			

Module 1

Introduction to RF Design, Wireless Technology and Basic Concepts: A wireless world, RF design is challenging, The big picture. General considerations, Effects of Nonlinearity, Noise, Sensitivity and dynamic range, Passive impedance transformation. Scattering parameters, Analysis of nonlinear dynamic systems, conversion of gains and distortion.

Module 2

Communication Concepts: General concepts, analog modulation, digital modulation, spectral re-growth, coherent and non-coherent detection, Mobile RF communications, Multiple access techniques, Wireless standards, Appendix 1: Differential phase shift keying.

Module 3

Transceiver Architecture: General considerations, Receiver architecture, Transmitter architectures, Direct conversion and two-step transmitters, RF testing for heterodyne, Homodyne, Image reject, Direct IF and sub sampled receivers.

Module 4

Low Noise Amplifiers and Mixers: General considerations, Problem of input matching, LNA topologies: common-source stage with inductive load, common-source stage with resistive feedback.
Mixers-General considerations, passive down conversion mixers, Various mixers- working and implementation.

Module 5

VCO and PLLs- Oscillators- Basic topologies VCO and definition of phase noise, Noise power and trade off. Resonator VCO designs, Quadrature and single sideband generators. Radio frequency Synthesizers- PLLS, Various RF synthesizer architectures and frequency dividers, Power Amplifier design.

Course outcomes:

At the end of the course the student will be able to:

1. Analyse the effect of nonlinearity and noise in RF and microwave design.
2. Exemplify the approaches taken in actual RF products.
3. Minimize the number of off-chip components required to design mixers, Low-Noise Amplifiers, VCO and PLLs.
4. Explain various receivers and transmitter topologies with their merits and drawbacks.
5. Demonstrate how the system requirements define the parameters of the circuits and the impact on the performance

Question paper pattern:

The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.

- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

Text Book:

'RF Microelectronics', B. Razavi, PHI, second edition.

Reference Books:

1. 'CMOS Circuit Design, layout and Simulation', R. Jacob Baker, H.W. Li, D.E. Boyce, PHI, 1998.
2. 'Design of CMOS RF Integrated Circuits', Thomas H. Lee, Cambridge University press, 1998.
3. 'Mixed Analog and Digital Devices and Technology', Y.P. Tsividis, TMH, 1996.

Business Intelligence and its Applications

CourseCode	**20ELD323**	CIEMarks	40
Lecture Hours/Week	**03**	SEE Marks	60
Total Number of LectureHours	**40**	Exam Hours	03
Credits - 03			

Module 1

Development Steps, BI Definitions, BI Decision Support Initiatives, DevelopmentApproaches, Parallel Development Tracks, BI Project Team Structure, Business Justification,Business Divers, Business Analysis Issues, Cost – Benefit Analysis, Risk Assessment,Business Case Assessment Activities, Roles Involved In These Activities, Risks of NotPerforming Step, Hardware, Middleware, DBMS Platform, NonTechnical InfrastructureEvaluation

Module 2

Managing The BI Project, Defining And Planning The BI Project, Project PlanningActivities, Roles And Risks Involved In These Activities, General Business Requirement,Project Specific Requirements, Interviewing Process.

Module 3

Differences in Database Design Philosophies, Logical Database Design, Physical DatabaseDesign, Activities, Roles And Risks Involved In These Activities, Incremental Rollout,Security Management, Database Backup And Recovery.

Module 4

Growth Management, Application Release Concept, Post Implementation Reviews, Release Evaluation Activities, The Information Asset and Data Valuation, Actionable Knowledge –ROI, BI Applications, The Intelligence Dashboard.

Module 5

Business View of Information technology Applications: Business Enterprise excellence, Key purpose of using IT, Type of digital data, basics of enterprise reporting, BI road ahead.

Course outcomes:

At the end of the course the students will be able to:

1.Evaluate the key elements of a successful business intelligence (BI) program

2. Apply a BI meta model that turns outcomes into actions

3. Extract and transform data from an operational data to a data business data

4. Evaluate business analytics and performance measurement tools

5. Demonstrate a business scenario, identify the metrics, indicators and make recommendations to achieve the business goal.

Question paper pattern:

The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.

- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

Text Books:

1. 'Business Intelligence Roadmap: The Complete ProjectLifecycle for Decision Support Applications', Larissa T Moss and ShakuAtre, Addison Wesley Information Technology Series, 2003.
2. 'Fundamentals of Business Analytics', R N Prasad, SeemaAcharya, Wiley India, 2011.

Reference Books:

1. 'Business Intelligence: The Savvy Manager's Guide', David Loshin, Publisher: MorganKaufmann, ISBN 1-55860-196-4.
2. 'Delivering Business Intelligence with Microsoft SQL Server2005', Brian Larson, McGraw Hill,2006.

3. 'Foundations of SQL Server 2008', Lynn Langit, Business Intelligence – Apress,ISBN13: 978-14302-3324-4,2011.

RF MEMS

CourseCode	**20ECS324**	CIEMarks	40
Lecture Hours/Week	**03**	SEE Marks	60
Total Number of LectureHours	**40**	Exam Hours	03
Credits - 03			

Module 1

Review: Introduction to MEMS: Fabrication for MEMS transducers and actuators, Microsensing for MEMS, Materials for MEMS.
MEMS materials and fabrication techniques: Metals, Semiconductors, Thin films, Materials for polymer MEMS, Bulk machining for Silicon based MEMS, Surface machining for Silicon based MEMS, Micro stereo-lithography for polymer MEMS.

Module 2

RF MEMS Switches and micro-relays: Switch parameters, Basics of switching, Switches for RF and Microwave applications, Actuation mechanisms, Micro-relays and micro-actuators, Dynamic of switch operations, MEMS switch design and design consideration, MEMS inductors and capacitors.

Module 3

Micro machined RF filters and phase shifters: RF filters, Modelling of mechanical filters, Micro-mechanical filters, SAW filters - Basic, Design consideration. Bulk acoustic wave filters, Micro-machined filters for millimetre wave frequencies. Micro-machined phase shifters, Types and limitations, MEMS and Ferroelectric phase shifters, Applications.

Module 4

Micromachined transmission line and components: Micromachined transmission line: Losses in transmission line, coplanar lines, Microshield and membrane supported lines, Microshield components, Micromachined waveguides, Directional couplers and Mixers, Resonators and Filters.

Module 5

Micromachined antennas: design, Fabrication and measurements. Integration and packaging for RF MEMS. Roles and types of packages, Flip chip techniques, Multichip module packaging and Wafer bonding, Reliability issues and thermal issues.

Course outcomes:

At the end of the course the students will be able to:

1. Comprehend the need for micromachining and MEMS based systems for RF and microwave applications
2. Describe the micromachining techniques and their use in the fabrication of micro switches, capacitors and inductors
3. Design MEMS based microwave components aimed at reducing insertion loss and increasing bandwidth.
4. Realize high Q micromechanical filters for frequencies up to and beyond 10 MHz, and micromachined surface acoustic wave (SAW) filters filling the gap up to 2 GHz.
5. Describe the packaging approaches used for these RF MEMS devices.

Question paper pattern:

The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.

- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

Text Book:

'RF MEMS and their Applications', Vijay K Varadan, K. J. Vinoy and K. A. Jose, Wiley India Pvt. Ltd., ISBN - 10 : 8126529911, 2011.

Reference books:

1. 'RF MEMS circuit design', J De Los Santos, Artech House, 2002.
2. 'Transaction Level Modelling with System C: TLM concepts and applications for Embedded Systems', Frank Ghenassia, Springer, 2005.
3. 'Networks on chips: Technology and Tools', Luca Beninid, Morgan Kaufmann Publishers, 2006.

Professional elective 4

VLSI Design for Signal Processing

CourseCode	**20EVE331**	CIEMarks	40
Lecture Hours/Week	**03**	SEE Marks	60
Total Number of LectureHours	**40**	Exam Hours	03
Credits - 03			

Module 1

Introduction to DSP Systems: Typical DSP Algorithms, DSP Application Demands and Scaled CMOS Technologies, Representations of DSP Algorithms.

Iteration Bounds: Data flow graph Representations, loop bound and Iteration bound. Algorithms for Computing Iteration Bound, Iteration Bound of multi rate data flow graphs.

Module 2

Pipelining and Parallel Processing: pipelining of FIR Digital Filters, parallel processing, Pipelining and parallel processing for low power.

Retiming: Definition and Properties, Solving Systems of Inequalities, Retiming Techniques.

Module 3

Unfolding: An Algorithm for Unfolding, Properties of Unfolding, Critical path, Unfolding and Retiming, Application of Unfolding.

Folding: Folding Transformation, Register Minimization Techniques, Register Minimization in Folded Architectures, Folding of Multirate Systems.

Module 4

Systolic Architecture Design: systolic array design Methodology, FIR systolic array, Selection of Scheduling Vector, Matrix-Matrix Multiplication and 2D systolic Array Design, Systolic Design for space representation containing Delays.

Fast convolution: Cook-Toom Algorithm, Winograd Algorithm, Iterated convolution, cyclic convolution Design of fast convolution Algorithm by Inspection.

Module 5

Pipelined and Parallel Recursive and Adaptive Filter: Pipeline Interleaving in Digital Filter, first order IIR digital Filter, Higher order IIR digital Filter, parallel processing for IIR filter, Combined pipelining and parallel processing for IIR Filter, Low power IIR Filter Design Using Pipelining and parallel processing, pipelined adaptive digital filter.

Course outcomes:

At the end of the course the students will be able to:

1. Illustrate the use of various DSP algorithms and addresses their representation using block diagrams, signal flow graphs and data-flow graphs.
2. Use pipelining and parallel processing in design of high-speed /low-power applications.
3. Apply unfolding in the design of parallel architecture.
4. Evaluate the use of look-ahead techniques in parallel and pipelined IIR Digital filters.
5. Develop an algorithm or architecture or circuit design for DSP applications.

Question paper pattern:

The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.

- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

Text Book:

'VLSI Digital Signal Processing systems, Design and implementation', Keshab KParthi, Wiley, 1999.

Reference Books:

1. 'Analog VLSI Signal and Information Processing', Mohammed Isamail and Terri Fiez, Mc Graw-Hill, 1994.
2. 'VLSI and Modern Signal Processing', S.Y. Kung, H.J. White House, T. Kailath, Prentice Hall, 1985.
3. 'Design of Analog - Digital VLSI Circuits for Telecommunication and Signal Processing', Jose E. France, Yannis Tsividis, Prentice Hall, 1994.
4. 'DSP Integrated Circuits', Lars Wanhammar, Academic Press Series in Engineering, 1st Edition.

Pattern Recognition & Machine Learning

CourseCode	**20ESP332**	CIEMarks	40
Lecture Hours/Week	**03**	SEE Marks	60
Total Number of LectureHours	**40**	Exam Hours	03
Credits - 03			

Module 1

Introduction: Probability Theory, Model Selection, The Curse of Dimensionality, Decision Theory, Information Theory
Distributions: Binary and Multinomial Variables, The Gaussian Distribution, The Exponential Family, Nonparametric Methods (Ch. 1,2).

Module-2

Supervised Learning
Linear Regression Models: Linear Basis Function Models, The Bias-Variance Decomposition, Bayesian Linear Regression, Bayesian Model Comparison
Classification & Linear Discriminant Analysis: Discriminant Functions, Probabilistic Generative Models, Probabilistic Discriminative Mode (Ch. 3,4).

Module-3

Supervised Learning
Kernels: Dual Representations, Constructing Kernels, Radial Basis Function Network, Gaussian Processes
Support Vector Machines: Maximum Margin Classifiers, Relevance Vector Machines
Neural Networks: Feed-forward Network, Network Training, Error Backpropagation (Ch. 5,6,7).

Module-4

Unsupervised Learning
Mixture Models: K-means Clustering, Mixtures of Gaussians, Maximum likelihood, EM for Gaussian mixtures, Alternative View of EM.
Dimensionality Reduction: Principal Component Analysis, Factor/Component Analysis, Probabilistic PCA, Kernel PCA, Nonlinear Latent Variable Models (Ch. 9,12).

Module-5

Probabilistic Graphical Models: Bayesian Networks, Conditional Independence, Markov Random Fields, Inference in Graphical Models, Markov Model, Hidden Markov Models (Ch.8,13).

Course outcomes:

At the end of the course the students will be able to:

1. Identify areas where Pattern Recognition and Machine Learning can offer a solution.
2. Describe the strength and limitations of some techniques used in computational Machine Learning for classification, regression and density estimation problems.
3. Describe and model data.
4. Solve problems in Regression and Classification.
5. Discuss main and modern concepts for model selection and parameter estimation in recognition, decision making and statistical learning problems.

Question paper pattern:

The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.

- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

Text Book:

'Pattern Recognition and Machine Learning', Christopher Bishop, Springer, 2006.

Internet of Things

CourseCode	**20ECS333**	CIEMarks	40
Lecture Hours/Week	**03**	SEE Marks	60
Total Number of LectureHours	**40**	Exam Hours	03
Credits - 03			

Module-1

What is IoT ?
Genesis, Digitization, Impact, Connected Roadways, Buildings, Challenges
IoT Network Architecture and Design
Drivers behind new network Architectures, Comparing IoT Architectures, M2M architecture, IoT world forum standard, IoT Reference Model, Simplified IoT Architecture.

Module-2

IoT Network Architecture and Design
Core IoT Functional Stack, Layer1 (Sensors and Actuators), Layer 2 (Communications Sublayer), Access network sublayer, Gateways and backhaul sublayer, Network transport sublayer, IoT Network management.
Layer 3 (Applications and Analytics) – Analytics vs Control, Data vs Network Analytics, IoT Data Management and Compute Stack

Module-3

Engineering IoT Networks
Things in IoT – Sensors, Actuators, MEMS and smart objects.
Sensor networks, WSN, Communication protocols for WSN
Communications Criteria, Range, Frequency bands, power consumption, Topology, Constrained Devices, Constrained Node Networks
IoT Access Technologies, IEEE 802.15.4
Competitive Technologies – Overview only of IEEE 802.15.4g, 4e, IEEE 1901.2a
Standard Alliances – LTE Cat 0, LTE-M, NB-IoT

Module-4

Engineering IoT Networks
IP as IoT network layer, Key Advantages, Adoption, Optimization, Constrained Nodes, Constrained Networks, IP versions, Optimizing IP for IoT.

Application Protocols for IoT – Transport Layer, Application Transport layer, Background only of SCADA, Generic web based protocols, IoT Application Layer
Data and Analytics for IoT – Introduction, Structured and Unstructured data, IoT Data Analytics overview and Challenges.

Module-5

IoT in Industry (Three Use cases)
IoT Strategy for Connected manufacturing, Architecture for Connected Factory
Utilities – Power utility, IT/OT divide, Grid blocks reference model, Reference Architecture, Primary substation grid block and automation.
Smart and Connected cities –Strategy, Smart city network Architecture, Street layer, city layer, Data center layer, services layer, Smart city security architecture, Smart street lighting.

Course outcomes:
At the end of the course the student will be able to:

1. Understand the basic concepts IoT Architecture and devices employed.
2. Analyze the sensor data generated and map it to IoT protocol stack for transport.
3. Apply communications knowledge to facilitate transport of IoT data over various available communications media.
4. Design a use case for a typical application in real life ranging from sensing devices to analyzing the data available on a server to perform tasks on the device.
5. Apply knowledge of Information technology to design of IoT applications (Operational Technology).

Question paper pattern:
The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.

- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

Text Book:

‘CISCO, IoT Fundamentals – Networking Technologies, Protocols, Use Cases for IoT’, David Hanes, Gonzalo Salgueiro, Patrick Grossetete, Robert Barton, Jerome Henry, Pearson Education, ISBN: 978-9386873743, First edition, 2017

Reference Book:

‘Internet of Things – A Hands on Approach’, ArshdeepBahga and Vijay Madisetti, Orient Blackswan Private Limited - New Delhi, First edition, 2015

Communication System Design using DSP algorithm

CourseCode	**20ESP334**	CIEMarks	40
Lecture Hours/Week	**03**	SEE Marks	60
Total Number of LectureHours	**40**	Exam Hours	03
Credits - 03			

Module 1

Introduction to the course: Digital filters, Discrete time convolution and frequency responses, FIR filters - Using circular buffers to implement FIR filters in C and using DSP hardware, Interfacing C and assembly functions, Linear assembly code and the assembly optimizer. IIR filters - realization and implementation, FFT and power spectrum estimation: DTFT window function, DFT and IDFT, FFT, Using FFT to implement power spectrum.

Module 2

Analog modulation scheme: Amplitude Modulation - Theory, generation and demodulation of AM, Spectrum of AM signal, Envelope detection and square law detection, Hilbert transform and complex envelope, DSP implementation of amplitude modulation and demodulation.
DSBSC: Theory generation of DSBSC, Demodulation, and demodulation using coherent detection and Costas loop. Implementation of DSBSC using DSP hardware.
SSB: Theory, SSB modulators, Coherent demodulator, Frequency translation, Implementation using DSP hardware.

Module 3

Frequency modulation: Theory, Single tone FM, Narrow band FM, FM bandwidth, FM demodulation, Discrimination and PLL methods, Implementation using DSP hardware.
Digital Modulation scheme: PRBS, and data scramblers: Generation of PRBS, Self-synchronizing data scramblers, Implementation of PRBS and data scramblers. RS-232C protocol and BER tester: The protocol, error rate for binary signaling on the Gaussian noise channels, Three-bit error rate tester and implementation.

Module 4

PAM and QAM: PAM theory, baseband pulse shaping and ISI, Implementation of transmit filter and interpolation filter bank. Simulation and theoretical exercises for PAM, Hardware exercises for PAM.

QAM fundamentals: Basic QAM transmitter, 2 constellation examples, QAM structures using passband shaping filters, Ideal QAM demodulation, QAM experiment. QAM receivers-Clock recovery and other frontend sub-systems. Equalizers and carrier recovery systems.

Module 5

Experiment for QAM receiver frontend, Adaptive equalizer, Phase splitting, Fractionally spaced equalizer. Decision directed carrier tracking, Blind equalization, Complex cross coupled equalizer and carrier tracking experiment. Echo cancellation for full duplex modems: Multicarrier modulation, ADSL architecture, Components of simplified ADSL transmitter, A simplified ADSL receiver, Implementing simple ADSL Transmitter and Receiver.

Course outcomes:

At the end of the course the students will be able to:

1. Realize communication systems, including algorithms that are particularly suited to DSP implementation
2. Implement DSP algorithms on TI DSP processors
3. Implement FIR, IIR digital filtering and FFT methods
4. Implement modulators and demodulators for AM, DSBSC-AM, SSB and FM
5. Design digital communication methods leading to the implementation of a line communication system.

Question paper pattern:

The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.

- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

Text Book:

'Communication System Design using DSP Algorithms with Laboratory Experiments for the TMS320C6713 DSK', Steven A Tretter, Springer, 2008.

Reference Books:

1. 'Modern Digital Signal Processing', Roberto Cristi, Cengage Publishers, India, 2003.
2. 'Digital Signal Processing: A Computer Based Approach', S. K. Mitra, TMH, India, 3rd edition, 2007.
3. 'Digital Signal Processing: A Practitioner's approach', E.C. Ifeachor, and B. W. Jarvis, Pearson Education, India, Second Edition, 2002,
4. 'Digital Signal Processing', Proakis and Manolakis, Prentice Hall, 3rd edition, 1996.

Project Work Phase – 1

CourseCode	**20ELD34**	CIEMarks	100
Number ofcontactHours/Week	**02**	SEE Marks	-
		Exam Hours	-
Credits - 02			

Course objectives:

- Support independent learning.
- Guide to select and utilize adequate information from varied resources maintaining ethics.
- Guide to organize the work in the appropriate manner and present information (acknowledging the sources) clearly.
- Develop interactive, communication, organisation, time management, and presentation skills.
- Impart flexibility and adaptability.
- Inspire independent and team working.
- Expand intellectual capacity, credibility, judgement, intuition.
- Adhere to punctuality, setting and meeting deadlines.
- Instil responsibilities to oneself and others.
- Train students to present the topic of project work in a seminar without any fear, face audience confidently, enhance communication skill, involve in group discussion to present and exchange ideas.

Project Phase-1 Students in consultation with the guide/s shall carry out literature survey/ visit industries to finalize the topic of the Project. Subsequently, the students shall collect the material required for the selected project, prepare synopsis and narrate the methodology to carry out the project work.

Seminar: Each student, under the guidance of a Faculty, is required to

- Present the seminar on the selected project orally and/or through power point slides.
- Answer the queries and involve in debate/discussion.
- Submit two copies of the typed report with a list of references.

The participants shall take part in discussion to foster friendly and stimulating environment in which the students are motivated to reach high standards and become self-confident.

Revised Bloom's Taxonomy Level	L_3 – Applying, L_4 – Analysing, L_5 – Evaluating, L_6 – Creating.

Course outcomes:

At the end of the course the student will be able to:

1. Demonstrate a sound technical knowledge of their selected project topic.
2. Undertake problem identification, formulation and solution.
3. Design engineering solutions to complex problems utilising a systems approach.
4. Communicate with engineers and the community at large in written an oral forms.
5. Demonstrate the knowledge, skills and attitudes of a professional engineer.

Continuous Internal Evaluation

CIE marks for the project report (50 marks), seminar (25 marks) and question and answer (25 marks) shall be awarded (based on the quality of report and presentation skill, participation in the question and answer session by the student) by the committee constituted for the purpose by the Head of the Department. The committee shall consist of three faculty from the department with the senior most acting as the Chairperson.

MINI PROJECT

CourseCode	**20ELD35**	CIEMarks	40
Number of contact Hours/Week	**02**	SEE Marks	60
		Exam Hours/ Batch	03
Credits - 02			

Course objectives:

- To support independent learning and innovative attitude.
- To guide to select and utilize adequate information from varied resources upholding ethics.
- To guide to organize the work in the appropriate manner and present information (acknowledging the sources) clearly.
- To develop interactive, communication, organisation, time management, and presentation skills.
- To impart flexibility and adaptability.
- To inspire independent and team working.
- To expand intellectual capacity, credibility, judgement, intuition.
- To adhere to punctuality, setting and meeting deadlines.
- To instil responsibilities to oneself and others.
- To train students to present the topic of project work in a seminar without any fear, face audience confidently, enhance communication skill, involve in group discussion to present and exchange ideas.

Mini-Project: Each student of the project batch shall involve in carrying out the project work jointly in constant consultation with internal guide, co-guide, and external guide and prepare the project report as per the norms avoiding plagiarism.

Course outcomes:

At the end of the course the student will be able to:

1. Present the mini-project and be able to defend it.
2. Make links across different areas of knowledge and to generate, develop and evaluate ideas and information so as to apply these skills to the project task.
3. Habituated to critical thinking and use problem solving skills.
4. Communicate effectively and to present ideas clearly and coherently in both the written and oral forms.
5. Work in a team to achieve common goal.
6. Learn on their own, reflect on their learning and take appropriate actions to improve it.

CIE procedure for Mini - Project:
The CIE marks awarded for Mini - Project, shall be based on the evaluation of Mini - Project Report, Project Presentation skill and Question and Answer session in the ratio 50:25:25.The marks awarded for Mini - Project report shall be the same for all the batch mates.

Semester End Examination
SEE marks for the mini-project shall be awarded based on the evaluation of Mini-Project Report, Presentation skill and Question and Answer session in the ratio 50:25:25 by the examiners appointed by the University.

Internship / Professional Practice

CourseCode	**20ELDI36**	CIEMarks	40
Number of contact Hours/Week	**02**	SEE Marks	60
		Exam Hours	03
Credits - 06			

Course objectives:
Internship/Professional practice provide students the opportunity of hands-on experience that include personal training, time and stress management, interactive skills, presentations, budgeting, marketing, liability and risk management, paperwork, equipment ordering, maintenance, responding to emergencies etc. The objectives are further,

- To put theory into practice.
- To expand thinking and broaden the knowledge and skills acquired through course work in the field.
- To relate to, interact with, and learn from current professionals in the field.
- To gain a greater understanding of the duties and responsibilities of a professional.
- To understand and adhere to professional standards in the field.
- To gain insight to professional communication including meetings, memos, reading, writing, public speaking, research, client interaction, input of ideas, and confidentiality.
- To identify personal strengths and weaknesses.
- To develop the initiative and motivation to be a self-starter and work independently

Internship/Professional practice: Students under the guidance of internal guide/s and external guide shall take part in all the activities regularly to acquire as much knowledge as possible without causing any inconvenience at the place of internship.

Seminar: Each student, is required to

- Present the seminar on the internship orally and/or through power point slides.
- Answer the queries and involve in debate/discussion.
- Submit the report duly certified by the external guide.

The participants shall take part in discussion to foster friendly and stimulating environment in which the students are motivated to reach high standards and become self-confident.

Course outcomes:

At the end of the course the student will be able to:

- Gain practical experience within industry in which the internship is done.
- Acquire knowledge of the industry in which the internship is done.
- Apply knowledge and skills learned to classroom work.
- Develop a greater understanding about career options while more clearly defining personal career goals.
- Experience the activities and functions of professionals.
- Develop and refine oral and written communication skills.
- Identify areas for future knowledge and skill development.
- Expand intellectual capacity, credibility, judgment, intuition.
- Acquire the knowledge of administration, marketing, finance and economics.

Continuous Internal Evaluation

CIE marks for the Internship/Professional practice report (20 marks), seminar (10 marks) and question and answer session (10 marks) shall be awarded (based on the quality of report and presentation skill, participation in the question and answer session by the student) by the committee constituted for the purpose by the Head of the Department. The committee shall consist of three faculty from the department with the senior most acting as the Chairperson.

Semester End Examination

SEE marks for the Internship Report (30 Marks), Seminar (15 Marks) and Question and Answer Session (15 marks) shall be awarded (based on the quality of report and presentation skill, participation in the question and answer session) by the examiners appointed by the University.

M.TECH IN DIGITAL ELECTRONICS / ELECTRONICS (ELD)

Choice Based Credit System (CBCS) and Outcome Based Education(OBE)
(Effective from the academic year 2020-21)

SEMESTER -IV

PROJECT WORK PHASE -2

CourseCode	**20ELD41**	CIEMarks	40
Number of contact Hours/Week	**04**	SEE Marks	60
		Exam Hours	03
Credits - 20			

Course objectives:

- To support independent learning.
- To guide to select and utilize adequate information from varied resources maintaining ethics.
- To guide to organize the work in the appropriate manner and present information (acknowledging the sources) clearly.
- To develop interactive, communication, organisation, time management, and presentation skills.
- To impart flexibility and adaptability.
- To inspire independent and team working.
- To expand intellectual capacity, credibility, judgement, intuition.
- To adhere to punctuality, setting and meeting deadlines.
- To instil responsibilities to oneself and others.
- To train students to present the topic of project work in a seminar without any fear, face audience confidently, enhance communication skill, involve in group discussion to present and exchange ideas.

Project Work Phase - II: Each student of the project batch shall involve in carrying out the project work jointly in constant consultation with internal guide, co-guide, and external guide and prepare the project report as per the norms avoiding plagiarism.

Course outcomes:
At the end of the course the student will be able to:

- Present the project and be able to defend it.

- Make links across different areas of knowledge and to generate, develop and evaluate ideas and information so as to apply these skills to the project task.
- Habituated to critical thinking and use problem solving skills
- Communicate effectively and to present ideas clearly and coherently in both the written and oral forms.
- Work in a team to achieve common goal.
- Learn on their own, reflect on their learning and take appropriate actions to improve it.

Continuous Internal Evaluation:

Project Report: 20 marks. The basis for awarding the marks shall be the involvement of the student in the project and in the preparation of project report. To be awarded by the internal guide in consultation with external guide if any.

Project Presentation: 10 marks.

The Project Presentation marks of the Project Work Phase -II shall be awarded by the committee constituted for the purpose by the Head of the Department. The committee shall consist of three faculty from the department with the senior most acting as the Chairperson.

Question and Answer: 10 marks.

The student shall be evaluated based on the ability in the Question and Answer session for 10 marks.

Semester End Examination

SEE marks for the project report (30 marks), seminar (15 marks) and question and answer session (15 marks) shall be awarded (based on the quality of report and presentation skill, participation in the question and answer session) by the examiners appointed by the University.