

VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI
Scheme of Teaching and Examinations – 2020 - 21
Choice Based Credit System (CBCS) and Outcome Based Education(OBE)

Programme: M.TECH IN INDUSTRIAL ELECTRONICS (EIE)

I SEMESTER

Sl. No	Course	Course Code	Course Title	Teaching Hours /Week		Examination				Credits
				Theory	Practical/ Field work/ Assignment	Duration in hours	CIE Marks	SEE Marks	Total Marks	
1	PCC	20ELD11	Advanced Engineering Mathematics	04	--	03	40	60	100	4
2	PCC	20ECS12	Advanced Digital Signal Processing	04	--	03	40	60	100	4
3	PCC	20EVE13	Advanced EmbeddedSystem	04	--	03	40	60	100	4
4	PCC	20ELD14	Digital Circuits and Logic Design	04	--	03	40	60	100	4
5	PCC	20EIE15	Advanced Control System	04	--	03	40	60	100	4
6	PCC	20EIEL16	Controls and VirtualInstrumentation lab	-	04	03	40	60	100	2
7	PCC	20RMI17	Research Methodology and IPR	02	--	03	40	60	100	2
TOTAL				22	04	21	280	420	700	24

Note: PCC: Professional core.

Skill Development Activities(SDA) is the responsibility of the corresponding Program (for all courses coming under **BoS ECE** purview)to train the students by providing them skills through identified mentors/facilitators with the objective of enhancing

their Employment/ Self-Employment opportunities. The SDA component is a part of the CIE. It should be **defined specifically** for each theory subject of **4 credits**. To meet the objectives the following guidelines are framed:

The SDA include:

1. **Formulating and incorporating** lab experiments in specified subjects, **at least in one subject per semester** from first to third semester. The students have to conduct lab experiments (extra) as a part of CIE marks along with other activities.
2. **In courses with strong industry connect, case studies/ latest trends** should be discussed as a part of subject seminar. The student **cannot assume the same cases will be part of the SEE question paper**.
3. At least one **industrial visit** before third semester is mandatory with the relevant report.
4. **Mini-project carried out in groups** with relevant literature review based on latest trends in industry / research with report in identified subject at second semester can be taken up. The **publishing of a base paper** based on the work is recommended.

For **Sl. No. 2 & 3 above**, at least 20% of the CIE marks are to be earmarked in the concerned subject, apart from regular assignments, quiz & seminars. For **Sl. No. 1 & 4**, the complete CIE evaluation can be based on the practical/ lab report. In all the Skill Development Activities, **students and course instructor/s** are to involve either individually or in groups to interact together to enhance the learning and application skills of the students.

Expected outcomes

The students shall

- 1) Gain confidence in modelling of systems and algorithms.
- 2) Work on different software/s (tools) to Simulate, analyze and authenticate the output to interpret and conclude.
- 3) Handle advanced instruments to enhance technical talent.
- 4) Involve in case studies and field visits/ field work.
- 5) Accustom with the use of standards/codes etc., to narrow the gap between academia and industry.

All activities should **enhance students' abilities and competencies** for employment and/or self-employment opportunities, solving engineering problems, project management skills, individual and team work, life-long learning, etc.

Internship: All the students have to undergo mandatory internship of 6 weeks during the vacation of I and II semesters and /or II and III semesters. A University examination shall be conducted during III semester and the prescribed credit shall be counted for the same semester. Internship shall be considered as a head of passing and shall be considered for the award of degree. Those, who do not take-up/complete the internship shall be declared as fail in internship course and have to complete the same during the subsequent University examination after satisfying the internship requirements.

Note: (i) Four credit courses are designed for 50 hours Teaching – Learning process.
(ii) Three credit courses are designed for 40 hours Teaching – Learning process.

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II SEMESTER

Sl. No	Course	Course Code	Course Title	Teaching Hours /Week			Examination			Credits
				Theory	Practical/ Field work/ Assignment/ Project	Duration in hours	CIE Marks	SEE Marks	Total Marks	
1	PCC	20EIE21	Process ControlInstrumentation	04	--	03	40	60	100	4
2	PCC	20EVE22	Real Time Operating System	04	--	03	40	60	100	4
3	PCC	20EIE23	Design of Power Converters	04	--	03	40	60	100	4
4	PEC	20XXX24X	Professional elective 1	04	--	03	40	60	100	4
5	PEC	20XXX25X	Professional elective 2	04	--	03	40	60	100	4
6	PCC	20EIEL26	Embedded and SignalProcessing Lab	--	04	03	40	60	100	2
7	PCC	20EIE27	Technical Seminar	--	02	--	100	--	100	2
TOTAL				20	06	20	340	360	700	24

Note: PCC: Professional core, PEC: Professional Elective.

Professional Elective 1		Professional Elective 2	
Course Code under 20XXX24X	Course title	Course Code under 20XXX25X	Course title
20ECS241	Wireless Sensor Networks	20EIE251	Automotive Electronics
20EVE242	Nanoelectronics	20EIE252	Industrial Drives
20ECS243	Cryptography and Network Security (20EVE334)	20ELD253	Micro Electro Mechanical Systems
20ELD244	Reconfigurable Computing	20EIE254	Synthesis and Optimization of Digital Circuits
Note:			
<p>1. Technical Seminar: CIE marks shall be awarded by a committee comprising of HoD as Chairman, Guide/co-guide, if any, and a senior faculty of the department. Participation in the seminar by all postgraduate students of the same and other semesters of the programme shall be mandatory.</p> <p>The CIE marks awarded for Technical Seminar, shall be based on the evaluation of Seminar Report, Presentation skill and Question and Answer session in the ratio 50:25:25.</p> <p>2. Internship: All the students shall have to undergo mandatory internship of 6 weeks during the vacation of I and II semesters and /or II and III semesters. A University examination shall be conducted during III semester and the prescribed credit shall be counted in the same semester. Internship shall be considered as a head of passing and shall be considered for the award of degree. Those, who do not take-up/complete the internship shall be declared as fail in internship course and have to complete the same during the subsequent University examination after satisfying the internship requirements.</p>			

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III SEMESTER

Sl. No	Course	Course Code	Course Title	Teaching Hours /Week		Examination				Credits
				Theory	Practical/ Field work/ Assignment	Duration in hours	CIE Marks	SEE Marks	Total Marks	
1	PCC	20EIE31	PLCs and Industrial Automation	04	--	03	40	60	100	4
2	PEC	20XXX32X	Professional elective 3	03	--	03	40	60	100	3
3	PEC	20XXX33X	Professional elective 4	03	--	03	40	60	100	3
4	PROJ	20EIE34	Project Work phase -1	--	02	--	100	--	100	2
5	PROJ	20EIE35	Mini-Project	--	02	--	100	--	100	2
6	INT	20EIE136	Internship	(Completed during the intervening vacation of I and II semesters and /or II and III semesters.)		03	40	60	100	6
TOTAL				10	04	12	360	240	600	20

Note: PCC: Professional core, PEC: Professional Elective.

Professional elective 3		Professional elective 4	
Course Code under 20XXX32X	Course title	Course Code under 20XXX33X	Course title
20ECS321	Advances in Image Processing	20EIE331	Advanced Power Electronic Converters and Applications
20EIE322	Medical Imaging	20ESP332	Pattern Recognition & Machine Learning
20ELD323	Business Intelligence and its Applications	20ECS333	Internet of Things
20ECS324	RF MEMS	20ESP334	Communication System Design using DSP Algorithms

Note:

- 1. Project Work Phase-1:** Students in consultation with the guide & co-guide if any, shall pursue literature survey and complete the preliminary requirements of selected Project work. Each student shall prepare relevant introductory project phase-I report, and make a project presentation.

CIE marks shall be awarded by a committee comprising of HoD as Chairman, Guide/co-guide if any, and a senior faculty of the department. The CIE marks awarded for project work phase -1, shall be based on the evaluation of Project Report, Project Presentation skill and Question and Answer session in the ratio 50:25:25.

SEE (University examination) shall be as per the University norms.
- 2. Mini-Project:** Each student shall involve in carrying out the Mini-project work in constant consultation with internal guide, prepare the project report as per the norms avoiding plagiarism. A mini project is an assignment that you try to complete at the end of semester to strengthen the understanding of his/her fundamentals through effective application of theoretical concepts.
- 3. Internship:** Those, who have not pursued /completed the internship shall be declared as fail in internship course and have to complete the same during subsequent University examinations after satisfying the internship requirements. Internship SEE (University examination) shall be as per the University norms.

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Choice Based Credit System (CBCS) and Outcome Based Education(OBE)

Programme: M.TECH IN INDUSTRIAL ELECTRONICS (EIE)**IV SEMESTER**

Sl. No	Course	Course Code	Course Title	Teaching Hours /Week		Examination			Credits	
				Theory	Practical/ Field work/ Assignment	Duration in hours	CIE Marks	SEE Marks Viva voce		Total Marks
1	Project	20EIE41	Project work phase -2	--	04	03	40	60	100	20
TOTAL				--	04	03	40	60	100	20

Note:**1. Project Phase-2:**

CIE marks shall be awarded by a committee comprising of HoD as Chairman, Guide/co-guide, if any, and a Senior faculty of the department. The CIE marks awarded for project work phase -2, shall be based on the evaluation of Project Report subjected to plagiarism check, Project Presentation skill and Question and Answer session in the ratio 50:25:25.

SEE shall be at the end of IV semester. Project work evaluation and Viva-Voce examination (SEE), after satisfying the plagiarism check, shall be as per the University norms.

**VISVESVARAYA TECHNOLOGICAL UNIVERSITY
BELAGAVI**

Scheme of Teaching and Examinations and Syllabus
M.Tech in **Industrial Electronics (EIE)**
(Effective from Academic year 2020 - 21)

M.TECH IN INDUSTRIAL ELECTRONICS (EIE)

Choice Based Credit System (CBCS) and Outcome Based Education (OBE)
(Effective from the academic year 2020-21)

SEMESTER -I

ADVANCED ENGINEERING MATHEMATICS

CourseCode	20ELD11	CIEMarks	40
Lecture Hours/Week	04	SEE Marks	60
Total Number of LectureHours	50	Exam Hours	03
Credits - 04			

Module-1

Linear Algebra-I

Introduction to vector spaces and sub-spaces, definitions, illustrative example. Linearly independent and dependent vectors- Basis-definition and problems. Linear transformations-definitions. Matrix form of linear transformations- Illustrative examples (Text Book1).

Module-2

Linear Algebra-II

Computation of eigen values and eigen vectors of real symmetric matrices- Given's method. Orthogonal vectors and orthogonal bases. Gram-Schmidt orthogonalization process (Text Book1).

Module-3

Calculus of Variations

Concept of functional- Eulers equation. Functional dependent on first and higher order derivatives, Functional on several dependent variables. Isoperimetric problems-variation problems with moving boundaries. (TextBook2).

Module-4

Probability Theory: Review of basic probability theory. Definitions of random variables and probability distributions, probability mass and density functions, expectation, moments, central moments, characteristic functions, probability generating and moment generating functions-illustrations. Poisson, Gaussian and Erlang distributions examples (Text Book 3).

Module-5

Engineering Applications on Random processes: Classification. Stationary, WSS and ergodic random process. Auto-correlation function - properties, Gaussian random process (Text Book 3).

Course outcomes:

At the end of the course the student will be able to:

1. Understand vector spaces, basis, linear transformations and the process of obtaining matrix of linear transformations arising in magnification and rotation of images.
2. Apply the technique of singular value decomposition for data compression, least square approximation in solving inconsistent linear systems.
3. Utilize the concepts of functional and their variations in the applications of communication systems, decision theory, synthesis and optimization of digital circuits.
4. Learn the idea of random variables (discrete/continuous) and probability distributions in analyzing the probability models arising in control systems and system communications.
5. Analyze random process through parameter-dependent variables in various random processes.

Question paper pattern:

The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.

- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

Textbooks:

1. 'Linear Algebra and its Applications', David C Lay, Steven R Lay and J J McDonald, Pearson Education Ltd., 5th Edition, 2015
2. 'Differential Equations and Calculus of Variations', Elsgolts L, MIR Publications, 3rd Edition, 1977
3. 'Probability, Statistics and Random Process', T Veerarajan, Tata Mc-Graw Hill Co., 3rd Edition, 2016

Reference Books:

1. 'Introduction to Linear Algebra', Gilbert Strang, Wellesley-Cambridge Press, 5th Edition, 2016
2. 'Schaum's Outlines of Theory and Problems of Matrix Operations', Richard Bronson, McGraw-Hill, 1988
3. 'Probability and Random Process with application to Signal Processing', Scott L Miller, Donald G Childers, Elsevier Academic Press, 2nd Edition, 2013

Advanced Digital Signal Processing

CourseCode	20ECS12	CIEMarks	40
Lecture Hours/Week	04	SEE Marks	60
Total Number of LectureHours	50	Exam Hours	03
Credits - 04			

Module-1

Multirate Digital Signal Processing: Introduction, decimation by a factor 'D', Interpolation by a factor 'I', sampling rate conversion by a factor 'I/D', Implementation of sampling rate conversion, Multistage implementation of sampling rate conversion, Applications of multirate signal processing, Digital filter banks, two channel quadrature mirror filter banks, M-channel QMF bank (Text 1).

Module-2

Linear prediction and Optimum Linear Filters: Random signals, Correlation Functions and Power Spectra, Innovations Representation of a Stationary Random Process. Forward and Backward Linear Prediction. Solution of the Normal Equations. The Levinson-Durbin Algorithm. Properties of the Linear Prediction-Error Filters (Text 1).

Module-3

Adaptive filters: Applications of Adaptive Filters-Adaptive Channel Equalization, Adaptive noise cancellation, Linear Predictive coding of Speech Signals, Adaptive direct form FIR filters-The LMS algorithm, Properties of LMS algorithm. Adaptive direct form filters- RLS algorithm (Text 1).

Module-4

Power Spectrum Estimation: Non parametric Methods for Power Spectrum Estimation - Bartlett Method, Welch Method, Blackman and Tukey Methods.

Parametric Methods for Power Spectrum Estimation: Relationship between the auto correlation and the model parameters, Yule and Walker methods for the AR Model Parameters, Burg Method for the AR Model parameters, Unconstrained least-squares method for the AR Model parameters, Sequential estimation methods for the AR Model parameters, ARMA Model for Power Spectrum Estimation (Text 1).

Module-5

WAVELET TRANSFORMS: The Age of Wavelets, The origin of Wavelets, Wavelets and other reality transforms, History of wavelets, Wavelets of the future.

Continuous Wavelet and Short Time Fourier Transform: Wavelet Transform, Mathematical preliminaries, Properties of wavelets.

Discrete Wavelet Transform: Haar scaling functions, Haar wavelet function, Daubechies Wavelets (Chapters 1, 3 & 4 of Text 2).

Course outcomes:

At the end of the course the student will be able to:

1. Design adaptive filters for a given application
2. Design multirate DSP Systems
3. Implement adaptive signal processing algorithm
4. Design active networks
5. Understand advanced signal processing techniques, including multi-rate processing and time-frequency analysis techniques

Question paper pattern:

The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.

- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

Textbooks:

1. 'Digital Signal Processing, Principles, Algorithms and Applications', John G. Proakis, Dimitris G.Manolakis, Pearson, Fourth edition, 2007
2. 'Insight into Wavelets- from Theory to Practice', K P Soman, Ramachandran, Resmi, PHI, Third Edition, 2010

Advanced Embedded System

CourseCode	20EVE13	CIEMarks	40
Lecture Hours/Week	04	SEE Marks	60
Total Number of LectureHours	50	Exam Hours	03
Credits - 04			

Module-1

Embedded System: Embedded vs General computing system, classification, application and purpose of ES. Core of an Embedded System, Memory, Sensors, Actuators, LED, Opto coupler, Communication Interface, Reset circuits, RTC, WDT, Characteristics and Quality Attributes of Embedded Systems (Text 1: Selected Topics from Ch -1, 2, 3).

Module-2

Hardware Software Co-Design, embedded firmware design approaches, computational models, embedded firmware development languages, Integration and testing of Embedded Hardware and firmware, Components in embedded system development environment (IDE), Files generated during compilation, simulators, emulators and debugging (Text 1: Selected Topics from Ch-7, 9, 12, 13).

Module-3

ARM-32 bit Microcontroller: Thumb-2 technology and applications of ARM, Architecture of ARM Cortex M3, Various Units in the architecture, General Purpose Registers, Special Registers, exceptions, interrupts, stack operation, reset sequence (Text 2: Ch 1, 2, 3).

Module-4

Instruction Sets: Assembly basics, Instruction list and description, useful instructions, Memory Systems, Memory maps, Cortex M3 implementation overview, pipeline and bus interface (Text 2: Ch-4, 5, 6).

Module-5

Exceptions, Nested Vector interrupt controller design, SysTick Timer, Cortex-M3 Programming using assembly and C language, CMSIS (Text 2: Ch-7, 8, 10).

Course outcomes:

At the end of the course the student will be able to:

1. Understand the basic hardware components and their selection method based on the characteristics and attributes of an embedded system.
2. Explain the hardware software co-design and firmware design approaches.
3. Understand the suitability of the instruction sets of ARM processors to design of embedded systems.
4. Acquire the knowledge of the architectural features of ARM CORTEX M3, a 32-bit microcontroller including memory map, interrupts and exceptions.
5. Apply the knowledge gained for Programming ARM CORTEX M3 for different applications.

Question paper pattern:

The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.

- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

Textbooks:

1. 'Introduction to embedded systems', K. V. Shibu, TMH education Pvt. Ltd., 2009
2. 'The Definitive Guide to the ARM Cortex-M3', Joseph Yiu, Newnes, (Elsevier), 2ndedn, 2010.

Reference Book:

'Embedded systems - A contemporary design tool', James K. Peckol, John Wiley, 2008

Digital Circuits and Logic Design

CourseCode	20ELD14	CIEMarks	40
Lecture Hours/Week	04	SEE Marks	60
Total Number of LectureHours	50	Exam Hours	03
Credits - 04			

Module-1

Threshold Logic: Introductory Concepts, Synthesis of Threshold Networks, Capabilities, Minimization, and Transformation of Sequential Machines: The Finite- State Model, Further Definitions, Capabilities.

Module-2

Fault Detection by Path Sensitizing, Detection of Multiple Faults, Failure-Tolerant Design, Quadded Logic, ReliableDesign and Fault Diagnosis Hazards: Fault Detection inCombinational Circuits.

Module-3

Fault-Location Experiments, Boolean Differences, Limitations ofFinite – State Machines, State Equivalence and MachineMinimization, Simplification of Incompletely SpecifiedMachines.

Module-4

Structure of Sequential Machines: Introductory Example, State Assignments Using Partitions, The Lattice of closed Partitions,Reductions of the Output Dependency, Input Independenceand Autonomous Clocks, Covers and Generation of closedPartitions by state splitting, Information Flow in SequentialMachines, decompositions, Synthesis of Multiple Machines.

Module-5

State Identifications and Fault-Detection Experiments: HomingExperiments, Distinguishing Experiments, MachineIdentification, Fault Detection Experiments, Design ofDiagnosable Machines, Second Algorithm for the Design ofFault Detection Experiments, Fault-Detection.

Course outcomes:

At the end of the course the student will be able to:

1. Understand the concepts of sequential machines.
2. Design Sequential Machines/Circuits.
3. Analyze the faults in the design of circuits.
4. Apply fault detection experiments to sequential circuits.
5. Comprehend the structure of sequential machines.

Question paper pattern:

The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.

- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

Textbook:

‘Switching and Finite Automata Theory’, ZviKohavi, TMH, ISBN: 978_0_07_099387_7, 2nd Edition, 2008.

Reference Books:

1. ‘Digital Circuits and logic Design’, Charles Roth Jr., Cengage Learning, 7th edition, 2014.
2. ‘Fault Tolerant and Fault Testable Hardware Design’, Parag K Lala, Prentice Hall Inc. 1985.
3. ‘Introductory Theory of Computer’, E. V. Krishnamurthy, Macmillan Press Ltd, 1983
4. ‘Theory of computer science – Automata, Languages and Computation’, Mishra & Chandrasekaran, 2nd Edition, PHI, 2004.

Advanced Control System

CourseCode	20EIE15	CIEMarks	40
Lecture Hours/Week	04	SEE Marks	60
Total Number of LectureHours	50	Exam Hours	03
Credits - 04			

Module 1

Digital Control Systems: Review of Difference equations, Z – transforms and Inverse Z transforms, The Z- transfer function(Pulse transfer function), The Z - Transform Analysis of Sampleddata Control Systems, The Z and S - domain relationship, Stabilityanalysis (Jury’s Stability Test and Bilinear Transformation)(Text 1,Text 2).

Module 2

State Models & Solution of State equations: State models for Linear Continuous Time and Linear Discrete Time systems,Diagonalization, Solution of State Equations (for both Continuousand Discrete Time systems), Relevant problems(Text1).

Module 3

State Feedback Systems: Concepts of Controllability and Observability (for both Continuous and Discrete Time systems),Pole Placement by State Feedback (for both continuous anddiscrete Time systems), Observer System (Full order and Reducedorder observers for both Continuous and Discrete Time systems),Relevant problems(Text 1, Text 2).

Module 4

Regulators: Dead beat Control by State Feedback, Optimal control problems using State Variable approach, State regulator andOutput regulator, Concepts of Model Reference Adaptive Control(MRAC)(Text 1, Text 2).

Module 5

Nonlinear Control Systems: Behavior of Nonlinear Systems, Common Physical Nonlinearities, Describing Function Method,Stability Analysis by Describing Function Method, Phase PlaneMethod, Stability Analysis by Phase Plane Method (Text 1).

Course Outcomes:

At the end of the course the student will be able to:

1. Derive the pulse transfer function for various closed loop configurations and understand the stability analysis of sampled data control systems.
2. Apply state space techniques to model linear continuous and discrete time systems, convert state space (SS) representations to transfer function (TF) representation and vice versa.
3. Apply controllability and observability tests.
4. Solve the optimal control problems using state variable approach and knowledge of adaptive control systems.
5. Understand the types of nonlinearities, characteristics of Nonlinear systems and the stability analysis of Nonlinear control systems.

Question paper pattern:

The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.

- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

Text Books:

1. 'Control Systems Engineering', IJ Nagrath & MGopal, New Age International Publishers, Fifth edition, 2007.
2. 'Discrete Time Control Systems', K Ogata, 2nd edition, PHI, 2009.

Reference Books:

1. 'Modern Control Engineering', K Ogata, PHI, 5th Edition, 2010.
2. 'Modern Control System Theory', M Gopal, New Age International, 2012.
3. 'Digital Control and State Variable methods', M Gopal, TataMcGrawHill, 4th edition, 2012.
4. 'Advanced Control Theory', A Nagoorkani, RBA publications, 2006.

Controls and Virtual Instrumentation lab

CourseCode	20EIEL16	CIEMarks	40
Teaching Hours/Week	04 (2 Hrs Tutorial + 2 Hrs Practical)	SEE Marks	60
		Exam Hours	03
Credits - 02			

Sl.No	Experiments
1	Use the suitable software simulation tool to develop and implement the ladder logic for PLC
a	Binary to Gray code using PLC. The logic should be solved using ladder diagram technique.
b	Bottle filling process using PLC. The logic should be solved using ladder diagram technique.
c	Elevator using PLC. The logic should be solved using ladder diagram technique.
d	Controlling the Rotation of the motor using timer. The logic should be solved using ladder diagram technique.

2	Introduction of the basics of data acquisition and computer-controlled Instrumentation using Virtual Instrumentation (LabVIEW programs)
a	Simulation of temperature indicators using LabVIEW.
b	Simple calculator using LabVIEW.
c	Design of a variable function generator using VI
d	Creation of a CRO using VI and measurement of frequency and amplitude
e	Data acquisition using VI for temperature measurement with thermocouple and AD590

3	ARM Cortex M3 Programs: (Programming to be done using Keil uVision 4 and download the program on to a M3 evaluation board such as NXP LPC1768 or ATMEL ATSAM3U).
a	Write an Assembly language program to calculate the sum and display the result for the addition of first ten numbers. SUM = 10+9+8+.....+1
b	Write a Assembly language program to link multiple object files and link them together.
c	Write an Assembly language program to store data in RAM.
d	Write a C program to Output the "Hello World" message using UART.
e	Write a C program to Design a Stopwatch using interrupts.

Course outcomes:

At the end of the course the student will be able to:

1. Simulate ladder logic for various applications using PLC.
2. Use LabVIEW for virtual instrumentation applications.
3. Design data acquisition experiments using LabVIEW DAQ cards.
4. Develop Assembly language programs for different applications using ARM-Cortex M3 Kit and Keil uVision-4 tool.
5. Develop C language programs for different applications using ARM- Cortex M3 Kit and Keiluvision-4 tool.

Conduct of Practical Examination:

1. All laboratory experiments are to be included for practical examination.
2. For examination, two questions using different tool to be set.
3. Students are allowed to pick one experiment from the lot.
4. Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.
5. Change of experiment is allowed only once and Marks allotted to the procedure part to be made zero.

Research Methodology and IPR

CourseCode	20RMI17	CIEMarks	40
Lecture Hours/Week	02	SEE Marks	60
		Exam Hours	03
Credits - 02			

Module-1

Research Methodology: Introduction, Meaning of Research, Objectives of Research, Motivation in Research, Types of Research, Research Approaches, Significance of Research, Research Methods versus Methodology, Research and Scientific Method, Importance of Knowing How Research is Done, Research Process, Criteria of Good Research, and Problems Encountered by Researchers in India.

Defining the Research Problem: Research Problem, Selecting the Problem, Necessity of Defining the Problem, Technique Involved in Defining a Problem, An Illustration.

Module-2

Reviewing the literature: Place of the literature review in research, Bringing clarity and focus to your research problem, Improving research methodology, Broadening knowledge base in research area, Enabling contextual findings, How to review the literature, searching the existing literature, reviewing the selected literature, Developing a theoretical framework, Developing a conceptual framework, Writing about the literature reviewed.

Research Design: Meaning of Research Design, Need for Research Design, Features of a Good Design, Important Concepts Relating to Research Design, Different Research Designs, Basic Principles of Experimental Designs, Important Experimental Designs.

Module-3

Design of Sampling: Introduction, Sample Design, Sampling and Non-sampling Errors, Sample Survey versus Census Survey, Types of Sampling Designs.

Measurement and Scaling: Qualitative and Quantitative Data, Classifications of Measurement Scales, Goodness of Measurement Scales, Sources of Error in Measurement Tools, Scaling, Scale Classification Bases, Scaling Technics, Multidimensional Scaling, Deciding the Scale.

Data Collection: Experimental and Surveys, Collection of Primary Data, Collection of Secondary Data, Selection of Appropriate Method for Data Collection, Case Study Method.

Module-4

Testing of Hypotheses: Hypothesis, Basic Concepts Concerning Testing of Hypotheses, Testing of Hypothesis, Test Statistics and Critical Region, Critical Value and Decision Rule, Procedure for Hypothesis Testing, Hypothesis Testing for Mean, Proportion, Variance, for Difference of Two Mean, for Difference of Two Proportions, for Difference of Two Variances, P-Value approach, Power of Test, Limitations of the Tests of Hypothesis.

Chi-square Test: Test of Difference of more than Two Proportions, Test of Independence of Attributes, Test of Goodness of Fit, Cautions in Using Chi Square Tests.

Module-5

Interpretation and Report Writing: Meaning of Interpretation, Technique of Interpretation, Precaution in Interpretation, Significance of Report Writing, Different Steps in Writing Report, Layout of the Research Report, Types of Reports, Oral Presentation, Mechanics of Writing a Research Report, Precautions for Writing Research Reports.

Intellectual Property: The Concept, Intellectual Property System in India, Development of TRIPS Complied Regime in India, Patents Act, 1970, Trade Mark Act, 1999, The Designs Act, 2000, The Geographical Indications of Goods (Registration and Protection) Act 1999, Copyright Act, 1957, The Protection of Plant Varieties and Farmers' Rights Act, 2001, The Semiconductor Integrated Circuits Layout Design Act, 2000, Trade Secrets, Utility Models, IPR and Biodiversity, The Convention on Biological Diversity (CBD) 1992, Competing Rationales for Protection of IPRs, Leading International Instruments Concerning IPR, World Intellectual Property Organisation (WIPO), WIPO and WTO, Paris Convention for the Protection of Industrial Property, National Treatment, Right of Priority, Common Rules, Patents, Marks, Industrial Designs, Trade Names, Indications of Source, Unfair Competition, Patent Cooperation Treaty (PCT), Advantages of PCT Filing, Berne Convention for the Protection of Literary and Artistic Works, Basic Principles, Duration of Protection, Trade Related Aspects of Intellectual Property Rights (TRIPS) Agreement, Covered under TRIPS Agreement, Features of the Agreement, Protection of Intellectual Property under TRIPS, Copyright and Related Rights, Trademarks, Geographical indications, Industrial Designs, Patents, Patentable Subject Matter, Rights Conferred, Exceptions, Term of protection, Conditions on Patent Applicants, Process Patents, Other Use without Authorization of the Right Holder, Layout-Designs of Integrated Circuits, Protection of Undisclosed Information, Enforcement of Intellectual Property Rights, UNSECO.

Course outcomes:

At the end of the course the student will be able to:

1. Discuss research methodology and the technique of defining a research problem
2. Explain the functions of the literature review in research, carrying out a literature search, developing theoretical and conceptual frameworks and writing a review.
3. Explain various research designs, sampling designs, measurement and scaling techniques and also different methods of data collections.
4. Explain several parametric tests of hypotheses, Chi-square test, art of interpretation and writing research reports
5. Discuss various forms of the intellectual property, its relevance and business impact in the changing global business environment and leading International Instruments concerning IPR.

Question paper pattern:

The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.

- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

Textbooks:

1. 'Research Methodology: Methods and Techniques', C.R. Kothari, Gaurav Garg, New Age International, 4th Edition, 2018
2. 'Research Methodology a step-by-step guide for beginners. (For the topic Reviewing the literature under module 2)', Ranjit Kumar, SAGE Publications, 3rd Edition, 2011
3. Study Material (For the topic Intellectual Property under module 5) Professional Programme Intellectual Property Rights, Law and Practice, The Institute of Company Secretaries of India, Statutory Body Under an Act of Parliament, September 2013.

Reference Books:

1. 'Research Methods: the concise knowledge base', Trochim, Atomic Dog Publishing, 2005
2. 'Conducting Research Literature Reviews: From the Internet to Paper', Fink A, Sage Publications, 2009

M.TECH IN Industrial Electronics (EIE)

Choice Based Credit System (CBCS) and Outcome Based Education(OBE)
(Effective from the academic year 2020-21)

SEMESTER -II

Process Control Instrumentation

CourseCode	20EIE21	CIEMarks	40
Lecture Hours/Week	04	SEE Marks	60
Total Number of LectureHours	50	Exam Hours	03
Credits - 04			

Module-1

Automation – Need and Benefit: Instrumentation subsystems- Structure, Signal Interface Standards, Input data reliability enhancement, Isolation and Protection, human interface subsystems - Operation panel, Construction, control subsystems – Structure, interfacing, automation strategies-Basic and advanced strategies.

Module-2

Data Acquisition and Control Unit: Hardware and Software- Basic modules, functional modules, DACU capacity expansion, system cables, Integrated assemblies, DACU construction, Data exchange on bus, Software structure, application programming, Programmable control subsystems.

Module-3

Data Communication and Networking: Communication network, signal and data transmission, Data communication protocol, Inter process communication, cyber security, Safe and redundant network.

Module-4

Fieldbus Technology & Safety Systems: Centralized, remote- input-output, Field bus- input-output, communication, device integration, Other networks. Safety systems introduction, Process and Machine safety management.

Module-5

Management and Information Technology in Industrial Processes: Introduction, Classification of industrial processes, Manufacturing and utility processes, industrial robotics, operation technology and IT, before and after convergence, ISA 95 standard, new developments.

Course outcomes:

At the end of the course the student will be able to:

1. Comprehend the interface between process and control subsystem, manual interaction with the processes, process industrial automation system.
2. Present the latest hardware and software modules for realizing the Data Acquisition and Control Unit.
3. Manage inter and intra systems data exchange in process industrial automation systems.
4. Explain the structure of field bus I/O and the management of safety in process plants.
5. Understand the manufacturing, utility in industrial processes and also to give the Integration of operational technology and Information Technology to derive operational and business excellence.

Question paper pattern:

The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.

- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

Textbook:

‘Overview of Industrial Process Automation’, K L S Sharma, 2nd edition, ELSEVIER, 2016.

Real Time Operating System

CourseCode	20EVE22	CIEMarks	40
Lecture Hours/Week	04	SEE Marks	60
Total Number of LectureHours	50	Exam Hours	03
Credits - 04			

Module-1

Real-Time Systems and Resources: Brief history of Real Time Systems, A brief history of Embedded Systems. System Resources, Resource Analysis, Real-Time Service Utility, Scheduler concepts, Real-Time OS, State transition diagram and tables, Thread Safe Reentrant Functions (Text 1: Selected sections from Chap. 1, 2).

Module-2

Processing with Real Time Scheduling: Scheduler Concepts, Preemptive Fixed Priority Scheduling Policies with timing diagrams and problems and issues, Feasibility, Rate Monotonic least upper bound, Necessary and Sufficient feasibility, Deadline –Monotonic Policy, Dynamic priority policies, Alternative to RM policy (Text 1: Chap. 2,3,7).

Module-3

Memory and I/O: Worst case execution time, Intermediate I/O, Shared Memory, ECC Memory, Flash file systems. Multi-resource Services, Blocking, Deadlock and live lock, Critical sections to protect shared resources, Missed deadline, QoS, Reliability and Availability, Similarities and differences, Reliable software, Available software (Text 1: Selected topics from Chap. 4,5,6,7,11).

Module-4

Firmware Components: The 3 firmware components, RTOS system software mechanisms, Software application components. Debugging Components, Exceptions, assert, Checking return codes, Single-step debugging, Test access ports, Trace Ports (Text 1: Selected topics from Chap. 8,9).

Module-5

Process and Threads: Process and thread creations, Programs related to semaphores, message queue, shared buffer applications involving inter task/thread communication (Text 2: Chap. 11).

Course outcomes:

At the end of the course the student will be able to:

1. Develop programs for real time services, firmware and RTOS, using the fundamentals of Real Time Embedded System, real time service utilities, debugging methodologies and optimization techniques.
2. Select the appropriate system resources (CPU, I/O, Memory, Cache, ECC Memory, Microcontroller/ FPGA/ ASIC) to improve the system performance.
3. Apply priority based static and dynamic real time scheduling techniques for the given specifications.
4. Analyze deadlock conditions, shared memory problem, critical section problem, missed deadlines, availability, reliability and QoS.
5. Develop programs for multithreaded applications using suitable techniques and data structure

Question paper pattern:

The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.

- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

Textbooks:

1. 'Real-Time Embedded Systems and Components', Sam Siewert, Cengage Learning, India Edition, 2007.
2. 'Embedded/Real Time Systems, Concepts, Design and Programming, Black Book', Dr. K.V.K.K Prasad, Dream Tech Press, New edition, 2010.

Reference Books:

1. 'Real Time System', James W S Liu, Pearson Education, 2008.
2. 'Programming for Embedded Systems', Dream Tech Software Team, John Wiley, India Pvt. Ltd., 2008.

Design of Power Converters

CourseCode	20EIE23	CIEMarks	40
Lecture Hours/Week	04	SEE Marks	60
Total Number of LectureHours	50	Exam Hours	03
Credits - 04			

Module-1

Introduction to Control characteristics of power semiconductor devices: SCR, BJT, MOSFET, GTO, MCT, SITH, IGBT. Comparison of controllable switches.

AC to Controlled DC Converter: Thyristor circuits and their control, Gate Triggering, Single phase converters, Three phase converters (Text 1).

Module-2

DC to DC converters: Introduction, control of DC-DC converters, Buck, Boost, Buck-Boost, Cuk converter.

Inverters: Introduction, principle of operation, single phase inverters, three phase inverters-120 and 180 modes of operation (Text 1).

Module-3

Switching DC power supplies: linear power supply, overview of switching power supply, DC - DC converters with electrical isolation, flyback converter, forward converter, push-pull converter, Half and Full bridge converter, current mode control, power supply protection (Text 1).

Module-4

Magnetics for switched mode converters: Power Handling capacity of a transformer, Area product, window utilization factor.

Transformer designs – forward converter, half and Full Bridge converter, Push-pull converter, Flyback converter. Design of Inductors, problems (Text 2).

Module-5

PWM controlling Techniques: single PWM, Multiple, sinusoidal, modified, phase displacement control.

Power electronic applications: UPS, control of motor drives, criteria for selecting drive components, High frequency fluorescent lighting.

Industrial applications: Induction heating, Electric welding (Text 1).

Course outcomes:

At the end of the course the student will be able to:

1. Describe the various power semiconductor devices.
2. Analyze and design different power converter circuits.
3. Analyze various single phase and three phase power converter circuits and understand their applications.
4. Develop skills to build, and troubleshoot power electronics circuits.
5. Understand the use of power converters in commercial and industrial applications.

Question paper pattern:

The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.

- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

Textbooks:

1. 'Power Electronics: Converters, Applications and Design', M Ned Mohan Tore, Undeland and William P Robbins, 3rd Edition, John Wiley and Sons, 2003
2. 'Design of Magnetic Components for Switched Mode Power Converters', Umanand L & SRBhat, Wiley Eastern Publication, 1992.

Reference Book:

- 'Power Electronics', M H Rashid, 3rd edition, PHI / Pearson publisher, 2004.

Professional Elective 1

Wireless Sensor Networks

CourseCode	20ECS241	CIEMarks	40
Lecture Hours/Week	04	SEE Marks	60
Total Number of LectureHours	50	Exam Hours	03
Credits - 04			

Module-1

Introduction: Sensor Mote Platforms, WSN Architecture and Protocol Stack (Chap. 1Text 1).

WSN Applications: Military Applications, Environmental Applications, Health Applications, Home Applications, Industrial Applications (Chap. 2 Text 1).

Module-2

Factors Influencing WSN Design: Hardware Constraints Fault Tolerance Scalability Production Costs WSN Topology, Transmission Media, Power Consumption (Chap. 3 Text 1).

Physical Layer: Physical Layer Technologies, Overview of RF Wireless Communication, Channel Coding (Error Control Coding), Modulation, Wireless Channel Effects, PHY Layer Standards (Chap. 4 of Text 1).

Module-3

Medium Access Control: Challenges for MAC, CSMA Mechanism, Contention-Based Medium Access, Reservation-Based Medium Access, Hybrid Medium Access (Chap. 5 of Text 1).

Network Layer: Challenges for Routing, Data-centric and Flat Architecture Protocols, Hierarchical Protocols, Geographical Routing Protocols (Chap. 7 of Text 1).

Module-4

Transport Layer: Challenges for Transport Layer, Reliable MultiSegment Transport (RMST) Protocol, Pump Slowly, Fetch Quickly (PSFQ) Protocol, Congestion Detection and Avoidance (CODA) Protocol, Event-to-Sink Reliable Transport (ESRT) Protocol, GARUDA (Chap. 8 Text 1).

Application Layer: Source Coding (Data Compression), Query Processing, Network Management (Chap. 9 Text 1).

Module-5

Time Synchronization: Challenges for Time Synchronization, Network Time Protocol, Timing-Sync Protocol for Sensor Networks (TPSN), Reference-Broadcast Synchronization (RBS), Adaptive Clock Synchronization (ACS) (Chap. 11 of Text1).

Localization; Challenges in Localization, Ranging Techniques, Range-Based Localization Protocols, Range-Free Localization Protocols. (Chap. 12 Text 1).

Course outcomes:

At the end of the course the student will be able to:

1. Acquire knowledge of characteristics of mobile/wireless communication channels
2. Apply statistical models of multipath fading
3. Understand the multiple radio access techniques, radio standards and communication protocols to be used for wireless sensor
4. Design wireless sensor network system for different applications under consideration.
5. Understand the hardware details of different types of sensors and select right type of sensor for various applications.

Question paper pattern:

The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.

- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

Textbooks:

1. 'Wireless Sensor Networks', Ian F. Akyildiz and Mehmet Can Vuran, John Wiley & Sons Ltd. ISBN 978-0-470-03601-3 (H/B), 2010
2. 'Wireless Sensor Networks:Signal Processing and Communications Perspectives', Ananthram Swami, et. al., John Wiley & Sons Ltd., ISBN 978-0470-03557-3, 2007

Nanoelectronics

CourseCode	20EVE242	CIEMarks	40
Lecture Hours/Week	04	SEE Marks	60
Total Number of LectureHours	50	Exam Hours	03
Credits - 04			

Module-1

Introduction: Overview of nanoscience and engineering. Development milestones in microfabrication and electronic industry. Moores' law and continued miniaturization, Classification of Nanostructures, Electronic properties of atoms and solids: Isolated atom, Bonding between atoms, Giant molecular solids, Free electron models and energy bands, crystalline solids, Periodicity of crystal lattices, Electronic conduction, effects of nanometer length scale, Fabrication methods: Top down processes, Bottom up processes methods for templating the growth of nanomaterials, ordering of nanosystems (Text 1).

Module-2

Characterization: Classification, Microscopic techniques, Field ion microscopy, scanning probe techniques, diffraction techniques: bulk and surface diffraction techniques, spectroscopy techniques: photon, radiofrequency, electron, surface analysis and dept profiling: electron, mass, Ion beam, Reflectometry, Techniques for property measurement: mechanical, electron, magnetic, thermal properties (Text1).

Module-3

Inorganic semiconductor nanostructures: overview of semiconductor physics. Quantum confinement in semiconductor nanostructures: quantum wells, quantum wires, quantum dots, super-lattices, band offsets, electronic density of states (Text1).

Carbon Nanostructures: Carbon molecules, Carbon Clusters, Carbon Nanotubes, application of Carbon Nanotubes (Text 2).

Module-4

Fabrication techniques: requirements of ideal semiconductor, epitaxial growth of quantum wells, lithography and etching, cleaved-edge over growth, growth of vicinal substrates, strain induced dots and wires, electrostatically induced dots and wires, Quantum well width fluctuations, thermally annealed quantum

wells, semiconductor nanocrystals, colloidal quantum dots, self-assembly techniques.

Physical processes: modulation doping, quantum hall effect, resonant tunneling, charging effects, ballistic carrier transport, Inter band absorption, intra band absorption, Light emission processes, phonon bottleneck, quantum confined stark effect, nonlinear effects, coherence and dephasing, characterization of semiconductor nanostructures: optical electrical and structural (Text1).

Module-5

Methods of measuring properties: atomic, crystallography, microscopy, spectroscopy (Text 2).

Applications: Injection lasers, quantum cascade lasers, single-photon sources, biological tagging, optical memories, coulomb blockade devices, photonic structures, QWIPs, NEMS, MEMS (Text1).

Course outcomes:

At the end of the course the student will be able to:

1. Know the principles behind Nanoscience engineering and Nanoelectronics.
2. Apply the knowledge to prepare and characterize nanomaterials.
3. Know the effect of particles size on mechanical, thermal, optical and electrical properties of nanomaterials.
4. Design the process flow required to fabricate state of the art transistor technology.
5. Analyze the requirements for new materials and device structure in the future technologies.

Question paper pattern:

The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.

- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

Textbooks:

1. 'Nanoscale Science and Technology', Ed Robert Kelsall, Ian Hamley, Mark Geoghegan, John Wiley, 2007
2. 'Introduction to Nanotechnology', Charles P Poole, Jr, Frank J Owens, John Wiley, Copyright 2006, Reprint 2011.

Reference Book:

'Hand Book of Nanoscience Engineering and Technology', Ed William A Goddard III, Donald W Brenner, Sergey E. Lyshevski, Gerald J Iafrate, CRC Press, 2003

Cryptography and Network Security

CourseCode	20ECS243	CIEMarks	40
Lecture Hours/Week	04	SEE Marks	60
Total Number of LectureHours	50	Exam Hours	03
Credits - 04			

Module-1

Foundations: Terminology, Steganography, substitution ciphers and transpositions ciphers, Simple XOR, One-Time Pads, Computer Algorithms (Text 2: Chapter 1: Section 1.1 to 1.6).

SYMMETRIC CIPHERS: Traditional Block Cipher structure, Data encryption standard (DES), The AES Cipher. (Text 1: Chapter 2: Section 2.1, 2.2, Chapter 4).

Module-2

Introduction to modular arithmetic, Prime Numbers, Fermat's and Euler's theorem, primality testing, Chinese Remainder theorem, discrete logarithm. (Text 1: Chapter 7: Section 1, 2, 3, 4, 5).

Principles of Public-Key Cryptosystems, The RSA algorithm, Diffie - Hellman Key Exchange, Elliptic Curve Arithmetic, Elliptic Curve Cryptography (Text 1: Chapter 8, Chapter 9: Section 9.1, 9.3, 9.4).

Module-3

Pseudo-Random-Sequence Generators and Stream Ciphers: Linear Congruential Generators, Linear Feedback Shift Registers, Design and analysis of stream ciphers, Stream ciphers using LFSRs, A5, Hughes XPD/KPD, Nanoteq, Rambutan, Additive generators, Gifford, Algorithm M, PKZIP (Text 2: Chapter 16).

Module-4

One-Way Hash Functions: Background, Snefru, N-Hash, MD4, MD5, Secure Hash Algorithm [SHA], One way hash functions using symmetric block algorithms, Using public key algorithms, Choosing a one-way hash functions, Message Authentication Codes. Digital Signature Algorithm, Discrete Logarithm Signature Scheme (Text 2: Chapter 18: Section 18.1 to 18.5, 18.7, 18.11 to 18.14 and Chapter 20: Section 20.1, 20.4).

Module-5

E-mail Security: Pretty Good Privacy-S/MIME (Text 1: Chapter 17: Section 17.1, 17.2).

IP Security: IP Security Overview, IP Security Policy, Encapsulation Security Payload (ESP), Combining security Associations. (Text 1: Chapter 18: Section 18.1 to 18.4).

Web Security: Web Security Considerations, SSL (Text 1: Chapter 15: Section 15.1, 15.2).

Course outcomes:

At the end of the course the student will be able to:

1. Understand the basics of symmetric key and public key cryptography.
2. Use basic cryptographic algorithms to encrypt the data.
3. Generate some pseudorandom numbers required for cryptographic applications.
4. Provide authentication and protection for encrypted data.
5. Understand the techniques and features of Email, IP and Web security.

Question paper pattern:

The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.

- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

Textbooks:

1. 'Cryptography and Network Security Principles and Practice', William Stallings, Pearson Education Inc., ISBN: 978-93325-1877-3, 6th Edition, 2014
2. 'Applied Cryptography Protocols, Algorithms, and Source code in C', Bruce Schneier, Wiley Publications ISBN: 9971-51348-X, 2nd Edition

Reference Books:

1. 'Cryptography and Network Security', Behrouz A. Forouzan, TMH, 2007
2. 'Cryptography and Network Security', Atul Kahate, TMH, 2003

Reconfigurable Computing

CourseCode	20ELD244	CIEMarks	40
Lecture Hours/Week	04	SEE Marks	60
Total Number of LectureHours	50	Exam Hours	03
Credits - 04			

Module -1

Introduction: History, Reconfigurable vs Processor based system, RC Architecture.

Reconfigurable Logic Devices: Field Programmable Gate Array, Coarse Grained Reconfigurable Arrays.

Reconfigurable Computing System: Parallel Processing on Reconfigurable Computers, A survey of Reconfigurable Computing System (Text 1).

Module-2

Languages and Compilation: Design Cycle, Languages, HDL, High Level Compilation, Low level Design flow, Debugging Reconfigurable Computing Applications (Text 1).

Module -3

Implementation: Integration, FPGA Design flow, Logic Synthesis.

High Level Synthesis for Reconfigurable Devices: Modelling, Temporal Partitioning Algorithms (Text 2).

Module-4

Partial Reconfiguration Design: Partial Reconfiguration Design, Bitstream Manipulation with JBits, The modular Design flow, The Early Access Design Flow, Creating Partially Reconfigurable Designs, Partial Reconfiguration using Hansel-C Designs, Platform Design (Text 2).

Module -5

Signal Processing Applications: Reconfigurable computing for DSP, DSP application building blocks, Examples: Beamforming, Software Radio, Image and video processing, Local Neighbourhood functions, Convolution (Text 1).

System on a Programmable Chip: Introduction to SoPC, Adaptive Multiprocessing on Chip(Text 2).

Course Outcomes:

At the end of the course the student will be able to:

1. Understand the fundamental principles and practices in reconfigurable architecture.
2. Simulate and synthesize the reconfigurable computing architectures.
3. Understand the FPGA design principles, and logic synthesis
4. Integrate hardware and software technologies for reconfiguration computing focusing on partial reconfiguration design.
5. Design digital systems for a variety of applications on signal processing and system on chip configurations.

Question paper pattern:

The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.

- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

Text Books:

1. 'Reconfigurable Computing: Accelerating Computation with Field-Programmable Gate Arrays', M. Gokhale and P. Graham, Springer, ISBN: 978-0-387-26105-8, 2005.
2. 'Introduction to Reconfigurable Computing: Architectures, Algorithms and Applications', C. Bobda, Springer, ISBN: 978-1-4020-6088-5, 2007.

Reference Books:

1. 'Practical FPGA Programming in C', D. Pellerin and S. Thibault, Prentice-Hall, 2005.
2. 'FPGA Based System Design', W. Wolf, Prentice-Hall, 2004.
3. 'Rapid System Prototyping with FPGAs: Accelerating the Design Process', R. Cofer and B. Harding, Newnes, 2005.

Professional Elective 2

Automotive Electronics

CourseCode	20EIE251	CIEMarks	40
Lecture Hours/Week	04	SEE Marks	60
Total Number of LectureHours	50	Exam Hours	03
Credits - 04			

Module 1

Automotive Fundamentals, the Systems Approach to Control and Instrumentation: Use of Electronics in the Automobile, Antilock Brake Systems(ABS), Electronic steering control, Power steering, Tractioncontrol, Electronically controlled suspension (Chap.1 and2 of Text).

Module 2

Automotive instrumentation Control: Operational amplifiers, Digital circuits, Logic circuits, Microcomputer fundamentals, Microcomputer operations, Microprocessor architecture, digital to analog converter, analog to digital converter, Microcomputer applications in automotive systems, Instrumentation applications of microcomputers, Microcomputer in control systems (Chap.3 and 4 of Text).

Module 3

The basics of Electronic Engine control: Integrated body: Climate controls, Motivation for ElectronicEngine Control, Concept of An Electronic Engine Control System,Definition of General Terms, Definition of EnginePerformanceTerms, Electronic fuel control system, Engine control sequence,Electronic Ignition, Sensors and Actuators, Applications of sensors and actuators, air flow rate sensor, Indirect measurementof mass air flow, Engine crankshaft angular position sensor,Automotive engine control actuators, Digital engine control,Engine speed sensor, Timing sensor for ignition and fuel delivery,Electronic ignition control systems, Safety systems, Interiorsafety, Lighting, Entertainment systems (Chap. 5 and 6 of Text).

Module 4

Vehicle Motion Control and Automotive diagnostics: Cruisecontrol system, Digital cruise control, Timing light, Engineanalyzer, On-board and off-board diagnostics, Expert systems.Stepper motor-based actuator, Cruise control electronics,Vacuum - antilock braking system, Electronic suspension system,

Electronic steering control, Computer-based instrumentationsystem, Sampling and Input/output signal conversion, Fuelquantity measurement, Coolant temperature measurement, Oilpressure measurement, Vehicle speed measurement, Displaydevices, Trip-Information-Computer, Occupant protectionsystems (Chap. 8 and 10 of Text).

Module 5

Future automotive electronic systems: Alternative Fuel Engines, Collision Wide Range Air/Fuel Sensor, Alternative Engine, Low Tire Pressure Warning System, Collisionavoidance Radar Warning Systems, Low Tire Pressure WarningSystem, Radio Navigation, Advance Driver information System. Alternative-Fuel Engines, Transmission Control, CollisionAvoidance Radar Warning System, Low Tire Pressure WarningSystem, Speech Synthesis Multiplexing in Automobiles, ControlSignal Multiplexing, Navigation Sensors, Radio Navigation, Signpost Navigation, Dead Reckoning Navigation Future Technology, Voice Recognition Cell Phone Dialing Advanced Driver informationSystem, Automatic Driving Control (Chap. 11 of Text).

Course Outcomes:

At the end of the course the student will be able to:

1. Implement various control requirements in the automotive system.
2. Comprehend dashboard electronics and engine system electronics.
3. Identify various physical parameters that are to be sensed and monitored for maintaining the stability of the vehicle under dynamicconditions.
4. Understand and implement the controls and actuator system pertainingto the comfort and safety of commuters.
5. Design sensor network for mechanical fault diagnostics in an automotive vehicle.

Question paper pattern:

The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.

- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.

- The students will have to answer five full questions, selecting one full question from each module.

Text Book:

‘Understanding Automotive Electronics’, William B. Ribbens, SAMS/Elsevier publishing, 6th Edition, 1997.

Reference Book:

‘Automotive Electrics and Automotive Electronics-Systems and Components, Networking and Hybrid Drive’, Robert Bosch GmbH, Springer Verlag, 5th Edition, 2007.

Industrial Drives

CourseCode	20EIE252	CIEMarks	40
Lecture Hours/Week	04	SEE Marks	60
Total Number of LectureHours	50	Exam Hours	03
Credits - 04			

Module-1

An Introduction to Electrical Drives & its Applications: Electrical Drives, Advantages of Electrical Drives, Parts of Electrical Drives, Choice of Electrical Drive, Status of DC and AC Drives, Fundamental Torque Equations, Speed Torque Conventions and Multi-quadrant Operation.

Applications: Rolling mill drives, cement mill drives, paper mill drives and textile mill drives.

Module 2

Selection of Motor Power Rating: Thermal model of motor for heating and cooling, Classes of motor duty, determination of motor rating.

DC Motor Drives 1: Starting braking, transient analysis, single-phase fully controlled rectifier, control of DC separately excited motor, Single-phase half controlled rectifier: control of DC separately excited motor.

Module 3

DC Motor Drives 2: Three phase fully controlled rectifier: control of DC separately excited motor, three phases half controlled rectifier: control of DC separately excited motor, multi-quadrant operation of DC separately excited motor fed from fully controlled rectifier. Rectifier control of DC series motor, chopper controlled DC drives, chopper control of separately excited DC motor. Chopper control of series motor.

Module 4

Induction Motor Drives: Operation with unbalanced source voltage and single phasing, operation with unbalanced rotor impedances, analysis of induction motor fed from non-sinusoidal voltage supply, starting braking, transient analysis. Stator voltage control variable voltage frequency control from voltage sources, voltage source inverter control, closed loop control, current source inverter control, current regulated voltage source inverter control.

Module 5

Synchronous Motor Drives: Operation form faced frequency supply, synchronous motor variable speed drives, and variable frequency control of multiple synchronous motors. Self-controlled synchronous motor drive employing load commutated thruster inverter.

Course Outcomes:

At the end of the course the student will be able to:

1. Identify suitable power converter from the available configurations.
2. Design controllers for closed-loop operation of a separately excited DC motor drive with symmetrical optimization technique.
3. Model existing and modified power converters under small signal and steady state condition.
4. Develop power converters with better performance for challenging applications.
5. Design power converters and feedback loops.

Question paper pattern:

The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.

- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

Text Book:

‘Fundamentals of Electrical Drives’, GK Dubey, 2nd Edition, 5th reprint, Narosa publishing house.

Reference Books:

1. ‘Electrical Drives’, NK De and PK Sen, PHI, 2007.
2. ‘A First Course on Electric Drives’, SK Pillai, Wiley Eastern Ltd 1990.
3. ‘Power Electronics, Devices, Circuits and Industrial Applications’, VR Moorthi, Oxford University Press, 2005.

Micro Electro Mechanical Systems

CourseCode	20ELD253	CIEMarks	40
Lecture Hours/Week	04	SEE Marks	60
Total Number of LectureHours	50	Exam Hours	03
Credits - 04			

Module 1

Overview of MEMS and Microsystems: MEMS and Microsystem, Typical MEMS and Microsystems Products, Evolution of Microfabrication, Microsystems and Microelectronics, Multidisciplinary Nature of Microsystems, Miniaturization. Applications and Markets.

Module 2

Working Principles of Microsystems: Introduction, Microsensors, Microactuation, MEMS with Microactuators, Microaccelerometers, Microfluidics.

Engineering Science for Microsystems Design and Fabrication: Introduction, Atomic Structure of Matters, Ions and Ionization, Molecular Theory of Matter and Inter-molecular Forces, Doping of Semiconductors, The Diffusion Process, Plasma Physics, Electrochemistry.

Module 3

Engineering Mechanics for Microsystems Design: Introduction, Static Bending of Thin Plates, Mechanical Vibration, Thermomechanics, Fracture Mechanics, Thin Film Mechanics, Overview on Finite Element Stress Analysis.

Module 4

Scaling Laws in Miniaturization:

Introduction, Scaling in Geometry, Scaling in Rigid-Body Dynamics, Scaling in Electrostatic Forces, Scaling of Electromagnetic Forces, Scaling in Electricity, Scaling in Fluid Mechanics, Scaling in Heat Transfer.

Module 5

Overview of Micro-manufacturing: Introduction, Bulk Micro-manufacturing, Surface Micromachining, The LIGA Process, Summary on Micromanufacturing.

Microsystem Design: Introduction, Design Considerations, Process Design, Mechanical Design, Using Finite Element Method.

Course Outcomes:

At the end of the course the student will be able to:

1. Understand the technologies related to Micro Electro Mechanical Systems.
2. Relate to the scaling laws in miniaturization.
3. Analyse the MEMS devices and develop suitable mathematical models
4. Understand the various application areas for MEMS devices
5. Describe the design and fabrication processes involved with MEMS devices.

Question paper pattern:

The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.

- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

Text Book:

‘MEMS and Micro systems: Design, Manufacture and Nanoscale Engineering’, Tai-Ran Hsu, John Wiley & Sons, ISBN: 978-0470-08301-7, 2nd Edition, 2008

Reference Books:

1. ‘Micro and Nano Fabrication: Tools and Processes’, Hans H. Gatzert, Volker Saile, Jurg Leuthold, Springer, 2015
2. ‘Micro Electro Mechanical Systems (MEMS)’, Dilip Kumar Bhattacharya, Brajesh Kumar Kaushik, Cengage Learning.

Synthesis and Optimization of Digital Circuits

CourseCode	20EIE254	CIEMarks	40
Lecture Hours/Week	04	SEE Marks	60
Total Number of LectureHours	50	Exam Hours	03
Credits - 04			

Module 1

Introduction to Synthesis and Optimization: Design of Microelectronics circuits, Computer aided Synthesis and Optimization.

Hardware Modeling: HDLs for Synthesis, Abstract models, Compilation and Behavioral Optimization(Text 1: Topics from Chap. 1,3).

Module 2

Graph theory for CAD for VLSI: Graphs, Combinatorial Optimization, Graph Optimization problems and Algorithms, Boolean Algebra and Applications.

Architectural Synthesis and Optimization: Fundamental Architectural Synthesis problems, Area and Performance Estimation, Strategies for Architectural Optimization, Datapath Synthesis, Control Path Synthesis (Text1: Topics from Chap. 2,4).

Module 3

Two level Combinational Logic Optimization: Introduction, Logic Optimizations, Operations on Two level Logic Covers, Algorithms for Logic Minimization, Symbolic Minimization and Encoding Problems.

Multiple Level Combinational Logic Optimization: Introduction, Models and Transformations for Combinational Networks, The Algebraic Model, The Boolean Model (Text1: Chap. 7, 8).

Module 4

Sequential Logic Optimization: Introduction, Sequential Logic Optimization using State based Models, Sequential Logic Optimization using Network Models, Implicit FSM Traversal Methods, Testability concerns for Synchronous Circuits (Text 1: Chap. 9).

Module 5

Scheduling Algorithms: Introduction, A Model for Scheduling problems, Scheduling with Resource Constraints, Scheduling without Resource

Constraints, Scheduling Algorithms for Extended Sequencing Models, Scheduling Pipelined Circuits.

Resource Sharing and Binding: Sharing and Binding for Resource dominated circuits, Sharing and Binding for General Circuits, Concurrent Binding and Scheduling(Text1: Chap. 5,6).

Course Outcomes:

At the end of the course the student will be able to:

- 1.Understand the process of synthesis and optimization in a top down approach for digital circuits models using HDLs.
2. Understand the terminologies of graph theory and its algorithms to optimize a Boolean equation.
3. Apply different two level and multilevel optimization algorithms for combinational circuits.
4. Apply the different sequential circuit optimization methods using state models and network models.
5. Apply different scheduling algorithms with resource binding and without resource binding for pipelined sequential circuits and extended sequencing models.

Question paper pattern:

The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.

- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

Text Book:

‘Synthesis and Optimization of Digital Circuits’, Giovanni De Micheli, Tata McGraw-Hill, ISBN: 9780070582781, 2003.

Reference Book:

‘Automatic Logic synthesis Techniques for Digital Systems’, Edwards M.D, Macmillan New Electronic Series, 1992.

Embedded and Signal Processing Lab

CourseCode	20EIEL26	CIEMarks	40
TeachingHours/Week	04 (2 Hrs Tutorial + 2 Hrs Practical)	SEE Marks	60
		Exam Hours	03
Credits - 02			

Laboratory Experiments:

PART-A: Following RTOS experiments to be done using Linux.

SL.N o.	Experiments
1	Develop and test programs to (a) create child process and display its ID and (b) Execute child process function using switch structure.
2	Develop and test the program for a multithreaded application, where communication is through a buffer for the conversion of lowercase text to uppercase text, using semaphore concept.
3	Develop and test the program for a multithreaded application, where communication is through shared memory for the conversion of lowercase text to uppercase text.
4	Develop program for inter-thread communication using message queue. Data is to be input from the keyboard for the chosen application.
5	Create 'n' number of child threads. Each thread prints the message "I'm in thread number ..." and sleeps for 50 ms and then quits. The main thread waits for complete execution of all the child threads and then quits. Compile and execute in Linux.
6	Implement the multi-thread application satisfying the following: i. Two child threads are created with normal priority. ii. Thread 1 receives and prints its priority and sleeps for 50ms and then quits. iii. Thread 2 prints the priority of the thread 1 and rises its priority to above normal and retrieves the new priority of thread 1, prints it and then quits. iv. The main thread waits for the child thread to complete its job and quits.
7	Implement the usage of anonymous pipe with 512 bytes for data

	sharing between parent and child processes using handle inheritance mechanism.
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PART-B: Digital Signal Processing using MATLAB

Sl. No.	Experiments
1	<p>Comparison of DFT and DCT (in terms of energy compactness)</p> <p>Generate the sequence $x[n] = n-64$ for $n=0, \dots, 127$.</p> <p>(a) Let $X[k]=DFT\{x[n]\}$. For various values of L, set to zero the “high frequency coefficients” $X[64-L]=\dots X[64]=\dots = X[64+L]=0$. Take the inverse DFT and plot the results.</p> <p>(b) Let $X_{DCT}[k]=DCT(x[n])$. For the same values of L, set to zero the high frequency coefficients $X_{DCT}[127-L]=\dots X_{DCT}[127]$. Take the inverse DCT for each case and compare the reconstruction with the previous case.</p>
2	<p>Design digital FIR LPF and HPF using the following windows techniques.</p> <p>i) Hamming window function</p> <p>ii) Kaiser window function</p>
3	<p>Design digital IIR Butterworth low pass and high pass filter using bilinear transformation.</p> <p>Compare FIR and IIR filter in terms of performance (accuracy in meeting specifications) and computational complexity.</p>
4	<p>Compute Fourier Transform & its inverse Fourier Transform of an image.</p>
5	<p>Compute FFT when N is not a power of 2.</p>
6	<p>Design an equiripple filter for the given specification.</p>

Course outcomes:

At the end of the course the student will be able to:

1. Select a suitable task switching technique in a multithreaded application.
2. Implement different techniques of message passing and Intertask/thread communication.
3. Implement different data structures such as pipes, queues, shared memory, semaphores, buffers in multithreaded programming.
4. Implement DCT, DFT, FFT and IFFT for the given input data.
5. Implement the appropriate design method for FIR and IIR filters.

Conduct of Practical Examination:

1. All laboratory experiments are to be included for practical examination.
2. Students are allowed to pick one experiment from the lot, consisting of two questions selected one from each part.
3. Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.
4. Change of experiment is allowed only once and Marks allotted to the procedure part to be made zero.

Technical Seminar

CourseCode	20EIE27	CIEMarks	100
Number of Contact Hours/Week	02	SEE Marks	-
		Exam Hours	-
Credits - 02			

Course objectives:

The objective of the seminar is to inculcate self-learning, face audience confidently, enhance communication skill, involve in group discussion and present and exchange ideas.

Each student, under the guidance of a Faculty, is required to

- Choose, preferably through peer reviewed journals, a recent topic of his/her interest relevant to the Course of Specialization.
- Carryout literature survey, organize the Course topics in a systematic order.
- Prepare the report with own sentences.
- Type the matter to acquaint with the use of Micro-soft equation and drawing tools or any such facilities.
- Present the seminar topic orally and/or through power point slides.
- Answer the queries and involve in debate/discussion.
- Submit two copies of the typed report with a list of references.

The participants shall take part in discussion to foster friendly and stimulating environment in which the students are motivated to reach high standards and become self-confident.

The CIE marks for the seminar shall be awarded (based on the relevance of the topic, presentation skill, participation in the question and answer session and quality of report) by the committee constituted for the purpose by the Head of the Department. The committee shall consist of three faculties from the department with the senior most acting as the Chairperson.

Marks distribution for CIE of the course 20EIE27 seminar:

Seminar Report: 50 marks
Presentation skill: 25 marks
Question and Answer: 25 marks

M.TECH IN Industrial Electronics (EIE)

Choice Based Credit System (CBCS) and Outcome Based Education(OBE)
(Effective from the academic year 2020-21)

SEMESTER -III

PLCs and Industrial Automation

CourseCode	20EIE31	CIEMarks	40
Lecture Hours/Week	04	SEE Marks	60
Total Number of LectureHours	50	Exam Hours	03
Credits - 04			

Module -1

Introduction to PLCs: Technical Definition, Advantages, Characteristic Functions, Chronological Evolution, Types, Unitary PLC, Modular PLC, SMEEI PLC, Medium PLC, Large PLC, Block Diagram Of PLC, Input / Output Section, Processor Section, Power Supply, Memory, Central Processing Unit, Processor Software / Executive Software, Multitasking, Languages, Ladder Language.

Bit Logic Instructions: Introduction, Input and Output Contact Program, Symbols, Numbering System of Inputs and Outputs, Program Format, Introduction to Logic, Equivalent Ladder Diagram of - AND Gate, OR Gate, NOT Gate, XOR Gate, NAND Gate, NOR Gate, Equivalent Ladder Diagram to Demonstrate De Morgan Theorem, Ladder Design.

Module -2

PLC Timers and Counters: Timer and its Classification, Characteristics of PLC Timer, Functions in Timer, Resetting – Retentive and Non-Retentive, Classification of PLC Timer, On Delay, and Off Delay Timers, Timer-On Delay, Timer Off Delay, Retentive And Non-Retentive Timers, Format of a Timer Instruction. PLC Counter, Operation of PLC Counter, Counter Parameters, Counter Instructions. Overview, Count Up (CTU), Count Down (CTD).

Advanced Instructions: Comparison Instructions, Addressing Data Files, Format of Logical Address, Addressing Format for Micrologic System, Different Addressing Types. Data Movement Instructions.

Module -3

Logical Instructions: Mathematical Instructions and its Features, Special Mathematical Instructions, Scale with Parameters or SCP Instruction. Data

Handling Instructions and its Features, Program Flow Control Instructions, Proportional Integral Derivative (PID) Instruction.

PLC I/O Modules and Power Supply: Classification of I/O, I/O System Overview, Practical I/O System and its mapping, Addressing Local and Expansion I/O, Input-Output Systems, Direct I/O Parallel I/O Systems Serial I/O Systems, Sinking and Sourcing, Sourcing and Sinking in PLC Interfacing, Discrete Input Module, Discrete DC Input Module, Discrete AC Input Module, Rectifier with Filter, Threshold Detection, Isolation, Logic Section, Discrete Output Modules, Advantages and Disadvantages of Output Modules, Types of Analog Input Module.

Module -4

Industrial Communication: Introduction, Evolution of Industrial Control Process, Types of Communication Interface, Types of Networking Channels, Parallel Communication Interface. Serial Communication Interface, communication mode, Synchronous and Asynchronous Transmissions, Standard Interface RS 232C, RS 422, EIA 485, Comparison, Software Protocol, Industrial Network. Network Topology, Media Access Methods.

Module -5

Industrial Networking: Open System Interconnection (OSI), Network Model, Network Components, Control Network Issues, Advantage of Standardized Industrial Network, Intelligent Devices, Industrial Network Bus Network, Device Bus Network vs. Process Bus Network, Controller Area Network (CAN), DeviceNet, ControlNet, Ethernet Protocol, AS-I Interface, FOUNDATION FIELDBUS, Application of Profibus for Real PLC Communication.

Industrial Automation: Introduction, Utility of Automation, General Structure of an Automated Process, Examples of Simple Automated Systems, Selection of PLC.

Course Outcomes:

At the end of the course the student will be able to:

1. Gain knowledge on Programmable Logic Controllers.
2. Understand different types of Devices to which PLC input and output modules are connected.
3. Create ladder diagrams from process control descriptions.
4. Apply PLC timers and counters for the control of industrial processes.
5. Acquire the Knowledge of Networking in Industrial automation.

Question paper pattern:

The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.

- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

Text Book:

‘Programmable LogicControllers and Industrial Automation’,
Madhuchhanda Mitra and Samarjit Sengupta, Penram International
Publishing (India) Pvt. Ltd., 2007. ISBN: 81-87972-17-3.

Reference Books:

1. ‘Introduction to Programmable Logic Controllers’, Garry Dunning,
2nd Edition, Delmar Thomson Learning, 2001. ISBN: 981-240-625-5.
2. ‘Computer Control of Processes’, M. Chidambaram, CRC Press, 2002.

Professional Elective 3

Advances in Image Processing

CourseCode	20ECS321	CIEMarks	40
Lecture Hours/Week	03	SEE Marks	60
Total Number of LectureHours	40	Exam Hours	03
Credits - 03			

Module-1

The image, its representations and properties: Image representations a few concepts, Image digitization, Digital image properties, Color images.

Module-2

Image Pre-processing: Pixel brightness transformations, geometric transformations, local pre-processing.

Module-3

Segmentation: Thresholding; Edge-based segmentation – Edge image thresholding, Edge relaxation, Border tracing, Hough transforms; Region – based segmentation – Region merging, Region splitting, Splitting and merging, Watershed segmentation, Region growing post-processing.

Module-4

Shape representation and description: Region identification; Contour-based shape representation and description – Chain codes, Simple geometric border representation, Fourier transforms of boundaries, Boundary description using segment sequences, B-spline representation; Region-based shape representation and description – Simple scalar region descriptors, Moments, Convex hull.

Module-5

Mathematical Morphology: Basic morphological concepts, Four morphological principles, Binary dilation and erosion, Skeletons and object marking, Morphological segmentations and watersheds.

Course outcomes:

At the end of the course the student will be able to:

1. Understand the representation of the digital image and its properties.
2. Apply pre-processing techniques required to enhance the image for its further analysis.
3. Use segmentation techniques to select the region of interest in the image for analysis.

4. Represent the image based on its shape and edge information and also describe the objects present in the image based on its properties and structure.
5. Use morphological operations to simplify images, and quantify and preserve the main shape characteristics of the objects.

Question paper pattern:

The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.

- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

Text Book:

‘Image Processing, Analysis, and Machine Vision’, Milan Sonka, Vaclav Hlavac, Roger Boyle, Cengage Learning, ISBN: 978-81-315-1883-0, 2013

Reference Books:

1. ‘Digital Image Processing for Medical Applications’, Geoff Dougherty, Cambridge university Press, 2010.
2. ‘Digital Image Processing’, S Jayaraman, S Esakkirajan, T Veerakumar, Tata McGraw Hill, 2011.

Medical Imaging

CourseCode	20EIE322	CIEMarks	40
Lecture Hours/Week	03	SEE Marks	60
Total Number of LectureHours	40	Exam Hours	03
Credits - 03			

Module 1

Generation and Detection of X-Rays: X-Ray generation and X-Ray generators, Filters, Beam Restrictors and Grids, Screens, X-RayDetectors.

X-Ray Diagnostic Methods: Conventional X-Ray Radiography,Fluoroscopy, Angiography, Mammography, Xeroradiography, ImageSubtraction.

X-Ray Image Characteristics: Spatial Resolution, Image Noise,Image contrast.

Biological Effects of Ionizing Radiation: Determination ofbiological effects, Short term and Long term effects.

Module 2

X-Ray Tomography: Conventional Tomography, Computed Tomography - Projection function, Algorithms for ImageReconstruction, CT number, Image Artifacts.

Digital Radiography: Digital Subtraction Angiography (DSA), DualEnergy Subtraction, K-Edge subtraction, 3-D Reconstruction.

Recent Developments: Dynamic Spatial Reconstructor (DSR),Imatron or Fastrac Electron Beam CT.

Module 3

Generation and Detection of Ultrasound: Piezoelectric effect,Ultrasonic Transducers, Transducer Beam Characteristics, Axial and Lateral resolution, Focusing and Arrays.

Ultrasonic Diagnostic Methods: Pulse Echo systems - A mode, Bmode, M mode and C mode, Transmission Methods, Dopplermethods, Duplex Imaging.

Biological Effects of Ultrasound: Acoustic phenomena at highintensity levels, Ultrasound Bioeffects.

Module 4

Generation and Detection of Nuclear Emission: Nuclear Sources, Radionuclide Generators, Nuclear Radiation Detectors, Collimators.

Diagnostic methods using Radiation Detector Probes: ThyroidFunction test, Renal function test, Blood volume measurement.

New Radio Nuclide Imaging methods: Longitudinal Section Tomography, SPECT and PET

Characteristics of Radionuclide Images: Spatial Resolution, Image contrast, Image Noise.

Module 5

Generation and Detection of NMR signal: The NMR Coil/Probe, The transmitter and the Receiver, Data acquisition.

Magnetic Resonance Imaging methods: Spin Echo Imaging, Gradient Echo Imaging, Blood flow Imaging.

Characteristics of MRI images: Spatial Resolution, Image Contrast.

Imaging Safety.

Course outcomes:

At the end of the course the student will be able to:

1. Understand the Generation and Detection of X-Rays, the Diagnostic Methods, Characteristics of X-ray images and Biological effects of X-rays.
2. Analyze Computed tomography and Digital Radiography.
3. Learn the techniques of Generation and Detection of Ultrasound, Pulse Echo Systems and Ultrasonic Diagnostic Methods.
4. Understand the principles of various radiological imaging techniques such as SPECT and PET.
5. Understand the principles of Magnetic Resonance Imaging, the concepts of Radionuclide Generation and Detection.

Question paper pattern:

The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.

- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

Text Book:

'Principles of Medical Imaging', Kirk Shung, Michael B Smith, Benjamin M W Tsui, Academic Press, 2012.

Reference Books:

1. 'Fundamentals of Medical Imaging', Zhong Hicho and Manbir Singh, John Wiley, 1993.
2. 'Nuclear Medicine Introductory Text', Peter Josefell & Edwards Sydney, William Blackwell Scientific Publishers, London.

Business Intelligence and its Applications

CourseCode	20ELD323	CIEMarks	40
Lecture Hours/Week	03	SEE Marks	60
Total Number of LectureHours	40	Exam Hours	03
Credits - 03			

Module 1

Development Steps, BI Definitions, BI Decision Support Initiatives, DevelopmentApproaches, Parallel Development Tracks, BI Project Team Structure, Business Justification,Business Divers, Business Analysis Issues, Cost – Benefit Analysis, Risk Assessment,Business Case Assessment Activities, Roles Involved In These Activities, Risks of NotPerforming Step, Hardware, Middleware, DBMS Platform, NonTechnical InfrastructureEvaluation

Module 2

Managing The BI Project, Defining And Planning The BI Project, Project PlanningActivities, Roles And Risks Involved In These Activities, General Business Requirement,Project Specific Requirements, Interviewing Process.

Module 3

Differences in Database Design Philosophies, Logical Database Design, Physical DatabaseDesign, Activities, Roles And Risks Involved In These Activities, Incremental Rollout,Security Management, Database Backup And Recovery.

Module 4

Growth Management, Application Release Concept, Post Implementation Reviews, Release Evaluation Activities, The Information Asset and Data Valuation, Actionable Knowledge –ROI, BI Applications, The Intelligence Dashboard.

Module 5

Business View of Information technology Applications: Business Enterprise excellence, Key purpose of using IT, Type of digital data, basics of enterprise reporting, BI road ahead.

Course outcomes:

At the end of the course the students will be able to:

1. Evaluate the key elements of a successful business intelligence (BI) program
2. Apply a BI meta model that turns outcomes into actions
3. Extract and transform data from an operational data to a data business data
4. Evaluate business analytics and performance measurement tools
5. Demonstrate a business scenario, identify the metrics, indicators and make recommendations to achieve the business goal.

Question paper pattern:

The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.

- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

Text Books:

1. 'Business Intelligence Roadmap: The Complete Project Lifecycle for Decision Support Applications', Larissa T Moss and ShakuAtre, Addison Wesley Information Technology Series, 2003.
2. 'Fundamentals of Business Analytics', R N Prasad, Seema Acharya, Wiley India, 2011.

Reference Books:

1. 'Business Intelligence: The Savvy Manager's Guide', David Loshin, Publisher: Morgan Kaufmann, ISBN 1-55860-196-4.
2. 'Delivering Business Intelligence with Microsoft SQL Server 2005', Brian Larson, McGraw Hill, 2006.
3. 'Foundations of SQL Server 2008', Lynn Langit, Business Intelligence – Apress, ISBN 13: 978-14302-3324-4, 2011.

RF MEMS

CourseCode	20ECS324	CIEMarks	40
Lecture Hours/Week	03	SEE Marks	60
Total Number of LectureHours	40	Exam Hours	03
Credits - 03			

Module 1

Review: Introduction to MEMS: Fabrication for MEMS transducers and actuators, Microsensing for MEMS, Materials for MEMS.

MEMS materials and fabrication techniques: Metals, Semiconductors, Thin films, Materials for polymer MEMS, Bulk machining for Silicon based MEMS, Surface machining for Silicon based MEMS, Micro stereo-lithography for polymer MEMS.

Module 2

RF MEMS Switches and micro-relays: Switch parameters, Basics of switching, Switches for RF and Microwave applications, Actuation mechanisms, Micro-relays and micro-actuators, Dynamic of switch operations, MEMS switch design and design consideration, MEMS inductors and capacitors.

Module 3

Micro machined RF filters and phase shifters: RF filters, Modelling of mechanical filters, Micro-mechanical filters, SAW filters - Basic, Design consideration. Bulk acoustic wave filters, Micro-machined filters for millimetre wave frequencies. Micro-machined phase shifters, Types and limitations, MEMS and Ferroelectric phase shifters, Applications.

Module 4

Micromachined transmission line and components: Micromachined transmission line: Losses in transmission line, coplanar lines, Microshield and membrane supported lines, Microshield components, Micromachined waveguides, Directional couplers and Mixers, Resonators and Filters.

Module 5

Micromachined antennas: design, Fabrication and measurements. Integration and packaging for RF MEMS. Roles and types of packages, Flip chip techniques, Multichip module packaging and Wafer bonding, Reliability issues and thermal issues.

Course outcomes:

At the end of the course the students will be able to:

1. Comprehend the need for micromachining and MEMS based systems for RF and microwave applications
2. Describe the micromachining techniques and their use in the fabrication of micro switches, capacitors and inductors
3. Design MEMS based microwave components aimed at reducing insertion loss and increasing bandwidth.
4. Realize high Q micromechanical filters for frequencies up to and beyond 10 MHz, and micromachined surface acoustic wave (SAW) filters filling the gap up to 2 GHz.
5. Describe the packaging approaches used for these RF MEMS devices.

Question paper pattern:

The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.

- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

Text Book:

‘RF MEMS and their Applications’, Vijay K Varadan, K. J. Vinoy and K. A. Jose, Wiley India Pvt. Ltd., ISBN - 10 : 8126529911, 2011.

Reference books:

1. ‘RF MEMS circuit design’, J De Los Santos, Artech House, 2002.
2. ‘Transaction Level Modelling with System C: TLM concepts and applications for Embedded Systems’, Frank Ghenassia, Springer, 2005.
3. ‘Networks on chips: Technology and Tools’, Luca Benini, Morgan Kaufmann Publishers, 2006.

Professional elective 4

Advanced Power Electronic Converters and Applications

CourseCode	20EIE331	CIEMarks	40
Lecture Hours/Week	03	SEE Marks	60
Total Number of LectureHours	40	Exam Hours	03
Credits - 03			

Module 1

Introduction to power electronics: Introduction to Power Processing, Several Applications of Power Electronics, Elements of Power Electronics.

Principles of Steady State Converter Analysis: Inductor Volt-Second Balance, Capacitor Charge Balance, and the Small-Ripple Approximation, Boost Converter Example, Cuk Converter Example Estimating the Output voltage ripple and inductor current ripple in converters Containing Two-Pole Low-Pass Filter (Text 1).

Module 2

Converter Dynamics and Control: AC Equivalent Circuit Modeling, The Basic AC Modeling Approach, State-Space Averaging, Circuit Averaging and Averaged Switch Modeling, The Canonical Circuit Model, Modeling the Pulse-Width Modulator, Analysis of Converter Transfer Functions, Graphical Construction of Impedances and Transfer Functions (Text 1).

Module 3

Controller Design: Introduction, Effect of Negative Feedback on the Network Transfer Functions, Construction of the Important Quantities $1/(1 + T)$ and $T/(1 + T)$ and the Closed-Loop Transfer Functions, Stability, The Phase Margin Test, The Relationship Between Phase Margin and Closed-Loop Damping Factor, Transient Response vs. Damping Factor, Regulator Design, Measurement of Loop Gains (Text 1).

Module 4

Modern Rectifiers and Power System Harmonics: Power and Harmonics in Nonsinusoidal Systems, Pulse-Width Modulated Rectifiers.

Resonant Converters: Sinusoidal Analysis of Resonant Converters with examples (Text 1).

Module 5

Power supply applications: Switching DC Power Supplies, Motor drive applications: Introduction to Motor Drives, DC-Motor Drives, Residential and Industrial Applications, Electric Utility Applications (Text 2).

Course outcomes:

At the end of the course the students will be able to:

1. Estimate and analyze the dynamics of power electronic converters
2. Understand the sustainable energy generation technologies.
3. Perform Modelling and analysis of power electronic systems and equipment using computational software.
4. Simulate and analyze resonant converters.
5. Apply the knowledge of mathematics to converter/machine dynamics in Electrical engineering.

Question paper pattern:

The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.

- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

Text Books:

1. 'Fundamentals of Power Electronics', Erickson and Maksimovic, 2nd Edition, Kluwer Academic Publishers, 2001.
2. 'Power Electronics converters, Applications and Design', M Ned Mohan, Tore Undeland and William P Robbins, John Wiley and Sons, 3rd Edition, 2002.

Reference Books:

1. 'Switching Power Supply Design', Abraham Pressman, McGraw-Hill Publishers, 1998.
2. 'Power Electronics Handbook', Muhammad H. Rashid, 2nd Edition, Academic Press, 2007.

Pattern Recognition & Machine Learning

CourseCode	20ESP332	CIEMarks	40
Lecture Hours/Week	03	SEE Marks	60
Total Number of LectureHours	40	Exam Hours	03
Credits - 03			

Module 1

Introduction: Probability Theory, Model Selection, The Curse of Dimensionality, Decision Theory, Information Theory

Distributions: Binary and Multinomial Variables, The Gaussian Distribution, The Exponential Family, Nonparametric Methods (Ch. 1,2).

Module-2

Supervised Learning

Linear Regression Models: Linear Basis Function Models, The Bias-Variance Decomposition, Bayesian Linear Regression, Bayesian Model Comparison

Classification & Linear Discriminant Analysis: Discriminant Functions, Probabilistic Generative Models, Probabilistic Discriminative Mode (Ch. 3,4).

Module-3

Supervised Learning

Kernels: Dual Representations, Constructing Kernels, Radial Basis Function Network, Gaussian Processes

Support Vector Machines: Maximum Margin Classifiers, Relevance Vector Machines

Neural Networks: Feed-forward Network, Network Training, Error Backpropagation (Ch. 5,6,7).

Module-4

Unsupervised Learning

Mixture Models: K-means Clustering, Mixtures of Gaussians, Maximum likelihood, EM for Gaussian mixtures, Alternative View of EM.

Dimensionality Reduction: Principal Component Analysis, Factor/Component Analysis, Probabilistic PCA, Kernel PCA, Nonlinear Latent Variable Models (Ch. 9,12).

Module-5

Probabilistic Graphical Models: Bayesian Networks, Conditional Independence, Markov Random Fields, Inference in Graphical Models, Markov Model, Hidden Markov Models (Ch.8,13).

Course outcomes:

At the end of the course the students will be able to:

1. Identify areas where Pattern Recognition and Machine Learning can offer a solution.
2. Describe the strength and limitations of some techniques used in computational Machine Learning for classification, regression and density estimation problems.
3. Describe and model data.
4. Solve problems in Regression and Classification.
5. Discuss main and modern concepts for model selection and parameter estimation in recognition, decision making and statistical learning problems.

Question paper pattern:

The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.

- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

Text Book:

‘Pattern Recognition and Machine Learning’, Christopher Bishop, Springer, 2006.

Internet of Things

CourseCode	20ECS333	CIEMarks	40
Lecture Hours/Week	03	SEE Marks	60
Total Number of LectureHours	40	Exam Hours	03
Credits - 03			

Module-1

What is IoT ?

Genesis, Digitization, Impact, Connected Roadways, Buildings, Challenges

IoT Network Architecture and Design

Drivers behind new network Architectures, Comparing IoT Architectures, M2M architecture, IoT world forum standard, IoT Reference Model, Simplified IoT Architecture.

Module-2

IoT Network Architecture and Design

Core IoT Functional Stack, Layer1 (Sensors and Actuators), Layer 2 (Communications Sublayer), Access network sublayer, Gateways and backhaul sublayer, Network transport sublayer, IoT Network management.

Layer 3 (Applications and Analytics) – Analytics vs Control, Data vs Network Analytics, IoT Data Management and Compute Stack

Module-3

Engineering IoT Networks

Things in IoT – Sensors, Actuators, MEMS and smart objects.

Sensor networks, WSN, Communication protocols for WSN

Communications Criteria, Range, Frequency bands, power consumption, Topology, Constrained Devices, Constrained Node Networks

IoT Access Technologies, IEEE 802.15.4

Competitive Technologies – Overview only of IEEE 802.15.4g, 4e, IEEE 1901.2a

Standard Alliances – LTE Cat 0, LTE-M, NB-IoT

Module-4

Engineering IoT Networks

IP as IoT network layer, Key Advantages, Adoption, Optimization, Constrained Nodes, Constrained Networks, IP versions, Optimizing IP for IoT.

Application Protocols for IoT – Transport Layer, Application Transport layer, Background only of SCADA, Generic web based protocols, IoT Application Layer

Data and Analytics for IoT – Introduction, Structured and Unstructured data, IoT Data Analytics overview and Challenges.

Module-5

IoT in Industry (Three Use cases)

IoT Strategy for Connected manufacturing, Architecture for Connected Factory Utilities – Power utility, IT/OT divide, Grid blocks reference model, Reference Architecture, Primary substation grid block and automation.

Smart and Connected cities –Strategy, Smart city network Architecture, Street layer, city layer, Data center layer, services layer, Smart city security architecture, Smart street lighting.

Course outcomes:

At the end of the course the student will be able to:

1. Understand the basic concepts IoT Architecture and devices employed.
2. Analyze the sensor data generated and map it to IoT protocol stack for transport.
3. Apply communications knowledge to facilitate transport of IoT data over various available communications media.
4. Design a use case for a typical application in real life ranging from sensing devices to analyzing the data available on a server to perform tasks on the device.
5. Apply knowledge of Information technology to design of IoT applications (Operational Technology).

Question paper pattern:

The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.

- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

Text Book:

‘CISCO, IoT Fundamentals – Networking Technologies, Protocols, Use Cases for IoT’, David Hanes, Gonzalo Salgueiro, Patrick Grossetete, Robert Barton, Jerome Henry, Pearson Education, ISBN: 978-9386873743, First edition, 2017

Reference Book:

‘Internet of Things – A Hands on Approach’, ArshdeepBahga and Vijay Madiseti, Orient Blackswan Private Limited - New Delhi, First edition, 2015

Communication System Design using DSP algorithm

CourseCode	20ESP334	CIEMarks	40
Lecture Hours/Week	03	SEE Marks	60
Total Number of LectureHours	40	Exam Hours	03
Credits - 03			

Module 1

Introduction to the course: Digital filters, Discrete time convolution and frequency responses, FIR filters - Using circular buffers to implement FIR filters in C and using DSP hardware, Interfacing C and assembly functions, Linear assembly code and the assembly optimizer. IIR filters - realization and implementation, FFT and power spectrum estimation: DTFT window function, DFT and IDFT, FFT, Using FFT to implement power spectrum.

Module 2

Analog modulation scheme: Amplitude Modulation - Theory, generation and demodulation of AM, Spectrum of AM signal, Envelope detection and square law detection, Hilbert transform and complex envelope, DSP implementation of amplitude modulation and demodulation.

DSBSC: Theory generation of DSBSC, Demodulation, and demodulation using coherent detection and Costas loop. Implementation of DSBSC using DSP hardware.

SSB: Theory, SSB modulators, Coherent demodulator, Frequency translation, Implementation using DSP hardware.

Module 3

Frequency modulation: Theory, Single tone FM, Narrow band FM, FM bandwidth, FM demodulation, Discrimination and PLL methods, Implementation using DSP hardware.

Digital Modulation scheme: PRBS, and data scramblers: Generation of PRBS, Self-synchronizing data scramblers, Implementation of PRBS and data scramblers. RS-232C protocol and BER tester: The protocol, error rate for binary signaling on the Gaussian noise channels, Three-bit error rate tester and implementation.

Module 4

PAM and QAM: PAM theory, baseband pulse shaping and ISI, Implementation of transmit filter and interpolation filter bank. Simulation and theoretical exercises for PAM, Hardware exercises for PAM.

QAM fundamentals: Basic QAM transmitter, 2 constellation examples, QAM structures using passband shaping filters, Ideal QAM demodulation, QAM experiment. QAM receivers-Clock recovery and other frontend sub-systems. Equalizers and carrier recovery systems.

Module 5

Experiment for QAM receiver frontend, Adaptive equalizer, Phase splitting, Fractionally spaced equalizer. Decision directed carrier tracking, Blind equalization, Complex cross coupled equalizer and carrier tracking experiment. Echo cancellation for full duplex modems: Multicarrier modulation, ADSL architecture, Components of simplified ADSL transmitter, A simplified ADSL receiver, Implementing simple ADSL Transmitter and Receiver.

Course outcomes:

At the end of the course the students will be able to:

1. Realize communication systems, including algorithms that are particularly suited to DSP implementation
2. Implement DSP algorithms on TI DSP processors
3. Implement FIR, IIR digital filtering and FFT methods
4. Implement modulators and demodulators for AM, DSBSC-AM, SSB and FM
5. Design digital communication methods leading to the implementation of a line communication system.

Question paper pattern:

The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.

- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

Text Book:

‘Communication System Design using DSP Algorithms with Laboratory Experiments for the TMS320C6713 DSK’, Steven A Tretter, Springer, 2008.

Reference Books:

1. 'Modern Digital Signal Processing', Roberto Cristi, Cengage Publishers, India, 2003.
2. 'Digital Signal Processing: A Computer Based Approach', S. K. Mitra, TMH, India, 3rd edition, 2007.
3. 'Digital Signal Processing: A Practitioner's approach', E.C. Ifeachor, and B. W. Jarvis, Pearson Education, India, Second Edition, 2002,
4. 'Digital Signal Processing', Proakis and Manolakis, Prentice Hall, 3rd edition, 1996.

Project Work Phase – 1

CourseCode	20EIE34	CIEMarks	100
Number ofcontactHours/Week	02	SEE Marks	-
		Exam Hours	-
Credits - 02			

Course objectives:

- Support independent learning.
- Guide to select and utilize adequate information from varied resources maintaining ethics.
- Guide to organize the work in the appropriate manner and present information (acknowledging the sources) clearly.
- Develop interactive, communication, organisation, time management, and presentation skills.
- Impart flexibility and adaptability.
- Inspire independent and team working.
- Expand intellectual capacity, credibility, judgement, intuition.
- Adhere to punctuality, setting and meeting deadlines.
- Instil responsibilities to oneself and others.
- Train students to present the topic of project work in a seminar without any fear, face audience confidently, enhance communication skill, involve in group discussion to present and exchange ideas.

Project Phase-1 Students in consultation with the guide/s shall carry out literature survey/ visit industries to finalize the topic of the Project. Subsequently, the students shall collect the material required for the selected project, prepare synopsis and narrate the methodology to carry out the project work.

Seminar:Each student, under the guidance of a Faculty, is required to

- Present the seminar on the selected project orally and/or through power point slides.
- Answer the queries and involve in debate/discussion.
- Submit two copies of the typed report with a list of references.

The participants shall take part in discussion to foster friendly and stimulating environment in which the students are motivated to reach high standards and become self-confident.

Revised Bloom's Taxonomy Level	L ₃ – Applying, L ₄ – Analysing, L ₅ – Evaluating, L ₆ – Creating.
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Course outcomes:

At the end of the course the student will be able to:

1. Demonstrate a sound technical knowledge of their selected project topic.
2. Undertake problem identification, formulation and solution.
3. Design engineering solutions to complex problems utilising a systems approach.
4. Communicate with engineers and the community at large in written and oral forms.
5. Demonstrate the knowledge, skills and attitudes of a professional engineer.

Continuous Internal Evaluation

CIE marks for the project report (50 marks), seminar (25 marks) and question and answer (25 marks) shall be awarded (based on the quality of report and presentation skill, participation in the question and answer session by the student) by the committee constituted for the purpose by the Head of the Department. The committee shall consist of three faculty from the department with the senior most acting as the Chairperson.

MINI PROJECT

CourseCode	20EIE35	CIEMarks	100
Number of contact Hours/Week	02	SEE Marks	-
		Exam Hours/ Batch	03
Credits - 02			

Course objectives:

- To support independent learning and innovative attitude.
- To guide to select and utilize adequate information from varied resources upholding ethics.
- To guide to organize the work in the appropriate manner and present information (acknowledging the sources) clearly.
- To develop interactive, communication, organisation, time management, and presentation skills.
- To impart flexibility and adaptability.
- To inspire independent and team working.
- To expand intellectual capacity, credibility, judgement, intuition.
- To adhere to punctuality, setting and meeting deadlines.
- To instil responsibilities to oneself and others.
- To train students to present the topic of project work in a seminar without any fear, face audience confidently, enhance communication skill, involve in group discussion to present and exchange ideas.

Mini-Project: Each student of the project batch shall involve in carrying out the project work jointly in constant consultation with internal guide, co-guide, and external guide and prepare the project report as per the norms avoiding plagiarism.

Course outcomes:

At the end of the course the student will be able to:

1. Present the mini-project and be able to defend it.
2. Make links across different areas of knowledge and to generate, develop and evaluate ideas and information so as to apply these skills to the project task.
3. Habituated to critical thinking and use problem solving skills.
4. Communicate effectively and to present ideas clearly and coherently in both the written and oral forms.
5. Work in a team to achieve common goal.
6. Learn on their own, reflect on their learning and take appropriate actions to improve it.

CIE procedure for Mini - Project:

The CIE marks awarded for Mini - Project, shall be based on the evaluation of Mini - Project Report, Project Presentation skill and Question and Answer session in the ratio 50:25:25. The marks awarded for Mini - Project report shall be the same for all the batch mates.

Internship / Professional Practice

CourseCode	20EIEI36	CIEMarks	40
Number of contact Hours/Week	02	SEE Marks	60
		Exam Hours	03
Credits - 06			

Course objectives:

Internship/Professional practice provide students the opportunity of hands-on experience that include personal training, time and stress management, interactive skills, presentations, budgeting, marketing, liability and risk management, paperwork, equipment ordering, maintenance, responding to emergencies etc. The objectives are further,

- To put theory into practice.
- To expand thinking and broaden the knowledge and skills acquired through course work in the field.
- To relate to, interact with, and learn from current professionals in the field.
- To gain a greater understanding of the duties and responsibilities of a professional.
- To understand and adhere to professional standards in the field.
- To gain insight to professional communication including meetings, memos, reading, writing, public speaking, research, client interaction, input of ideas, and confidentiality.
- To identify personal strengths and weaknesses.
- To develop the initiative and motivation to be a self-starter and work independently

Internship/Professional practice: Students under the guidance of internal guide/s and external guide shall take part in all the activities regularly to acquire as much knowledge as possible without causing any inconvenience at the place of internship.

Seminar: Each student, is required to

- Present the seminar on the internship orally and/or through power point slides.
- Answer the queries and involve in debate/discussion.
- Submit the report duly certified by the external guide.

The participants shall take part in discussion to foster friendly and stimulating environment in which the students are motivated to reach high standards and become self-confident.

Course outcomes:

At the end of the course the student will be able to:

- Gain practical experience within industry in which the internship is done.
- Acquire knowledge of the industry in which the internship is done.
- Apply knowledge and skills learned to classroom work.
- Develop a greater understanding about career options while more clearly defining personal career goals.
- Experience the activities and functions of professionals.
- Develop and refine oral and written communication skills.
- Identify areas for future knowledge and skill development.
- Expand intellectual capacity, credibility, judgment, intuition.
- Acquire the knowledge of administration, marketing, finance and economics.

Continuous Internal Evaluation

CIE marks for the Internship/Professional practice report (20 marks), seminar (10 marks) and question and answer session (10 marks) shall be awarded (based on the quality of report and presentation skill, participation in the question and answer session by the student) by the committee constituted for the purpose by the Head of the Department. The committee shall consist of three faculty from the department with the senior most acting as the Chairperson.

Semester End Examination

SEE marks for the Internship Report (30 Marks), Seminar (15 Marks) and Question and Answer Session (15 marks) shall be awarded (based on the quality of report and presentation skill, participation in the question and answer session) by the examiners appointed by the University.

M.TECH IN Industrial Electronics (EIE)

Choice Based Credit System (CBCS) and Outcome Based Education(OBE)
(Effective from the academic year 2020-21)

SEMESTER -IV

PROJECT WORK PHASE -2

CourseCode	20EIE41	CIEMarks	40
Number of contact Hours/Week	04	SEE Marks	60
		Exam Hours	03
Credits - 20			

Course objectives:

- To support independent learning.
- To guide to select and utilize adequate information from varied resources maintaining ethics.
- To guide to organize the work in the appropriate manner and present information (acknowledging the sources) clearly.
- To develop interactive, communication, organisation, time management, and presentation skills.
- To impart flexibility and adaptability.
- To inspire independent and team working.
- To expand intellectual capacity, credibility, judgement, intuition.
- To adhere to punctuality, setting and meeting deadlines.
- To instil responsibilities to oneself and others.
- To train students to present the topic of project work in a seminar without any fear, face audience confidently, enhance communication skill, involve in group discussion to present and exchange ideas.

Project Work Phase - II: Each student of the project batch shall involve in carrying out the project work jointly in constant consultation with internal guide, co-guide, and external guide and prepare the project report as per the norms avoiding plagiarism.

Course outcomes:

At the end of the course the student will be able to:

- Present the project and be able to defend it.

- Make links across different areas of knowledge and to generate, develop and evaluate ideas and information so as to apply these skills to the project task.
- Habituated to critical thinking and use problem solving skills
- Communicate effectively and to present ideas clearly and coherently in both the written and oral forms.
- Work in a team to achieve common goal.
- Learn on their own, reflect on their learning and take appropriate actions to improve it.

Continuous Internal Evaluation:

Project Report: 20 marks. The basis for awarding the marks shall be the involvement of the student in the project and in the preparation of project report. To be awarded by the internal guide in consultation with external guide if any.

Project Presentation: 10 marks.

The Project Presentation marks of the Project Work Phase -II shall be awarded by the committee constituted for the purpose by the Head of the Department. The committee shall consist of three faculty from the department with the senior most acting as the Chairperson.

Question and Answer: 10 marks.

The student shall be evaluated based on the ability in the Question and Answer session for 10 marks.

Semester End Examination

SEE marks for the project report (30 marks), seminar (15 marks) and question and answer session (15 marks) shall be awarded (based on the quality of report and presentation skill, participation in the question and answer session) by the examiners appointed by the University.