VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI.

Scheme of Teaching and Examinations and Syllabus

M.Tech. in Digital Electronics LDE

(Effective from the Academic year 2022-23)

M.TECH IN DIGITAL ELECTRONICS
(LDE)

Choice Based Credit System (CBCS) and Outcome Based Education (OBE)
(Effective from the academic year 2022-23)

SEMESTER -I

ADVANCED DIGITAL SIGNAL PROCESSING			
Course Code	**22LDE12**	CIE Marks	50
Teaching Hours/Week (L:P: SDA)	3:2:0	SEE Marks	50
Total Hours of Pedagogy	40 Hours Theory + 10-12 Lab slots	Total Marks	100
Credits	04	Exam Hours	03

Course Learning objectives: This course will enable students:

- To know the analysis of discrete time signals.
- To study the modern digital signal processing algorithms and applications.
- To Have an in-depth knowledge of use of digital systems in real time applications
- To Apply the algorithms for wide area of recent applications.

MODULE-1

Introduction to Digital Signal Processing: Review of Discrete time signals and systems and frequency analysis of discrete time linear time invariant systems, implementation of discrete time systems, correlation of discrete time systems Sampling, decimation by a factor 'D', Interpolation by a factor 'I', sampling rate conversion by a factor 'I/D', Implementation of sampling rate conversion, Multistage implementation of sampling rate conversion. **RBT Level: L1, L2, L3, L4**

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE-2

Multirate Digital Signal Processing: Multirate signal processing and its applications, Design of Digital filters, Design of FIR filters, Design of IIR filters, frequency transformations, Digital filter banks, two channel quadrature mirror filter banks, M-channel QMF bank. **RBT Level: L1, L2, L3, L4**

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE-3

Linear prediction and Optimum Linear Filters: Random signals, Correlation Functions and Power Spectra, Innovations Representation of a Stationary Random Process. Forward and Backward Linear Prediction. Solution of the Normal Equations. The Levinson-Durbin Algorithm. Properties of the Linear Prediction-Error Filters. **RBT Level: L1, L2, L3, L4**

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE 4

Adaptive filters:
Applications of Adaptive Filters-Adaptive Channel Equalization, Adaptive noise cancellation, Linear Predictive coding of Speech Signals, Adaptive direct form FIR filters-The LMS algorithm, Properties of LMS algorithm. Adaptive direct form filters- RLS algorithm. **RBT Level: L1, L2, L3, L4**

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE 5

Power Spectrum Estimation:

Non parametric Methods for Power Spectrum Estimation - Bartlett Method, Welch Method, Blackman &Tukey Methods.

Parametric Methods for Power Spectrum Estimation: Relationship between the auto correlation and the model parameters, Yule and Walker methods for the AR Model Parameters, Burg Method for the AR Model parameters, Unconstrained least-squares method for the AR Model parameters, Sequential estimation methods for the AR Model parameters, ARMA Model for Power Spectrum Estimation.

RBT Level: L1, L2

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

PRACTICAL COMPONENT OF IPCC:

Conduct the experiments using MATLAB/Scilab/TMS 320 C5X DSP Processors

Sl. No	Experiments
1	Generate various fundamental discrete time signals
2	Basic operations on signals (Multiplication, Folding, Scaling).
3	Find out the DFT & IDFT of a given sequence without using inbuilt instructions.
4	Interpolation & decimation of a given sequence.
5	Generation of DTMF (Dual Tone Multiple Frequency) signals
6	Estimate the PSD of a noisy signal using periodogram and modified periodogram
7	Estimation of PSD using different methods (Bartlett, Welch, Blackman-Tukey).
8	Design of Chebyshev Type I, II Filters.
9	Cascade Digital IIR Filter Realization.
10	Parallel Realization of IIR filter.
11	Estimation of power spectrum using parametric methods (YuleWalker &Burg).
12	Time-Frequency Analysis with the Continuous Wavelet Transform.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

CIE for the theory component of IPCC

1. Two Tests each of **20 Marks**
2. Two assignments each of **10 Marks/One Skill Development Activity of 20 marks**
3. Total Marks of two tests and two assignments/one Skill Development Activity added will be CIE for 60 marks, marks scored will be proportionally scaled down to **30 marks**.

CIE for the practical component of IPCC

1. On completion of every experiment/program in the laboratory, the students shall be evaluated and marks shall be awarded on the same day. The **15 marks** are for conducting the experiment and preparation of the laboratory record, the other **05 marks shall be for the test** conducted at the end of the semester.
2. The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to 15 marks.
3. The laboratory test at the end /after completion of all the experiments shall be conducted for 50 marks and scaled down to 05 marks**.**

Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **20 marks**.

SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (duration 03 Hours)

The question paper will be set for 100 marks and marks scored will be scaled down proportionately to 50 marks.

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper shall include questions from the practical component).

4. The minimum marks to be secured in CIE to appear for SEE shall be the 15 (50% of maximum marks-30) in the theory component and 10 (50% of maximum marks -20) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included**.** The maximum of 04/05 questions to be set from the practical component of IPCC, the total marks of all questions should not be more than the 20 marks.
5. SEE will be conducted for 100 marks and students shall secure 40% of the maximum marks to qualify in the SEE. Marks secured will be scaled down to 50. (Student has to secure an aggregate of 50% of maximum marks of the course(CIE+SEE)

Suggested Learning Resources:

Text Books

1. **Digital Signal Processing Principles, Algorithms, and Applications by John G. Proakis, Prentice-Hall International Inc., 4th Edition, 2012.**
2. **Theory and Application of Digital Signal Processing by Lawrence R. Rabiner and Bernard Gold.**

Reference Books

1. **Oppenheim, Alan V. Discrete-time signal processing. Pearson Education India, 1999.**
2. **Mitra, Sanjit Kumar, and Yonghong Kuo. Digital signal processing: a computer-based approach. Volume 2. New York: McGraw-Hill Higher Education, 2006.**

Web links and Video Lectures (e-Resources):

- **https://ekeeda.com/degree-courses/electrical-engineering/advanced-digital-signal-processing**
- **https://dss-kiel.de/index.php/teaching/lectures/lecture-advanced-digital-signal-processing**

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- **Mini Project in the area Advanced signal processing using modern tools like MATLAB, Python**

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Able to analyze and implement the frequency analysis & correlation of discrete-time linear time invariant systems.	Analyze
CO2	Able to implement sampling rate conversion by decimation & Interpolation process and design digital filter banks	Analyze
CO3	Able to analyze forward and backward linear prediction of a stationary random process using Levinson-Durbin Algorithm	Analyze
CO4	Able to understand and analyze adaptive filters and its application using LMS algorithm & RLS algorithm.	Analyze
CO5	Able to understand parametric & non-parametric methods for power spectrum estimation.	Understand

Program Outcome of this course

Sl. No.	Description	POs
1	An ability to independently carry out research /investigation and development work to solve practical problems	PO1
2	An ability to write and present a substantial technical report/document	PO2
3	Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program	PO3
4	An ability to create, select, apply appropriate techniques, resources and modern tools to solve complex engineering activities with an understanding of their limitations.	PO4
5	An ability to apply Professional ethics, responsibilities and norms of the engineering.	PO5
6	An ability to recognize the need to engage in independent and life-long learning in Digital Communication and Networking domain.	PO6

Mapping of COS and POs

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	**1**	**1**	**1**	**2**	**1**	**1**
CO2	**1**	**1**	**1**	**2**	**1**	**1**
CO3	**2**	**1**	**2**	**2**	**1**	**1**
CO4	**1**	**1**	**1**	**2**	**1**	**1**
CO5	**1**	**1**	**1**	**2**	**1**	**1**

ADVANCED COMMUNICATION SYSTEM 1			
Course Code	**22LDE13**	CIE Marks	50
Teaching Hours/Week (L:P: SDA)	3:0:2	SEE Marks	50
Total Hours of Pedagogy	40 Hours Theory + 10 Hours SDA	Total Marks	100
Credits	04	Exam Hours	03

Course Learning objectives: This course will enable students:

- To know modulation techniques.
- To study the demodulation techniques.
- To Have an in-depth knowledge of band limited channels and equalizers
- To understand spread spectrum.

MODULE-1

Signal Representation: Low pass representation of bandpass signals, Low pass representation of bandpass random process [Text 1, Chapter 2:2.1, and 2.9 only]. **Modulation**: Representation of digitally modulated Signals, Modulation Schemes without memory (Band Limited Schemes - PAM, BPSK, QPSK, MPSK, MQAM, Power Limited Schemes – FSK, MFSK, DPSK, DQPSK), modulation schemes with memory (Basics of CPFSK and CPM – Full Treatment of MSK), Transmit PSD for Modulation Schemes. **RBT Level: L1, L2**

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE-2

Demodulation: Vector Channel, Vector Channel +AWGN, Performance parameters, Optimum Coherent Detection for power limited and Bandlimited schemes, Optimal Coherent detection for schemes with memory, Optimal Non– Coherent detection for schemes without and with memory (FSK, DPSK, DQPSK), Comparison of detection schemes. **RBT Level: L1, L2**

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE-3

Bandlimited Channels: Bandlimited channel characterization, signaling through band limited linear filter channels, Sinc, RC, Duobinary and Modified Duobinary signaling schemes, Optimum receiver for channel with ISI and AWGN. **Linear Equalizers**: Zero forcing Equalizer, MSE and MMSE, Baseband and Passband Linear Equalizers. Performance of ZFE and MSE.

RBT Level: L1, L2, L3, L4

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE 4

Non-Linear Equalizers: Decision - feedback equalization, Predictive DFE, Performance of DFE [.

Adaptive equalization: Adaptive linear equalizer, adaptive decision feedback equalizer, Adaptive Fractionally spaced Equalizer (Tap Leakage Algorithm), Adaptive equalization of Trellis - coded signals

RBT Level: L3, L4

Teaching-Learning	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

Process	

MODULE 5

Spread spectrum signals for digital communication: Model of spread spectrum digital communication system, Direct sequence spread spectrum signals, some applications of DS spread spectrum signals, generation of PN sequences, Frequency hopped spread spectrum signals, Time hopping SS, Synchronization of SS systems.

RBT Level: L3,L4

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.

The students will have to answer five full questions, selecting one full question from each module.

Textbook:

'Digital Communications', John G. Proakis, Masoud Salehi, Pearson Education, ISBN:978-9332535893, 5th edition, 2014

Reference Books:

1. 'Digital Communications: Fundamentals and Applications: Fundamentals & Applications', Bernard Sklar, Pearson Education, ISBN:9788131720929, 2nd edition, 2009

2. 'Digital Communications Systems', Simon Haykin, Wiley, ISBN:9788126542314, 1st edition, 2014

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Ability to explain the concept of low pass and Bandpass signals representations at the Transmitter, the process of Detection and Estimation at the receiver in the presence of AWGN only.	Explain
CO2	Able to Evaluate Receiver performance for various types of single carrier symbol modulations through ideal and AWGN Non-bandlimited and bandlimited channels.	Understand
CO3	Analyze and demonstrate the model of discrete time channel with ISI & the model of discrete time channel by equalizer.	Analyze
CO4	Design single carrier equalizers for various symbol modulation schemes and detection methods for defined channel models, and compute parameters to meet desired rate and performance requirements.	Analyze
CO5	Design and Evaluate Non band limited and Non power limited spread spectrum systems for communications in a Jamming environment, multiuser situation and low power intercept environment.	Design and analyze

Program Outcome of this course

Sl. No.	Description	POs
1	An ability to independently carry out research /investigation and development work to solve practical problems	PO1
2	An ability to write and present a substantial technical report/document	PO2
3	Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program	PO3
4	An ability to create, select, apply appropriate techniques, resources and modern tools to solve complex engineering activities with an understanding of their limitations.	PO4
5	An ability to apply Professional ethics, responsibilities and norms of the engineering.	PO5
6	An ability to recognize the need to engage in independent and life-long learning in Digital Communication domain.	PO6

Mapping of COS and POs

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	**1**	**1**	**1**	**2**	**1**	**1**
CO2	**1**	**1**	**1**	**2**	**1**	**1**
CO3	**2**	**1**	**2**	**2**	**1**	**1**
CO4	**1**	**1**	**1**	**2**	**1**	**1**
CO5	**1**	**1**	**1**	**2**	**1**	**1**

DIGITAL CIRCUITS AND LOGIC DESIGN

Course Code	**22LDE 14**	CIE Marks	50
Teaching Hours/Week (L:P: SDA)	2:0:2	SEE Marks	50
Total Hours of Pedagogy	30 Hours Theory + 10 Hours SDA	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives: This course will enable students:

1. Understand the concepts of sequential machines.
2. Design Sequential Machines/Circuits.
3. Analyze the faults in the design of circuits.
4. Apply fault detection experiments to sequential circuits.
5. Comprehend the structure of sequential machines.

MODULE-1

Threshold Logic: Introductory Concepts, Synthesis of Threshold Networks, Capabilities, Minimization, and Transformation of Sequential Machines: The Finite- State Model, Further Definitions, And Capabilities.

RBT Level: L1, L2

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE-2

Fault Detection by Path Sensitizing, Detection of Multiple Faults, Failure-Tolerant Design, Quadded Logic, Reliable Design and Fault Diagnosis Hazards: Fault Detection in Combinational Circuits.

RBT Level: L1, L2

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE-3

Fault-Location Experiments, Boolean Differences, Limitations of Finite – State Machines, State Equivalence and Machine Minimization, Simplification of Incompletely Specified Machines.

RBT Level: L1, L2

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE 4

Structure of Sequential Machines: Introductory Example, State Assignments Using Partitions, The Lattice of closed Partitions, Reductions of the Output Dependency, Input Independence and Autonomous Clocks, Covers and Generation of closed Partitions by state splitting, Information Flow in Sequential Machines, decompositions, Synthesis of Multiple Machines.

RBT Level: L2, L3

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE 5

State Identifications and Fault-Detection Experiments:

Homing Experiments, Distinguishing Experiments, Machine Identification, Fault Detection Experiments, Design of Diagnosable Machines, Second Algorithm for the Design of Fault Detection Experiments, Fault-Detection.

RBT Level: L1,L2,L3

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

Assessment Details (both CIE and SEE)

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Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks.**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs.

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks.**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.

The students will have to answer five full questions, selecting one full question from each module.

Textbook:

'Switching and Finite Automata Theory', Zvi Kohavi, TMH, ISBN: 978_0_07_099387_7, 2ndEdition, 2008.

Reference Books:

1. 'Digital Circuits and logic Design', Charles Roth Jr., Cengage Learning, 7thedition, 2014.
2. 'Fault Tolerant and Fault Testable Hardware Design', Parag K Lala, Prentice Hall Inc. 1985.
3. 'Introductory Theory of Computer', E. V. Krishnamurthy, Macmillan Press Ltd, 1983
4. 'Theory of computer science – Automata, Languages and Computation', Mishra & Chandrasekaran, 2nd Edition, PHI, 2004.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Understand the concepts of sequential machines	Understand
CO2	Design Sequential Machines/Circuits.	Design
CO3	Analyze the faults in the design of circuits.	Analyze
CO4	Apply fault detection experiments to sequential circuits.	Apply
CO5	Comprehend the structure of sequential machines.	Understand

Program Outcome of this course

Sl. No.	Description	POs
1	An ability to independently carry out research /investigation and development work to solve practical problems	PO1
2	An ability to write and present a substantial technical report/document	PO2
3	Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program	PO3
4	An ability to create, select, apply appropriate techniques, resources and modern tools to solve complex engineering activities with an understanding of their limitations.	PO4
5	An ability to apply Professional ethics, responsibilities and norms of the engineering.	PO5
6	An ability to recognize the need to engage in independent and life-long learning in Digital Communication domain.	PO6

Mapping of COS and POs

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	**1**	**1**	**1**	**1**	**2**	**1**
CO2	**1**	**1**	**1**	**2**	**1**	**1**
CO3	**2**	**1**	**2**	**1**	**1**	**1**
CO4	**1**	**1**	**1**	**2**	**1**	**1**
CO5	**1**	**1**	**2**	**1**	**1**	**1**

DIGITAL VLSI DESIGN			
Course Code	**22LDE15**	CIE Marks	50
Teaching Hours/Week (L:P: SDA)	2:0:2	SEE Marks	50
Total Hours of Pedagogy	30 Hours Theory + 10 Hours SDA	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives: This course will enable students:

1. 1. Analyse issues of On-chip interconnect Modelling and Interconnect delay calculation.
2. Analyse the Switching Characteristics in Digital Integrated Circuits.
3. Use the Dynamic Logic circuits in state-of-the-art VLSI chips.
4. Study critical issues such as ESD protection, Clock distribution, Clock buffering, and Latch phenomenon.
5. Use Bipolar and Bi-CMOS circuits in very high speed design.

MODULE-1

MOS Transistor: The Metal Oxide Semiconductor (MOS) Structure, The MOS System under External Bias, Structure and Operation of MOS Transistor, MOSFET Current-Voltage Characteristics, MOSFET Scaling and Small Geometry Effects. MOS Inverters-Static Characteristics: Introduction, Resistive-Load Inverter, Inverters with nType MOSFET Load.

RBT Level: L1, L2

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE-2

MOS Inverters-Static Characteristics: CMOS Inverter. MOS Inverters: Switching Characteristics and Interconnect Effects: Introduction, Delay-Time Definition, Calculation of Delay Times, Inverter Design with Delay Constraints, Estimation of Interconnect Parasitics, Calculation of Interconnect Delay, Switching Power Dissipation of CMOS Inverters.

RBT Level: L1, L2

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE-3

Semiconductor Memories: Introduction, Dynamic Random Access Memory (DRAM), Static Random Access Memory (SRAM), Nonvolatile Memory, Flash Memory, Ferroelectric Random Access Memory (FRAM).

RBT Level: L1, L2

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE 4

Dynamic Logic Circuits: Introduction, Basic Principles of Pass Transistor Circuits, Voltage Bootstrapping, Synchronous Dynamic Circuit Techniques, Dynamic CMOS Circuit Techniques, High Performance Dynamic CMOS circuits. BiCMOS Logic Circuits: Introduction, Bipolar Junction Transistor (BJT): Structure and Operation, Dynamic Behavior of BJTs, Basic BiCMOS Circuits: Static Behavior, Switching Delay in BiCMOS Logic Circuits, BiCMOS Applications

RBT Level: L2, L3

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE 5

Chip Input and Output (I/O) Circuits: Introduction, ESD Protection, Input Circuits, Output Circuits and L(di/dt) Noise, On-Chip Clock Generation and Distribution, Latch-Up and Its Prevention. 13 Design for Manufacturability: Introduction, Process Variations, Basic Concepts and Definitions, Design of Experiments and Performance Modeling.

RBT Level: L1,L2,L3

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks.**
2. Two assignments each of 20 **Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs.

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**
CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.

The students will have to answer five full questions, selecting one full question from each module

Text Book

'CMOS Digital Integrated Circuits: Analysis and Design', Sung Mo Kang & Yusuf Leblebici, Tata McGraw-Hill, Third Edition

Reference Books:

1. 'Principles of CMOS VLSI Design: A System Perspective', Neil Weste and K. Eshraghian, Pearson Education (Asia) Pvt. Ltd., Second Edition, 2000
2. 'Modern VLSI Design: System on Silicon', Wayne, Wolf, Prentice Hall PTR/ Pearson Education, Second Edition, 1998
3. 'Basic VLSI Design', Douglas A Pucknell & Kamran Eshraghian, PHI, 3rd Edition (original Edition 1994

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Analyse issues of On-chip interconnect Modelling and Interconnect delay calculation	Analyze
CO2	Analyse the Switching Characteristics in Digital Integrated Circuits.	Analyze
CO3	Use the Dynamic Logic circuits in state-of-the-art VLSI chips.	Analyze
CO4	Study critical issues such as ESD protection, Clock distribution, Clock buffering, and Latch phenomenon	Understand
CO5	Use Bipolar and Bi-CMOS circuits in very high speed design.	Understand

Program Outcome of this course

Sl. No.	Description	POs
1	An ability to independently carry out research /investigation and development work to solve practical problems	PO1
2	An ability to write and present a substantial technical report/document	PO2
3	Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program	PO3
4	An ability to create, select, apply appropriate techniques, resources and modern tools to solve complex engineering activities with an understanding of their limitations.	PO4
5	An ability to apply Professional ethics, responsibilities and norms of the engineering.	PO5
6	An ability to recognize the need to engage in independent and life-long learning in Digital Communication domain.	PO6

Mapping of COS and POs

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	**1**	**1**	**1**	**1**	**2**	**1**
CO2	**1**	**2**	**1**	**2**	**1**	**1**
CO3	**1**	**1**	**2**	**1**	**1**	**1**
CO4	**1**	**1**	**1**	**2**	**1**	**1**
CO5	**1**	**1**	**2**	**1**	**1**	**1**

EMBEDDED SYSTEMS LABORATORY			
Course Code	**22LDEL17**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	1:2:0	SEE Marks	50
Credits	2	Exam Hours	100

Course objectives: This course will enable students:

- To understand the computer aided design tools for the electronic circuit designs.
- To analyze, design and verify analog circuits such as ADC, DAC, Controllers, etc. And digital systems using simulation tools or any EDA tool.
- To understand Architecture of ARM-32 bit Microcontroller and to analyze Instruction sets by Assembly basics, Instruction list and description.
- To learn Cortex-M3 programming using C language.

Part A: EDA Using Cadence OrCAD or OrCAD Lite or any EDA Tool, design and verify the following:

Sl. No	Experiments
1	3½ Digit Digital Voltmeter
2	Monolithic function Generator
3	Regulated Power supplies
4	Batch counter using TTL ICs
5	DAC and ADC
6	P, PI, PID and ON/OFF Controllers
7	programmable Timers
8	Filters and Resonance Circuits

PART-B: ARM-CORTEX M3 [Programming to be done using Keil uVision 4 and download the program on to a M3 evaluation board such as NXP LPC1768 or ATMEL ATSAM3U]

Sl. No	Experiments
1	Write an Assembly language program to calculate 10+9+8+...+1
2	Write an Assembly language program to link Multiple object files and link them together.
3	Write an Assembly language program to store data in RAM.
4	Write a C program to Output the "Hello World" message using UART.
5	Write a C program to Design a Stopwatch using interrupts.
6	Write an Exception vector table in C.

7	Write an Assembly Language Program for locking a Mutex.
8	Write a SVC handler in C. Use the wrapper code to extract the correct stack frame starting location. The C handler can then use this to extract the stacked PC location and the stacked register values.

Note: Conduct the experiments using C/NS2/Qualnet/OPNET/OMNET simulation tools

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

1. Understand the computer aided design tools for the electronic circuit designs.
2. Design and verify analog circuits such as ADC, DAC, Controllers, etc. using simulation tools
3. Create and verify digital systems using Cadence OrCAD, OrCAD Lite or any EDA tool.
4. Develop assembly programs for different applications using ARM Cortex M3 and Keil uVision-4 tool.
5. Develop C Programs for different applications using ARM-Cortex M3 and Keil u Vision - 4 tool.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 40%of maximum marks in the semester-end examination (SEE). In total of CIE and SEE student has to secure 50% maximum marks of the course.

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.
The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8^{th} week of the semester and the second test shall be conducted after the 14^{th} week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of **scaled-down** marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.
SEE shall be conducted jointly by the two examiners of the same institute; examiners are appointed by the University.

- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.
- Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.
- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.
- General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)
- Change of experiment is allowed only once and 10% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 Hours.

SEMESTER -II

ADVANCED COMPUTER ARCHITECTURE			
Course Code	**22LDE21**	CIE Marks	50
Teaching Hours/Week (L:P: SDA)	2:0:2	SEE Marks	50
Total Hours of Pedagogy	30 Hours Theory + 10 Hours SDA	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives: This course will enable students:

1. Understand the basic concepts for parallel processing
2. Analyze program partitioning and flow mechanisms
3. Apply pipelining concept for the performance evaluation
4. Learn the advanced processor architectures for suitable applications
5. Understand parallel Programming

MODULE-1

Parallel Computer Models: The State of Computing, Multiprocessors and multicomputers, Multivector and SIMD computers.

Program and Network Properties: Conditions of parallelism, Program Partitioning & Scheduling, Program Flow Mechanisms. **RBT Level: L1, L2**

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE-2

Principles of Scalable Performance: Performance Metrics and Measures, Parallel Processing Applications, Speedup Performance Laws, Scalability Analysis and Approaches.

Processors & Memory Hierarchy: Advanced processor technology, Super Scalars & Vector Processors, Memory Hierarchy Technology, Virtual Memory Technology.

RBT Level: L1, L2

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE-3

Bus, Cache and Shared Memory: Bus Systems, Cache Memory Organizations, Shared Memory Organizations, Sequential & Weak Consistency Model.

Pipelining & Superscalar Technologies: Linear Pipeline Processors, Nonlinear Pipeline Processors, Instruction Pipeline Design, Arithmetic Pipeline Design, Superscalar Pipeline Design.

RBT Level: L1, L2

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE 4

Multivector & SIMD Computers: Vector Processing principles, Multivector Multiprocessors, Compound Vector Processing, SIMD Computer Organization.

Scalable, Multithreaded and Data Flow Computers: Latency Hiding Techniques, Principles of Multithreading, Fine Grain Multi Computers, Scalable and Multithreaded Architectures, Data Flow and Hybrid Architectures. **RBT Level: L2, L3**

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE 5

Parallel Models, Languages and Compilers: Parallel Programming Models, Parallel Languages & Compilers, Dependence Analysis and Data Arrays, Code Optimization and Scheduling, Loop Parallelization and Pipelining.

Parallel Program Development and Environments: Parallel Programming Environments, Synchronization and Multi-Processor Modes, Shared Variable Program Structures.

RBT Level: L1,L2,L3

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks.**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs.

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks.**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.

The students will have to answer five full questions, selecting one full question from each module

Textbook:

'Advanced Computer Architecture: Parallelism, Scalability, Programmability', Kai Hwang & Narendra Jotwani, McGraw Hill Education, ISBN: 978-93-392-2092-1, 3rdEdition,2016.

Reference Books:

1. 'Computer Architecture, Pipelined and Parallel Processor Design', M.J. Flynn, Narosa Publishing, 2002.

2. 'Parallel programming in C with MPI and OpenMP', Michael J Quinn, Tata McGraw Hill, 2013.

3. 'An Introduction to Parallel Computing: Design and Analysis of Algorithms', Ananth Grama, Pearson, 2ndEdition, 2004.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	1. Understand the basic concepts for parallel processing	Understand
CO2	2. Analyze program partitioning and flow mechanisms	Analyze
CO3	3. Apply pipelining concept for the performance evaluation	Analyze
CO4	Learn the advanced processor architectures for suitable applications	Apply
CO5	Understand parallel Programming	Understand

Program Outcome of this course

Sl. No.	Description	POs
1	An ability to independently carry out research /investigation and development work to solve practical problems	PO1
2	An ability to write and present a substantial technical report/document	PO2
3	Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program	PO3
4	An ability to create, select, apply appropriate techniques, resources and modern tools to solve complex engineering activities with an understanding of their limitations.	PO4
5	An ability to apply Professional ethics, responsibilities and norms of the engineering.	PO5
6	An ability to recognize the need to engage in independent and life-long learning in Digital Communication domain.	PO6

Mapping of COS and POs

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	**1**	**1**	**1**	**1**	**2**	**1**
CO2	**1**	**1**	**1**	**2**	**1**	**1**
CO3	**2**	**1**	**2**	**1**	**1**	**1**
CO4	**1**	**1**	**1**	**2**	**1**	**1**
CO5	**1**	**1**	**2**	**1**	**1**	**1**

REAL TIME OPERATING SYSTEM			
Course Code	**22LDE22**	CIE Marks	50
Teaching Hours/Week (L:P: SDA)	3:0:2	SEE Marks	50
Total Hours of Pedagogy	40 Hours Theory + 10 Hours SDA	Total Marks	100
Credits	04	Exam Hours	03

Course Learning objectives: This course will enable students:

1. Analyse issues of On-chip interconnect Modelling and Interconnect delay calculation.
2. Analyse the Switching Characteristics in Digital Integrated Circuits.
3. Use the Dynamic Logic circuits in state-of-the-art VLSI chips.
4. Study critical issues such as ESD protection, Clock distribution, Clock buffering, and Latch phenomenon
5. Use Bipolar and Bi-CMOS circuits in very high speed design.

MODULE-1

Real-Time Systems and Resources: Brief history of Real Time Systems, A brief history of Embedded Systems. System Resources, Resource Analysis, Real-Time Service Utility, Scheduler concepts, Real-Time OS, State transition diagram and tables, Thread Safe Reentrant Functions.

RBT Level: L1, L2

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE-2

Processing with Real Time Scheduling: Scheduler Concepts, Pre-emptive Fixed Priority Scheduling Policies with timing diagrams and problems and issues, Feasibility, Rate Monotonic least upper bound, Necessary and Sufficient feasibility, Deadline –Monotonic Policy, Dynamic priority policies, Alternative to RM policy.

RBT Level: L1, L2

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE-3

Memory and I/O: Worst case execution time, Intermediate I/O, Shared Memory, ECC Memory, Flash file systems. Multi-resource Services, Blocking, Deadlock and live lock, Critical sections to protect shared resources, Missed deadline, QoS, Reliability and Availability, Similarities and differences, Reliable software, Available software

RBT Level: L1, L2

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE 4	
Firmware Components: The 3 firmware components, RTOS system software mechanisms, Software application components. Debugging Components, Exceptions, assert, Checking return codes, Single-step debugging, Test access ports, Trace Ports. **RBT Level: L2, L3**	
Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar
MODULE 5	
Process and Threads: Process and thread creations, Programs related to semaphores, message queue, shared buffer applications involving inter task/thread communication. **RBT Level: L1,L2,L3**	
Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.

The students will have to answer five full questions, selecting one full question from each module.

Textbooks:

1. 'Real-Time Embedded Systems and Components', Sam Siewert, Cengage Learning, India Edition, 2007.

2. 'Embedded/Real Time Systems, Concepts, Design and Programming, Black Book', Dr. K.V.K.K Prasad, Dream Tech Press, New edition, 2010.

Reference Books:

1. 'Real Time System', James W S Liu, Pearson Education, 2008.

2. 'Programming for Embedded Systems', Dream Tech Software Team, John Wiley, India Pvt. Ltd., 2008.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Analyse issues of On-chip interconnect Modelling and Interconnect delay calculation	Analyze
CO2	Analyse the Switching Characteristics in Digital Integrated Circuits.	Analyze
CO3	Use the Dynamic Logic circuits in state-of-the-art VLSI chips.	Analyze
CO4	Study critical issues such as ESD protection, Clock distribution, Clock buffering, and Latch phenomenon	Understand
CO5	Use Bipolar and Bi-CMOS circuits in very high speed design.	Understand

Program Outcome of this course

Sl. No.	Description	POs
1	An ability to independently carry out research /investigation and development work to solve practical problems	PO1
2	An ability to write and present a substantial technical report/document	PO2
3	Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program	PO3
4	An ability to create, select, apply appropriate techniques, resources and modern tools to solve complex engineering activities with an understanding of their limitations.	PO4
5	An ability to apply Professional ethics, responsibilities and norms of the engineering.	PO5
6	An ability to recognize the need to engage in independent and life-long learning in Digital Communication domain.	PO6

Mapping of COS and POs

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	**1**	**1**	**1**	**1**	**2**	**1**
CO2	**1**	**2**	**1**	**2**	**1**	**1**
CO3	**1**	**1**	**2**	**1**	**1**	**1**
CO4	**1**	**1**	**1**	**2**	**1**	**1**
CO5	**1**	**1**	**2**	**1**	**1**	**1**

Professional Elective 1

WIRELESS SENSOR NETWORKS			
Course Code	**22 LDE 231**	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	(2:0:2)	SEE Marks	50
Total Hours of Pedagogy	30 Hours Theory+10 Hours SDA	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives: This course will enable students to:

- Learn the basic concepts of Wireless sensor networks architecture and protocols.
- Understand the challenges in designing a Wireless sensor networks.
- Understand the function of Data link and Network layer Protocols.
- Understand the function of Transport layer Protocols.
- Analyze wireless sensor network system for different applications under consideration

Module-1

INTRODUCTION: Sensor Mote Platforms, WSN Architecture and Protocol Stack (Chap.1Text 1). WSN Applications: Military Applications, Environmental Applications, Health Applications, Home Applications, Industrial Applications. **RBT Level: L1, L2**

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

Module-2

FACTORS INFLUENCING WSN DESIGN: Hardware Constraints Fault Tolerance Scalability Production Costs WSN Topology, Transmission Media, Power Consumption (Chap. 3 Text 1). Physical Layer: Physical Layer Technologies, Overview of RF Wireless Communication, Channel Coding (Error Control Coding), Modulation, Wireless Channel Effects, PHY Layer Standards. **RBT Level: L1, L2, L3**

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

Module-3

MEDIUM ACCESS CONTROL: Challenges for MAC, CSMA Mechanism, Contention-Based Medium Access, Reservation-Based Medium Access, Hybrid Medium Access (Chap. 5 of Text 1). Network Layer: Challenges for Routing, Data-centric and Flat Architecture Protocols, Hierarchical Protocols, Geographical Routing Protocols. **RBT Level: L1, L2**

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

Module-4

Transport Layer: Challenges for Transport Layer, Reliable Multi Segment Transport (RMST) Protocol, Pump Slowly, Fetch Quickly (PSFQ) Protocol, Congestion Detection and Avoidance (CODA) Protocol, Event-to-Sink Reliable Transport (ESRT) Protocol, GARUDA

Application Layer: Source Coding (Data Compression), Query Processing, Network Management (Chap. 9 Text 1). **RBT Level: L1, L2, L3, L4**

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

Module-5

SPREAD SPECTRUM SIGNALS FOR DIGITAL COMMUNICATION: Model of spread spectrum digital communication system, Direct sequence spread spectrum signals, some applications of DS spread spectrum signals, generation of PN sequences, Frequency hopped spread spectrum signals, Time hopping SS,

Synchronization of SS systems. **RBT Level: L1, L2**	
Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Books:

1.Wireless Sensor Networks, Ian F. Akyildiz and Mehmet Can Vuran, John Wiley & Sons Ltd. ISBN 978-0-470-3601-3 (H/B),2010

2. Wireless Sensor Networks: Signal Processing and Communications Perspectives', Ananthram Swami, et.al, John Wiley & Sons Ltd., ISBN 978-0470-03557-3, 2007.

Web links and Video Lectures (e-Resources):

Massive Open Online Courses:

https://archive.nptel.ac.in/courses/106/105/106105160/#- **Wireless** Ad Hoc and **Sensor Networks** -BY Prof. SUDIP MISHRA,IITKGP

Skill Development Activities Suggested

- Mini projects carried out in groups based on latest trends in Industry and continue work to prepare a research Article.
- Implement Networking concepts using NS2/NS3/OMNET/OPNET/QUALNET software tool.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Acquire knowledge of characteristics of mobile/wireless communication channels	Understand
CO2	Apply statistical models of multipath fading	Apply
CO3	Understand the multiple radio access techniques, radio standards and communication protocols to be used for wireless sensor	Understand
CO4	Design wireless sensor network system for different applications under consideration.	Analyze
CO5	Understand the hardware details of different types of sensors and select right type of sensor for various applications.	Understand

Program Outcome of this course

Sl. No.	Description	POs
1	An ability to independently carry out research /investigation and development work to solve practical problems	PO1
2	An ability to write and present a substantial technical report/document	PO2
3	Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program	PO3
4	An ability to create, select, apply appropriate techniques, resources and modern tools to solve complex engineering activities with an understanding of their limitations.	PO4
5	An ability to apply Professional ethics, responsibilities and norms of the engineering.	PO5
6	An ability to recognize the need to engage in independent and life-long learning in Digital Communication and Networking domain.	PO6

Mapping of COS and POs

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	**1**	**-**	**1**	**3**	**-**	**2**
CO2	**1**	**-**	**1**	**3**	**-**	**2**
CO3	**1**	**-**	**1**	**3**	**-**	**2**
CO4	**1**	**1**	**1**	**3**	**-**	**2**
CO5	**1**	**1**	**1**	**3**	**-**	**2**

NANOELECTRONICS			
Course Code	**22 LDE 232**	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	(2:0:2)	SEE Marks	50
Total Hours of Pedagogy	30 Hours Theory+10 Hours SDA	Total Marks	100
Credits	03	Exam Hours	3

Course Learning objectives: This course will enable students to:

- Know the principles behind Nanoscience engineering and Nanoelectronics.
- Apply the knowledge to prepare and characterize nanomaterials.
- Know the effect of particles size on mechanical, thermal, optical and electrical properties of nanomaterials.
- Design the process flow required to fabricate state of the art transistor technology.
- Analyze the requirements for new materials and device structure in the future technologies.

Module-1

Introduction: Overview of nanoscience and engineering. Development milestones in microfabrication and electronic industry. Moores' law and continued miniaturization, Classification of Nanostructures, Electronic properties of atoms and solids: Isolated atom, Bonding between atoms, Giant molecular solids, Free electron models and energy bands, crystalline solids, Periodicity of crystal lattices, Electronic conduction, effects of nanometer length scale, Fabrication methods: Top down processes, Bottom up processes methods for templating the growth of nanomaterials, ordering of nano systems. **RBT Level: L1, L2**

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

Module-2

Characterization: Classification, Microscopic techniques, Field ion microscopy, scanning probe techniques, diffraction techniques: bulk and surface diffraction techniques, spectroscopy techniques: photon, radiofrequency, electron, surface analysis and dept profiling: electron, mass, Ion beam, Reflectometry, Techniques for property measurement: mechanical, electron, magnetic, thermal properties.

RBT Level: L1, L2, L3

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

Module-3

Inorganic semiconductor nanostructures: overview of semiconductor physics. Quantum confinement in semiconductor nanostructures: quantum wells, quantum wires, quantum dots, super-lattices, band offsets, electronic density of states.

Carbon Nanostructures: Carbon molecules, Carbon Clusters, Carbon Nanotubes, application of Carbon Nanotubes. **RBT Level: L1, L2**

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

Module-4

Fabrication techniques: requirements of ideal semiconductor, epitaxial growth of quantum wells, lithography and etching, cleaved-edge over growth, growth of vicinal substrates, strain induced dots and wires, electrostatically induced dots and wires, Quantum well width fluctuations, thermally annealed quantum wells, semiconductor nanocrystals, colloidal quantum dots, self-assembly techniques.

Physical processes: modulation doping, quantum hall effect, resonant tunneling, charging effects, ballistic carrier transport, Inter band absorption, intra band absorption, Light emission processes, phonon bottleneck, quantum confined stark effect, nonlinear effects, coherence and dephasing, characterization of semiconductor

nanostructures: optical electrical and structural (Text1). **RBT Level: L1, L2, L3**	
Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

Module-5

Methods of measuring properties: atomic, crystallography, microscopy, spectroscopy
Applications: Injection lasers, quantum cascade lasers, single-photon sources, biological tagging, optical memories, coulomb blockade devices, photonic structures, QWIPs, NEMS, MEMS. **RBT Level: L1, L2, L3**

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**
CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Textbooks:

1. 'Nanoscale Science and Technology', Ed Robert Kelsall, Ian Hamley, Mark Geoghegan, John Wiley, 2007
2. 'Introduction to Nanotechnology', Charles P Poole, Jr, Frank J Owens, John Wiley, Copyright 2006, Reprint 2011.

Reference Book:

1. 'Hand Book of Nanoscience Engineering and Technology', Ed William A Goddard III, Donald W Brenner, Sergey E. Lyshevski, Gerald J Iafrate, CRC press, 2003

Web links and Video Lectures (e-Resources):

- https://www.digimat.in/nptel/courses/video/117108047/L01.html
- https://archive.nptel.ac.in/courses/117/108/117108047/

Skill Development Activities Suggested

- Seminar on recent applications of Carbon nano tubes

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Know the principles behind Nanoscience engineering and Nanoelectronics.	Understand
CO2	Apply the knowledge to prepare and characterize nanomaterials.	Apply
CO3	Know the effect of particles size on mechanical, thermal, optical and electrical properties of nanomaterials	Understand
CO4	Design the process flow required to fabricate state of the art transistor technology	Apply
CO5	Analyze the requirements for new materials and device structure in the future technologies.	Apply

Program Outcome of this course

Sl. No.	Description	POs
1.	An ability to independently carry out research /investigation and development work to solve practical problems	PO1
2.	An ability to write and present a substantial technical report/document	PO2
3.	Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program	PO3
4.	An ability to create, select, apply appropriate techniques, resources and modern tools to solve complex engineering activities with an understanding of their limitations.	PO4
5.	An ability to apply Professional ethics, responsibilities and norms of the engineering	PO5
6.	An ability to recognize the need to engage in independent and life-long learning in Digital Communication and Networking domain	PO6

Mapping of COS and POs

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	**-**	**1**	**2**	**2**	**-**	**-**
CO2	**2**	**1**	**2**	**2**	**-**	**-**
CO3	**2**	**1**	**2**	**2**	**-**	**-**
CO4	**2**	**1**	**2**	**2**	**-**	**-**
CO5	**-**	**1**	**2**	**2**	**-**	**-**

CRYPTOGRAPHY AND NETWORK SECURITY			
Course Code	**22 LDE 233**	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	(2:0:2)	SEE Marks	50
Total Hours of Pedagogy	30 Hours Theory+10 Hours SDA	Total Marks	100
Credits	03	Exam Hours	3

Course outcomes: This course will enable students to:

- Understand the basics of symmetric key.
- Use basic cryptographic algorithms to encrypt the data.
- Generate some pseudorandom numbers required for cryptographic applications.
- Provide authentication and protection for encrypted data.
- Understand the techniques and features of Email, IP and Web security.

Module-1

Foundations: Terminology, Steganography, substitution ciphers and transpositions ciphers, Simple XOR, One-Time Pads, Computer Algorithms

SYMMETRIC CIPHERS: Traditional Block Cipher structure, Data Encryption Standard (DES), The AES Structure, AES Key Expansion. **RBT Level: L1, L2**

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

Module-2

More Number Theory: Prime Numbers, Fermat's and Euler's theorem, Testing for Primality, The Chinese Remainder theorem, Discrete Logarithms.

Principles of Public-Key Cryptosystems, The RSA algorithm, Diffie - Hellman Key Exchange, Elliptic Curve Arithmetic, Elliptic Curve Cryptography.

RBT Level: L1, L2, L3

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

Module-3

Pseudo-Random-Sequence Generators and Stream Ciphers: Linear Congruential Generators, Linear Feedback Shift Registers, Design and analysis of stream ciphers, Stream ciphers using LFSRs, A5, Hughes XPD/KPD, Nanoteq, Rambutan, Additive generators, Gifford, Algorithm M, PKZIP

RBT Level: L1, L2, L3

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

Module-4

One-Way Hash Functions: Background, Snefru, N-Hash, MD4, MD5, Secure Hash Algorithm [SHA], One way hash functions using symmetric block algorithms, Using public key algorithms, Choosing a one-way hash functions, Message Authentication Codes.

Digital Signature Algorithm, Discrete Logarithm Signature Scheme

RBT Level: L1, L2, L3

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

Module-5

E-mail Security: Pretty Good Privacy-S/MIME.

IP Security: IP Security Overview, IP Security Policy, Encapsulation Security Payload (ESP)

.

Web Security: Web Security Considerations, SSL.

RBT Level: L1, L2

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

Assessment Details (both CIE and SEE)

The weight age of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks**
   to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Textbooks:

1. "Cryptography and Network Security Principles and Practice", William Stallings, Pearson Education Inc., ISBN: 978-93325-1877-3, 6th Edition, 2015

2. "Applied Cryptography Protocols, Algorithms, and Source code in C", Bruce Schneier, Wiley Publications ISBN: 9971-51348-X, 2nd Edition

Reference Books:

1. "Cryptography and Network Security", Behrouz A. Forouzan, TMH, 2007

2. "Cryptography and Network Security", Atul Kahate, TMH, 200

Web links and Video Lectures (e-Resources):

- https://nptel.ac.in/courses/106105162
- Cryptography & Network Security, IIT Kharagpur, Prof. Sourav Mukophadhyay

Skill Development Activities Suggested

- Online certification course on probability and random process.
- Miniprojects can be suggested on the related area.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Understand the basics of symmetric key.	Understand
CO2	Use basic cryptographic algorithms to encrypt the data.	Apply
CO3	Generate some pseudorandom numbers required for cryptographic applications.	Apply
CO4	Provide authentication and protection for encrypted data.	Apply
CO5	Understand the techniques and features of Email, IP and Web security.	Understand

Program Outcome of this course

Sl. No.	Description	POs
1	An ability to independently carry out research /investigation and development work to solve practical problems	PO1
2	An ability to write and present a substantial technical report/document	PO2
3	Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program	PO3
4	An ability to create, select, apply appropriate techniques, resources and modern tools to solve complex engineering activities with an understanding of their limitations.	PO4
5	An ability to apply Professional ethics, responsibilities and norms of the engineering.	PO5
6	An ability to recognize the need to engage in independent and life-long learning in Digital Communication and Networking domain.	PO6

Mapping of COS and POs

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	**1**	**1**	**2**	**1**	**1**	**1**
CO2	**1**	**1**	**2**	**1**	**1**	**1**
CO3	**1**	**1**	**2**	**1**	**1**	**1**
CO4	**1**	**1**	**2**	**1**	**1**	**1**
CO5	**1**	**1**	**2**	**1**	**1**	**1**

OPTICAL COMMUNICATION AND NETWORKING			
Course Code	**22 LDE 234**	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	(2:0:2)	SEE Marks	50
Total Hours of Pedagogy	30 Hours Theory+10 Hours SDA	Total Marks	100
Credits	03	Exam Hours	3

Course Learning objectives: This course will enable students to:

- Understand the various optical devices and how they operate.
- Recognize and choose various components for optical networking in accordance with the established design requirements
- Acquire knowledge of the elements of data transmission, loss obstacles, and other network operating artifacts.
- Acquire knowledge of the problems associated with setting up and maintaining the optical network's access component while keeping up with current data transmission trends.
- Build a WDM network and explore the management of components and networks.

Module-1	
Introduction to optical networks: Optical Networks, optical packet switching, Propagation of signals in optical fiber: Different losses, Nonlinear effects, Solitons. Optical Components (Part-1): Couplers, Isolators, and Circulators. **RBT Level: L1, L2**	
Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar
Module-2	
Optical Components (Part-2): Multiplexers and Filters, Optical Amplifiers, detectors. Modulation - Demodulation: Formats, Ideal receivers, Practical direct detection receivers, Optical preamplifiers, Bit error rates, Coherent detection. **RBT Level: L1, L2**	
Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar
Module-3	
Transmission System Engineering: System model, Power penalty, Transmitter, Receiver, Crosstalk. Client Layers of optical layer: SONET/SDH: Multiplexing, layers, Frame structure. Asynchronous Transfer Mode: ATM functions, Adaptation layers, Quality of Service (QoS) and flow control, Signaling and Routing. **RBT Level: L1, L2**	
Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar
Module-4	
WDM network elements: Optical line terminals, Optical line amplifiers, Optical Add/ Drop Multiplexers, Optical cross-connects. WDM Network Design: Cost trade-offs, LTD and RWA problems, Routing and wavelength assignment, Wavelength conversion. **RBT Level: L1, L2**	
Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar
Module-5	

Control and Management (Part-1): Network management functions, management framework, Information model, management protocols, Layers within the optical layer. 37 Control and Management (Part-2): Performance and fault management, Impact of transparency, BER measurement, Optical trace, Alarm management, Configuration management, Optical Safety. **RBT Level: L1, L2, L3, L4**

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Textbooks:

1. ''Optical Networks', Rajiv Ramaswami, Kumar N. Sivarajan and Galan H Sasaki, Morgan Kaufman Publishers, 3rd edition, 2010.

Reference Books:

1. 'Optical fiber communication', John M. Senior, Pearson edition, 2000.
2. 'Optical fiber Communication', Gerd Keiser, John Wiley, New York, 5th Edition, 2017.
3. 'Fiber Optic Networks', P. E. Green, Prentice Hall, 1994.

Web links and Video Lectures (e-Resources):

https://onlinecourses.nptel.ac.in/noc20_ph07/preview
https://www.classcentral.com/course/swayam-optical-communications-6699

Skill Development Activities Suggested

- Mini Projects can be suggested to improve the programming skills.
- Online certification courses can be suggested in the related area.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Comprehend the various optical devices and their working strategies	Understand
CO2	Recognize and select various optical networking components according to the prescribed design specifications	Understand
CO3	Learn the aspects of data transmission, loss hindrances, and other artifacts affecting the network operation	Understand
CO4	Learn the issues involved in setting up and maintaining access part of the optical network with the latest trends in the data communication	Understand
CO5	Design a WDM network and study the component and network management aspects	Analyze

Program Outcome of this course

Sl. No.	Description	POs
1	An ability to independently carry out research /investigation and development work to solve practical problems	PO1
2	An ability to write and present a substantial technical report/document	PO2
3	To demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor's program	PO3
4	An ability to create, select, and apply appropriate techniques, resources, and modern tools to solve complex engineering activities with an understanding of their limitations.	PO4
5	An ability to apply Professional ethics, responsibilities, and norms of engineering.	PO5
6	An ability to recognize the need to engage in independent and lifelong learning in Digital Communication and Networking domain.	PO6

Mapping of COS and POs

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	**1**	**1**	**-**	**1**	**-**	**2**
CO2	**1**	**1**	**-**	**1**	**-**	**2**
CO3	**2**	**1**	**1**	**1**	**-**	**2**
CO4	**2**	**1**	**1**	**1**	**-**	**2**
CO5	**2**	**1**	**2**	**1**	**-**	**2**

DIGITAL COMPRESSION

Course Code	**22LDE235**	CIE Marks	50
Teaching Hours/Week (L:P: SDA)	2:0:2	SEE Marks	50
Total Hours of Pedagogy	30 Hours Theory + 10 Hours SDA	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives: This course will enable students:

1 Explain the evolution and fundamental concepts of Data Compression and Coding techniques.

2. Acquire contemporary knowledge in Data Compression and Coding.

3. Analyze the operation of a range of commonly used Coding and Compression techniques

4. Identify the basic software and hardware tools used for data compression.

5. Analyze and evaluate the performance of different Data Compression and Coding methods.

MODULE-1

Introduction: Compression techniques, Modelling & coding, Distortion criteria, Differential Entropy, Rate Distortion Theory, Vector Spaces, Information theory, Models for sources, Coding uniquely decodable codes, Prefix codes, Kraft McMillan Inequality.

Quantization: Quantization problem, Uniform Quantizer, Adaptive Quantization, Non-uniform Quantization; Entropy coded Quantization, Vector Quantization, LBG algorithm; Tree structured VQ, Structured VQ.

RBT Level: L1, L2

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE-2

Differential Encoding: Basic algorithm, Prediction in DPCM, Adaptive DPCM, Delta Modulation, Speech coding–G.726, Image coding.

Transform Coding: Transforms – KLT, DCT, DST, DWHT; Quantization and coding of transform coefficients, Application to Image compression – JPEG, Application to audio compression.

RBT Level: L1, L2

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE-3

Sub-band Coding: Filters, Sub-band coding algorithm, Design of filter banks, Perfect reconstruction using two channel filter banks, M-band QMF filter banks, Poly-phase decomposition, Bit allocation, Speech coding–G.722, Audio coding–MPEG audio, Image compression.

RBT Level: L1, L2

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE 4

Wavelet Based Compression: Wavelets, Multi resolution analysis & scaling function, Implementation using filters, Image compression–EZW, SPIHT, JPEG 2000.

Analysis/Synthesis Schemes: Speech compression–LPC10, CELP, MELP. **Video Compression:** Motion compensation, Video signal representation, Algorithms for video conferencing & video phones–H.261, H.263, Asymmetric applications–MPEG 4, MPEG 7, Packet video.

RBT Level: L2, L3

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE 5

Loss less Coding: Huffman coding, Adaptive Huffman coding, Golomb codes, Rice codes, Tunstall codes, Applications of Huffman coding, Arithmetic coding, Algorithm implementation, Applications of Arithmetic coding, Dictionary techniques–LZ77, LZ78, Applications of LZ78– JBIG, JBIG2, Predictive coding–Prediction with partial match, Burrows Wheeler Transform, Applications– CALIC, JPEG-LS.

RBT Level: L1,L2,L3

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks.**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs.
3. The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5.

The students will have to answer five full questions, selecting one full question from each module.

Textbook:

'Introduction to Data Compression', K Sayood, Harcourt India Pvt. Ltd. & Morgan Kaufmann Publishers, 1996.

Reference Books:

1. 'Digital Coding of Waveforms: Principles and Applications to Speech and Video', N Jayant and P Noll, Prentice Hall, USA, 1984.

2. 'Data Compression: The Complete Reference', D Salomon, Springer, 2000.

3. 'Fundamentals of Multimedia', Z Li and M S Drew, Pearson Education (Asia) Pvt. Ltd., 2004

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Explain the evolution and fundamental concepts of Data Compression and Coding techniques.	Understand
CO2	Acquire contemporary knowledge in Data Compression and Coding.	Understand
CO3	Analyze the operation of a range of commonly used Coding and Compression techniques	Analyze
CO4	Identify the basic software and hardware tools used for data compression.	Apply
CO5	Analyze and evaluate the performance of different Data Compression and Coding methods	Analyze

Program Outcome of this course

Sl. No.	Description	POs
1	An ability to independently carry out research /investigation and development work to solve practical problems	PO1
2	An ability to write and present a substantial technical report/document	PO2
3	Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program	PO3
4	An ability to create, select, apply appropriate techniques, resources and modern tools to solve complex engineering activities with an understanding of their limitations.	PO4
5	An ability to apply Professional ethics, responsibilities and norms of the engineering.	PO5
6	An ability to recognize the need to engage in independent and life-long learning in Digital Communication domain.	PO6

Mapping of COS and POs

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	**1**	**1**	**1**	**1**	**2**	**1**
CO2	**1**	**1**	**1**	**2**	**1**	**1**
CO3	**2**	**1**	**2**	**1**	**1**	**1**
CO4	**1**	**1**	**1**	**2**	**1**	**1**
CO5	**1**	**1**	**2**	**1**	**1**	**1**

Professional Elective 2

AUTOMOTIVE ELECTRONICS			
Course Code	**22LDE241**	CIE Marks	50
Teaching Hours/Week (L:P: SDA)	2:0:2	SEE Marks	50
Total Hours of Pedagogy	30 Hours Theory + 10 Hours SDA	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives: This course will enable students:

1. Implement various control requirements in the automotive system.
2. Comprehend dashboard electronics and engine system electronics.
3. Identify various physical parameters that are to be sensed and monitored for maintaining the stability of the vehicle under dynamic conditions.
4. Understand and implement the controls and actuator system pertaining to the comfort and safety of commuters.
5. Design sensor network for mechanical fault diagnostics in an automotive vehicle.

MODULE-1

Automotive Fundamentals, the Systems Approach to Control and Instrumentation: Use of Electronics in the Automobile, Antilock Brake Systems (ABS), Electronic steering control, Power steering, Traction control, Electronically controlled suspension. .

RBT Level: L1, L2

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE-2

Automotive instrumentation Control: Operational amplifiers, Digital circuits, Logic circuits, Microcomputer fundamentals, Microcomputer operations, Microprocessor architecture, digital to analog converter, analog to digital converter, Microcomputer applications in automotive systems, Instrumentation applications of microcomputers, Microcomputer in control systems.

RBT Level: L1, L2

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE-3

The basics of Electronic Engine control: Integrated body: Climate controls, Motivation for Electronic Engine Control, Concept of An Electronic Engine Control System,Definition of General Terms, Definition of Engine Performance Terms, Electronic fuel control system, Engine control sequence, Electronic Ignition, Sensors and Actuators, Applications of sensors and actuators, air flow rate sensor,

Indirect measurement of mass air flow, Engine crankshaft angular position sensor, Automotive engine control actuators, Digital engine control, Engine speed sensor, Timing sensor for ignition and fuel delivery, Electronic ignition control systems, Safety systems, Interior safety, Lighting, Entertainment systems. **RBT Level: L1, L2**	
Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar
MODULE 4	
Vehicle Motion Control and Automotive diagnostics: Cruise control system, Digital cruise control, Timing light, Engine analyzer, On-board and off-board diagnostics, Expert systems. Stepper motor-based actuator, Cruise control electronics, Vacuum - antilock braking system, Electronic suspension system Electronic steering control, Computer-based instrumentation system, Sampling and Input\output signal conversion, Fuel quantity measurement, Coolant temperature measurement, Oil pressure measurement, Vehicle speed measurement, Display devices, Trip-Information-Computer, Occupant protection systems. **RBT Level: L2, L3**	
Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar
MODULE 5	
Future automotive electronic systems: Alternative Fuel Engines, Collision Wide Range Air/Fuel Sensor, Alternative Engine, Low Tire Pressure Warning System, Collision avoidance Radar Warning Systems, Low Tire Pressure Warning System, Radio Navigation, Advance Driver information System. Alternative-Fuel Engines, Transmission Control, Collision Avoidance Radar Warning System, Low Tire Pressure Warning System, Speech Synthesis Multiplexing in Automobiles, Control Signal Multiplexing, Navigation Sensors, Radio Navigation, Signpost Navigation, Dead Reckoning Navigation Future Technology, Voice Recognition Cell Phone Dialling Advanced Driver information System, Automatic Driving Control. . **RBT Level: L1,L2,L3**	
Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks.**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs.

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks.**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.

The students will have to answer five full questions, selecting one full question from each module.

Text Book:

'Understanding Automotive Electronics', William B. Ribbens, SAMS/Elsevier publishing, 6thEdition, 1997.

Reference Book:

'Automotive Electrics and Automotive Electronics-Systems and Components, Networking and Hybrid Drive', Robert Bosch Gmbh, Springer Verlag, 5th Edition, 2007.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Implement various control requirements in the automotive system.	Understand
CO2	Comprehend dashboard electronics and engine system electronics.	Analyze
CO3	Identify various physical parameters that are to be sensed and monitored for maintaining the stability of the vehicle under dynamicconditions.	Analyze
CO4	Understand and implement the controls and actuator system pertainingto the comfort and safety of commuters.	Understand
CO5	Design sensor network for mechanical fault diagnostics in an automotive vehicle.	Understand

Program Outcome of this course

Sl. No.	Description	POs
1	An ability to independently carry out research /investigation and development work to solve practical problems	PO1
2	An ability to write and present a substantial technical report/document	PO2
3	Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program	PO3
4	An ability to create, select, apply appropriate techniques, resources and modern tools to solve complex engineering activities with an understanding of their limitations.	PO4
5	An ability to apply Professional ethics, responsibilities and norms of the engineering.	PO5
6	An ability to recognize the need to engage in independent and life-long learning in Digital Communication domain.	PO6

Mapping of COS and POs

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	**1**	**1**	**1**	**1**	**2**	**1**
CO2	**1**	**2**	**1**	**2**	**1**	**1**
CO3	**1**	**1**	**2**	**1**	**1**	**1**
CO4	**1**	**1**	**1**	**1**	**1**	**1**
CO5	**1**	**1**	**1**	**1**	**1**	**1**

SOC DESIGN

Course Code	**22LDE242**	CIE Marks	50
Teaching Hours/Week (L:P: SDA)	2:0:2	SEE Marks	50
Total Hours of Pedagogy	30 Hours Theory + 10 Hours SDA	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives: This course will enable students:

1. Apply the 3- and 5-stage pipeline ARM processor cores and analyse the implementation issues.
2. Use the concepts and methodologies employed in designing a System- on chip (SoC) based around a microprocessor core and in designing the microprocessor core itself.
3. Understand how SoCs and microprocessors are designed and used, and why a modern processor is designed the way that it is.
4. Use integrated ARM CPU cores (including StrongARM) that incorporate full support for memory management.
5. Analyze the requirements of a modern operating system and use the ARM architecture to address the same.

MODULE-1

ARM Organization and Implementation: 3-stage pipeline ARM organization, 5-stage pipeline ARM organization, ARM instruction execution, ARM implementation, The ARM coprocessor interface. The ARM Instruction Set: Introduction, Exceptions, Conditional execution, Branch and Branch with Link (B, BL), Branch, Branch with Link and exchange (BX, BLX), Software Interrupt (SWI), Data processing instructions, Multiply instructions, Count leading zeros (CLZ - architecture v5T only), Single word and unsigned byte data transfer instruction, Half-word and signed byte data transfer instructions, Multiple register transfer instructions, Swap memory and register instructions (SWP), Status register to general register transfer instructions, General register to status register transfer instructions, Coprocessor instructions, Coprocessor data operations, Coprocessor data transfers, Coprocessor register transfers, Breakpoint instruction (BRK - architecture v5T only), Unused instruction space, Memory faults, ARM architecture variants. .

RBT Level: L1, L2

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE-2

Architectural Support for High-Level Languages: Abstraction in software design, Data types, Floating-point data types, The ARM floating-point architecture, Expressions, Conditional statements,

Loops, Functions and procedures, Use of memory, Run-time environment. Architectural Support for System Development: The ARM memory interface, The Advanced Microcontroller Bus Architecture (AMBA), The ARM reference peripheral specification, Hardware system prototyping tools, The ARMulator, The JTAG boundary scan test architecture, The ARM debug architecture, Embedded Trace, Signal processing support.

RBT Level: L1, L2

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE-3

ARM Processor Cores: ARM7TDMI, ARM8, ARM9TDMI, ARM10TDMI, Discussion, Example and exercises. Memory Hierarchy: Memory size and speed, On-chip memory, Caches, Cache design - an example, Memory management, Examples and exercises.

RBT Level: L1, L2

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE 4

Architectural Support for Operating Systems: An introduction to operating systems, The ARM system control coprocessor, CP15 protection unit registers, ARM protection unit, CP15 MMU registers, ARM MMU architecture, Synchronization, Context switching, Input/ Output, Example and exercises. ARM CPU Cores: The ARM710T, ARM720T and ARM740T, The ARM810, The Strong ARM SA-110, The ARM920T and ARM940T, The ARM946E-S and ARM966E-S, The ARM1020E, Discussion, Example and exercises.

RBT Level: L2, L3

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE 5

Embedded ARM Applications: The VLSI Ruby II Advanced Communication Processor, The VLSI ISDN Subscriber Processor, The One C™VWS22100 GSM chip, The Ericsson-VLSI Bluetooth Baseband Controller, The ARM7500 and ARM7500FE, The ARM7100 364, The SA-1100 368, Examples and exercises. The AMULET Asynchronous ARM Processors: Self-timed design 375, AMULET1 377, AMULET2 381, AMULET2e 384, AMULET3 387, The DRACO telecommunications controller 390, A self-timed future? 396, Example and exercises.

RBT Level: L1,L2,L3

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks.**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.

The students will have to answer five full questions, selecting one full question from each module

Text Book:

'ARM System-On-Chip Architecture', Steve Furber, Addison Wesley, 2nd edition.

Reference Books:

1. 'The Definitive Guide to the ARM Cortex-M3', Joseph Yiu, Newnes, (Elsevier), 2nd edition, 2010.

2. 'On-Chip Communication Architectures: System on Chip Interconnect', Sudeep Pasricha and Nikil Dutt, Morgan Kaufmann Publishers, 2008.

3. 'Reuse Methodology Manual for System on Chip designs', Michael Keating, Pierre Bricaud, Kluwer Academic Publishers, 2nd edition, 2008

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Apply the 3- and 5-stage pipeline ARM processor cores and analyse the implementation issues	Understand
CO2	Use the concepts and methodologies employed in designing a System-onchip (SoC) based around a microprocessor core and in designing the microprocessor core itself.	Analyze
CO3	Understand how SoCs and microprocessors are designed and used, and why a modern processor is designed the way that it is.	Analyze
CO4	Use integrated ARM CPU cores (including StrongARM) that incorporate full support for memory management.	Understand
CO5	Analyze the requirements of a modern operating system and use the ARM architecture to address the same.	Understand

Program Outcome of this course

Sl. No.	Description	POs
1	An ability to independently carry out research /investigation and development work to solve practical problems	PO1
2	An ability to write and present a substantial technical report/document	PO2
3	Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program	PO3
4	An ability to create, select, apply appropriate techniques, resources and modern tools to solve complex engineering activities with an understanding of their limitations.	PO4
5	An ability to apply Professional ethics, responsibilities and norms of the engineering.	PO5
6	An ability to recognize the need to engage in independent and life-long learning in Digital Communication domain.	PO6

Mapping of COS and POs

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	**1**	**1**	**1**	**1**	**2**	**1**
CO2	**2**	**2**	**1**	**2**	**1**	**1**
CO3	**1**	**1**	**2**	**1**	**1**	**1**
CO4	**1**	**1**	**1**	**2**	**1**	**1**
CO5	**1**	**1**	**2**	**1**	**1**	**1**

Micro Electro Mechanical Systems

Course Code	**22LDE243**	CIE Marks	50
Teaching Hours/Week (L:P: SDA)	2:0:2	SEE Marks	50
Total Hours of Pedagogy	30 Hours Theory + 10 Hours SDA	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives: This course will enable students:

1. Understand the technologies related to Micro Electro Mechanical Systems.
2. Relate to the scaling laws in miniaturization.
3. Analyse the MEMS devices and develop suitable mathematical models
4. Understand the various application areas for MEMS devices
5. Describe the design and fabrication processes involved with MEMS devices.

MODULE-1

Overview of MEMS and Microsystems: MEMS and Microsystem, Typical MEMS and Microsystems Products, Evolution of Microfabrication, Microsystems and Microelectronics, Multidisciplinary Nature of Microsystems, Miniaturization. Applications and Markets.

RBT Level: L1, L2

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE-2

Working Principles of Microsystems: Introduction, Micro sensors, Micro actuation, MEMS with Micro actuators, Micro accelerometers, Microfluidics.

Engineering Science for Microsystems Design and Fabrication:

Introduction, Atomic Structure of Matters, Ions and Ionization, Molecular Theory of Matter and Inter-molecular Forces, Doping of Semiconductors, The Diffusion Process, Plasma Physics, Electrochemistry.

RBT Level: L1, L2

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE-3

Engineering Mechanics for Microsystems Design: Introduction, Static Bending of Thin Plates, Mechanical Vibration, Thermomechanics, Fracture Mechanics, Thin Film Mechanics, Overview on Finite Element Stress Analysis.

RBT Level: L1, L2

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE 4

Introduction, Scaling in Geometry, Scaling in Rigid-Body Dynamics, Scaling in Electrostatic Forces, Scaling of Electromagnetic Forces, Scaling in Electricity, Scaling in Fluid Mechanics, Scaling in Heat Transfer.

RBT Level: L2, L3

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE 5

Overview of Micro-manufacturing: Introduction, Bulk Micro-manufacturing, Surface Micromachining, The LIGA Process, Summary on Micro manufacturing.

Microsystem Design: Introduction, Design Considerations, Process Design, Mechanical Design, Using Finite Element Method.

RBT Level: L1,L2,L3

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.

The students will have to answer five full questions, selecting one full question from each module.

Text Book:

'MEMS and Micro systems: Design, Manufacture and Nanoscale Engineering', Tai-Ran Hsu, John Wiley & Sons, ISBN: 978-0470-08301-7,2nd Edition, 2008

Reference Books:

1. 'Micro and Nano Fabrication: Tools and Processes', Hans H. Gatzen, Volker Saile, Jurg Leuthold, Springer, 2015
2. 'Micro Electro Mechanical Systems (MEMS)', Dilip Kumar Bhattacharya, Brajesh Kumar Kaushik, Cengage Learning.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Understand the technologies related to Micro Electro Mechanical Systems.	Understand
CO2	Relate to the scaling laws in miniaturization.	Analyze
CO3	Analyse the MEMS devices and develop suitable mathematical models	Analyze
CO4	Understand the various application areas for MEMS devices	Understand
CO5	Describe the design and fabrication processes involved with MEMS devices	Understand

Program Outcome of this course

Sl. No.	Description	POs
1	An ability to independently carry out research /investigation and development work to solve practical problems	PO1
2	An ability to write and present a substantial technical report/document	PO2
3	Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program	PO3
4	An ability to create, select, apply appropriate techniques, resources and modern tools to solve complex engineering activities with an understanding of their limitations.	PO4
5	An ability to apply Professional ethics, responsibilities and norms of the engineering.	PO5
6	An ability to recognize the need to engage in independent and life-long learning in Digital Communication domain.	PO6

Mapping of COS and POs

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	1	1	1	1	2	1
CO2	2	2	1	2	1	1
CO3	1	1	2	1	1	1
CO4	1	1	1	2	1	1
CO5	1	1	2	1	1	1

Advanced Control System

Course Code	**22LDE244**	CIE Marks	50
Teaching Hours/Week (L:P: SDA)	2:0:2	SEE Marks	50
Total Hours of Pedagogy	30 Hours Theory + 10 Hours SDA	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives: This course will enable students:

1. Derive the pulse transfer function for various closed loop configurations and understand the stability analysis of sampled data control systems.
2. Apply state space techniques to model linear continuous and discrete time systems, convert state space (SS) representations to transfer function (TF) representation and vice versa.
3. Apply controllability and observability tests.
4. Solve the optimal control problems using state variable approach and knowledge of adaptive control systems.
5. Understand the types of nonlinearities, characteristics of Non-linear systems and the stability analysis of Non-linear control systems.

MODULE-1

Digital Control Systems: Review of Difference equations, Z – transforms and Inverse Z transforms, The Z- transfer function(Pulse transfer function), The Z - Transform Analysis of Sampled data Control Systems, The Z and S - domain relationship, Stability analysis (Jury's Stability Test and Bilinear Transformation **RBT Level: L1, L2**

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE-2

State Models & Solution of State equations: State models for Linear Continuous Time and Linear Discrete Time systems, Diagonalization, Solution of State Equations (for both Continuous and Discrete Time systems), Relevant problems. **RBT Level: L1, L2**

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE-3

State Feedback Systems: Concepts of Controllability and Observability (for both Continuous and Discrete Time systems),Pole Placement by State Feedback (for both continuous and discrete Time systems), Observer System (Full order and Reduced order observers for both Continuous and Discrete Time systems),Relevant problems

RBT Level: L1, L2

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE 4

Regulators: Dead beat Control by State Feedback, Optimal control problems using State Variable approach, State regulator and Output regulator, Concepts of Model Reference Adaptive Control (MRAC).

RBT Level: L2, L3

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE 5

Nonlinear Control Systems: Behaviour of Nonlinear Systems, Common Physical Nonlinearities, Describing Function Method, Stability Analysis by Describing Function Method, Phase Plane Method, Stability Analysis by Phase Plane Method.

RBT Level: L1,L2,L3

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks.**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.

The students will have to answer five full questions, selecting one full question from each module.

Text Book:

1. 'Control Systems Engineering', IJ Nagrath& MGopal, New Age International Publishers, Fifth edition, 2007.

2. 'Discrete Time Control Systems', K Ogata, 2ndedition, PHI, 2009.

Reference Books:

1. 'Modern Control Engineering', K Ogata, PHI, 5thEdition, 2010.

2. 'Modern Control System Theory', M Gopal,New Age International, 2012.

3. 'Digital Control and State Variable methods', M Gopal, TataMcGrawHill, 4 thedition, 2012.

4. 'Advanced Control Theory', A Nagoorkani, RBA publications, 2006.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Derive the pulse transfer function for various closed loop configurations and understand the stability analysis of sampled data control systems	Design
CO2	Apply state space techniques to model linear continuous and discrete time systems, convert state space (SS) representations to transfer function (TF) representation and vice versa.	Apply
CO3	Apply controllability and observability tests.	Apply
CO4	Solve the optimal control problems using state variable approach and knowledge of adaptive control systems.	Analyse
CO5	Understand the types of nonlinearities, characteristics of Nonlinear systems and the stability analysis of Nonlinear control systems.	Understand

Program Outcome of this course

Sl. No.	Description	POs
1	An ability to independently carry out research /investigation and development work to solve practical problems	PO1
2	An ability to write and present a substantial technical report/document	PO2
3	Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program	PO3
4	An ability to create, select, apply appropriate techniques, resources and modern tools to solve complex engineering activities with an understanding of their limitations.	PO4
5	An ability to apply Professional ethics, responsibilities and norms of the engineering.	PO5
6	An ability to recognize the need to engage in independent and life-long learning in Digital Communication domain.	PO6

Mapping of COS and POs

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	**1**	**1**	**1**	**1**	**2**	**1**
CO2	**2**	**2**	**1**	**2**	**1**	**1**
CO3	**1**	**1**	**2**	**1**	**1**	**1**
CO4	**1**	**1**	**1**	**2**	**1**	**1**
CO5	**1**	**1**	**2**	**1**	**1**	**1**

Simulation, Modelling and Analysis

Course Code	**22LDE245**	CIE Marks	50
Teaching Hours/Week (L:P: SDA)	2:0:2	SEE Marks	50
Total Hours of Pedagogy	30 Hours Theory + 10 Hours SDA	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives: This course will enable students:

1. Define the need of simulation and modeling.
2. Comprehend the simulation of deterministic and probabilistic models, with a focus on statistical data analysis and simulation data.
3. Describe various simulation models.
4. Discuss the process of selecting of probability distributions.
5. Perform output data analysis.

MODULE-1

Basic Simulation Modeling: Nature of simulation, Systems, Models and Simulation, Discrete- Event Simulation, Simulation of Single Server Queuing System, Simulation of inventory system, Parallel and distributed simulation and the high level architecture, Steps in sound simulation study, and Other types of simulation, Advantages and disadvantages. **RBT Level: L1, L2,L3**

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE-2

Review of Basic Probability and Statistics: Random Variables and their properties, Simulation Output Data and Stochastic Processes, Estimation of Means, Variances and Correlations, Confidence Intervals and Hypothesis tests for the Mean

Building valid, credible and appropriately detailed simulation models:

Introduction and definitions, Guidelines for determining the level of models detail, Management's Role in the Simulation Process, Techniques for increasing model validity and credibility, Statistical procedure for comparing the real world observations and simulation output data.

RBT Level: L1, L2

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE-3

Selecting Input Probability Distributions: Useful probability distributions, activity I, II and III. Shifted and truncated distributions; Specifying multivariate distribution, correlations, and stochastic

processes; Selecting the distribution in the absence of data, Models of arrival process

RBT Level: L1, L2

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE 4

Random Number Generators: Linear congruential Generators, Other kinds, Testing number generators.

Generating the Random Variates: General approaches, Generating continuous random variates, Generating discrete random variates, Generating random vectors, and correlated random variates; Generating arrival processes.

RBT Level: L2, L3

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE 5

Output data analysis for a single system: Transient and steady state behavior of a stochastic process; Types of simulations with regard to analysis; Statistical analysis for terminating simulation; Statistical analysis for steady state parameters; Statistical analysis for steady state cycle parameters; Multiple measures of performance, Time plots of important variables.

RBT Level: L1,L2,L3

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks.**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.

The students will have to answer five full questions, selecting one full question from each module.

Text Book:

'Simulation modeling and analysis', Averill Law, McGraw Hill, 4th edition, 2007.

Reference Books:

1. 'Simulation modeling and analysis with ARENA', Tayfur Altiok and Benjamin Melamed, Elsevier, Academic press, 2007.

2. 'Discrete event system Simulation', Jerry Banks, Pearson, 2009

3. 'Applied simulation modeling', Seila Ceric and Tadikamalla, Cengage 2009.

4. 'Discrete event simulation', George. S. Fishman, Springer, 2001.

5. 'System modeling and simulation', Frank L. Severance, Wiley, 2009.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Define the need of simulation and modeling.	Understand
CO2	Comprehend the simulation of deterministic and probabilistic models, with a focus on statistical data analysis and simulation data.	Understand
CO3	Describe various simulation models.	Understand
CO4	Discuss the process of selecting of probability distributions.	Analysez
CO5	Perform output data analysis.	Understand

Program Outcome of this course

Sl. No.	Description	POs
1	An ability to independently carry out research /investigation and development work to solve practical problems	PO1
2	An ability to write and present a substantial technical report/document	PO2
3	Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program	PO3
4	An ability to create, select, apply appropriate techniques, resources and modern tools to solve complex engineering activities with an understanding of their limitations.	PO4
5	An ability to apply Professional ethics, responsibilities and norms of the engineering.	PO5
6	An ability to recognize the need to engage in independent and life-long learning in Digital Communication domain.	PO6

Mapping of COS and POs

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	**1**	**1**	**1**	**1**	**2**	**1**
CO2	**2**	**2**	**1**	**2**	**1**	**1**
CO3	**1**	**1**	**2**	**1**	**1**	**1**
CO4	**1**	**1**	**1**	**2**	**1**	**1**
CO5	**1**	**1**	**2**	**1**	**1**	**1**

DIGITAL CIRCUITS SIMULATION LABORATORY

Course Code	**22LDEL26**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	1:2:0	SEE Marks	50
Credits	2	Exam Hours	100

Course objectives: This course will enable students:

- To understand the digital circuits using graphical programming tool LabVIEW.
- To understand the interfaces and observe the results with digital circuits.
- To learn and develop Verilog Programs for Digital Circuit design.
- To analyze digital systems on FPGA/CPLD.
- To analyze and validate digital systems using Logic analyzer/Chipscope.

Part A:

Graphical Programming using LabVIEW.

Sl. No.	Experiments
1	Design of 4 bit Adders (CLA, CSA, CMA, Parallel adders)
2	Design of Binary Subtractors
3	Design of Encoder (8 x 3), Decoder(3 x 8)
4	Design of Multiplexer (8 x 1) and De-multiplexer (1 x 8)
5	Design of code converters & Comparator
6	Design of FF (SR, D, T, JK, and Master Slave with delays)
7	Design of registers using latches and flip-flops
8	Design of 8-bit Shift registers
9	Design of Asynchronous & Synchronous Counters

PART-B:

Develop Verilog Program for design and testing the following digital circuits (for 4/8 bits) using FPGA/CPLD. Use logic analyzer/ Chipscope for the verification of results.

(Note: Programming can be done using any complier. Download the programs on FPGA/CPLD boards and performance testing may be done using pattern generator (32 channels and logic analyzer)/Chipscope pro. Implementing the above designs on Xilinx/Altera/Cypress/equivalent based FPGA/CPLD kits.)

Sl. No.	Experiments
1	Carry skip and carry look ahead adder
2	BCD adder and subtractor
3	Array Multiplication (signed and unsigned)
4	Booth multiplication (radix-4)
5	Magnitude comparator
6	LFSR
7	Parity generator
8	Universal Shift Register
9	Sequence generation (11101 say) using Mealy/Moore FSM

Note: Conduct the experiments using C/NS2/Qualnet/OPNET/OMNET simulation tools

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

1. Simulate the digital circuits using graphical programming tool LabVIEW.
2. Build user friendly interfaces to interact with the digital circuits and to observe the outputs.
3. Develop Verilog Programs for Digital Circuit design simulation.
4. Implement digital systems on FPGA/CPLD.
5. Test and validate digital systems using Logic analyzer/Chipscope.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 40%of maximum marks in the semester-end examination (SEE). In total of CIE and SEE student has to secure 50% maximum marks of the course.

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be

evaluated for 10 marks.

- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of the semester and the second test shall be conducted after the 14th week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of **scaled-down** marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute; examiners are appointed by the University.

- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.
- Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.
- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.
- General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)
- Change of experiment is allowed only once and 10% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 Hours.

SEMESTER –III

ERROR CONTROL CODING			
Course Code	**22LDE31**	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	(3:0:2)	SEE Marks	50
Total Hours of Pedagogy	40 Hours Theory + 10 Hours SDA	Total Marks	100
Credits	04	Exam Hours	3

Course Learning objectives: This course will enable students to:

- Understand the concept of the Entropy, information rate and capacity for the discrete memoryless channel.
- Apply modern algebra and probability theory for the coding.
- Compare Block codes such as Linear Block Codes, Cyclic codes, etc. and Convolutional codes.
- Detect and correct errors for different data communication and storage systems.
- Analyze and implement different Block code encoders and decoders, and also convolutional encoders and decoders including soft and hard Viterbi algorithm.

Module-1

Information theory: Introduction, Entropy, Source coding theorem, discrete memoryless channel, Mutual Information, Channel Capacity Channel coding theorem (Chap. 5 of Text 1).

Introduction to algebra: Groups, Fields, binary field arithmetic, Construction of Galois Fields GF (2m) and its properties, (Only statements of theorems without proof) Computation using Galois field GF (2m) arithmetic, Vector spaces and Matrices. **RBT Level: L1, L2, L3**

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

Module-2

Linear block codes: Generator and parity check matrices, Encoding circuits, Syndrome and error detection, Minimum distance considerations, Error detecting and error correcting capabilities, Standard array and syndrome decoding, Single Parity Check Codes (SPC),Repetition codes, Self dual codes, Hamming codes, Reed-Muller codes. Product codes and Interleaved codes **RBT Level: L1, L2, L3**

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

Module-3

Cyclic codes: Introduction, Generator and parity check polynomials, Encoding of cyclic codes, Syndrome computing and error detection, Decoding of cyclic codes, Error trapping Decoding, Cyclic hamming codes, Shortened cyclic codes (Chap. 4 of Text2). **RBT Level: L1, L2, L3**

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

Module-4

BCH codes: Binary primitive BCH codes, Decoding procedures, Implementation of Galois field arithmetic. (6.1,6.2,6.7 of Text 2) Primitive BCH codes over GF (q),

Reed -Solomon codes

Majority Logic decodable codes: One -step majority logic decoding, Multiple step majority logic (8.1, 8.4 of Text 2). **RBT Level: L1, L2, L3**

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

Module-5

Convolution codes: Encoding of convolutional codes: Systematic and Non-systematic Convolutional Codes, Feedforward encoder inverse, A catastrophic encoder, Structural properties of convolutional codes: state diagram, state table, state transition table, tree diagram, trellis diagram. Viterbi algorithm, Sequential decoding: Log Likelihood Metric for Sequential Decoding. **RBT Level: L1, L2, L3**

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks**

to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Textbooks:

1. 'Digital Communication systems', Simon Haykin, Wiley India Private. Ltd, ISBN 978-81-265-4231-4, First edition, 2014
2. 'Error control coding', Shu Lin and Daniel J. Costello. Jr, Pearson, Prentice Hall, 2nd edition, 2004

Reference Books:

1. 'Theory and practice of error control codes', Blahut. R. E, Addison Wesley, 1984
2. 'Introduction to Error control coding', Salvatore Gravano, Oxford University Press, 2007
3. 'Digital Communications - Fundamentals and Applications', Bernard Sklar, Pearson Education (Asia) Pvt. Ltd., 2nd Edition, 2001

Web links and Video Lectures (e-Resources):

Skill Development Activities Suggested

- NPTEL Course on Information Theory and Coding

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Understand the concept of the Entropy, information rate and capacity for the Discrete memoryless channel.	Understand
CO2	Apply modern algebra and probability theory for the coding.	Apply
CO3	Compare Block codes such as Linear Block Codes, Cyclic codes, etc. and Convolutional codes.	Apply
CO4	Detect and correct errors for different data communication and storage systems.	Apply
CO5	Analyze and implement different Block code encoders and decoders, and also convolutional encoders and decoders including soft and hard Viterbi algorithm.	Apply

Program Outcome of this course

Sl. No.	Description	POs
1	An ability to independently carry out research /investigation and development work to solve practical problems	PO1
2	An ability to write and present a substantial technical report/document	PO2
3	Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program	PO3
4	An ability to create, select, apply appropriate techniques, resources and modern tools to solve complex engineering activities with an understanding of their limitations.	PO4
5	An ability to apply Professional ethics, responsibilities and norms of the engineering.	PO5
6	An ability to recognize the need to engage in independent and life-long learning in Digital Communication and Networking domain	PO6

Mapping of COS and POs

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	**1**	**-**	**1**	**1**	**-**	**1**
CO2	**1**	**-**	**1**	**1**	**-**	**1**
CO3	**1**	**-**	**1**	**1**	**-**	**1**
CO4	**1**	**-**	**1**	**1**	**-**	**1**
CO5	**1**	**-**	**1**	**1**	**-**	**1**

Professional elective 3

ADVANCES IN IMAGE PROCESSING			
Course Code	**22LDE321**	CIE Marks	50
Teaching Hours/Week (L:P: SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40 Hours Theory	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives: This course will enable students:

1. Understand the representation of the digital image and its properties.
2. Apply pre-processing techniques required to enhance the image for its further analysis.
3. Use segmentation techniques to select the region of interest in the image for analysis.
4. Represent the image based on its shape and edge information and also describe the objects present in the image based on its properties and structure.
5. Use morphological operations to simplify images, and quantify and preserve the main shape characteristics of the objects.

MODULE-1

The image, its representations and properties: Image representations a few concepts, Image digitization, Digital image properties, Color images.

RBT Level: L1, L2

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE-2

Image Pre-processing: Pixel brightness transformations, geometric transformations, local pre-processing.

RBT Level: L1, L2

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE-3

Segmentation: Thresholding; Edge-based segmentation – Edge image thresholding, Edge relaxation, Border tracing, Hough transforms; Region – based segmentation – Region merging, Region splitting, Splitting and merging, Watershed segmentation, Region growing post-processing.

RBT Level: L1, L2

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE 4

Shape representation and description: Region identification; Contour-based shape representation and description – Chain codes, Simple geometric border representation, Fourier transforms of boundaries, Boundary description using segment sequences, B-spline representation; Region-based shape representation and description – Simple scalar region descriptors, Moments, Convex hull.

RBT Level: L2, L3

Teaching-	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity

Learning Process	based method, Seminar

MODULE 5

Mathematical Morphology: Basic morphological concepts, Four morphological principles, Binary dilation and erosion, Skeletons and object marking, Morphological segmentations and watersheds.

RBT Level: L1,L3

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.

The students will have to answer five full questions, selecting one full question from each module.

Text Book:

'Image Processing, Analysis, and Machine Vision', Milan Sonka, Vaclav Hlavac, Roger Boyle, Cengage Learning, ISBN: 978-81-315-1883-0, 2013

Reference Books:

1. 'Digital Image Processing for Medical Applications', Geoff Doughertry, Cambridge university Press, 2010.

2. 'Digital Image Processing', S Jayaraman, S Esakkirajan, T Veerakumar, Tata McGraw Hill, 2011.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Understand the representation of the digital image and its properties.	Understand
CO2	Apply pre-processing techniques required to enhance the image for its further analysis.	Understand
CO3	Use segmentation techniques to select the region of interest in the image for analysis.	Understand
CO4	Represent the image based on its shape and edge information and also describe the objects present in the image based on its properties and structure.	Understand
CO5	Use morphological operations to simplify images, and quantify and preserve the main shape characteristics of the objects	Apply

Program Outcome of this course

Sl. No.	Description	POs
1	An ability to independently carry out research /investigation and development work to solve practical problems	PO1
2	An ability to write and present a substantial technical report/document	PO2
3	Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program	PO3
4	An ability to create, select, apply appropriate techniques, resources and modern tools to solve complex engineering activities with an understanding of their limitations.	PO4
5	An ability to apply Professional ethics, responsibilities and norms of the engineering.	PO5
6	An ability to recognize the need to engage in independent and life-long learning in Digital Communication domain.	PO6

Mapping of COS and POs

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	**1**	**1**	**1**	**1**	**2**	**1**
CO2	**1**	**1**	**1**	**2**	**1**	**1**
CO3	**2**	**1**	**2**	**1**	**1**	**1**
CO4	**1**	**1**	**1**	**2**	**1**	**1**
CO5	**1**	**1**	**2**	**1**	**1**	**1**

CMOS RF Circuits Design			
Course Code	**22LDE322**	CIE Marks	50
Teaching Hours/Week (L:P: SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40 Hours Theory	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives: This course will enable students to:

1. Analyse the effect of nonlinearity and noise in RF and microwave design.
2. Exemplify the approaches taken in actual RF products.
3. Minimize the number of off-chip components required to design mixers, Low-Noise Amplifiers, VCO and PLLs.
4. Explain various receivers and transmitter topologies with their merits and drawbacks.
5. Demonstrate how the system requirements define the parameters of the circuits and the impact on the performance.

MODULE-1

Introduction to RF Design, Wireless Technology and Basic Concepts: A wireless world, RF design is challenging, The big picture. General considerations, Effects of Nonlinearity, Noise, Sensitivity and dynamic range, Passive impedance transformation. Scattering parameters, Analysis of nonlinear dynamic systems, conversion of gains and distortion.

RBT Level: L1, L2,L3

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE-2

Communication Concepts: General concepts, analog modulation, digital modulation, spectral re-growth, coherent and non-coherent detection, Mobile RF communications, Multiple access techniques, Wireless standards, Appendix 1: Differential phase shift keying.

RBT Level: L1, L2

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE-3

Transceiver Architecture: General considerations, Receiver architecture, Transmitter architectures, Direct conversion and two-step transmitters, RF testing for heterodyne, Homodyne, Image reject, Direct IF and sub sampled receivers.

RBT Level: L1, L2

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE 4

Low Noise Amplifiers and Mixers: General considerations, Problem of input matching, LNA topologies: common-source stage with inductive load, common-source stage with resistive feedback. Mixers-General considerations, passive down conversion mixers, Various mixers- working and implementation. **RBT Level: L2, L3**

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE 5

VCO and PLLs- Oscillators- Basic topologies VCO and definition of phase noise, Noise power and trade off. Resonator VCO designs, Quadrature and single sideband generators. Radio frequency Synthesizers- PLLS, Various RF synthesizer architectures and frequency dividers, Power Amplifier design. **RBT Level: L1,L2,L3**

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks.**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.

The students will have to answer five full questions, selecting one full question from each module.

Text Book: 'RF Microelectronics', B. Razavi, PHI, second edition.

Reference Books:

1. 'CMOS Circuit Design, layout and Simulation', R. Jacob Baker, H.W. Li, D.E. Boyce, PHI, 1998.
2. 'Design of CMOS RF Integrated Circuits', Thomas H. Lee, Cambridge University press, 1998.
3. 'Mixed Analog and Digital Devices and Technology', Y.P. Tsividis, TMH, 1996.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Analyse the effect of nonlinearity and noise in RF and microwave design.	Analyze
CO2	Exemplify the approaches taken in actual RF products.	Understand
CO3	Minimize the number of off-chip components required to design mixers, Low-Noise Amplifiers, VCO and PLLs	Analyze
CO4	Explain various receivers and transmitter topologies with their merits and drawbacks.	Analyze
CO5	Demonstrate how the system requirements define the parameters of the circuits and the impact on the performance	Analyze

Program Outcome of this course

Sl. No.	Description	POs
1	An ability to independently carry out research /investigation and development work to solve practical problems	PO1
2	An ability to write and present a substantial technical report/document	PO2
3	Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program	PO3
4	An ability to create, select, apply appropriate techniques, resources and modern tools to solve complex engineering activities with an understanding of their limitations.	PO4
5	An ability to apply Professional ethics, responsibilities and norms of the engineering.	PO5
6	An ability to recognize the need to engage in independent and life-long learning in Digital Communication domain.	PO6

Mapping of COS and POs

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	**1**	**1**	**1**	**1**	**2**	**1**
CO2	**2**	**2**	**1**	**2**	**1**	**1**
CO3	**1**	**1**	**2**	**1**	**1**	**1**
CO4	**1**	**1**	**1**	**2**	**1**	**1**
CO5	**1**	**1**	**2**	**1**	**1**	**1**

Real Time Systems			
Course Code	**22LDE323**	CIE Marks	50
Teaching Hours/Week (L:P: SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40 Hours Theory	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives: This course will enable students to:

1. Analyze Real time systems.
2. Distinguish a real-time system with other systems.
3. Describe the functions of Real time operating systems.
4. Demonstrate embedded system applications.
5. Design a Real Time system.

MODULE-1

Introduction to Real-Time Embedded Systems: Brief history of Real Time Systems, A brief history of Embedded Systems.

System Resources: Resource Analysis, Real-Time Service Utility, Scheduling Classes, The Cyclic Executive, Scheduler Concepts, Pre-emptive Fixed Priority Scheduling Policies, Real-Time OS, Thread Safe Re-entrant Functions. **RBT Level: L1, L2,L3**

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE-2

Processing: Pre-emptive Fixed-Priority Policy, Feasibility, Rate Monotonic least upper bound, and Necessary and Sufficient feasibility, Deadline – Monotonic Policy, Dynamic priority policies.

I/O Resources: Worst-case Execution time, Intermediate I/O, Execution efficiency, I/O Architecture.

Memory: Physical hierarchy, Capacity and allocation, Shared Memory, ECC Memory, Flash file systems. **RBT Level: L1, L2**

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE-3

Multi-resource Services: Blocking, Deadlock and livestock, Critical sections to protect shared resources, priority inversion.

Soft Real-Time Services: Missed Deadlines, QoS, and Alternatives to rate monotonic policy, Mixed hard and soft real-time services.

RBT Level: L1, L2

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE 4

Embedded System Components: Firmware components, RTOS system software mechanisms, Software application components.

Debugging Components: Exceptions assert, Checking return codes, Single step debugging, kernel scheduler traces, Test access ports, Trace ports, Power- On self-test and diagnostics.

RBT Level: L2, L3

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE 5

Performance Tuning: Basic concepts of drill-down tuning, hardware – supported profiling and tracing, Building performance monitoring into software, Path length.

High availability and Reliability Design: Reliability and Availability, Similarities and differences, Reliability, Reliable software, Available software, Design trade-offs, Hierarchical applications for Fail-safe design.

RBT Level: L1,L2,L3

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.

The students will have to answer five full questions, selecting one full question from each module

Text Book:

"Real-Time Embedded Systems and Components", Sam Siewert, Cengage Learning India Edition, 2007.

Reference Books:

1. "Real time systems", Krishna CM and Kang Singh G, Tata McGraw Hill ISBN: 0-07-114243-64, 2003.

2. "Real-Time Concepts for Embedded Systems", Qing Li and Carolyn Yao, CMP Books, ISBN: 1578201241, 2003.

3. "Real Time Systems", Jane W. S. Liu, Prentice Hall, ISBN: 0130996513, 2000.

4. "Real-Time Systems Design and Analysis", Phillip A. Laplante, John Wiley & Sons, 2004

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Analyze Real time systems.	Analyze
CO2	Distinguish a real-time system with other systems.	Understand
CO3	Describe the functions of Real time operating systems.	Analyze
CO4	Demonstrate embedded system applications.	Analyze
CO5	Design a Real Time system.	Design

Program Outcome of this course

Sl. No.	Description	POs
1	An ability to independently carry out research /investigation and development work to solve practical problems	PO1
2	An ability to write and present a substantial technical report/document	PO2
3	Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program	PO3
4	An ability to create, select, apply appropriate techniques, resources and modern tools to solve complex engineering activities with an understanding of their limitations.	PO4
5	An ability to apply Professional ethics, responsibilities and norms of the engineering.	PO5
6	An ability to recognize the need to engage in independent and life-long learning in Digital Communication domain.	PO6

Mapping of COS and POs

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	**1**	**1**	**1**	**1**	**2**	**1**
CO2	**2**	**2**	**1**	**2**	**1**	**1**
CO3	**1**	**1**	**2**	**1**	**1**	**1**
CO4	**1**	**1**	**1**	**2**	**1**	**1**
CO5	**1**	**1**	**2**	**1**	**1**	**1**

RF MEMS			
Course Code	**22LDE324**	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40 Hours Theory	Total Marks	100
Credits	03	Exam Hours	3

Course Learning objectives: This course will enable students to:

- Comprehend the need for micromachining and MEMS based systems for RF and microwave applications
- Describe the micromachining techniques and their use in the fabrication of micro switches, capacitors and inductors
- Design MEMS based microwave components aimed at reducing insertion loss and increasing bandwidth.
- Realize high Q micromechanical filters for frequencies up to and beyond 10 MHz, and micro machined surface acoustic wave (SAW) filters filling the gap up to 2 GHz.
- Describe the packaging approaches used for these RF MEMS devices.

Module-1

Review: Introduction to MEMS: Fabrication for MEMS transducers and actuators, Micro-sensing for MEMS, Materials for MEMS. MEMS materials and fabrication techniques: Metals, Semiconductors, Thin films, Materials for polymer MEMS, Bulk machining for Silicon based MEMS, Surface machining for Silicon based MEMS, Micro stereo-lithography for polymer MEMS.

RBT Level: L1, L2

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

Module-2

RF MEMS Switches and micro-relays: Switch parameters, Basics of switching, Switches for RF and Microwave applications, Actuation mechanisms, Micro-relays and micro-actuators, Dynamic of switch operations; MEMS switch design and design consideration, MEMS inductors and capacitors.

RBT Level: L1, L2, L3

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

Module-3

Micro machined RF filters and phase shifters: RF filters, Modelling of mechanical filters, Micro-mechanical filters, SAW filters - Basic, Design consideration. Bulk acoustic wave filters, Micro-machined filters for millimetre wave frequencies. Micro-machined phase shifters, Types and limitations, MEMS and Ferroelectric phase shifters, Applications. **RBT Level: L1, L2, L3, L4**

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

Module-4

Micromachined transmission line and components: Micromachined transmission line: Losses in transmission line, coplanar lines, Microshield and membrane supported lines, Microshield components, Micro machined waveguides, Directional couplers and Mixers, Resonators and Filters.

RBT Level: L1, L2, L3

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

Module-5

Micromachined antennas: design, Fabrication and measurements. Integration and packaging for RF MEMS. Roles and types of packages, Flip chip techniques, Multichip module packaging and Wafer bonding, Reliability issues and thermal issues

RBT Level: L1, L2, L3, L4

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks.**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Text Book:

'RF MEMS and their Applications', Vijay K Varadan, K. J. Vinoy and K. A. Jose, Wiley India Pvt. Ltd., ISBN - 10 : 8126529911, 2011.

Reference books:

1. 'RF MEMS circuit design', J De Los Santos, Artech House, 2002.
2. 'Transaction Level Modelling with System C: TLM concepts and applications for Embedded Systems', Frank Ghenassia, Springer, 2005.
3. 'Networks on chips: Technology and Tools', Luca Beninid, Morgan Kaufmann Publishers, 2006.

Skill Development Activities Suggested

- RF & Millimetre wave circuit design.
- Microwave active circuit design.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Comprehend the need for micromachining and MEMS based systems for RF and microwave applications	Understand
CO2	Describe the micromachining techniques and their use in the fabrication of micro switches, capacitors and inductors	Apply
CO3	Design MEMS based microwave components aimed at reducing insertion loss and increasing bandwidth	Analyze
CO4	Realize high Q micromechanical filters for frequencies up to and beyond 10 MHz, and micromachined surface acoustic wave (SAW) filters filling the gap up to 2 GHz	Apply
CO5	Describe the packaging approaches used for these RF MEMS devices.	Analyze

Program Outcome of this course

Sl. No.	Description	POs
1.	An ability to independently carry out research /investigation and development work to solve practical problems	PO1
2.	An ability to write and present a substantial technical report/document	PO2
3.	Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program	PO3
4.	An ability to create, select, apply appropriate techniques, resources and modern tools to solve complex engineering activities with an understanding of their limitations.	PO4
5.	An ability to apply Professional ethics,responsibilities and norms of the engineering	PO5
6.	An ability to recognize the need to engage in independent and life-long learning in Digital Communication and Networking domain	PO6

Mapping of COS and POs

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	**1**	**2**	**2**	**2**	**-**	**2**
CO2	**1**	**2**	**2**	**2**	**-**	**2**
CO3	**1**	**2**	**2**	**2**	**-**	**2**
CO4	**1**	**2**	**2**	**2**	**-**	**3**
CO5	**1**	**2**	**2**	**2**	**-**	**3**

Synthesis and Optimization of Digital Circuits			
Course Code	**22LDE325**	CIE Marks	50
Teaching Hours/Week (L:P: SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40 Hours Theory	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives: This course will enable students to:

1. Understand the process of synthesis and optimization in a top down approach for digital circuits' models using HDLs.
2. Understand the terminologies of graph theory and its algorithms to optimize a Boolean equation.
3. Apply different two level and multilevel optimization algorithms for combinational circuits.
4. Apply the different sequential circuit optimization methods using state models and network models.
5. Apply different scheduling algorithms with resource binding and without resource binding for pipelined sequential circuits and extended sequencing models.

MODULE-1

Introduction to Synthesis and optimization: Design of Microelectronics circuits, Computer aided Synthesis and Optimization. Hardware Modeling: HDLs for Synthesis, Abstract models, Compilation and Behavioral Optimization.

RBT Level: L1, L2,L3

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE-2

Graph theory for CAD for VLSI: Graphs, Combinatorial Optimization, Graph Optimization problems and Algorithms, Boolean Algebra and Applications. Architectural Synthesis and Optimization: Fundamental Architectural Synthesis problems, Area and Performance Estimation, Strategies for Architectural Optimization, Data path Synthesis, Control Path Synthesis.

RBT Level: L1, L2

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE-3

Two level Combinational Logic Optimization: Introduction, Logic Optimizations, and Operations on Two level Logic Covers, Algorithms for Logic Minimization, Symbolic Minimization and Encoding Problems. Multiple Levels Combinational Logic Optimization: Introduction, Models and Transformations for Combinational Networks, The Algebraic Model, The Boolean Model.

RBT Level: L1, L2

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE 4

Sequential Logic Optimization: Introduction, Sequential Logic Optimization using State based Models, Sequential Logic Optimization using Network Models, Implicit FSM Traversal Methods, Testability concerns for Synchronous Circuits.

RBT Level: L2, L3

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE 5

Scheduling Algorithms: Introduction, A Model for Scheduling problems, Scheduling with Resource Constraints, Scheduling without Resource Constraints, Scheduling Algorithms for Extended Sequencing Models, Scheduling Pipelined Circuits. Resource Sharing and Binding: Sharing and Binding for Resource dominated circuits, Sharing and Binding for General Circuits, Concurrent Binding and Scheduling.

RBT Level: L1,L2,L3

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks.**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.

The students will have to answer five full questions, selecting one full question from each module

Text Book:

'Synthesis and Optimization of Digital Circuits', Giovanni De Micheli, Tata McGraw-Hill, ISBN: 9780070582781, 2003.

Reference Book: 'Automatic Logic synthesis Techniques for Digital Systems', Edwars M.D, Macmillan New Electronic Series, 1992

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Understand the process of synthesis and optimization in a top down approach for digital circuits models using HDLs	Understand
CO2	Understand the terminologies of graph theory and its algorithms to optimize a Boolean equation.	Understand
CO3	Apply different two level and multilevel optimization algorithms for combinational circuits.	Apply
CO4	Apply the different sequential circuit optimization methods using state models and network models.	Apply
CO5	Apply different scheduling algorithms with resource binding and without resource binding for pipelined sequential circuits and extended sequencing models.	Apply

Program Outcome of this course

Sl. No.	Description	POs
1	An ability to independently carry out research /investigation and development work to solve practical problems	PO1
2	An ability to write and present a substantial technical report/document	PO2
3	Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program	PO3
4	An ability to create, select, apply appropriate techniques, resources and modern tools to solve complex engineering activities with an understanding of their limitations.	PO4
5	An ability to apply Professional ethics, responsibilities and norms of the engineering.	PO5
6	An ability to recognize the need to engage in independent and life-long learning in Digital Communication domain.	PO6

Mapping of COS and POs

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	**1**	**1**	**1**	**1**	**2**	**1**
CO2	**2**	**2**	**1**	**2**	**1**	**1**
CO3	**1**	**1**	**2**	**1**	**1**	**1**
CO4	**1**	**1**	**1**	**2**	**1**	**1**
CO5	**1**	**1**	**2**	**1**	**1**	**1**

PROFESSIONAL ELECTIVE 4

PATTERN RECOGNITION AND MACHINE LEARNING			
Course Code	**22LDE331**	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	(3:0:0)	SEE Marks	50
Total Hours of Pedagogy	40 Hours Theory	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives: This course will enable students to:

- Develop the mathematical tools required for the pattern recognition.
- Enable the student with basic knowledge on the techniques to build an intellectual machine for making decisions behalf of humans.
- Understand the techniques on how to make learning by a model, how it can be evaluated, what are all different algorithms to construct a learning model.

Module-1

Introduction: Definition of PR, Applications, Datasets for PR, Different paradigms for PR, Introduction to probability, events, random variables, Joint distributions and densities, moments, Estimation minimum risk estimators, problems. **RBT Level: L1, L2**

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

Module-2

Representation: Data structures for PR, Representation of clusters, proximity measures, size of patterns, Abstraction of Data set, Feature extraction, Feature selection, Evaluation **RBT Level: L1, L2**

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

Module-3

Nearest Neighbor based classifiers & Bayes classifier: Nearest neighbor algorithm, variants of NN algorithms use of NN for transaction databases, efficient algorithms, Data reduction, prototype selection, Bayes theorem, minimum error rate classifier, estimation of probabilities, estimation of probabilities, comparison with NNC, Naive Bayes classifier, Bayessian belief network. **RBT Level: L1, L2, L3, L4**

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

Module-4

Machine Learning Basics: Learning Algorithms, Capacity, Overfitting and Under fitting, Hyper parameters and Validation Sets, Estimator, Bias and Variance, Maximum Likelihood Estimation, Bayesian Statistics, Supervised Learning Algorithms, Unsupervised Learning Algorithms, Stochastic Gradient Decent, building a Machine Learning Algorithm, Challenges Motivating Deep Learning. **RBT Level: L1, L2**

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

Module-5

Optimization for Training Deep Models: How Learning Differs from Pure Optimization, Challenges in Neural Network Optimization, Basic Algorithms. Parameter Initialization Strategies, Algorithms with Adaptive Learning Rates.

Convolutional Networks: The Convolution Operation, Motivation, Pooling, Convolution and Pooling as an Infinitely Strong

Prior, Variants of the Basic Convolution Function, Structured Outputs, Data Types, Efficient Convolution

Algorithms, Random or Unsupervised Features. **RBT Level: L1, L2, L3**

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

Assessment Details (both CIE and SEE)

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Continuous Internal Evaluation:

1.Three Unit Tests each of **20 Marks**

2.Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Text Books

1. "Pattern Recognition (An Introduction)", V Susheela Devi, M Narsimha Murthy, Universities Press, 2011.
2. "Pattern Recognition & Image Analysis", Earl Gose, Richard Johnson baugh, Steve Jost, PH,1996.
3. "Deep Learning", Lan Good fellow and Yoshua Bengio and Aaron Courville, MIT Press,2016.

Reference Books:

1. 'Pattern Classification', Duda R. O., P.E. Hart, D.G. Stork, John Wiley and sons, 2000.
2. "Pattern Recognition and machine Learning", Chirstopher Bishop,2007.

Web links and Video Lectures (e-Resources):

- https://link.springer.com › book
- https://www.microsoft.com/en-us/research/uploads/prod/2006/01/Bishop-Pattern-Recognition-and-Machine-Learning-2006.pdf
- http://cgm.cs.mcgill.ca/~godfried/teaching/pr-web.html

Skill Development Activities Suggested

- ProgrammingAssignments/MiniProjectscanbegiventoimproveprogrammingskills.
- Online course certification related to this domain may be included.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Explain pattern recognition principals.	Understand
CO2	Develop algorithms for Pattern Recognition.	Understand
CO3	Design the nearest neighbor classifier.	Analyze
CO4	Identify the deep learning algorithms which are more appropriate for various types of learning tasks .	Understand
CO5	Implement deep learning algorithms and Execute performance metrics of Deep Learning Techniques.	Apply

Program Outcome of this course

Sl. No.	Description	POs
1	An ability to independently carry out research /investigation and development work to solve practical problems	PO1
2	An ability to write and present a substantial technical report/document	PO2
3	Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program	PO3
4	An ability to create, select, apply appropriate techniques, resources and modern tools to solve complex engineering activities with an understanding of their limitations.	PO4
5	An ability to apply Professional ethics, responsibilities and norms of the engineering	PO5
6	An ability to recognize the need to engage in independent and life-long learning in Digital Communication and Networking domain	PO6

Mapping of COS and POs

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	**1**	**1**	**-**	**-**	**-**	**2**
CO2	**1**	**1**	**-**	**-**	**-**	**2**
CO3	**2**	**1**	**1**	**-**	**-**	**2**
CO4	**2**	**1**	**1**	**2**	**-**	**2**
CO5	**2**	**1**	**2**	**-**	**2**	**2**

VLSI DESIGN FOR SIGNAL PROCESSING

Course Code	**22LDE332**	CIE Marks	50
Teaching Hours/Week (L:P: SDA)	(3:0:0)	SEE Marks	50
Total Hours of Pedagogy	40 Hours Theory	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives: This course will enable students:

1. Illustrate the use of various DSP algorithms and addresses their representation using block diagrams, signal flow graphs and data-flow graphs
2. Use pipelining and parallel processing in design of high-speed /low-power applications
3. Apply unfolding in the design of parallel architecture
4. Evaluate the use of look-ahead techniques in parallel and pipelined IIR Digital filters.
5. Develop an algorithm or architecture or circuit design for DSP applications

MODULE-1

Introduction to DSP Systems: Typical DSP Algorithms, DSP Application Demands and Scaled CMOS Technologies, Representations of DSP Algorithms.

Iteration Bounds: Data flow graph Representations, loop bound and Iteration bound. Algorithms for Computing Iteration Bound, Iteration Bound of multi rate data flow graphs.

RBT Level: L1, L2

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE-2

Pipelining and Parallel Processing: pipelining of FIR Digital Filters, parallel processing, Pipelining and parallel processing for low power. **Retiming**: Definition and Properties, Solving Systems of Inequalities, Retiming Techniques. **RBT Level: L1, L2**

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE-3

Unfolding: An Algorithm for Unfolding, Properties of Unfolding, Critical path, Unfolding and Retiming, Application of Unfolding.

Folding: Folding Transformation, Register Minimization Techniques, Register Minimization in Folded Architectures, Folding of Multirate Systems.

RBT Level: L1, L2

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE 4

Systolic Architecture Design: systolic array design Methodology, FIR systolic array, Selection of Scheduling Vector, Matrix-Matrix Multiplication and 2D systolic Array Design, Systolic Design for space representation containing Delays.

Fast convolution: Cook-Toom Algorithm, Winograd Algorithm, Iterated convolution, cyclic convolution Design of fast convolution Algorithm by Inspection.

RBT Level: L2, L3

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE 5

Pipelined and Parallel Recursive and Adaptive Filter: Pipeline Interleaving in Digital Filter, first order IIR digital Filter, Higher order IIR digital Filter, parallel processing for IIR filter, Combined pipelining and parallel processing for IIR Filter, Low power IIR Filter Design Using Pipelining and parallel processing, pipelined adaptive digital filter.

RBT Level: L1,L2,L3

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

Assessment Details (both CIE and SEE)

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Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.

The students will have to answer five full questions, selecting one full question from each module.

Text Book

- VLSI Digital Signal Processing systems, Design and implementation Keshab K.Parthi Wiley 1999

Reference Book

- Analog VLSI Signal and Information Processing Mohammed Isamail and Terri Fiez Mc Graw-Hill 1994
- VLSI and Modern Signal Processing S.Y. Kung, H.J. White House, T. Kailath Prentice Hall 1985
- Design of Analog - Digital VLSI Circuits for Telecommunication and Signal Processing Jose E. France, Yannis Tsividis Prentice Hall 1994
- DSP Integrated Circuits Lars Wanhammar Academic Press Series in Engineering 1st Edition

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Illustrate the use of various DSP algorithms and addresses their representation using block diagrams, signal flow graphs and data-flow graphs	Understand
CO2	Use pipelining and parallel processing in design of high-speed /low-power	Understand
CO3	Apply unfolding in the design of parallel architecture	Apply
CO4	Evaluate the use of look-ahead techniques in parallel and pipelined IIR Digital filters.	Apply
CO5	Develop an algorithm or architecture or circuit design for DSP applications	Apply

Program Outcome of this course

Sl. No.	Description	POs
1	An ability to independently carry out research /investigation and development work to solve practical problems	PO1
2	An ability to write and present a substantial technical report/document	PO2
3	Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program	PO3
4	An ability to create, select, apply appropriate techniques, resources and modern tools to solve complex engineering activities with an understanding of their limitations.	PO4
5	An ability to apply Professional ethics, responsibilities and norms of the engineering.	PO5
6	An ability to recognize the need to engage in independent and life-long learning in Digital Communication domain.	PO6

Mapping of COS and POs

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	**1**	**1**	**1**	**2**	**1**	**1**
CO2	**1**	**1**	**1**	**2**	**1**	**1**
CO3	**2**	**1**	**2**	**1**	**1**	**1**
CO4	**1**	**1**	**1**	**2**	**1**	**1**
CO5	**1**	**1**	**2**	**1**	**1**	**1**

INTERNET OF THINGS			
Course Code	**22LDE333**	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	(3:0:0)	SEE Marks	50
Total Hours of Pedagogy	40 Hours Theory	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives: This course will enable students to:

- Understand the challenges and history behind Internet of things.
- Design the network architecture and Layered structure of IoT.
- Understand the Things in IoT and the various Technologies involved.
- 4. Apply the concepts of IoT in three different use cases.

Module-1

WHAT IS IOT? Genesis, Digitization, Impact, Connected Roadways, Buildings, Challenges **IoT Network Architecture and Design** Drivers behind new network Architectures, Comparing IoT Architectures, M2M architecture, IoT world forum standard, IoT Reference Model, Simplified IoT Architecture.

RBT Level: L1, L2

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

Module-2

IOT NETWORK ARCHITECTURE AND DESIGN: Core IoT Functional Stack, Layer1 (Sensors and Actuators), Layer 2 (Communications Sublayer), Access network sublayer, Gateways and backhaul sublayer, Network transport sublayer, IoT Network management. Layer 3 (Applications and Analytics) – Analytics vs Control, Data vs Network Analytics, IoT Data Management and Compute Stack.

RBT Level: L1, L2, L3, L4

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

Module-3

ENGINEERING IOT NETWORKS: Things in IoT – Sensors, Actuators, MEMS and smart objects. Sensor networks, WSN, Communication protocols for WSN Communications Criteria, Range, Frequency bands, power consumption, Topology, Constrained Devices, Constrained Node Networks IoT Access Technologies, IEEE 802.15.4 Competitive Technologies – Overview only of IEEE 802.15.4g, 4e, IEEE 1901.2a Standard Alliances – LTE Cat 0, LTE-M, NB-IoT. **RBT Level: L1, L2, L3**

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

Module-4

ENGINEERING IOT NETWORKS: IP as IoT network layer, Key Advantages, Adoption, Optimization, Constrained Nodes, Constrained Networks, IP versions, Optimizing IP for IoT. Application Protocols for IoT – Transport Layer, Application Transport layer, Background only of SCADA, Generic web-based protocols, IoT Application Layer Data and Analytics for IoT – Introduction, Structured and Unstructured data, IoT Data Analytics overview and Challenges. **RBT Level: L1, L2, L3**

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

Module-5

IoT in Industry (Three Use cases): IoT Strategy for Connected manufacturing, Architecture for Connected Factory Utilities – Power utility, IT/OT divide, Grid blocks reference model, Reference Architecture, Primary

substation grid block and automation. Smart and Connected cities –Strategy, Smart city network Architecture, Street layer, city layer, Data center layer, services layer, Smart city security architecture, Smart Street lighting.

RBT Level: L1, L2, L3

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1.Three Unit Tests each of **20 Marks**

2.Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Books

1.'CISCO, IoT Fundamentals – Networking Technologies, Protocols, Use Cases for IoT', David Hanes, Gonzalo Salgueiro, Patrick Grossetete, Robert Barton, Jerome Henry, Pearson Education, ISBN: 978-9386873743, First edition, 2017

2.'Internet of Things – A Hands on Approach', Arshdeep Bahga and Vijay Madisetti, Orient Blackswan Private Limited - New Delhi, First edition, 2015

Web links and Video Lectures (e-Resources):

Massive Open Online Courses:

1. Introduction to Internet of Things-By Prof. Sudip Misra | IIT Kharagpur
2. An Introduction to Programming the Internet of Things-COURSERA University of California, Irvine

Skill Development Activities Suggested

- Mini projects carried out in groups based on latest trends in Industry and continue work to prepare a research Article.
- Industrial Visit or Seminar on any new topic.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Understand the basic concepts IoT Architecture and devices employed.	Understand
CO2	Analyse the sensor data generated and map it to IoT protocol stack for transport. t	Analyse
CO3	Apply communications knowledge to facilitate transport of IoT data over various available communications media	Apply
CO4	Design a use case for a typical application in real life ranging from sensing devices to analysing the data available on a server to perform tasks on the device	Apply
CO5	Apply knowledge of Information technology to design of IoT applications (Operational Technology).	Apply

Program Outcome of this course

Sl. No.	Description	POs
1	An ability to independently carry out research /investigation and development work to solve practical problems	PO1
2	An ability to write and present a substantial technical report/document	PO2
3	Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program	PO3
4	An ability to create, select, apply appropriate techniques, resources and modern tools to solve complex engineering activities with an understanding of their limitations.	PO4
5	An ability to apply Professional ethics, responsibilities and norms of the engineering.	PO5
6	An ability to recognize the need to engage in independent and life-long learning in Digital Communication and Networking domain.	PO6

Mapping of COS and POs

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	**1**	**-**	**1**	**3**	**1**	**2**
CO2	**1**	**-**	**1**	**3**	**1**	**2**
CO3	**1**	**-**	**1**	**3**	**1**	**2**
CO4	**1**	**1**	**1**	**3**	**1**	**2**
CO5	**1**	**1**	**1**	**3**	**1**	**2**

WAVELET TRANSFORMS AND APPLICATIONS			
Course Code	**22LDE334**	CIE Marks	50
Teaching Hours/Week (L:P: SDA)	(3:0:0)	SEE Marks	50
Total Hours of Pedagogy	40 Hours Theory	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives: This course will enable students:

1. 1 Classify various wavelet transform and explain importance of it.
2. Describe Continuous Wavelet Transform (CWT) and Discrete Wavelet Transform (DWT).
3. Explain the properties and application of wavelet transform.
4. Develop and realize computationally efficient wavelet-based algorithms for signal and image processing.
5. Explain brief features and strength of transform beyond wavelet. .

MODULE-1

Continuous Wavelet Transform: Continuous time frequency representation of signals, The Windowed Fourier Transform, Uncertainty Principle and time frequency tiling, Wavelets, specifications, admissibility conditions, Continuous wavelet transform, CWT as a correlation, CWT as an operator, Inverse CWT.

RBT Level: L1, L2

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE-2

Discrete wavelet Transform: Approximations of vectors in nested linear vector spaces, Example of an MRA, Formal definition of MRA, Construction of genera orthonormal MRA, a Wavelet basis for MRA, Digital filtering interpretations- Decomposition and Reconstruction filters, examples of orthogonal basis generating wavelets, interpreting orthonormal MRA for Discrete time signals, Mallat algorithm Filter bank implementation of DWT. .

RBT Level: L1, L2

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE-3

Alternative wavelet representations- Biorthogonal Wavelets: biorthogonality in vector space, biorthogonal wavelet bases, signal representation using biorthogonal wavelet system, advantages of biorthogonal wavelets, biorthogonal analysis and synthesis, Filter bank implementation, Two dimensional Wavelets, filter bank implementation of two-dimensional wavelet transform.

RBT Level: L1, L2

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE 4

Lifting scheme: Wavelet Transform using polyphase matrix factorization, Geometrical foundations of the lifting scheme, lifting scheme in the z- domain, mathematical preliminaries for polyphase factorization, Dealing with Signal Boundary.

RBT Level: L2, L3

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE 5

Applications: Image Compression: EZW Coding, SPIHT, Wavelet Difference Reduction Compression Algorithm, De-noising, speckle removal, edge detection and object isolation, audio compression, communication applications – scaling functions as signaling pulses, Discrete Wavelet Multitone Modulation. **Beyond Wavelet:** Ridge lets and curve lets: Ridge let transform and Digital Curve let transform, Curve let construction, Properties and applications.

RBT Level: L1,L2,L3

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

Assessment Details (both CIE and SEE)

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Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
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3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.

The students will have to answer five full questions, selecting one full question from each module

Textbook:

1. Wavelet Transforms –Introduction and applications - Raguveer M. Rao and Ajit S. Bopardikar- - Pearson Education, 2008

2. Insight into Wavelets from Theory to practice - K.P Soman, K. I. Ramachandran, PHI, 2006

3. Fundamentals of Wavelets: Theory, Algorithms and Applications- J C Goswamy and A K Chan, WileyInder science Publications, John Wiley and Sons, 1999.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Classify various wavelet transform and explain importance of it.	Understand
CO2	Describe Continuous Wavelet Transform (CWT) and Discrete Wavelet Transform (DWT).	Understand
CO3	Explain the properties and application of wavelet transform.	Analyze
CO4	Develop and realize computationally efficient wavelet-based algorithms for signal and image processing.	Apply
CO5	Explain brief features and strength of transform beyond wavelet.	Analyze

Program Outcome of this course

Sl. No.	Description	POs
1	An ability to independently carry out research /investigation and development work to solve practical problems	PO1
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Mapping of COS and POs

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	**2**	**1**	**1**	**1**	**2**	**1**
CO2	**1**	**1**	**1**	**2**	**1**	**1**
CO3	**2**	**1**	**2**	**1**	**1**	**1**
CO4	**1**	**1**	**1**	**2**	**1**	**1**
CO5	**1**	**1**	**2**	**1**	**1**	**1**

ADVANCED COMMUNICATION SYSTEM			
Course Code	**22LDE335**	CIE Marks	50
Teaching Hours/Week (L:P: SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40 Hours Theory	Total Marks	100
Credits	04	Exam Hours	03

Course Learning objectives: This course will enable students:

- To know modulation techniques.
- To study the demodulation techniques.
- To Have an in-depth knowledge of band limited channels and equalizers
- To understand spread spectrum.

MODULE-1

Signal Representation: Low pass representation of bandpass signals, Low pass representation of bandpass random process [Text 1, Chapter 2:2.1, and 2.9 only]. **Modulation**: Representation of digitally modulated Signals, Modulation Schemes without memory (Band Limited Schemes - PAM, BPSK, QPSK, MPSK, MQAM, Power Limited Schemes – FSK, MFSK, DPSK, DQPSK), modulation schemes with memory (Basics of CPFSK and CPM – Full Treatment of MSK), Transmit PSD for Modulation Schemes. **RBT Level: L1, L2**

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE-2

Demodulation: Vector Channel, Vector Channel +AWGN, Performance parameters, Optimum Coherent Detection for power limited and Bandlimited schemes, Optimal Coherent detection for schemes with memory, Optimal Non– Coherent detection for schemes without and with memory (FSK, DPSK, DQPSK), Comparison of detection schemes. **RBT Level: L1, L2**

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE-3

Bandlimited Channels: Bandlimited channel characterization, signaling through band limited linear filter channels, Sinc, RC, Duobinary and Modified Duobinary signaling schemes, Optimum receiver for channel with ISI and AWGN. **Linear Equalizers**: Zero forcing Equalizer, MSE and MMSE, Baseband and Passband Linear Equalizers. Performance of ZFE and MSE.

RBT Level: L1, L2, L3, L4

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE 4

Non-Linear Equalizers: Decision - feedback equalization, Predictive DFE, Performance of DFE [.

Adaptive equalization: Adaptive linear equalizer, adaptive decision feedback equalizer, Adaptive Fractionally spaced Equalizer (Tap Leakage Algorithm), Adaptive equalization of Trellis - coded signals.

RBT Level: L3, L4

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

MODULE 5

Spread spectrum signals for digital communication: Model of spread spectrum digital communication system, Direct sequence spread spectrum signals, some applications of DS spread spectrum signals, generation of PN sequences, Frequency hopped spread spectrum signals, Time hopping SS, Synchronization of SS systems. **RBT Level: L3,L4**

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

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The students will have to answer five full questions, selecting one full question from each module.

Textbook:

'Digital Communications', John G. Proakis, Masoud Salehi, Pearson Education, ISBN:978-9332535893, 5th edition, 2014

Reference Books:

1. 'Digital Communications: Fundamentals and Applications: Fundamentals & Applications', Bernard Sklar, Pearson Education, ISBN:9788131720929, 2nd edition, 2009

2. 'Digital Communications Systems', Simon Haykin, Wiley, ISBN:9788126542314, 1st edition, 2014

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Ability to explain the concept of low pass and Bandpass signals representations at the Transmitter, the process of Detection and Estimation at the receiver in the presence of AWGN only.	Explain
CO2	Able to Evaluate Receiver performance for various types of single carrier symbol modulations through ideal and AWGN Non-bandlimited and bandlimited channels.	Understand
CO3	Analyze and demonstrate the model of discrete time channel with ISI & the model of discrete time channel by equalizer.	Analyze
CO4	Design single carrier equalizers for various symbol modulation schemes and detection methods for defined channel models, and compute parameters to meet desired rate and performance requirements.	Analyze
CO5	Design and Evaluate Non band limited and Non power limited spread spectrum systems for communications in a Jamming environment, multiuser situation and low power intercept environment.	Design and analyze

Program Outcome of this course

Sl. No.	Description	POs
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Mapping of COS and POs

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CO1	**1**	**1**	**1**	**2**	**1**	**1**
CO2	**1**	**1**	**1**	**2**	**1**	**1**
CO3	**2**	**1**	**2**	**2**	**1**	**1**
CO4	**1**	**1**	**1**	**2**	**1**	**1**
CO5	**1**	**1**	**1**	**2**	**1**	**1**