Digital VLSI Design			
Course Code	22LEL12	CIE Marks	50
Teaching Hours/Week (L:P: SDA)	3:0:2	SEE Marks	50
Total Hours of Pedagogy	25 Hours Theory and 10 -12 Practical Sessions	Total Marks	100
Credits	04	Exam Hours	04

Course Learning Objectives:

- To understand the operation of MOS transistor, Scaling and Small Geometry Effects.
- To study Static Characteristics, Switching Characteristics and Interconnect Effect of MOS Inverter.
- To provide the insight of Semiconductor Memories, Dynamic Logic Circuits and BiCMOS Logic Circuits.
- To know Chip Input and Output Circuits, Clock Generation and Distribution Circuits, Design for Manufacturability.

Module-1

MOS Transistor: The Metal Oxide Semiconductor (MOS) Structure, The MOS System under External Bias, Structure and Operation of MOS Transistor, MOSFET Current-Voltage Characteristics, MOSFET Scaling and Small-Geometry Effects.

Teaching-Learning Process	Chalk and Talk, Power Point Presentations.

Module-2

MOS Inverters-Static Characteristics: Introduction, Resistive-Load Inverter, Inverters with n_Type MOSFET Load, CMOS Inverter.

Teaching-Learning Process	Chalk and Talk / Power Point Presentations.

Module-3

Dynamic Logic Circuits: Introduction, Basic Principles of Pass Transistor Circuits, Voltage Bootstrapping, Synchronous Dynamic Circuit Techniques, Dynamic CMOS Circuit Techniques, High Performance Dynamic CMOS circuits.

Teaching-Learning Process	Chalk and Talk / Power Point Presentations.

Module-4

Semiconductor Memories: Introduction, Dynamic Random-Access Memory (DRAM), Static Random-Access Memory (SRAM).

Teaching-Learning Process	Chalk and Talk / Power Point Presentations.

Module-5

BiCMOS Logic Circuits: Introduction, BiCMOS Applications.
Chip Input and Output (I/O) Circuits: Introduction, ESD Protection, On-Chip Clock Generation and Distribution, Latch-Up and Its Prevention.

Teaching-Learning Process	Chalk and Talk / Power Point Presentations.

Practical Component of IPCC: Conduct the experiments using Cadence/ Mentor Graphics / Xilinx ISE System Edition 14.7/ XUP SPARTAN 3E Kit with USB Programming cable

Sl. No.	Experiments
1	To plot the (i) output characteristics & (ii) transfer characteristics of an n-channel and p-channel MOSFET.
2	To design and plot the static (VTC) and dynamic characteristics of a digital CMOS inverter.
3	To design and plot the dynamic characteristics of 2-input NAND, NOR, XOR and XNOR logic gates using CMOS technology.
4	To design and plot the characteristics of a 4x1 digital multiplexer using pass transistor logic.
5	To design and plot the characteristics of a positive and negative latch based on multiplexers.
6	To design and plot the characteristics of a master-slave positive and negative edge triggered registers based on multiplexers
7	To Design D, T, JK Flip Flops
8	To Design BCD adder
9	To Design ALU

Assessment Details (both CIE and SEE)
The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark

for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

.

Suggested Learning Resources:

Books

1. "Sung Mo Kang & Yusuf Leblebici", CMOS Digital Integrated Circuits: Analysis and Design, Tata McGraw-Hill, Third Edition.
2. "Neil Weste and K. Eshraghian", Principles of CMOS VLSI Design: A System Perspective Pearson Education (Asia) Pvt. Ltd. Second Edition, 2000.
3. "Wayne, Wolf", Modern VLSI Design: System on Silicon, Prentice Hall PTR/ Pearson Education Second Edition, 1998
4. "Douglas A Pucknell& Kamran Eshraghian", Basic VLSI Design PHI 3rd Edition

Web links and Video Lectures (e-Resources):

1. https://www.youtube.com/watch?v=57uTCtSQV50&list=PLHO2NKv71TvsSqYwVvUCZwNkY-jUyUHdS
2. https://www.youtube.com/watch?v=oL8SKNxEaHs&list=PLLy_2iUCG87Bdulp9brz9AcvW_TnFCUmM

Skill Development Activities Suggested:

1. Interact with industry (small, medium, and large).
2. Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3. Involve in case studies and field visits/ fieldwork.
4. Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5. Handle advanced instruments to enhance technical talent.
6. Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7. Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc.

Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical – activities which will enhance their skill. The prepared report shall be evaluated for CIE marks.

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

Sl. No.	Description	Blooms Level
CO1	Analyse issues of On-chip interconnect Modelling and Interconnect delay calculation.	L4
CO2	Analyse the Switching Characteristics in Digital Integrated Circuits.	L4
CO3	Use the Dynamic Logic circuits in state-of-the-art VLSI chips.	L3
CO4	Interpret critical issues such as ESD protection, Clock distribution, Clock buffering, and Latch phenomenon	L2
CO5	Use Bipolar and Bi-CMOS circuits in very high-speed design.	L3

Advanced Embedded System			
Course Code	22LEL13	CIE Marks	50
Teaching Hours/Week (L:P: SDA)	2:0:2	SEE Marks	50
Total Hours of Pedagogy	25 Hours of teaching and 10-12 sessions for Skill Development Activities	Total Marks	100
Credits	3	Exam Hours	03

Course Learning Objectives:

- To understand the concepts of embedded system design.
- To learn real design challenges of the system under development.
- To gain the essential knowledge required to design practical real-time embedded systems and appropriate real-time operating system (RTOS) product to be used.
- To know networking aspects of the embedded systems and Hardware-Software Co-design.

Module-1

Introduction of Embedded System: Embedded System: Embedded vs General computing system, classification, application and purpose of ES.
Typical of Embedded System: Communication Interface
The Strategy: Definition, Common Characteristics, Some Quality Metrics in ES Design, Versatility Factors for ES Product, Technologies Involved (Processors, Platforms, Devices-IC Technology), Hardware/Software Co-design
Use Cases: What Are Use Cases, Casual Versus Structured Version, Black Box Versus White Box, Hub and Spoke Model,
Details of the Use Case Model Entities (Actor, Stakeholder, Primary Actor, Supporting Actor, Scope, Scenarios, Levels, Use Case Entities and Their Relation, When Are We Done, Standard Use Case Template)

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-2

Models and Architectures: Representation of a Design, Model Taxonomy, Finite-State Machine (Mealy) Model, Petri Nets, Hierarchical Concurrent FSMs, Activity-Oriented Data Flow Graphs, Control Flow Graphs (Flowchart), Structure-Oriented Models, Data-Oriented Entity-Relationship Model, Jackson's Structured Programming Model, Heterogeneous Models

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-3

Specification Languages: SystemC: Characteristics of ESL for Embedded Systems, SystemC, Processes.
UML for Embedded Systems: Motivation, Typical Tasks and Roles in System Engineering, UML Diagrams, Structural Diagrams, Behavioural Diagrams

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-4

Real-Time Systems: Definition and Examples, Broad Classification of RTS, Terms in RT Systems, Periodic Schedule, Precedence Constraints and Dependencies, Scheduling Algorithms–Classification, Clock-Driven Scheduling, Priority-Driven Periodic Tasks, Dynamic Priority Algorithms, Scheduling Sporadic Jobs, Resource Access and Contention.
Real-Time Operating Systems (RTOS): Introduction, RTOS Concepts, Basic Design Using RTOS Case Study 1, Concept-Process and Threads.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-5

Real-Time Operating Systems (RTOS): Posix, pThreads, Thread Synchronization, Design Strategies
Networked Embedded Systems (NES): Introduction, Characteristics, Broad Segments of NES, Automotive NES, CAN (Controller Area Network).
HW-SW Co-design: Introduction, Factors Driving Co-design, Co-design Problems, Conventional Model for HW-SW Design Process, Integrated Co-design Process, System Partitioning, Partitioning Algorithms.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Assessment Details (both CIE and SEE)
The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark

for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

.

Suggested Learning Resources:

Books

1. (Transactions on computer systems and networks) k. c. s. murti - design principles for embedded systems-springer (2022)
2. Introduction to embedded systems K. V. Shibu TMH education Pvt. Ltd. 2009
3. Embedded systems - A contemporary design tool James K. Peckol John Wiley 2008
4. The Definitive Guide to the ARM Cortex-M3 Joseph Yiu Newnes, (Elsevier) 2 ndedn, 2010.

Web links and Video Lectures (e-Resources):

1. https://youtu.be/GaZBpY9Ys1Y
2. https://youtu.be/SUusup7FfJo
3. https://youtu.be/dHsHP9RrXBw?list=PLJ5C_6qdAvBH-JNRIlupFb44miyx9M8JD
4. https://youtu.be/vn7aT9-cYzQ
5. https://youtu.be/-rWGzFDLnAY

Skill Development Activities Suggested:

1. Interact with industry (small, medium, and large).
2. Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3. Involve in case studies and field visits/ fieldwork.
4. Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5. Handle advanced instruments to enhance technical talent.
6. Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7. Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc.

Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical – activities which will enhance their skill. The prepared report shall be evaluated for CIE marks.

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

Sl. No.	Description	Blooms Level
CO1	Design and Develop Embedded Systems with hardware software co-design.	L3
CO2	Analyze different models and architecture of the Embedded Systems and Networked Embedded Systems	L4
CO3	Verify the performance of RTS and RTOS	L3, L4

Digital Circuits and Logic Design			
Course Code	22LEL14	CIE Marks	50
Teaching Hours/Week (L:P: SDA)	2:0:2	SEE Marks	50
Total Hours of Pedagogy	25 Hours of teaching and 10-12 sessions for Skill Development Activities	Total Marks	100
Credits	3	Exam Hours	03

Course Learning objectives:

- Understand the concepts of sequential machines.
- Design Sequential Machines/Circuits.
- Analyze the faults in the design of circuits.
- Apply fault detection experiments to sequential circuits.
- Comprehend the structure of sequential machines

Module-1

Threshold Logic: Introductory Concepts, Synthesis of Threshold Networks, Capabilities, Minimization, and Transformation of Sequential Machines: The Finite- State Model, Further Definitions, Capabilities.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-2

Fault Detection by Path Sensitizing, Detection of Multiple Faults, Failure-Tolerant Design, Quadded Logic, Reliable Design and Fault Diagnosis Hazards: Fault Detection in Combinational Circuits.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-3

Fault-Location Experiments, Boolean Differences, Limitations of Finite – State Machines, State Equivalence and Machine Minimization, Simplification of Incompletely Specified Machines.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-4

Structure of Sequential Machines: Introductory Example, State Assignments Using Partitions, The Lattice of closed Partitions, Reductions of the Output Dependency, Input Independence and Autonomous Clocks, Covers and Generation of closed Partitions by state splitting, Information Flow in Sequential Machines, decompositions, Synthesis of Multiple Machines.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-5

Homing Experiments, Distinguishing Experiments, Machine Identification, Fault Detection Experiments, Design of Diagnosable Machines, Second Algorithm for the Design of Fault Detection Experiments, Fault-Detection.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks**

to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Textbook:

'Switching and Finite Automata Theory', Zvi Kohavi, TMH, ISBN: 978_0_07_099387_7, 2ndEdition, 2008.

Reference Books:

1. 'Digital Circuits and logic Design', Charles Roth Jr., Cengage Learning, 7thedition, 2014.
2. 'Fault Tolerant and Fault Testable Hardware Design', Parag K Lala, Prentice Hall Inc. 1985.
3. 'Introductory Theory of Computer', E. V. Krishnamurthy, Macmillan Press Ltd, 1983
4. 'Theory of computer science – Automata, Languages and Computation', Mishra & Chandrasekaran, 2ndEdition, PHI, 2004.

Skill Development Activities Suggested:

1. Interact with industry (small, medium, and large).
2. Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3. Involve in case studies and field visits/ fieldwork.
4. Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5. Handle advanced instruments to enhance technical talent.
6. Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7. Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc.

Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical – activities which will enhance their skill. The prepared report shall be evaluated for CIE marks.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Understand the concepts of sequential machines.	L2
CO2	Design Sequential Machines/Circuits.	L3
CO3	Analyze the faults in the design of circuits.	L4
CO4	Apply fault detection experiments to sequential circuits.	L3
CO5	Understand the structure of sequential machines.	L2

WIRELESS SENSOR NETWORKS			
Course Code	22LEL15	CIE Marks	50
Teaching Hours/Week (L:P: SDA)	2:0:2	SEE Marks	50
Total Hours of Pedagogy	25 Hours of teaching and 10-12 sessions for Skill Development Activities	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives: This course will enable students to:

- Learn the basic concepts of Wireless sensor networks architecture and protocols.
- Understand the challenges in designing a Wireless sensor network.
- Understand the function of Data link and Network layer Protocols.
- Understand the function of Transport layer Protocols.
- Analyze wireless sensor network system for different applications under consideration

Module-1

INTRODUCTION: Sensor Mote Platforms, WSN Architecture and Protocol Stack.
WSN Applications: Military Applications, Environmental Applications, Health Applications, Home Applications, Industrial Applications.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-2

FACTORS INFLUENCING WSN DESIGN: Hardware Constraints Fault Tolerance Scalability Production Costs WSN Topology, Transmission Media, Power Consumption.
Physical Layer: Physical Layer Technologies, Overview of RF Wireless Communication, Channel Coding (Error Control Coding), Modulation, Wireless Channel Effects, PHY Layer Standards.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-3

MEDIUM ACCESS CONTROL: Challenges for MAC, CSMA Mechanism, Contention-Based Medium Access, Reservation-Based Medium Access, Hybrid Medium Access.
Network Layer: Challenges for Routing, Data-centric and Flat Architecture Protocols, Hierarchical Protocols, Geographical Routing Protocols.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-4

Transport Layer: Challenges for Transport Layer, Reliable Multi Segment Transport (RMST) Protocol, Pump Slowly, Fetch Quickly (PSFQ) Protocol, Congestion Detection and Avoidance (CODA) Protocol, Event-to-Sink Reliable Transport (ESRT) Protocol, GARUDA
Application Layer: Source Coding (Data Compression), Query Processing, Network Management.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-5

SPREAD SPECTRUM SIGNALS FOR DIGITAL COMMUNICATION: Model of spread spectrum digital communication system, Direct sequence spread spectrum signals, some applications of DS spread spectrum signals, generation of PN sequences, Frequency hopped spread spectrum signals, Time hopping SS, Synchronization of SS systems.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks**

to attain the Cos and Pos

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Text Books

1. Wireless Sensor Networks', Ian F. Akyildiz and Mehmet Can Vuran, John Wiley & Sons Ltd. ISBN 978-0-470-03601-3 (H/B), 2010
2. 'Wireless Sensor Networks: Signal Processing and Communications Perspectives', Ananthram Swami, et. Al., John Wiley & Sons Ltd., ISBN 978-0470-03557-3, 2007.

Massive Open Online Courses:

https://archive.nptel.ac.in/courses/106/105/106105160/#- **Wireless** Ad Hoc and **Sensor Networks** -BY Prof. SUDIP MISHRA,IITKGP

Skill Development Activities Suggested:

1. Interact with industry (small, medium, and large).
2. Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3. Involve in case studies and field visits/ fieldwork.
4. Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5. Handle advanced instruments to enhance technical talent.
6. Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7. Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc.

Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical – activities which will enhance their skill. The prepared report shall be evaluated for CIE marks.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Understand challenges and technologies for wireless networks	L2
CO2	Understand architecture and sensors	L2
CO3	Describe the communication, energy efficiency, computing, storage and transmission	L4
CO4	Establishing infrastructure and simulations	L4
CO5	Explain the concept of programming in the WSN environment	L3

Research Methodology and IPR			
Course Code	22RMI16	CIE Marks	50
Teaching Hours/Week (L:P: SDA)	2:0:2	SEE Marks	50
Total Hours of Pedagogy	25 Hours Teaching and 10-12 hours a Skill activities	Total Marks	100
Credits	3	Exam Hours	03

Course Learning Objectives:

- To study an overview of the research methodology and explain the technique of defining a research problem.
- To understand ways of carrying out a literature search, its review, developing theoretical and conceptual frameworks and writing a review.
- To study various research designs and their characteristics, different methods of data collection.
- To know different parametric tests of hypotheses, Chi-square test, art of interpretation and writing research reports.
  To gain the knowledge on Intellectual Property Rights.

Module-1

Research Methodology: Introduction, Meaning of Research, Objectives of Research, Motivation in Research, Types of Research, Research Approaches, Significance of Research, Research Methods versus Methodology, Research and Scientific Method, Importance of Knowing How Research is Done, Research Process, Criteria of Good Research, and Problems Encountered by Researchers in India.

Defining the Research Problem: Research Problem, Selecting the Problem, Necessity of Defining the Problem, Technique Involved in Defining a Problem, An Illustration.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentation

Module-2

Reviewing the literature: Place of the literature review in research, Bringing clarity and focus to your research problem, Improving research methodology, Broadening knowledge base in research area, Enabling contextualfindings, How to review the literature, searching the existing literature, reviewing the selected literature, Developing a theoretical framework, Developing a conceptual framework, Writing about the literature reviewed.

Research Design: Meaning of Research Design, Need for Research Design, Features of a Good Design, Important Concepts Relating to Research Design, Different Research Designs, Basic Principles of Experimental Designs, Important Experimental Designs.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentation

Module-3

Design of Sampling: Introduction, Sample Design, Sampling and Non-sampling Errors, Sample Survey versus Census Survey, Types of Sampling Designs.

Measurement and Scaling: Qualitative and Quantitative Data, Classifications of Measurement Scales, Goodness of Measurement Scales, Sources of Error in Measurement Tools, Scaling, Scale Classification Bases, Scaling Techniques, Multidimensional Scaling, Deciding the Scale.

Data Collection: Experimental and Surveys, Collection of Primary Data, Collection of Secondary Data, Selection of Appropriate Method for Data Collection, Case Study Method.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentation

Module-4

Testing of Hypotheses: Hypothesis, Basic Concepts Concerning Testing of Hypotheses, Testing of Hypothesis, Test Statistics and Critical Region, Critical Value and Decision Rule, Procedure for Hypothesis Testing, Hypothesis Testing for Mean, Proportion, Variance, for Difference of Two Mean, for Difference of Two Proportions, for Difference of Two Variances, P-Value approach, Power of Test, Limitations of the Tests of Hypothesis.

Chi-square Test: Test of Difference of more than Two Proportions, Test of Independence of Attributes, Test of Goodness of Fit, Cautions in Using Chi Square Tests.

Interpretation and Report Writing: Meaning of Interpretation, Technique of Interpretation, Precaution in Interpretation, Significance of Report Writing, Different Steps in Writing Report, Layout of the Research Report, Types of Reports, Oral Presentation, Mechanics of Writing a Research Report, Precautions for Writing Research Reports.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentation

Module-5

Intellectual Property: The Concept, Intellectual Property System in India, Development of TRIPS Complied Regime in India, Patents Act, 1970, Trade Mark Act, 1999,The Designs Act, 2000, The Geographical Indications of Goods (Registration and Protection) Act1999, Copyright Act,1957,The Protection of Plant Varieties and Farmers' Rights Act, 2001,The Semi-Conductor Integrated Circuits Layout Design Act, 2000, Trade Secrets, Utility Models, IPR and Biodiversity, The Convention on Biological Diversity (CBD) 1992, Competing Rationales for Protection of IPRs, Leading International Instruments Concerning IPR, World Intellectual Property Organization (WIPO),WIPO and WTO, Paris Convention for the Protection of Industrial Property, National Treatment, Right of Priority, Common Rules, Patents, Marks, Industrial Designs, Trade Names, Indications of Source, Unfair Competition, Patent Cooperation Treaty (PCT), Advantages of PCT Filing, Berne Convention for the Protection of Literary and Artistic Works, Basic Principles, Duration of Protection, Trade Related Aspects of Intellectual Property Rights(TRIPS) Agreement, Covered under TRIPS Agreement, Features of the Agreement, Protection of Intellectual Property under TRIPS, Copyright and Related Rights, Trademarks, Geographical indications, Industrial Designs, Patents, Patentable Subject Matter, Rights Conferred, Exceptions, Term of protection, Conditions on Patent Applicants, Process Patents, Other Use without Authorization of the Right Holder, Layout-Designs of Integrated Circuits, Protection of Undisclosed Information, Enforcement of Intellectual Property Rights, UNSECO.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentation

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

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Suggested Learning Resources:

Text Books

1. C.R. Kothari, Gaurav Garg, "Research Methodology: Methods and Techniques", New Age International, 4th Edition, 2018.
2. Ranjit Kumar, "Research Methodology a step-by-step guide for beginners", SAGE Publications, 3rd Edition, 2011 (For the topic Reviewing the literature under module 2)
3. Study Material - Professional Programme Intellectual Property Rights, Law and Practice, The Institute of Company Secretaries of India, Statutory Body Under an Act of Parliament, September 2013. (For the topic Intellectual Property under module 5)

Reference Books:

1. Trochim, "Research Methods: the concise knowledge base", Atomic Dog Publishing, 2005.
2. Fink A, "Conducting Research Literature Reviews: From the Internet to Paper", Sage Publications, 20112009.

Web links and Video Lectures (e-Resources):

1. https://archive.nptel.ac.in/courses/127/106/127106227/
2. https://www.youtube.com/watch?v=GSeeyJVD0JU

Skill Development Activities Suggested:

1. Interact with industry (small, medium, and large).
2. Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3. Involve in case studies and field visits/ fieldwork.
4. to the use of standards/codes etc., to narrow the gap between academia and industry.
5. Handle advanced instruments to enhance technical talent.
6. Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7. Accustom Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc.

Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical –activities which will enhance their skill. The prepared report shall be evaluated for CIE marks.

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

Sl. No.	Description	Blooms Level
CO1	Discuss research methodology and the technique of defining a research problem.	L1, L2
CO2	Explain the functions of the literature review in research, carrying out a literature search, developing theoretical and conceptual frameworks and writing a review.	L1, L2
CO3	Explain various research designs, sampling designs, measurement and scaling techniques and also different methods of data collections.	L1, L2
CO4	Explain several parametric tests of hypotheses, Chi-square test, art of interpretation and writing research reports.	L1, L2, L3
CO5	Discuss various forms of the intellectual property, its relevance and business impact in the changing global business environment and leading International Instruments concerning IPR.	L1, L2, L3, L4

Embedded Systems Lab			
Course Code	22LELL17	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	1:2:0	SEE Marks	50
Total Hours of Pedagogy	13 Hours of teaching and 10-13 Practical sessions	Total Marks	100
Credits	2	Exam Hours	03

Part A: EDA Using Cadence OrCAD or OrCAD Lite or any EDA Tool,design and verify the following:

Sl. No.	Experiments
1	3½ Digit Digital Voltmeter
2	Monolithic function Generator
3	Regulated Power supplies
4	Batch counter using TTL ICs
5	DAC and ADC
6	P, PI, PID and ON/OFF Controllers
7	Programmable Timers
8	Filters and Resonance Circuits

PART-B: ARM-CORTEX M3 [Programming to be done using Keil uVision 4 and download the program on to M3 evaluation board such as NXP LPC1768 or ATMEL ATSAM3U]

Sl. No.	Experiments
1	Write an Assembly language program to calculate 10+9+8+…..+1
2	Write an Assembly language program to link Multiple object filesand link them together.
3	Write an Assembly language program to store data in RAM.
4	Write a C program to Output the "Hello World" message usingUART.
5	Write a C program to Design a Stopwatch using interrupts.
6	Write an Exception vector table in C
7	Write an Assembly Language Program for locking a Mutex.
8	Write a SVC handler in C. Use the wrapper code to extract the correct stack frame starting location. The C handler can then use this to extract the stacked PC location and the stacked register values.

Course outcomes:

At the end of the course the student will be able to:

1. Understand the computer aided design tools for the electronic circuitdesigns.
2. Design and verify analog circuits such as ADC, DAC, Controllers, etc.using simulation tools
3. Create and verify digital systems using Cadence OrCAD, OrCAD Lite orany EDA tool.
4. Develop assembly programs for different applications using ARM CortexM3 and Keil uVision-4 tool.
5. Develop C Programs for different applications using ARM-Cortex M3 andKeil uVision-4 tool.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 40% of maximum marks in the semester-end examination (SEE). In total of CIE and SEE student has to secure 50% maximum marks of the course.

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the

journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.

- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of the semester and the second test shall be conducted after the 14th week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University.

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 10% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours

BOS Recommended ONLINE Courses

Sl. No.	Course code	Course Title	National Coordinator	Instructor
1	22AUD18/ 22AEC18	Design Thinking - A Primer (4 Weeks)	NPTEL	Prof. Ashwin Mahalingam, Prof. Bala Ramadurai IIT Madras
2		Computer Networks and Internet Protocol (12 Weeks)	NPTEL	Prof. Soumya Kanti Ghosh & Prof. Sandip Chakraborty IITKGP
3		Advanced IOT Applications (8 Weeks)	NPTEL	Prof. T V Prabhakar IISc
4		Spread Spectrum Communications and Jamming (12 Weeks)	NPTEL	Prof. Debarati Sen IITKGP
5		Optical Wireless Communications for Beyond 5G Networks and IoT (12 Weeks)	NPTEL	Prof. Anand Srivastava IIITD
6		Employment Communication A Lab based course (8 Weeks)	NPTEL	Prof. Seema Singh IIT KGP
7		Embedded System Design with ARM (8 Weeks)	NPTEL	Prof. Indranil Sengupta and Kamalika Dutta IITKGP

ASIC Design

Course Code	22LEL21	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	2:0:2	SEE Marks	50
Total Hours of Pedagogy	25 Hours of teaching and 10-12 sessions for Skill development activities	Total Marks	100
Credits	3	Exam Hours	03

Course Learning objectives:

- To learn ASIC methodologies and programmable logic cells.
- To analyse physical design flow, including partitioning, floor-planning, placement and routing.
- To gain sufficient knowledge for carrying out ASIC designs.

Module-1

Introduction to ASICs: Full custom, Semi-custom and Programmable ASICs, ASIC Design flow, ASIC cell libraries.
CMOS Logic: Data path Logic Cells: Data Path Elements, Data path Operators, Cell Compilers.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-2

ASIC Library Design: Logical effort: Logical area and logical efficiency, Logical paths, Multi stage cells.
Programmable ASIC Logic Cells: Acted ACT: ACT 1, ACT 2 and ACT 3 Logic Modules, Xilinx LCA: XC3000 CLB, Programmable ASIC I/O Cells: Xilinx I/O Block.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-3

Low-level Design Entry: Schematic entry: Hierarchical design, The cell library, Names, Schematic Icons & Symbols, Nets, Connections, vectored instances & buses, Edit in place, attributes, Netlist screener.
ASIC Construction: Physical Design, CAD Tools.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-4

Partitioning: Goals and objectives, Constructive Partitioning, Iterative Partitioning Improvement., KL algorithm.
Floor planning: Goals and objectives, Measurement of delay in Floor planning.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-5

Placement: Goals and Objectives, Min-cut Placement algorithm, Iterative Placement Improvement.
Routing: Global Routing: Goals and objectives, Global routing between blocks. Detailed Routing: Goals and objectives, Left-Edge Algorithm, Special Routing, Circuit extraction and DRC.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks**

to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.

3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Text Books

1. Michael John Sebastian Smith, "Application - Specific Integrated Circuits", Addison- Wesley Professional, 2005.
2. Neil H.E. Weste, David Harris, and Ayan Banerjee, "CMOS VLSI Design: A Circuits and Systems Perspective", 3rd edition, Addison Wesley/ Pearson education, 2011.
3. Vikram Arkalgud Chandrasetty, "VLSI Design: A Practical Guide for FPGA and ASIC Implementations", Springer, 2011, ISBN: 978-1-4614-1119-2.
4. Rakesh Chadha, Bhasker J., "An ASIC Low Power Primer", Springer, ISBN: 978-1-4614-4270-7.

Web links and Video Lectures (e-Resources):

1. https://www.youtube.com/watch?v=oZSv68esbgI
2. https://www.youtube.com/watch?v=4cPkr1VHu7Q
3. https://nptel.ac.in/courses/106105161

Skill Development Activities Suggested

1. Interact with industry (small, medium, and large).
2. Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3. Involve in case studies and field visits/ fieldwork.
4. Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5. Handle advanced instruments to enhance technical talent.
6. Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7. Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc.

Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical – activities which will enhance their skill. The prepared report shall be evaluated for CIE marks.

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

Sl. No.	Description	Blooms Level
CO1	Describe the concepts of ASIC design methodology, data path elements, logical effort.	L1, L2
CO2	Analyze the design of ASICs suitable for specific tasks, perform design entry and explain the physical design flow.	L2, L3
CO3	Design data path elements for ASIC cell libraries and compute optimum path delay.	L3
CO4	Create floor plan including partition and routing with the use of CAD algorithms.	L3
CO5	Design CAD algorithms and explain how these concepts interact in ASIC design.	L2, L3

Advanced Digital Signal Processing			
Course Code	22LEL22	CIE Marks	50
Teaching Hours/Week (L:P: SDA)	3:2:0	SEE Marks	50
Total Hours of Pedagogy	25 Hours of teaching and 10-12 Practical sessions	Total Marks	100
Credits	4	Exam Hours	03

Course Learning objectives: This course will enable students:

- To Know the analysis of discrete time signals.
- To study the modern digital signal processing algorithms and applications.
- To Have an in-depth knowledge of use of digital systems in real time applications
- To Apply the algorithms for wide area of recent applications.

Module-1

Introduction to Digital Signal Processing: Review of Discrete time signals and systems and frequency analysis of discrete time linear time invariant systems, implementation of discrete time systems, correlation of discrete time systems Sampling, decimation by a factor 'D', Interpolation by a factor 'I', sampling rate conversion by a factor 'I/D', Implementation of sampling rate conversion, Multistage implementation of sampling rate conversion.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-2

Multirate Digital Signal Processing: Multirate signal processing and its applications, Design of Digital filters, Design of FIR filters, Design of IIR filters, frequency transformations, Digital filter banks, two channel quadrature mirror filter banks.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-3

Linear prediction and Optimum Linear Filters: Random signals, Correlation Functions and Power Spectra, Innovations Representation of a Stationary Random Process. Forward and Backward Linear Prediction. Solution of the Normal Equations. The Levinson-Durbin Algorithm. Properties of the Linear Prediction-Error Filters.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-4

Adaptive filters: Applications of Adaptive Filters-Adaptive Channel Equalization, Adaptive noise cancellation, Linear Predictive coding of Speech Signals, Adaptive direct form FIR filters-The LMS algorithm, Properties of LMS algorithm. Adaptive direct form filters- RLS algorithm.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-5

Power Spectrum Estimation:
Non parametric Methods for Power Spectrum Estimation - Bartlett Method, Welch Method, Blackman &Tukey Methods.
Parametric Methods for Power Spectrum Estimation: Relationship between the auto correlation and the model parameters, Yule and Walker methods for the AR Model Parameters, Burg Method for the AR Model parameters, Unconstrained least-squares method for the AR Model parameters, Sequential estimation methods for the AR Model parameters, ARMA Model for Power Spectrum Estimation.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Practical Component of IPCC: Conduct the experiments using MATLAB/Scilab/TMS 320 C5X DSP Processors

Sl. No.	**Experiments**
1.	Generate various fundamental discrete time signals
2.	Basic operations on signals (Multiplication, Folding, Scaling).
3.	Find out the DFT & IDFT of a given sequence without using inbuilt instructions.
4.	Interpolation & decimation of a given sequence.
5.	Generation of DTMF (Dual Tone Multiple Frequency) signals
6.	Estimate the PSD of a noisy signal using periodogram and modified periodogram

7.	Estimation of PSD using different methods (Bartlett, Welch, Blackman-Tukey).
8.	Design of Chebyshev Type I, II Filters.
9.	Cascade Digital IIR Filter Realization.
10.	Parallel Realization of IIR filter.
11.	Estimation of power spectrum using parametric methods (YuleWalker &Burg).
12.	Time-Frequency Analysis with the Continuous Wavelet Transform.
13.	Signal Reconstruction from Continuous Wavelet Transform Coefficients.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIEis 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

CIE for the theory component of IPCC

1. Two Tests each of **20 Marks**
2. Two assignments each of **10 Marks/One Skill Development Activity of 20 marks**
3. Total Marks of two tests and two assignments/one Skill Development Activity added will be CIE for 60 marks, marks scored will beproportionally scaled down to **30 marks**.

CIE for the practical component of IPCC

- On completion of every experiment/program in the laboratory, the students shall be evaluated and marks shall be awarded on the same day. The **15 marks** are for conducting the experiment and preparation of the laboratory record, the other **05 marks shall be for the test** conducted at the end of the semester.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments‟ write-ups are added and scaled down to 15 marks.
- The laboratory test at the end /after completion of all the experiments shall be conducted for 50 marks and scaled down to 05 marks**.**

Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **20 marks**.**SEE for IPCC**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (duration 03 hours)

The question paper will be set for 100 marks and marks scored will be scaled down proportionately to 50 marks.

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of sub-questions), **should have amix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questionsmentioned in the SEE paper shall include questions from the practical component).

1. The minimum marks to be secured in CIE to appear for SEE shall be the 15 (50% of maximum marks-30) in the theory component and 10 (50% of maximum marks -20) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included**.** The maximum of 04/05 questions to be set from the practical componentof IPCC, the total marks of all questions should not be more than the 20 marks.
2. SEE will be conducted for 100 marks and students shall secure 40% of the maximum marks to qualify in the SEE. Marks secured will bescaled down to 50. (Student has to secure an aggregate of 50% of maximum marks of the course (CIE+SEE)

Suggested Learning Resources:

Text Books

1. Digital Signal Processing Principles, Algorithms, and Applications by John G. Proakis, Prentice-Hall International Inc., 4th Edition, 2012.
2. Theory and Application of Digital Signal Processing by Lawrence R. Rabiner and Bernard Gold.

Reference Books

1. Oppenheim, Alan V. Discrete-time signal processing. Pearson Education India, 1999.
2. Mitra, Sanjit Kumar, and Yonghong Kuo. Digital signal processing: a computer-based approach. Volume 2. New York: McGraw-Hill Higher Education, 2006.

Web links and Video Lectures (e-Resources):

1. https://ekeeda.com/degree-courses/electrical-engineering/advanced-digital-signal-processing
2. https://dss-kiel.de/index.php/teaching/lectures/lecture-advanced-digital-signal-processing

Skill Development Activities Suggested

1. Interact with industry (small, medium, and large).
2. Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3. Involve in case studies and field visits/ fieldwork.
4. Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5. Handle advanced instruments to enhance technical talent.
6. Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7. Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc.

Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical – activities which will enhance their skill. The prepared report shall be evaluated for CIE marks.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Able to analyze and implement the frequency analysis & correlation of discrete-time linear time invariant systems.	L4
CO2	Able to implement sampling rate conversion by decimation & Interpolation process and design digital filter banks	L4
CO3	Able to analyze forward and backward linear prediction of a stationary random process using Levinson-Durbin Algorithm	L4
CO4	Able to understand and analyze adaptive filters and its application using LMS algorithm & RLS algorithm.	L4
CO5	Able to understand parametric & non-parametric methods for power spectrum estimation.	L2

Professional Elective -I

Nanoelectronics			
Course Code	22LEL231	CIE Marks	50
Teaching Hours/Week (L:P: SDA)	2:0:2	SEE Marks	50
Total Hours of Pedagogy	25 Hours of teaching and 10-12 sessions for Skill Development Activities	Total Marks	100
Credits	3	Exam Hours	03

Course Learning objectives: This course will enable students to:

- Know the principles behind Nanoscience engineering and Nanoelectronics.
- Apply the knowledge to prepare and characterize nanomaterials.
- Know the effect of particles size on mechanical, thermal, optical and electrical properties of nanomaterials.
- Design the process flow required to fabricate state of the art transistor technology.
- Analyse the requirements for new materials and device structure in the future technologies.

Module-1

Introduction: Overview of nanoscience and engineering. Development milestones in microfabrication and electronic industry. Moores' law and continued miniaturization, Classification of Nanostructures, Electronic properties of atoms and solids: Isolated atom, Bonding between atoms, Giant molecular solids, Free electron models and energy bands, crystalline solids, Periodicity of crystal lattices, Electronic conduction, effects of nanometer length scale, Fabrication methods: Top down processes, Bottom up processes methods for templating the growth of nanomaterials, ordering of nano systems.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-2

Characterization: Classification, Microscopic techniques, Field ion microscopy, scanning probe techniques, diffraction techniques: bulk and surface diffraction techniques, spectroscopy techniques: photon, radiofrequency, electron, surface analysis and dept profiling: electron, mass, Ion beam, Reflectometry, Techniques for property measurement: mechanical, electron, magnetic, thermal properties.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-3

Inorganic semiconductor nanostructures: overview of semiconductor physics. Quantum confinement in semiconductor nanostructures: quantum wells, quantum wires, quantum dots, super-lattices, band offsets, electronic density of states.

Carbon Nanostructures: Carbon molecules, Carbon Clusters, Carbon Nanotubes, application of Carbon Nanotubes.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-4

Fabrication techniques: requirements of ideal semiconductor, epitaxial growth of quantum wells, lithography and etching, cleaved-edge over growth, growth of vicinal substrates, strain induced dots and wires, electrostatically induced dots and wires, Quantum well width fluctuations, thermally annealed quantum wells, semiconductor nanocrystals, colloidal quantum dots, self-assembly techniques.

Physical processes: modulation doping, quantum hall effect, resonant tunneling, charging effects, ballistic carrier transport, Inter band absorption, intra band absorption, Light emission processes, phonon bottleneck, quantum confined stark effect, nonlinear effects, coherence and dephasing, characterization of semiconductor nanostructures: optical electrical and structural.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-5

Methods of measuring properties: atomic, crystallography, microscopy, spectroscopy.

Applications: Injection lasers, quantum cascade lasers, single-photon sources, biological tagging, optical memories, coulomb blockade devices, photonic structures, QWIPs, NEMS, MEMS.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks**

to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Text Books

1. 'Nanoscale Science and Technology', Ed Robert Kelsall, Ian Hamley, Mark Geoghegan, John Wiley, 2007

2. 'Introduction to Nanotechnology', Charles P Poole, Jr, Frank J Owens, John Wiley, Copyright 2006, Reprint 2011.

Reference Book:

1.'Hand Book of Nanoscience Engineering and Technology', Ed William A Goddard III, Donald W Brenner, Sergey E. Lyshevski, Gerald J Iafrate, CRC press, 2003

Web links and Video Lectures (e-Resources):

1. https://www.digimat.in/nptel/courses/video/117108047/L01.html
2. https://archive.nptel.ac.in/courses/117/108/117108047/

Skill Development Activities Suggested:

1. Interact with industry (small, medium, and large).
2. Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3. Involve in case studies and field visits/ fieldwork.
4. Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5. Handle advanced instruments to enhance technical talent.
6. Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7. Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc.

Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical – activities which will enhance their skill. The prepared report shall be evaluated for CIE marks.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Know the principles behind Nanoscience engineering and Nanoelectronics.	L2
CO2	Apply the knowledge to prepare and characterize nanomaterials.	L3
CO3	Know the effect of particles size on mechanical, thermal, optical and electrical properties of nanomaterials	L2
CO4	Design the process flow required to fabricate state of the art transistor technology	L3
CO5	Analyze the requirements for new materials and device structure in the future technologies.	L3

Reconfigurable Computing			
Course Code	22LEL232	CIE Marks	50
Teaching Hours/Week (L:P: SDA)	2:0:2	SEE Marks	50
Total Hours of Pedagogy	25 Hours of teaching and 10-12 sessions for Skill Development Activities	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives: This course will enable students to:

- Understand the fundamental principles and practices in reconfigurable architecture.
- Simulate and synthesize the reconfigurable computing architectures.
- Understand the FPGA design principles, and logic synthesis
- Integrate hardware and software technologies for reconfiguration computing focusing on partial reconfiguration design.
- Design digital systems for a variety of applications on signal processing and system on chip configurations.

Module-1

Introduction: History, Reconfigurable vs Processor based system, RC Architecture. Reconfigurable Logic Devices: Field Programmable Gate Array, Coarse Grained Reconfigurable Arrays. Reconfigurable Computing System: Parallel Processing on Reconfigurable Computers, A survey of Reconfigurable Computing System.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-2

Languages and Compilation: Design Cycle, Languages, HDL, High Level Compilation, Low level Design flow, Debugging Reconfigurable Computing Applications.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-3

Implementation: Integration, FPGA Design flow, Logic Synthesis. High Level Synthesis for Reconfigurable Devices**:** Modelling, Temporal Partitioning Algorithms.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-4

Partial Reconfiguration Design: Partial Reconfiguration Design, Bitstream Manipulation with JBits, The modular Design flow, The Early Access Design Flow, Creating Partially Reconfigurable Designs, Partial Reconfiguration using Hansel-C Designs, Platform Design.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-5

Signal Processing Applications: Reconfigurable computing for DSP, DSP application building blocks, Examples: Beamforming, Software Radio, Image and video processing, Local Neighbourhood functions, Convolution.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

3. Three Unit Tests each of **20 Marks**
4. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks**

to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

6. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
7. The question paper will have ten full questions carrying equal marks.
8. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
9. Each full question will have a sub-question covering all the topics under a module.
10. The students will have to answer five full questions, selecting one full question from each module

.

Suggested Learning Resources:

Text Books

1. Reconfigurable Computing: Accelerating Computation with Field-Programmable Gate Arrays by M. Gokhale and P. Graham, Springer, ISBN: 978-0-387-26105-8, 2005.
2. Introduction to Reconfigurable Computing: Architectures, Algorithms and Applications by C. Bobda, Springer, ISBN: 978-1-4020-6088-5, 2007.

Skill Development Activities Suggested:

1. Interact with industry (small, medium, and large).
2. Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3. Involve in case studies and field visits/ fieldwork.
4. Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5. Handle advanced instruments to enhance technical talent.
6. Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7. Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc.

Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical – activities which will enhance their skill. The prepared report shall be evaluated for CIE marks.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Understand the new paradigm of Computing which offers flexibility, scalability and performance.	L2
CO2	Understand the notion of system/circuit redesign on the fly using dynamic reconfiguration. T	L2
CO3	Able to optimize the given system specific to underlying reconfigurable hardware.	L3
CO4	Able to bring the notion of evolvable circuit on Reconfigurable hardware.	L3
CO5	Designing a reconfigurable computing and how to utilize them for solving challenging computational problems.	L3

Cryptography and Network Security			
Course Code	22LEL233	CIE Marks	50
Teaching Hours/Week (L:P: SDA)	2:0:2	SEE Marks	50
Total Hours of Pedagogy	25 Hours of teaching and 10-12 sessions for Skill Development Activities	Total Marks	100
Credits	3	Exam Hours	

Course Learning objectives:

- Study the network security model, security attacks, mechanisms and services and to demonstrate use of various symmetric key ciphers and their principles.
- Understand the concept of Modular Arithmetic and its application in public key cryptography and apply the knowledge to solve security related problems.
- Understand the design principles of Public key cryptosystems for encryption, key exchange and authentication.
- Comprehend the concept of secured electronic transaction with web security considerations.
- Study the security threats to networks and their counter measures.

Module-1

Security services, mechanisms and attacks, OSI security model, symmetric key cryptography, substitution techniques: playfair and transposition techniques, SDES: encryption, decryption and key generation, DES: design principles, AES: encryption and decryption model, steganography.

Teaching-Learning Process	Chalk and Talk / Power Point Presentations

Module-2

Galois fields, extended Euclid's theorem, discrete log problem, Chinese remainder theorem, elliptic curve arithmetic, principles of public key cryptosystems.

Teaching-Learning Process	Chalk and Talk / Power Point Presentations

Module-3

Principles of public-key cryptosystems: public-key cryptosystems, applications for public-key cryptosystems, requirements for public-key cryptography, public-key cryptanalysis, the RSA: description of the algorithm, computational aspects, the security of RSA algorithm, Diffie Hellman key exchange, cryptographic hash functions: applications of cryptographic hash functions, two simple hash functions, requirements and security, hash functions based on cipher block chaining, secure hash algorithm (SHA).

Teaching-Learning Process	Chalk and Talk / Power Point Presentations

Module-4

Web security considerations: web security threats, web traffic security approaches, secure sockets layer and transport layer security: SSL architecture, SSL record protocol, change cipher spec protocol, alert protocol, handshake protocol, cryptographic computations, transport layer security, secure electronic transaction: SET overview, Dual signature, payment processing.

Teaching-Learning Process	Chalk and Talk / Power Point Presentations

Module-5

Viruses and related threats: Malicious programs, the nature of viruses, types of viruses, macro viruses, e-mail viruses, worms, firewalls: Firewall characteristics, types of firewalls, firewall configurations, Trusted systems: Data access control, the concept of trusted systems, trojan horse defence.

Teaching-Learning Process	Chalk and Talk / Power Point Presentations

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks**

to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

.

Suggested Learning Resources:

Books

1. William Stallings, "Cryptography and Network security: principles and practice", 2nd Edition, Prentice Hall of India, New Delhi,2002 and onwards
2. Behrouz A. Fourouzan, “Cryptography and Network security” Tata McGraw-Hill, 2008 and onwards.
3. Atul Kahate,” Cryptography and Network security”, 2ndEdition, Tata McGraw-Hill, 2008 and onwards.
4. H. Yang et al., Security in Mobile Ad Hoc Networks: Challenges and Solution, IEEE Wireless Communications, 2004 and onwards.

Web links and Video Lectures (e-Resources):

1. https://swayam.gov.in/
2. https://nptel.ac.in/

Skill Development Activities Suggested

1. Interact with industry (small, medium, and large).
2. Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3. Involve in case studies and field visits/ fieldwork.
4. Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5. Handle advanced instruments to enhance technical talent.
6. Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7. Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student’s abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc.

Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical – activities which will enhance their skill. The prepared report shall be evaluated for CIE marks.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Identify and describe different techniques in modern cryptography	L2
CO2	Employ the modular arithmetic fundamentals to cryptography	L4
CO3	Describe, recognize and use the principles of Public key cryptosystems for various applications.	L4
CO4	Recognize the use of cryptography in Data Networks	L4
CO5	Analyze the security issues related to internet and networks	L5

ADVANCED COMMUNICATION SYSTEMS			
Course Code	22LEL234	CIE Marks	50
Teaching Hours/Week (L:P: SDA)	(2:0:2)	SEE Marks	50
Total Hours of Pedagogy	25 Hours of teaching and 10-12 sessions for Skill Development Activities	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives: This course will enable students:

- To understand the concept of low pass and Band pass signals during modulation at the Transmitter.
- To analyze the Receiver performance for various types of single carrier symbol modulations through ideal and AWGN channels.
- To apply single carrier equalizers for various modulation schemes and detection methods for defined channel models
- To understand the concepts of synchronization for carrier and symbol timing recovery at receiver.
- To understand the concepts of spread spectrum systems for communications in a Jamming, multiuser and low power intercept environment.

Module-1

Signal Representation: Low pass representation of band pass signals, Low pass representation of band pass random process.
Modulation: Representation of digitally modulated Signals, Modulation Schemes without memory (Band Limited Schemes - PAM, BPSK, QPSK, MPSK, MQAM, Power Limited Schemes – FSK, MFSK, DPSK, DQPSK), modulation schemes with memory (Basics of CPFSK and CPM – Full Treatment of MSK), Transmit PSD for Modulation Schemes.

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

Module-2

Demodulation: Vector Channel, Vector Channel +AWGN, Performance parameters, Optimum Coherent Detection for power limited and Band limited schemes, Optimal Coherent detection for schemes with memory, Optimal Non– Coherent detection for schemes without and with memory (FSK, DPSK, DQPSK), Comparison of detection schemes.

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

Module-3

Bandlimited Channels: Band limited channel characterization, signalling through band limited linear filter channels, Sinc, RC, Duobinary and Modified Duobinary signalling schemes.
Linear Equalizers: Zero forcing Equalizer, MSE and MMSE. **Non-Linear Equalizers**: Decision - feedback equalization, Predictive DFE, Performance of DFE.
Adaptive equalization: Adaptive linear equalizer, adaptive decision feedback equalizer.

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

Module-4

Synchronization – Signal Parameter estimation, Carrier Phase Estimation, Symbol Timing Recovery, Performance of ML estimators. Fading – Large scale, small scale; Statistical characterization of multipath channels – Delay and Doppler spread, classification of multipath channels, Binary signalling over frequency non selective Rayleigh fading channel.

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

Module-5

Spread Spectrum Signals For Digital Communication: Model of spread spectrum digital communication system, Direct sequence spread spectrum signals, some applications of DS spread spectrum signals, generation of PN sequences, Frequency hopped spread spectrum signals, Time hopping SS, Synchronization of SS systems.

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Books

1. 1'Digital Communications', John G. Proakis, Masoud Salehi, Pearson Education, ISBN:978-9332535893, 5th edition, 2014
2. Digital Communications: Fundamentals and Applications: Fundamentals & Applications', Bernard Sklar, Pearson Education,ISBN:9788131720929, 2nd edition, 2009
3. 'Digital Communications Systems', Simon Haykin, Wiley, ISBN:9788126542314, 1st edition, 2014

Massive Open Online Courses:

1. Modern Digital Communication Techniques-By Prof. Suvra Sekhar Das | IIT Kharagpur
2. Principles of Signal Estimation for MIMO/ OFDM Wireless Communication-**By Prof. Aditya K. Jagannatham | IIT Kanpur**

Skill Development Activities Suggested

1. Interact with industry (small, medium, and large).
2. Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3. Involve in case studies and field visits/ fieldwork.
4. Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5. Handle advanced instruments to enhance technical talent.
6. Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7. Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc.

Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical – activities which will enhance their skill. The prepared report shall be evaluated for CIE marks.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Explain the concept of low pass and Bandpass signals representations at the Transmitter, process of Detection and Estimation at the receiver in the presence of AWGN only.	L2
CO2	Evaluate Receiver performance for various types of single carrier symbol modulations through ideal and AWGN Non-bandlimited and bandlimited channels.	L3
CO3	Design single carrier equalizers for various symbol modulation schemes and detection methods for defined channel models, and compute parameters to meet desired rate and performance requirements.	L4
CO4	Explain the concepts of multi-channel signaling scheme and synchronization for carrier and symbol timing recovery at receiver.	L2
CO5	Design and Evaluate Non band limited and Non power limited spread spectrum systems for communications in a Jamming environment, multiuser situation and low power intercept environment.	L4

Optical Communication and Networking			
Course Code	22LEL235	CIE Marks	50
Teaching Hours/Week (L:P: SDA)	2:0:2	SEE Marks	50
Total Hours of Pedagogy	25 Hours of teaching and 10-12 sessions for Skill Development Activities	Total Marks	100
Credits	3	Exam Hours	03

Course Learning objectives: This course will enable students to:

- Understand the various optical devices and how they operate.
- Recognize and choose various components for optical networking in accordance with the established design requirements
- Acquire knowledge of the elements of data transmission, loss obstacles, and other network operating artifacts.
- Acquire knowledge of the problems associated with setting up and maintaining the optical network's access component while keeping up with current data transmission trends.
- Build a WDM network and explore the management of components and networks.

Module-1

Introduction to optical networks: Optical Networks, optical packet switching, **Propagation of signals in optical fiber:** Different losses, Nonlineareffects, Solutions. **Optical Components (Part-1):** Couplers, Isolators and Circulators.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-2

Optical Components (Part-2): Multiplexers and Filters, Optical Amplifiers, detectors. **Modulation - Demodulation:** Formats, Ideal receivers, Practical direct detection receivers, Optical preamplifiers, Bit error rates, Coherent detection.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-3

Transmission System Engineering: System model, Power penalty, Transmitter, Receiver, Crosstalk.
Client Layers of optical layer: SONET/SDH: Multiplexing, layers, Frame structure.
Asynchronous Transfer Mode: ATM functions, Adaptation layers, Quality of Service (QoS) and flow control, Signaling and Routing.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-4

WDM network elements: Optical line terminals, Optical line amplifiers, Optical Add/ Drop Multiplexers, Optical cross connects.
WDM Network Design: Cost trade-offs, LTD and RWA problems, Routing and wavelength assignment, Wavelength conversion.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-5

Control and Management (Part-1): Network management functions, management framework, Information model, management protocols, Layerswithin optical layer.
Control and Management (Part-2): Performance and fault management, Impact of transparency, BER measurement, Optical trace, Alarmmanagement, Configuration management, Optical Safety.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks**

to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Text Books

'Optical Networks', Rajiv Ramaswami, Kumar N. Sivarajan and Galan H Sasaki, Morgan Kaufman Publishers, 3rd edition, 2010.

Reference Books:

1. 'Optical fiber communication', John M. Senior, Pearson edition, 2000.
2. 'Optical fiber Communication', Gerd Keiser, John Wiley, New York, 5th Edition, 2017.
3. 'Fiber Optic Networks', P. E. Green, Prentice Hall, 1994.

Web links and Video Lectures (e-Resources):

1. https://onlinecourses.nptel.ac.in/noc20_ph07/preview
2. https://www.classcentral.com/course/swayam-optical-communications-6699

Skill Development Activities Suggested:

1. Interact with industry (small, medium, and large).
2. Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3. Involve in case studies and field visits/ fieldwork.
4. Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5. Handle advanced instruments to enhance technical talent.
6. Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7. Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc.

Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical – activities which will enhance their skill. The prepared report shall be evaluated for CIE marks.

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Comprehend the various optical devices and their working strategies	L2
CO2	Recognize and select various optical networking components according to the prescribed design specifications	L2
CO3	Learn the aspects of data transmission, loss hindrances, and other artifacts affecting the network operation	L2
CO4	Learn the issues involved in setting up and maintaining access part of the optical network with the latest trends in the data communication	L2
CO5	Design a WDM network and study the component and network management aspects	L4

Professional Elective- 2

Error Control Coding			
Course Code	22LEL241	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	2:0:2	SEE Marks	50
Total Hours of Pedagogy	25 Hours of Teaching and 10 to 12 sessions of Skill Development Activities.	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives: This course will enable students to:

- Understand the concept of the Entropy, information rate and capacity for the Discrete memoryless channel.
- Apply modern algebra and probability theory for the coding.
- Compare Block codes such as Linear Block Codes, Cyclic codes, etc. and Convolutional codes.
- Detect and correct errors for different data communication and storage systems.
- Analyze and implement different Block code encoders and decoders, and also convolutional encoders and decoders including soft and hard Viterbi algorithm.

Module-1

Information theory: Introduction, Entropy, Source coding theorem, discrete memoryless channel, Mutual Information, Channel Capacity Channel coding theorem. **Introduction to algebra:** Groups, Fields, binary field arithmetic, Construction of Galois Fields GF (2m) and its properties, (Only statements of theorems without proof) Computation using Galois field GF (2m) arithmetic, Vector spaces and Matrices.

Teaching-Learning Process	Chalk and Talk / Power Point Presentations.

Module-2

Linear block codes: Generator and parity check matrices, Encoding circuits, Syndrome and error detection, Minimum distance considerations, Error detecting and error correcting capabilities, Standard array and syndrome decoding, Single Parity Check Codes (SPC),Repetition codes, Self dual codes, Hamming codes, Reed-Muller codes. Product codes and Interleaved codes.

Teaching-Learning Process	Chalk and Talk / Power Point Presentations.

Module-3

Cyclic codes: Introduction, Generator and parity check polynomials, Encoding of cyclic codes, Syndrome computing and error detection, Decoding of cyclic codes, Error trapping Decoding, Cyclic hamming codes, Shortened cyclic codes.

Teaching-Learning Process	Chalk and Talk / Power Point Presentations.

Module-4	
BCH codes: Binary primitive BCH codes, Decoding procedures, Implementation of Galois field arithmetic. (Primitive BCH codes over GF (q), Reed -Solomon codes. **Majority Logic decodable codes:** One -step majority logic decoding, Multiple-step majority logic.	
Teaching-Learning Process	Chalk and Talk / Power Point Presentations.
Module-5	
Convolution codes: Encoding of convolutional codes: Systematic and Nonsystematic Convolutional Codes, Feedforward encoder inverse, A catastrophic encoder, Structural properties of convolutional codes: state diagram, state table, state transition table, tree diagram, trellis diagram. Viterbi algorithm, Sequential decoding: Log Likelihood Metric for Sequential Decoding.	
Teaching-Learning Process	Chalk and Talk / Power Point Presentations.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks**

to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Textbooks:

1. 'Digital Communication systems', Simon Haykin, Wiley India Private. Ltd, ISBN 978-81-265-4231-4, First edition, 2014
2. 'Error control coding', Shu Lin and Daniel J. Costello. Jr, Pearson, Prentice Hall, 2nd edition, 2004

Reference Books:

1. 'Theory and practice of error control codes', Blahut. R. E, Addison Wesley, 1984
2. 'Introduction to Error control coding', Salvatore Gravano, Oxford University Press, 2007
3. 'Digital Communications - Fundamentals and Applications', Bernard Sklar, Pearson Education (Asia) Pvt. Ltd., 2nd Edition, 2001

Web links and Video Lectures (e-Resources):

1. https://www.mooc.org/
2. https://onlinecourses.nptel.ac.in/

Skill Development Activities Suggested:

1. Interact with industry (small, medium, and large).
2. Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3. Involve in case studies and field visits/ fieldwork.
4. Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5. Handle advanced instruments to enhance technical talent.
6. Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7. Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc.

Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical – activities which will enhance their skill. The prepared report shall be evaluated for CIE marks.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Understand the concept of the Entropy, information rate and capacity for the Discrete memoryless channel.	L2
CO2	Apply modern algebra and probability theory for the coding.	L3
CO3	Compare Block codes such as Linear Block Codes, Cyclic codes, etc. and Convolutional codes.	L2
CO4	Detect and correct errors for different data communication and storage systems.	L3
CO5	Analyze and implement different Block code encoders and decoders, and also convolutional encoders and decoders including soft and hard Viterbi algorithm.	L4

SoC Design			
Course Code	22LEL242	CIE Marks	50
Teaching Hours/Week (L:P: SDA)	2:0:2	SEE Marks	50
Total Hours of Pedagogy	25 Hours of teaching and 10-12 sessions for Skill Development Activities	Total Marks	100
Credits	3	Exam Hours	3

Course Learning Objectives:

- To understand the organization and implementation of the 3- and 5-stage pipeline ARM processor cores and ARM instruction set architecture.
- To understand the needs high-level language in application development.
- To Know the issues involved in debugging systems in embedded processor cores and in the production testing of board-level systems.
- To learn different ARM integer cores, concept of memory hierarchy and management.

Module-1

ARM Organization and Implementation: 3-stage pipeline ARM organization, 5-stage pipeline ARM organization, ARM instruction execution, ARM implementation, The ARM coprocessor interface.

The ARM Instruction Set: Introduction, Exceptions, Conditional execution, Branch and Branch with Link (B, BL), Branch, Branch with Link and exchange (BX, BLX), Software Interrupt (SWI).

Teaching-Learning Process	Chalk and talk / Power point presentations

Module-2

The ARM Instruction Set (Continued) Data processing instructions, Multiply instructions, Count leading zeros (CLZ - architecture v5T only), Single word and unsigned byte data transfer instruction, Half-word and signed byte data transfer instructions, Multiple register transfer instructions, Swap memory and register instructions (SWP), Status register to general register transfer instructions, General register to status register transfer instructions, Coprocessor instructions, Coprocessor data operations, Coprocessor data transfers, Coprocessor register transfers, Breakpoint instruction (BRK - architecture v5T only), Unused instruction space, Memory faults, ARM architecture variants

Teaching-Learning Process	Chalk and talk / Power point presentations

Module-3

Architectural Support for High-Level Languages: Abstraction in software design, Data types, Floating-point data types, The ARM floating-point architecture, Expressions, Conditional statements, Loops, Functions and procedures, Use of memory, Run-time environment.

Teaching-Learning Process	Chalk and talk / Power point presentations

Module-4

Architectural Support for System Development: The ARM memory interface, The Advanced Microcontroller Bus Architecture(AMBA), The ARM reference peripheral specification, Hardware system prototyping tools, The ARMulator, The JTAG boundary scan test architecture, The ARM debug architecture, Embedded Trace, Signal processing support

Teaching-Learning Process	Chalk and talk / Power point presentations

Module-5

ARM Processor Cores: ARM7TDMI, ARM8, ARM9TDMI, ARM10TDMI, Discussion, Example and exercises.

Memory Hierarchy: Memory size and speed, On-chip memory, Caches, Cache design - an example, Memory management, Examples and exercises.

Teaching-Learning Process	Chalk and talk / Power point presentations

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks**

to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Books

1. Steve Furber "ARM System-On-Chip Architecture" Addison Wesley, 2ndedition
2. Joseph Yiu "The Definitive Guide to the ARM Cortex-M3", Newnes, (Elsevier) , 2ndedition, 2010.
3. Sudeep Pasricha and Nikil Dutt," On-Chip Communication Architectures: System on Chip Interconnect", Morgan Kaufmann Publishers, 2008.
4. Michael Keating, Pierre Bricaud "Reuse Methodology Manual for System on Chip designs", Kluwer Academic Publishers, 2ndedition, 2008.

Web links and Video Lectures (e-Resources):

1. https://youtu.be/PRQXzjTrCJY
2. https://youtu.be/HNbeVvfFKsQ

Skill Development Activities Suggested:

1. Interact with industry (small, medium, and large).
2. Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3. Involve in case studies and field visits/ fieldwork.
4. Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5. Handle advanced instruments to enhance technical talent.
6. Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7. Work on different software / s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc.

Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical – activities which will enhance their skill. The prepared report shall be evaluated for CIE marks.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Apply the 3- and 5-stage pipeline ARM processor cores and analyse the implementation issues.	L3
CO2	Use the concepts and methodologies employed in designing a System- on-chip (SoC) based around a microprocessor core and in designing the microprocessor core itself.	L3
CO3	Understand how SoCs and microprocessors are designed and used, and why a modern processor is designed the way that it is.	L2
CO4	Use integrated ARM CPU cores (including Strong ARM) that incorporate full support for memory management.	L3
CO5	Analyze the requirements of a modern operating system and use the ARM architecture to address the same	L4

Micro Electro Mechanical Systems			
Course Code	22LEL243	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	2:0:2	SEE Marks	50
Total Hours of Pedagogy	25 Hours of teaching and 10-12 sessions for Skill Development Activities	Total Marks	100
Credits	3	Exam Hours	03

Course Learning objectives:

- To explain MEMS
- To understand the working principles of micro systems
- To analyze the scaling laws in miniaturization

Module-1	
Overview of MEMS and Microsystems: MEMS and Microsystem, Typical MEMS and Microsystems Products, Evolution of Microfabrication,Microsystems and Microelectronics, Multidisciplinary Nature of Microsystems, Miniaturization. Applications and Markets.	
Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations
Module-2	
Working Principles of Microsystems: Introduction, Microsensors, Microactuation, MEMS with Microactuators, Microaccelerometers,Microfluidics. **Engineering Science for Microsystems Design and Fabrication:** Introduction, Atomic Structure of Matters, Ions and Ionization, Molecular Theory of Matter and Inter-molecular Forces, Doping of Semiconductors, The Diffusion Process, Plasma Physics, Electrochemistry.	
Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations
Module-3	
Engineering Mechanics for Microsystems Design: Introduction, Static Bending of Thin Plates, Mechanical Vibration, Thermomechanics, FractureMechanics, Thin Film Mechanics, Overview on Finite Element Stress Analysis.	
Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations
Module-4	
Scaling Laws in Miniaturization: Introduction, Scaling in Geometry, Scaling in Rigid-Body Dynamics, Scaling in Electrostatic Forces, Scaling of Electromagnetic Forces, Scaling inElectricity, Scaling in Fluid Mechanics, Scaling in Heat Transfer.	
Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations
Module-5	
Overview of Micro-manufacturing: Introduction, Bulk Micro-manufacturing, Surface Micromachining, The LIGA Process, Summary onMicromanufacturing. **Microsystem Design**: Introduction, Design Considerations, Process Design, Mechanical Design, Using Finite Element Method.	
Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks**

to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Text Books

MEMS and Micro systems: Design, Manufacture and Nanoscale Engineering', Tai-Ran Hsu, John Wiley & Sons, ISBN: 978-0470-08301-7,2ndEdition, 2008

Reference Books:

1. 'Micro and Nano Fabrication: Tools and Processes', Hans H. Gatzen, Volker Saile, Jurg Leuthold, Springer, 2015
2. 'Micro Electro Mechanical Systems (MEMS)', Dilip Kumar Bhattacharya, Brajesh Kumar Kaushik, Cengage Learning.

Web links and Video Lectures (e-Resources):

1. https://www.mooc.org/
2. https://onlinecourses.nptel.ac.in/

Skill Development Activities Suggested:

1. Interact with industry (small, medium, and large).
2. Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3. Involve in case studies and field visits/ fieldwork.
4. Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5. Handle advanced instruments to enhance technical talent.
6. Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7. Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc.

Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical – activities which will enhance their skill. The prepared report shall be evaluated for CIE marks.

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Able to understand the MEMS and Micro systems	L1 L2
CO2	Able to understand and analyze the mechanics for Microsystems design	L1 L2 L3
CO3	Able to analyze the scaling laws in miniaturization	L4
CO4	Simplify the design of micro devices, micro systems using the MEMS fabrication process	L4
CO5	Choose a micromachining technique, such as bulk micromachining and surface micromachining for a specific MEMS fabrication process	L3

Real Time Operating System			
Course Code	22LEL244	CIE Marks	50
Teaching Hours/Week (L:P: SDA)	2:0:2	SEE Marks	50
Total Hours of Pedagogy	25 Hours of teaching and 10-12 sessions for Skill Development Activities	Total Marks	100
Credits	3	Exam Hours	03

Course Learning objectives:

- To understand a typical embedded system and its constituents
- To learn the selection process of processor and memory for the embedded systems
- To learn communication buses and protocols used in the embedded and real-time systems
- To understand real-time operating system and the types of RTOS
- To learn various approaches to real-time scheduling
- To learn software development process and tools for RTOS applications

Module-1

Real-Time Systems and Resources: Brief history of Real Time Systems, A brief history of Embedded Systems. System Resources, Resource Analysis, Real-Time Service Utility, Scheduler concepts, Real-Time OS, State transition diagram and tables, Thread Safe Re-entrant Functions.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-2

Processing with Real Time Scheduling: Scheduler Concepts, Pre-emptive Fixed Priority Scheduling Policies with timing diagrams and problems and issues, Feasibility, Rate Monotonic least upper bound, Necessary and Sufficient feasibility, Deadline –Monotonic Policy, Dynamic priority policies, Alternative to RM policy.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-3

Memory and I/O: Worst case execution time, Intermediate I/O, Shared Memory, ECC Memory, Flash file systems. Multi-resource Services, Blocking, Deadlock and live lock, Critical sections to protect shared resources, Missed deadline, QoS, Reliability and Availability, Similarities and differences, Reliable software, Available software.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-4

Firmware Components: The 3 firmware components, RTOS system software mechanisms, Software application components. Debugging Components, Exceptions, assert, checking return codes, Single-step debugging, Test access ports, Trace Ports.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-5

Process and Threads: Process and thread creations, Programs related to semaphores, message queue, shared buffer applications involving intertask /thread communication.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Assessment Details (both CIE and SEE)

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Continuous Internal Evaluation:

1) Three Unit Tests each of **20 Marks**
2) Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1) The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2) The question paper will have ten full questions carrying equal marks.
3) Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4) Each full question will have a sub-question covering all the topics under a module.
5) The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Textbooks:

1. 'Real-Time Embedded Systems and Components', Sam Siewert, Cengage Learning, India Edition, 2007.
2. 'Embedded/Real Time Systems, Concepts, Design and Programming, Black Book', Dr. K.V.K.K Prasad, Dream Tech Press, New edition, 2010.

Reference Books:

1. 'Real Time System', James W S Liu, Pearson Education, 2008.
2. 'Programming for Embedded Systems', Dream Tech Software Team, John Wiley, India Pvt. Ltd., 2008.

Skill Development Activities Suggested:

1. Interact with industry (small, medium, and large).
2. Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3. Involve in case studies and field visits/ fieldwork.
4. Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5. Handle advanced instruments to enhance technical talent.
6. Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7. Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc.

Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical – activities which will enhance their skill. The prepared report shall be evaluated for CIE marks.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Recognize and classify real-time systems	L2
CO2	Apply software development process to a given RTOS application	L2
CO3	Design a given RTOS based application	L3
CO4	Ability to use commercial tools to develop RTOS based applications	L3

Simulation, Modelling and Analysis			
Course Code	22LEL245	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	2:0:2	SEE Marks	50
Total Hours of Pedagogy	25 Hours of teaching and 10-12 sessions for Skill Development Activities	Total Marks	100
Credits	3	Exam Hours	03

Course Learning objectives: This course will enable students to:

- Define the basics of simulation modelling and replicating the practical situations in organizations
- Generate random numbers and random variates using different techniques.
- Develop simulation model using heuristic methods.
- Analysis of Simulation models using input analyzer, and output analyzer.
- Explain Verification and Validation of simulation model.

Module-1

Basic Simulation Modeling: Nature of simulation, Systems, Models and Simulation, Discrete- Event Simulation, Simulation of Single Server Queuing System, Simulation of inventory system, Parallel and distributed simulation and the high-level architecture, Steps in sound simulation study, and other types of simulation, Advantages and disadvantages.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-2

Review of Basic Probability and Statistics: Random Variables and their properties, Simulation Output Data and Stochastic Processes, Estimation of Means, Variances and Correlations, Confidence Intervals and Hypothesis tests for the Mean**.**

Building valid, credible and appropriately detailed simulation models: Introduction and definitions, Guidelines for determining the level of model's detail, Management's Role in the Simulation Process, Techniques for increasing model validity and credibility, Statistical procedure for comparing the real-world observations and simulation output data.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-3

Selecting Input Probability Distributions: Useful probability distributions, activity I, II and III. Shifted and truncated distributions; Specifying multivariate distribution, correlations, and stochastic processes; Selecting the distribution in the absence of data, Models of arrival process**.**

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-4

Random Number Generators: Linear congruential Generators, Other kinds, Testing number generators,

Generating the Random Variates: General approaches, generating continuous random variates, generating discrete random variates, generating random vectors, and correlated random variates; Generating arrival processes.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-5

Output data analysis for a single system: Transient and steady state behavior of a stochastic process; Types of simulations with regard to analysis; Statistical analysis for terminating simulation; Statistical analysis for steady state parameters; Statistical analysis for steady state cycle parameters; Multiple measures of performance, Time plots of important variables.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks**

to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each

module.

4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Text Books

1. Averill Law, "Simulation modeling and analysis", McGraw Hill 4th edition, 2007.

Reference Books:

2. Tayfur Altiok and Benjamin Melamed, “Simulation modeling and analysis with ARENA”, Elsevier, Academic press, 2007.
3. Jerry Banks, “Discrete event system Simulation”, Pearson, 2009
4. Seila Ceric and Tadikamalla, “Applied simulation modeling”, Cengage, 2009.
5. George. S. Fishman, “Discrete event simulation”, Springer, 2001.
6. Frank L. Severance, “System modeling and simulation”, Wiley, 2009..

Skill Development Activities Suggested:

1. Interact with industry (small, medium, and large).
2. Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3. Involve in case studies and field visits/ fieldwork.
4. Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5. Handle advanced instruments to enhance technical talent.
6. Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7. Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student’s abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc.

Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical – activities which will enhance their skill. The prepared report shall be evaluated for CIE marks.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Describe the role of important elements of discrete event simulation and modeling paradigm	L2
CO2	Conceptualize real world situations related to systems development decisions, originating from source requirements and goals.	L4
CO3	Develop skills to apply simulation software to construct and execute goal-driven system models.	L4
CO4	Interpret the model and apply the results to resolve critical issues in a real world environment.	L3

Advanced Communication Lab			
Course Code	22LELL26	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	1:2:0	SEE Marks	50
Total Hours of Pedagogy	13 Hours of teaching and 10-13 Practical sessions	Total Marks	100

Credits	2	Exam Hours	03

Part A: EDA Using Cadence OrCAD or OrCAD Lite or any EDA Tool,design and verify the following:

Sl. No.	Experiments
1	Simulation of ASK modulation and demodulation
2	Simulation of FSK modulation and demodulation
3	Simulation of BPSK modulation and demodulation
4	Simulation of QPSK modulation and demodulation
5	Simulation of signal constellation QPSK with Rayleigh fading and AWGN
6	Simulation of signal constellation M-ary QAM with AWGN fading
7	To simulate the communication link
8	To simulate Zero Forcing algorithm
9	To simulate LMS algorithm
10	Generation of m-Sequence and verify its properties
11	Generation Gold Sequence and verify its properties

Conduct of Practical Examination:

1. All laboratory experiments are to be included for practical examination.
2. Students are allowed to pick one experiment from the lot.
3. Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.
4. Change of experiment is allowed only once and Marks allotted to the procedure part to be made zero.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIEis 50% of the maximum marks. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course.The student has to secure not less than 40% of maximum marks in the semester-end examination (SEE). In total of CIE and SEE student has to secure 50% maximum marks of the course.

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

1. Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
2. Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
3. Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
4. Weightage to be given for neatness and submission of record/write-up on time.
5. Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8^{th} week of the semester and the second testshall be conducted after the 14^{th} week of the semester.
6. In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and therest 40% for viva-voce.
7. The suitable rubrics can be designed to evaluate each students performance and learning ability.
8. The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of **scaled-down** marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

9. SEE marks for the practical course is 50 Marks.
10. SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University.
11. All laboratory experiments are to be included for practical examination.

12. (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners.
    OR based on the course requirement evaluation rubrics shall be decided jointly by examiners.
13. Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.
14. Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.
15. General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)
16. Change of experiment is allowed only once and 10% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours

Suggested ONLINE courses

Sl. No.	Course code	Course Title	National Coordinator	Instructor
1	22AUD27	Introduction To Internet Of Things (12 Weeks)	NPTEL	Prof. Sudip Misra IIT Kharagpur

2		Basics of software defined Radios (4 Weeks)	NPTEL	Prof. Meenakshi Rawat IIT Roorkee
3		Principles of Signal Estimation for MIMO/ OFDM Wireless Communication (12 Weeks)	NPTEL	Prof. Aditya K. Jagannatham IIT Kanpur
4		Programming In Java (12 Weeks)	NPTEL	Prof. Debasis Samanta IIT Kharagpur
5		Fiber Optic Communication Technology (12 Weeks)	NPTEL	Prof. Deepa Venkatesh IIT Madras
6		Introduction to Wireless and Cellular Communications (12 Weeks)	NPTEL	Prof. R. David Koilpillai IIT Madras
7		Introduction to Computer and Network Performance Analysis using Queuing Systems (4 Weeks)	NPTEL	Prof. Varsha Apte IIT Bombay
8		LaTeX & XFig - typesetting software (06 Weeks)	AICTE	Prof Kannan Moudgalya, Principal Investigator of Spoken Tutorial Project Indian Institute of Technology Bombay

Synthesis and optimization of Digital circuits			
Course Code	22LEL31	CIE Marks	50
Teaching Hours/Week (L:P: SDA)	3:0:2	SEE Marks	50

Total Hours of Pedagogy	25 Hours of teaching and 10-12 sessions for Skill Development Activities	Total Marks	100
Credits	4	Exam Hours	03

Course Learning objectives:

- Understand the need for optimization and dimensions of optimization for digital circuits
- Understand the basic optimization techniques used in circuits design
- Understand advanced tools and techniques in digital systems design including Hardware Modelling and Compilation Techniques.
- Explain the details of Logic level Synthesis and optimization techniques for combinational and sequential circuits
- Explain the concept of scheduling and resource binding for optimization

Module-1

Introduction to Synthesis and optimization: Design of Microelectronics circuits, Computer aided Synthesis and Optimization.
Hardware Modeling: HDLs for Synthesis, Abstract models, Compilation and Behavioral Optimization.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-2

Graph theory for CAD for VLSI: Graphs, Combinatorial Optimization, Graph Optimization problems and Algorithms, Boolean Algebra and Applications.
Architectural Synthesis and Optimization: Fundamental Architectural Synthesis problems, Area and Performance Estimation, Strategies for Architectural Optimization, Datapath Synthesis, Control Path Synthesis.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-3

Two level Combinational Logic Optimization: Introduction, Logic Optimizations, Operations on Two level Logic Covers, Algorithms for Logic Minimization, Symbolic Minimization and Encoding Problems.
Multiple Level Combinational Logic Optimization: Introduction, Models and Transformations for Combinational Networks, The Algebraic Model, The Boolean Model.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-4

Sequential Logic Optimization: Introduction, Sequential Logic Optimization using State based Models, Sequential Logic Optimization using Network Models, Implicit FSM Traversal Methods, Testability concerns for Synchronous Circuits.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-5

Scheduling Algorithms: Introduction, A Model for Scheduling problems, Scheduling with Resource Constraints, Scheduling without Resource Constraints, Scheduling Algorithms for Extended Sequencing Models, Scheduling Pipelined Circuits.
Resource Sharing and Binding: Sharing and Binding for Resource dominated circuits, Sharing and Binding for General Circuits, Concurrent Binding and Scheduling.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks**

to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.

2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Text Book:

'Synthesis and Optimization of Digital Circuits', Giovanni De Micheli,Tata McGraw-Hill, ISBN: 9780070582781, 2003.

Reference Book:

'Automatic Logic synthesis Techniques for Digital Systems', EdwarsM.D, Macmillan New Electronic Series, 1992.

Skill Development Activities Suggested:

1. Interact with industry (small, medium, and large).
2. Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3. Involve in case studies and field visits/ fieldwork.
4. Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5. Handle advanced instruments to enhance technical talent.
6. Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7. Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc.

Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical – activities which will enhance their skill. The prepared report shall be evaluated for CIE marks.

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

1. Understand the process of synthesis and optimization in a top down approach for digital circuits models using HDLs.
2. Understand the terminologies of graph theory and its algorithms to optimize a Boolean equation.
3. Apply different two level and multilevel optimization algorithms for combinational circuits.
4. Apply the different sequential circuit optimization methods using state models and network models.
5. Apply different scheduling algorithms with resource binding and without resource binding for pipelined sequential circuits and extended sequencing models.

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Understand the process of synthesis and optimization in a top-down approach for digital circuits models using HDLs	L2
CO2	Understand the terminologies of graph theory and its algorithms to optimize a Boolean equation	L2
CO3	Apply the different two level and multilevel optimization algorithms for combinational circuits	L3
CO4	Apply different sequential circuits optimization methods using state models and network models	L2
CO5	Apply different scheduling algorithms with resource binding and without resource binding for pipelined sequential circuits and extended sequencing models	L3

Professional Elective 3

Advances in Image Processing			
Course Code	22LEL321	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	25 Hours of teaching and 10-12 sessions for Skill Development Activities	Total Marks	100
Credits	3	Exam Hours	03

Course Learning objectives:

1. To understand the image digitization techniques and properties.
2. To learn the need for image transforms different types of image transforms and their properties.
3. To introduce segmentation and morphological processing techniques.

Module-1

The image, its representations and properties: Image representations a few concepts, Image digitization, Digital image properties, Color images.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-2

Image Pre-processing: Pixel brightness transformations, geometric transformations, local pre-processing.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-3

Segmentation: Thresholding; Edge-based segmentation – Edge image thresholding, Edge relaxation, Border tracing, Hough transforms; Region –based segmentation – Region merging, Region splitting, Splitting and merging, Watershed segmentation, Region growing post-processing.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-4

Shape representation and description: Region identification; Contour-based shape representation and description – Chain codes, Simple geometric border representation, Fourier transforms of boundaries, Boundary description using segment sequences, B-spline representation; Region-based shape representation and description – Simple scalar region descriptors, Moments,Convex hull.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-5

Mathematical Morphology: Basic morphological concepts, Four morphological principles, Binary dilation and erosion, Skeletons and objectmarking, Morphological segmentations and watersheds.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks**

to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Text Book:

'Image Processing, Analysis, and Machine Vision', Milan Sonka, Vaclav Hlavac, Roger Boyle, Cengage Learning, ISBN: 978-81-315-1883-0, 2013

Reference Books:

1. 'Digital Image Processing for Medical Applications', Geoff Doughertry, Cambridge university Press, 2010.
2. 'Digital Image Processing', S Jayaraman, S Esakkirajan, T Veerakumar, Tata McGraw Hill, 2011.

Skill Development Activities Suggested:

1. Interact with industry (small, medium, and large).
2. Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3. Involve in case studies and field visits/ fieldwork.
4. Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5. Handle advanced instruments to enhance technical talent.
6. Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7. Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc.

Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical – activities which will enhance their skill. The prepared report shall be evaluated for CIE marks.

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Apply pre-processing techniques required to enhance the image for its further analysis.	L2
CO2	Use segmentation techniques to select the region of interest in the image for analysis.	L2
CO3	Represent the image based on its shape and edge information and also describe the objects present in the image based on its properties andstructure.	L3
CO4	Use morphological operations to simplify images, and quantify and preserve the main shape characteristics of the objects.	L3

CMOS RF Circuit Design			
Course Code	22LEL322	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	25 Hours of teaching and 10-12 sessions for Skill Development Activities	Total Marks	100
Credits	03	Exam Hours	3

Course Learning Objectives:

- To provide understanding of designing RF integrated circuits in state-of-the-art CMOS technology.
- To study transceiver, Low Noise Amplifiers, PLLs and other related concepts and circuits.

Module-1

Introduction to RF Design, Wireless Technology and Basic Concepts: A wireless world, RF design is challenging, The big picture. General considerations, Effects of Nonlinearity, Noise, Sensitivity and dynamic range, Passive impedance transformation. Scattering parameters, Analysis of nonlinear dynamic systems, conversion of gains and distortion.

Teaching-Learning Process	Chalk and Talk / Power Point Presentations.

Module-2

Communication Concepts: General concepts, analog modulation, digital modulation, spectral re-growth, coherent and non-coherent detection, Mobile RF communications, Multiple access techniques, Wireless standards, Appendix 1: Differential phase shift keying

Teaching-Learning Process	Chalk and Talk / Power Point Presentations.

Module-3

Transceiver Architecture: General considerations, Receiver architecture, Transmitter architectures, Direct conversion and two-step transmitters, RF testing for heterodyne, Homodyne, Image reject, Direct IF and sub sampled receivers.

Teaching-Learning Process	Chalk and Talk / Power Point Presentations.

Module-4

Low Noise Amplifiers and Mixers: General considerations, Problem of input matching, LNA topologies: common-source stage with inductive load, common-source stage with resistive feedback. Mixers-General considerations, passive down conversion mixers, Various mixers- working and implementation.

Teaching-Learning Process	Chalk and Talk / Power Point Presentations.

Module-5

VCO and PLLs- Oscillators- Basic topologies VCO and definition of phase noise, Noise power and trade off. Resonator VCO designs, Quadrature and single sideband generators. Radio frequency Synthesizers- PLLS, Various RF synthesizer architectures and frequency dividers, Power Amplifier design.

Teaching-Learning Process	Chalk and Talk / Power Point Presentations.

Assessment Details (both CIE and SEE)

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Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks**

to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.

2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

1. B. Razavi, "RF Microelectronics" second edition, PHI
2. R. Jacob Baker, H.W. Li, D.E. Boyce, "CMOS Circuit Design, layout and Simulation" PHI 1998
3. Thomas H. Lee, "Design of CMOS RF Integrated Circuits" Cambridge University press 1998
4. Y.P. Tsividis, "Mixed Analog and Digital Devices and Technology" , TMH 1996

Web links and Video Lectures (e-Resources):

1. https://nptel.ac.in/courses/108106105
2. https://www.youtube.com/watch?v=T0Kbt7CcqUA&list=PLQorUaRee4AEeyuqnpysZcGT4FFgRdkuM

Skill Development Activities Suggested:

1. Interact with industry (small, medium, and large).
2. Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3. Involve in case studies and field visits/ fieldwork.
4. Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5. Handle advanced instruments to enhance technical talent.
6. Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7. Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc.

Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical – activities which will enhance their skill. The prepared report shall be evaluated for CIE marks.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Analyze the effect of nonlinearity and noise in RF and microwave design.	L4
CO2	Exemplify the approaches taken in actual RF products	L2
CO3	Minimize the number of off-chip components required to design mixers, Low-Noise Amplifiers, VCO and PLLs.	L3
CO4	Explain various receivers and transmitter topologies with their merits and drawbacks.	L2
CO5	Demonstrate how the system requirements define the parameters of the circuits and the impact on the performance.	L2

Multimedia Communication			
Course Code	22LEL323	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	25 Hours of teaching and 10-12 sessions for Skill Development Activities	Total Marks	100
Credits	3	Exam Hours	03

Course Learning objectives:

- To learn the several multimedia networks and applications.
- To learn about the MPEG 4 systems.
- To study the multimedia communication across network.

Module-1	
Multimedia Communications: Multimedia information representation, multimedia networks, multimedia applications, network QoS and application of QoS.	
Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-2	
Information representation: Text, images, audio and video. Text and image compression, compression principles, text compression, image compression, Audio and video compression, audio compression, video compression, video compression principles, video compression standards: H.261,H.263,P1.323,MPEG1,MPEG2, other coding formats text, speech, image and video.	
Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-3	
Detailed Study of MPEG4: coding of audio visual objects, MPEG4 systems, MPEG4 audio and video, profiles and levels, MPEG 7 standardization process of multimedia content description, MPEG21 multimedia framework, Significant features of JPEG 2000, MPEG 4 transport across the internet.	
Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-4	
Synchronization: Notion of synchronization, presentation requirements, reference model for synchronization, Synchronization specification, Multimedia operating systems, Resource management, process management techniques.	
Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-5	
Multimedia Communication Across Networks: Layered video coding, error resilient video coding techniques, multimedia transport across IP networks and relevant protocols such as RSVP, RTP, RTCP, DVMRP, multimedia in mobile networks, multimedia in broadcast networks.	
Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks**

to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Text Books

1. Fred Halsall, "Multimedia Communications", Pearson Education, 2001
2. K. R Rao, Zoran S. Bojkovic, Dragorad A. Milovanovic, "Multimedia Communication Systems", Pearson Education, 2004.

Reference Books

1. Raifsteinmetz, Klara Nahrstedt, "Multimedia: Computing, Communications and Applications", Pearson Education, 2002
2. John Billamil, Louis Molina, "Multimedia An introduction", PHI 2002.

Skill Development Activities Suggested:

1. Interact with industry (small, medium, and large).
2. Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3. Involve in case studies and field visits/ fieldwork.
4. Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5. Handle advanced instruments to enhance technical talent.
6. Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7. Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc.

Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical – activities which will enhance their skill. The prepared report shall be evaluated for CIE marks.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Understand basics of different multimedia networks and applications	L2
CO2	Analyse different compression techniques to compress audio and video.	L3
CO3	Describe the MPEG4 and other systems	L2
CO4	Analyse synchronization and multimedia operating system	L3
CO5	Describe multimedia Communication across Networks.	L2

Automotive Electronics			
Course Code	22LEL324	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	25 Hours of teaching and 10-12 sessions for Skill Development Activities	Total Marks	100
Credits	3	Exam Hours	3

Course Learning Objectives:

- To introduce the fundamentals of automotive electronics.
- To create complete understanding of Sensors and actuators related to engine.
- To study the Digital Control systems of engine.
- To impart the knowledge of Bus architectures in automotive field.
- To know the Vehicle Electronics Architecture.

Module-1

Automotive Fundamentals Overview – Evolution of Automotive Electronics, Automobile Physical Configuration, Survey of Major Automotive Systems, The Engine – Engine Block, Cylinder Head, Four Stroke Cycle, Engine Control, Ignition System – Spark plug, High voltage circuit and distribution, Spark pulse generation, Ignition Timing, Diesel Engine, Drive Train -Transmission, Drive Shaft, Differential, Suspension, Brakes, Steering System Starter Battery -Operating principle: The Basics of Electronic Engine Control – Motivation for Electronic Engine Control – Exhaust Emissions, Fuel Economy, Concept of an Electronic Engine control system, Definition of General terms, Definition of Engine performance terms, Engine mapping, Effect of Air/Fuel ratio, spark timing and EGR on performance, Control Strategy, Electronic Fuel control system, Analysis of intake manifold pressure, Electronic Ignition.

Teaching-Learning Process	Chalk and talk, Power point presentation, NPTEL, VTU E-learning resources, Experimental learning, Problem based learning.

Module-2

Automotive Sensors – Automotive Control System applications of Sensors and Actuators -Variables to be measured, Airflow rate sensor, Strain Gauge MAP sensor, Engine Crankshaft Angular Position Sensor, Magnetic Reluctance Position Sensor, Hall effect Position Sensor, Shielded Field Sensor, Optical Crankshaft Position Sensor, Throttle Angle Sensor (TAS), Engine Coolant Temperature (ECT) Sensor, Exhaust Gas Oxygen (O2/EGO) Lambda Sensors, Piezoelectric Knock Sensor. Automotive Engine Control Actuators – Solenoid, Fuel Injector, EGR Actuator, Ignition System.

Teaching-Learning Process	Chalk and talk, Power point presentation, VTU E-learning resources, Experimental learning, Problem based learning

Module-3

Digital Engine Control Systems -Digital Engine control features, Control modes for fuel Control (Seven Modes), EGR Control, Electronic Ignition Control -Closed loop Ignition timing, Spark Advance Correction Scheme, Integrated Engine Control System-Secondary Air Management, Evaporative Emissions Canister Purge, Automatic System Adjustment, System Diagnostics.

Teaching-Learning Process	Chalk and talk, Power point presentation, NPTEL, VTU E-learning resources, Experimental learning, Problem based learning

Module-4

Automotive Networking -Bus Systems – Classification, Applications in the vehicle, Coupling of networks, Examples of networked vehicles Buses – CAN Bus, LIN Bus, MOST Bus, Bluetooth, Flex Ray, Diagnostic Interfaces. Vehicle Motion Control – Typical Cruise Control System, Digital Cruise Control System, Digital Speed Sensor, Throttle Actuator, Digital Cruise Control configuration, Cruise Control Electronics (Digital only), Antilock Brake System (ABS).

Teaching-Learning Process	Chalk and talk, Power point presentation, NPTEL, VTU E-learning resources, Experimental learning, Problem based learning

Module-5

Vehicle Electronics Architecture Introduction ,Instrument Cluster ,Heating and Cooling, Airbag Safety Traction and Stability , Power Assist Steering ,Avionics Fly-By-Wire (FBW) ,Automotive X- By-Wire, Tire Pressure Monitoring ,Modules Count , Straight-Wire-Switch Topology , Embedded Function, A Conventional Radio, An Embedded Radio ,Distributed Vehicle Architecture ,Custom Built Modules ,Modules Cross Compatibility , Integrating Dissimilar Functions ,Integrating Identical Functions: A Universal Module, Key-Off Load Current ,12V/42V Electrical Supply System , Vehicle Input Sensors and Switches 1.23 Vehicle Output Devices ,Vehicle Interior Lights Dimming ,H-Bridge Motor Driver , Microcontrollers Programming Options, Vehicle Operating Softwares.

Teaching-Learning Process	Chalk and talk, Power point presentation, NPTEL, VTU E-learning resources, Experimental learning, Problem based learning

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks**

to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Books

1. William B. Ribbens, Understanding Automotive Electronics, Seventh edition 2012, Elsevier Publishing.
2. Robert Bosch Gmbh (Ed) Bosch Automotive Electrics and Automotive Electronics Systems and Components, Networking and Hybrid Drive, 5th edition, John Wiley& Sons Inc., 2007.
3. Najamuz Zaman" Automotive Electronics Design Fundamentals, Springer International Publishing Switzerland 2015.

Web links and Video Lectures (e-Resources):

1. https://www.etf.ues.rs.ba/~slubura/Mehatronicki%20sistemi%20kod%20motora%20i%20vozila/Literatura/understanding%20automative%20electronics.pdf
2. https://link.springer.com/book/10.1007/978-3-319-17584-3.

Skill Development Activities Suggested:

1. Interact with industry (small, medium, and large).
2. Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3. Involve in case studies and field visits/ fieldwork.
4. Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5. Handle advanced instruments to enhance technical talent.
6. Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7. Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc. Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical –activities which will enhance their skill. The prepared report shall be evaluated for CIE marks.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Understand fundamentals of automotive electronics.	L2
CO2	Apply the Sensors and actuators on engine.	L3
CO3	Analyse the Digital Control systems of engine.	L4
CO4	Identify the Bus architectures in automotive field.	L1,L2
CO5	Gain the knowledge of Vehicle Electronics Architecture	L1,L2

VLSI Design for Signal Processing			
Course Code	22LEL325	CIE Marks	50
Teaching Hours/Week (L:P: SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	25 Hours of teaching and 10-12 sessions for Skill Development Activities	Total Marks	100
Credits	3	Exam Hours	03

Course Learning objectives:

- To learn performance optimization techniques in VLSI signal processing,
- Transformations for high speed and power reduction using pipelining, retiming, parallel processing techniques, supply voltage reduction as well as for strength or capacitance reduction,
- Area reduction using folding techniques, Strategies for arithmetic implementation,
- Synchronous, wave, and asynchronous pipelining

Module-1

Introduction to DSP Systems: Typical DSP Algorithms, DSP Application Demands and Scaled CMOS Technologies, Representations of DSP Algorithms.
Iteration Bounds: Data flow graph Representations, loop bound and Iteration bound. Algorithms for Computing Iteration Bound, Iteration Bound of multi rate data flow graphs.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-2

Pipelining and Parallel Processing: pipelining of FIR Digital Filters, parallel processing, Pipelining and parallel processing for low power. **Retiming**: Definition and Properties, Solving Systems of Inequalities, Retiming Techniques.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-3

Unfolding: An Algorithm for Unfolding, Properties of Unfolding, Critical path, Unfolding and Retiming, Application of Unfolding.
Folding: Folding Transformation, Register Minimization Techniques, Register Minimization in Folded Architectures, Folding of Multirate Systems.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-4

Systolic Architecture Design: systolic array design Methodology, FIR systolic array, Selection of Scheduling Vector, Matrix-Matrix Multiplication and 2D systolic Array Design, Systolic Design for space representation containing Delays.
Fast convolution: Cook-Toom Algorithm, Winograd Algorithm, Iterated convolution, cyclic convolution Design of fast convolution Algorithm by Inspection.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-5

Pipelined and Parallel Recursive and Adaptive Filter: Pipeline Interleaving in Digital Filter, first order IIR digital Filter, Higher order IIR digital Filter, parallel processing for IIR filter, Combined pipelining and parallel processing for IIR Filter, Low power IIR Filter Design Using Pipelining and parallel processing, pipelined adaptive digital filter.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks**

to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.

3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Text Books

VLSI Digital Signal Processing systems, Design and implementation Keshab K.Parthi Wiley 1999

Reference Book

1. Analog VLSI Signal and Information Processing Mohammed Isamail and Terri Fiez Mc Graw-Hill 1994
2. VLSI and Modern Signal Processing S.Y. Kung, H.J. White House, T. Kailath Prentice Hall 1985
3. Design of Analog - Digital VLSI Circuits for Telecommunication and Signal Processing Jose E. France, Yannis Tsividis Prentice Hall 1994
4. DSP Integrated Circuits Lars Wanhammar Academic Press Series in Engineering 1st Edition

Skill Development Activities Suggested:

1. Interact with industry (small, medium, and large).
2. Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3. Involve in case studies and field visits/ fieldwork.
4. Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5. Handle advanced instruments to enhance technical talent.
6. Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7. Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc.

Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical – activities which will enhance their skill. The prepared report shall be evaluated for CIE marks.

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

1. Apply unfolding in the design of parallel architecture
2. Develop an algorithm or architecture or circuit design for DSP applications

At the end of the course the student will be able to:

Sl. No.	Description	Blooms Level
CO1	Illustrate the use of various DSP algorithms and addresses their representation using block diagrams, signal flow graphs and data-flow graphs	L2
CO2	Use pipelining and parallel processing in design of high-speed /low-power applications	L2
CO3	Apply unfolding in the design of parallel architecture	L3
CO4	Evaluate the use of look-ahead techniques in parallel and pipelined IIR Digital filters.	L3

Professional electives 4

Antenna Theory and Design			
Course Code	22LEL331	CIE Marks	50
Teaching Hours/Week (L:P: SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	25 Hours of teaching and 10-12 sessions for Skill Development Activities	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives:

- To classify different types of antennas
- To define and illustrate various types of array antennas
- To design antennas like Yagi-Uda, Helical antennas and other broad band antennas
- To describe different antenna synthesis methods
- To apply methods like Method of Moments, Pocklington's integral equation, Source modelling.

Module-1

Antenna Fundamentals and Definitions: Radiation Mechanisms, Overview, EM Fundamentals, Solution of Maxwell's Equations for Radiation Problems, Ideal Dipole, Radiation patterns, Directivity and Gain, Antenna impedance, Radiation efficiency, Antenna polarization.

Teaching-Learning Process	Chalk and Talk / Power Point Presentations

Module-2

Arrays: Array factor for linear arrays, uniformly excited equally spaced linear arrays, Pattern multiplication, Directivity of linear arrays, Nonuniformly excited equally spaced linear arrays, Mutual coupling.
Antenna Synthesis: Formulation of the synthesis problem, Synthesis principles, Line sources shaped beam synthesis, Linear array shaped beam synthesis, Fourier series, Woodward - Lawson sampling method, Comparison of shaped beam synthesis methods, low side lobe narrow main beam synthesis methods, Dolph Chebyshev linear array, Taylor line source method.

Teaching-Learning Process	Chalk and Talk / Power Point Presentations

Module-3

Resonant Antennas: Wires and Patches, Dipole antenna, Yagi-Uda antennas, Micro-strip antenna.
Broadband antennas: Traveling wave antennas Helical antennas, Biconical antennas, Sleeve antennas, and Principles of frequency independent antennas, Spiral antennas, and Log - periodic antennas.

Teaching-Learning Process	Chalk and Talk / Power Point Presentations

Module-4

Aperture antennas: Techniques for evaluating gain, Reflector antennas, Parabolic reflector antenna principles, Axi-symmetric parabolic reflector antenna, offset parabolic reflectors, Dual reflector antennas, Gain calculations for reflector antennas, Feed antennas for reflectors, Field representations, Matching the feed to the reflector, General feed model, Feed antennas used in practice.

Teaching-Learning Process	Chalk and Talk / Power Point Presentations

Module-5

Antenna in systems & Measurements: Receiving properties of antennas, Antenna temperature & radiometry.
CEM for antennas: The method of moments: Introduction of the methods moments, Pocklington's integral equation, Integral equation and Kirchhoff's networking equations, Source modelling weighted residual formulations and computational consideration, Calculation of antenna and scatter characteristics.

Teaching-Learning Process	Chalk and Talk / Power Point Presentations

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks**

to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

.

Suggested Learning Resources:

Books

1. 'Antenna Theory and Design', Stutzman and Thiele, John Wiley, 2nd Edition, 2010

Reference Books

1. 'Antenna Theory Analysis and Design', C. A. Balanis, John Wiley, 2nd Edition, 2007
2. 'Antennas and Wave Propagation', J. D. Krauss, McGraw Hill TMH, 4th Edition, 2010
3. 'Antennas and propagation', A.R.Harish, M.Sachidanada, Pearson Education, 2015

Web links and Video Lectures (e-Resources):

1. https://www.youtube.com/watch?v=fIbdW0NGIU0
2. https://nptel.ac.in/courses/117107035

Skill Development Activities Suggested:

1. Different types of antenna synthesis or technical seminar on advanced types of antennas.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc.

Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical – activities which will enhance their skill. The prepared report shall be evaluated for CIE marks.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Classify different types of antennas	L1 L2
CO2	Define and illustrate various types of array antennas	L1 L2
CO3	Design antennas like Yagi-Uda, Helical antennas and other broad band antennas	L2
CO4	Describe different antenna synthesis methods	L2
CO5	Apply methods like Method of Moments, Pocklington's integral equation, Source modelling.	L3

Probability Theory and Random Process			
Course Code	22LEL332	CIE Marks	50
Teaching Hours/Week (L:P: SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	25 Hours of teaching and 10-12 sessions for Skill Development Activities	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives:

- To understand Discrete and Continuous Random variables, Random Processes and their applications inElectronic Transmissions.
- To apply concepts of Probability to solve problems in communication Engineering.
- To find functional relationship between random inputs and outputs with the use of Random ProcessTechniques
- Analyse about the correlation Functions.

Module-1

Probability and Random Variable Probability: Set theory, Experiments and Sample Spaces, Discrete and Continuous Sample Spaces, Events, Probability Definitions and Axioms, Mathematical Model of Experiments, Joint Probability, Conditional Probability, Total Probability, Bayes' Theorem, and Independent Events, Bernoulli's trials. The Random Variable: Definition of a Random Variable, Conditions for a Function to be a Random Variable, Discrete and Continuous, Mixed Random Variable.

Teaching-Learning Process	Chalk and Talk / Power Point Presentations

Module-2

Distribution and density functions and Operations on One Random Variable Distribution and density functions: Distribution and Density functions, Properties, Binomial, Poisson, Uniform, Exponential Gaussian, Rayleigh and Conditional Distribution, Methods of defining Conditioning Event, Conditional Density function and its properties, problems.

Operation on One Random Variable: Expected value of a random variable, function of a random variable, moments about the origin, central moments, variance and skew, characteristic function, moment generating function, transformations of a random variable, monotonic transformations for a continuous random variable, non- monotonic transformations of continuous random variable, transformations of Discrete random variable.

Teaching-Learning Process	Chalk and Talk / Power Point Presentations

Module-3

Multiple Random Variables and Operations on Multiple Random Variables Multiple Random Variables: Vector Random Variables, Joint Distribution Function and Properties, Joint density Function and Properties, Marginal Distribution and density Functions, conditional Distribution and density Functions, Statistical Independence, Distribution and density functions of Sum of Two Random Variables and Sum of Several Random Variables, Central Limit Theorem - Unequal Distribution, **Equal Distributions Operations on Multiple Random Variables:** Expected Value of a Function of Random Variables, Joint Moments about the Origin, Joint Central Moments, Joint Characteristic Functions, and **Jointly Gaussian Random Variables:** Two Random Variables case and N Random Variable case, Properties, Transformations of Multiple Random Variables.

Teaching-Learning Process	Chalk and Talk / Power Point Presentations

Module-4

Stochastic Processes-Temporal Characteristics: The Stochastic process Concept, Classification of Processes, Deterministic and Nondeterministic Processes, Distribution and Density Functions.

Statistical Independence and concept of Stationarity: First-Order Stationary Processes, Second Order and Wide-Sense Stationarity, Nth-Order and Strict-Sense Stationarity, Time Averages and 1 Ergodicity, Mean-Ergodic Processes, Correlation-Ergodic Processes Autocorrelation Function and Its Properties, Cross-Correlation Function and Its Properties, Covariance Functions and its properties, Gaussian Random Processes.

Linear system Response: Mean and Mean-squared value, Autocorrelation, Cross-Correlation Functions.

Teaching-Learning Process	Chalk and Talk / Power Point Presentations

Module-5

Stochastic Processes-Spectral Characteristics: The Power Spectrum and its Properties, Relationship between Power Spectrum and Autocorrelation Function, the Cross-Power Density Spectrum and Properties, Relationship between Cross-Power Spectrum and Cross-Correlation Function.

Spectral characteristics of system response: power density spectrum of response, cross power spectral density of input and output of a linear system.

Teaching-Learning Process	Chalk and Talk / Power Point Presentations

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks**

to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

.

Suggested Learning Resources:

Text Books

1. Probability, Random Variables & Random Signal Principles -Peyton Z. Peebles, TMH, 4th Edition, 2001.
2. Probability and Random Processes-Scott Miller, Donald Childers,2nd Edition, Elsevier,2012.

Skill Development Activities Suggested:

1. Online certification course on probability and random process.
2. Mini projects can be suggested on the related area.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc.

Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical – activities which will enhance their skill. The prepared report shall be evaluated for CIE marks.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Understand Discrete and Continuous Random variables, Random Processes and their applications in Electronic Transmissions	L2
CO2	To apply concepts of Probability to solve problems in communication Engineering.	L3
CO3	To find functional relationship between random inputs and outputs with the use of Random Process Techniques	L3
CO4	Analyse about the correlation Functions	L4

Statistical Signal Processing			
Course Code	22LEL333	CIE Marks	50
Teaching Hours/Week (L:P: SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	25 Hours of teaching and 10-12 sessions for Skill Development Activities	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives:

- Understand random processes and its properties
- Understand the basic theory of signal detection and estimation
- Identifytheengineeringproblemsthatcanbeputintotheframeofstatisticalsignal processing
- Solvetheidentifiedproblemsusingthestandardtechniqueslearnedthroughthiscourse.
- Makecontributionstothetheoryandthepracticeofstatisticalsignalprocessing.

Module-1

Random Processes: Random variables, random processes, white noise, filtering random processes, spectral factorization, ARMA, AR and MA processes.

Teaching-Learning Process	Chalk and Talk / Power Point Presentations

Module-2

Signal Modelling: Least squares method, Pade approximation, Prony's method, finite data records, stochastic models, Levinson-Durbin recursion; Schur recursion; Levinson recursion.

Teaching-Learning Process	Chalk and Talk / Power Point Presentations

Module-3

Spectrum Estimation: Non parametric methods, minimum-variance spectrum estimation, maximum entropy method, parametric methods, frequency estimation, principal components spectrum estimation.

Teaching-Learning Process	Chalk and Talk / Power Point Presentations

Module-4

Optimal and Adaptive Filtering: FIR and IIR Wiener filters, Discrete Kalman filter, **FIRAdaptive filters:** Steepest descent, LMS, LMS-based algorithms, adaptive recursive filters, RLS algorithms.

Teaching-Learning Process	Chalk and Talk / Power Point Presentations

Module-5

Array Processing: Array fundamentals, beam-forming, optimum array processing, performance considerations, adaptive beam-forming, linearly constrained minimum-variance beam-formers,side-lobe cancellers.

Teaching-Learning Process	Chalk and Talk / Power Point Presentations

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks**

to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

.

Suggested Learning Resources:

Text Books

1. Monson H. Hayes, "Statistical Digital Signal Processing and Modeling",John Wiley & Sons (Asia) Pvt. Ltd.,2002.
2. Dimitris G. Manolakis, Vinay K. Ingle, and Stephen M. Kogon, "Statistical and Adaptive Signal Processing : Spectral Estimation, Signal Modeling, Adaptive Filtering and Array Processing" ,McGraw-Hill International Edition, 2000.

Web links and Video Lectures (e-Resources):

- https://www.youtube.com/watch?v=o1qL2Eb87Ew&list=PLwdnzlV3ogoVj-FLNpzXInhZxcnibqb56
- https://www.youtube.com/watch?v=QqqA7V47z7A&list=PLItUftQ-Nkb90TGFxTv8I8LXGgQZyJUC9

Skill Development Activities Suggested:

1. Mathematical modelling of signals: linear vs. nonlinear, deterministic signals, random signals, unknown parameters.
2. Mathematical modelling of noise: white Gaussian noise, coloured Gaussian noise, general Gaussian noise, IID non-Gaussian noise.
3. Specific algorithms for estimation, detection, and spectral estimation: parameter estimation, signal extraction, adaptive filtering, sinusoidal estimation, matched filters, estimator-correlator, spectral estimation via Fourier and high-resolution methods.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc.

Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical – activities which will enhance their skill. The prepared report shall be evaluated for CIE marks.

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

Sl. No.	Description	Blooms Level
CO1	Design statistical DSP algorithms to meet desired needs	L4
CO2	Apply vector space methods to statistical signal processing problems	L3
CO3	Identify the engineering problems that can be put into the frame ofstatistical signal processing	L2
CO4	Understand Wiener filter theory and design discrete and continuous Wiener filters	L2
CO5	Understand Kalman Filter theory and design discrete Kalman filters	L2

Artificial Intelligence and Machine Learning			
Course Code	22LEL334	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	25 Hours of teaching and 10-12 sessions for Skill Development Activities	Total Marks	100
Credits	3	Exam Hours	03

Course Learning objectives:

- To describe artificial intelligence & machine learning
- To analyse the support vector machine algorithms

Module-1

Introduction: Introduction to Agents and environment; Rationality; the nature of environment; the structure of agents. Problem solving: Problem-solving agents; Example problems; Searching for solution; uninformed search strategies. Informed Search and Exploration: Informed search strategies; Heuristicfunctions; Constraint Satisfaction: Backtracking search for CSPs.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-2

Knowledge and Reasoning: Logical Agents: Knowledge-based agents; The Wumpus world as an example world; Logic; propositional logic: A very Simple Logic: Reasoning patterns in propositional logic; Effective propositional inference; Agents based on propositional logic. First-Order Logic, Inference in First-Order Logic – 1 : Representation revisited; Syntax and semantics of first-order logic; Using first-order logic; Knowledge engineering in first-order logic

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-3

Inference in First-Order Logic – 2: Propositional versus first-order inference; Unification and lifting forward chaining; backward chaining; Resolution.
Knowledge Representation: Ontological engineering; Categories and objects; Actions, situations, and events; Mental events and mental objects; The Internet shopping world; Reasoning systems for categories; Reasoning with default information; Truth maintenance systems.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-4

Uncertainty Measure: Probability Theory, Bayesian Belief Networks,
Machine Learning Paradigms: Machine learning system, supervised and unsupervised learnings,Inductive, deductive learning, Clustering

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-5

Support vector Machine, case-based reasoning and learning. ANN: Single Layer, Multilayer. RBF, Design issues in ANN, Recurrent Network

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks**

to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.

2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Text Books

1. Artificial Intelligence A Modern Approach: Stuart Russel and Peter Norvig, 2nd Edition, Pearson Education, 2003.
2. Artificial Intelligence: Saroj Kaushik Cengage Learning2014 Edition
3. Artificial Intelligence: Structuresand Strategies for Complex Problem-Solving George F Luger Pearso Addison Wesley 6th Ed, 2008.
4. Artificial Intelligence: Elaine Rich, Kevin Knight, 3rd Edition, Tata McGraw Hill, 2009.
5. Principles of Artificial Intelligence: Nils J. Nilsson, Elsevier, 1980.

Web links and Video Lectures (e-Resources):

1. https://www.mooc.org/
2. https://onlinecourses.nptel.ac.in/

Skill Development Activities Suggested:

1. Experiments to be performed on artificial intelligence and machine learning using Matlab software

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc.

Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical – activities which will enhance their skill. The prepared report shall be evaluated for CIE marks.

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

Sl. No.	Description	Blooms Level
CO1	Able to understand the agents and environment in artificial intelligence	L2
CO2	Able to understand and analyse the knowledge and reasoning in artificial intelligence	L2 L4
CO3	Able to analyse the machine learning paradigms	L4
CO4	Able to understand and analyse support vector machine for classifications	L2 L4

IoT			
Course Code	22LEL335	CIE Marks	50
Teaching Hours/Week (L:P: SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	25 Hours of teaching and 10-12 sessions for Skill Development Activities	Total Marks	100
Credits	3	Exam Hours	03

Course Learning objectives:

- To understand the concepts of IOT and its applications in today's scenario.
- To study the IoT network architecture and design.
- To understand IOT content generation and transport through networks.
- To know the devices employed for IOT data acquisition and use cases of IoT.

Module-1

What is IoT?: Genesis, Digitization, Impact, Challenges

IoT Network Architecture and Design: Drivers behind new network Architectures, M2M architecture, IoT world forum standard architecture, Simplified IoT Architecture

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentation

Module-2

IoT Network Architecture and Design: Core IoT Functional Stack, Layer1 (Sensors and Actuators), Layer2 (Communications Sublayer), Access network sublayer, Gateways and backhaul sublayer, Network transport sublayer, IoT Network management.**,** Layer3 (Applications and Analytics), IoT Data Management and Compute Stack

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentation

Module-3

Engineering IoT Networks: Things in IoT – Sensors, Actuators, MEMS and smart objects. Communications Criteria – Range, Frequency bands, power consumption, Topology, Constrained Devices, Constrained Node Networks IoT Access Technologies - IEEE802.15.4

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentation

Module-4

Engineering IoT Networks: IP as IoT network layer – Key Advantages, Optimization, Optimizing IP for IoT. Application Protocols for IoT – Transport Layer, Application Transport layer, IoT Application Layer Data and Analytics for IoT – IoT Data Analytics overview and Challenges.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentation

Module-5

IoT in Industry: IoT Strategy for Connected manufacturing, Architecture for Connected Factory Utilities – Power utility, IT/OT divide, Grid blocks reference model Smart and Connected cities – Strategy, Smart city network Architecture, Street layer, city layer, Data center layer, services layer

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentation

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks**

to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each

module.

4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

.

Suggested Learning Resources:

1. David Hanes, Gonzalo Salgueiro, Patrick Grossetete, Robert Barton, Jerome Henry, "Cisco, IOT Fundamentals – Networking Technologies, Protocols, Use Cases for IOT", Pearson Education; First edition 2017, ISBN: 978-9386873743.
2. Arshdeep Bahga and Vijay Madisetti, "Internet of Things – A Hands on Approach", Orient Blackswan Private Limited - New Delhi; First edition.

Web links and Video Lectures (e-Resources):

1. https://archive.nptel.ac.in/courses/106/105/106105166/
2. https://www.youtube.com/watch?v=urUBLmXFKl0&list=PLgMDNELGJ1CaBrefq-0eYatfOnoncW0y-
3. https://www.youtube.com/watch?v=Yci9PfPppiw&list=PLgMDNELGJ1CZoUIF-iKcH9TSVcmG6IBcU

Skill Development Activities Suggested:

1. Interact with industry (small, medium, and large).
2. Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3. Involve in case studies and field visits/ fieldwork.
4. Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5. Handle advanced instruments to enhance technical talent.
6. Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7. Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc.

Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical – activities which will enhance their skill. The prepared report shall be evaluated for CIE marks.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Understand the basic concepts IoT Architecture and devices employed.	L1, L2
CO2	Analyze the sensor data generated and map it to IoT protocol stack for transport.	L2, L3
CO3	Apply communications knowledge to facilitate transport of IoT data over various available communications media.	L2, L3
CO4	Design a use case for a typical application in real life ranging from sensing devices to analyzing the data available on a server to perform tasks on the device.	L3, L4
CO5	Apply knowledge of Information technology to design the IoT applications.	L3, L4

Project Work phase-1			
Course Code	22LEL34	CIE Marks	100
Teaching Hours/Week (L:P: SDA)	0:6:0	SEE Marks	-
Total Hours of Pedagogy	Practical	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives:

- To support independent learning.
- To guide to select and utilize adequate information from varied resources maintaining ethics.
- To guide to organize the work in the appropriate manner and present information (acknowledging the sources) clearly.
- To develop interactive, communication, organisation, time management, and presentation skills.
- To impart flexibility and adaptability.
- To inspire independent and team working.
- To expand intellectual capacity, credibility, judgement, intuition.
- To adhere to punctuality, setting and meeting deadlines.
- To instil responsibilities to oneself and others.
- To train students to present the topic of project work in a seminar without any fear, face audience confidently, enhance communication skill, involve in group discussion to present and exchange ideas.

Project Phase-1

Students in consultation with the guide/s shall carry out literature survey/ visit industries to finalize the topic of the Project. Subsequently, the students shall collect the material required for the selected project, prepare synopsis and narrate the methodology to carry out the project work.

Seminar: Each student, under the guidance of a Faculty, is required to

- Present the seminar on the selected project orally and/or through power point slides.
- Answer the queries and involve in debate/discussion.
- Submit two copies of the typed report with a list of references.

The participants shall take part in discussion to foster friendly and stimulating environment in which the students are motivated to reach high standards and become self-confident.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Demonstrate a sound technical knowledge of their selected project topic.	L2
CO2	Undertake problem identification, formulation and solution.	L4
CO3	Design engineering solutions to complex problems utilising a systems approach.	L3
CO4	Justify with engineers and the community at large in written an oral form.	L5
CO5	Demonstrate the knowledge, skills and attitudes of a professional engineer.	L2

Continuous Internal Evaluation CIE marks for the project report (50 marks), seminar (25 marks) and question and answer (25 marks) shall be awarded (based on the quality of report and presentation skill, participation in the question and answer session by the student) by the committee constituted for the purpose by the Head of the Department. The committee shall consist of three faculty from the department with the senior most acting as the Chairperson.

Societal Project			
Course Code	22LEL35	CIE Marks	100
Teaching Hours/Week (L:P: SDA)	0:6:0	SEE Marks	-
Total Hours of Pedagogy	Practical	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives:

- To support independent learning.
- To guide to select and utilize adequate information from varied resources maintaining ethics.
- To guide to organize the work in the appropriate manner and present information (acknowledging the sources) clearly.
- To develop interactive, communication, organisation, time management, and presentation skills.
- To impart flexibility and adaptability.
- To inspire independent and team working.
- To expand intellectual capacity, credibility, judgement, intuition.
- To adhere to punctuality, setting and meeting deadlines.
- To instil responsibilities to oneself and others.
- To train students to present the topic of project work in a seminar without any fear, face audience confidently, enhance communication skill, involve in group discussion to present and exchange ideas.

Societal Project

Each student of the project batch shall involve in carrying out the project work jointly in constant consultation with internal guide, co-guide, and external guide and prepare the project report as per the norms avoiding plagiarism.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Demonstrate the Societal Project and be able to defend it.	L2
CO2	Undertake links across different areas of knowledge and to generate, develop and evaluate ideas and information so as to apply these skills to the project task.	L4
CO3	Habituated to critical thinking and use problem solving skills.	L3
CO4	Justify effectively and to present ideas clearly and coherently in both the written and oral forms.	L5
CO5	Demonstrate Work in a team to achieve common goal.	L2

CIE procedure for Societal Project: The CIE marks awarded for Mini - Project, shall be based on the evaluation of Mini - Project Report, Project Presentation skill and Question and Answer session in the ratio 50:25:25. The marks awarded for Mini - Project report shall be the same for all the batch mates.

Internship			
Course Code	22LELI36	CIE Marks	50
Teaching Hours/Week (L:P: SDA)	(06 weeks Internship Completed during the intervening vacation of II and III semesters.)	SEE Marks	50
Total Hours of Pedagogy	Practical	Total Marks	100
Credits	06	Exam Hours	03

Course Learning objectives:

Internship/Professional practice provide students the opportunity of hands-on experience that include personal training, time and stress management, interactive skills, presentations, budgeting, marketing, liability and risk management, paperwork, equipment ordering, maintenance, responding to emergencies etc.

The objectives are further,

- To put theory into practice.
- To expand thinking and broaden the knowledge and skills acquired through course work in the field. • To relate to, interact with, and learn from current professionals in the field.
- To gain a greater understanding of the duties and responsibilities of a professional.
- To understand and adhere to professional standards in the field.
- To gain insight to professional communication including meetings, memos, reading, writing, public speaking, research, client interaction, input of ideas, and confidentiality.
- To identify personal strengths and weaknesses.
- To develop the initiative and motivation to be a self-starter and work independently.

Internship/Professional practice: Students under the guidance of internal guide/s and external guide shall take part in all the activities regularly to acquire as much knowledge as possible without causing any inconvenience at the place of internship.

Seminar: Each student, is required to

- Present the seminar on the internship orally and/or through power point slides.
- Answer the queries and involve in debate/discussion.
- Submit the report duly certified by the external guide.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Demonstrate knowledge of the industry in which the internship is done.	L2
CO2	Apply knowledge and skills learned to classroom work.	L3
CO3	Develop a greater understanding about career options while more clearly defining personal career goals.	L6
CO4	Develop and refine oral and written communication skills.	L6
CO5	Identify areas for future knowledge and skill development.	L2

Continuous Internal Evaluation: CIE marks for the Internship/Professional practice report (20 marks), seminar (10 marks) and question and answer session (10 marks) shall be awarded (based on the quality of report and presentation skill, participation in the question-and-answer session by the student) by the committee constituted for the purpose by the Head of the Department. The committee shall consist of three faculty from the department with the senior most acting as the Chairperson.

Semester End Examination: SEE marks for the Internship Report (30 Marks), Seminar (15 Marks) and Question and Answer Session (15 marks) shall be awarded (based on the quality of report and presentation skill, participation in the question-and-answer session) by the examiners appointed by the University.

Project work phase -2			
Course Code	22LEL41	CIE Marks	100
Teaching Hours/Week (L:P: SDA)	0:8	SEE Marks	100
Total Hours of Pedagogy	(06 weeks Internship Completed during the intervening vacation of II and III semesters.)	Total Marks	200
Credits	18	Exam Hours	03

Course Learning objectives:

- To support independent learning.
- To guide to select and utilize adequate information from varied resources maintaining ethics.
- To guide to organize the work in the appropriate manner and present information (acknowledging the sources) clearly.
- To develop interactive, communication, organisation, time management, and presentation skills.
- To impart flexibility and adaptability.
- To inspire independent and team working.
- To expand intellectual capacity, credibility, judgement, intuition.
- To adhere to punctuality, setting and meeting deadlines.
- To instil responsibilities to oneself and others.
- To train students to present the topic of project work in a seminar without any fear, face audience confidently, enhance communication skill, involve in group discussion to present and exchange ideas.

Project Work Phase - II: Each student of the project batch shall involve in carrying out the project work jointly in constant consultation with internal guide, co-guide, and external guide and prepare the project report as per the norms avoiding plagiarism.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Demonstrate the project and be able to defend it.	L2
CO2	Apply links across different areas of knowledge and to generate, develop and evaluate ideas and information so as to apply these skills to the project task..	L3
CO3	Develop a critical thinking and use problem solving skills.	L6
CO4	Develop effectively and to present ideas clearly and coherently in both the written and oral forms.	L6
CO5	Identify on their own, reflect on their learning and take appropriate actions to improve it.	L2

Continuous Internal Evaluation: Project Report: 20 marks. The basis for awarding the marks shall be the involvement of the student in the project and in the preparation of project report. To be awarded by the internal guide in consultation with external guide if any.
Project Presentation: 10 marks. The Project Presentation marks of the Project Work Phase -II shall be awarded by the committee constituted for the purpose by the Head of the Department. The committee shall consist of three faculty from the department with the senior most acting as the Chairperson.
Question and Answer: 10 marks. The student shall be evaluated based on the ability in the Question-and-Answer session for 10 marks.

Semester End Examination: SEE marks for the Internship Report (30 Marks), Seminar (15 Marks) and Question and Answer Session (15 marks) shall be awarded (based on the quality of report and presentation skill, participation in the question-and-answer session) by the examiners appointed by the University.