ADVANCED CONTROL SYSTEM			
Course Code	22LIE12	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:2:0	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory + 10-12 Lab slots	Total Marks	100
Credits	04	Exam Hours	03

Course objectives:

1. To define and explain the basic properties of difference equations, Z- transform, inverse Z-transform, Z - Transform Analysis of Sampled data Control Systems.
2. To acquire the knowledge of state models and solve relevant problems using state equations.
3. To acquire knowledge of state space and state feedback in modern control systems, pole placement, design of state observers and output feedback controllers.
4. To explain the concept of Dead beat Control by State Feedback, solving problems using State Variable approach, State regulator and Output regulator, understanding Concepts of Model Reference Adaptive Control.
5. To understand the behaviour of nonlinear systems, nonlinearities, Stability Analysis by Describing Function Method, Phase Plane Method.

MODULE-1	
Digital Control Systems: Review of Difference equations, Z – transforms and Inverse Z transforms, The Z-transfer function(Pulse transfer function), The Z - Transform Analysis of Sampled data Control Systems, The Z and S - domain relationship, Stability analysis (Jury's Stability Test and Bilinear Transformation).	
Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos
MODULE-2	
State Models & Solution of State equations: State models for Linear Continuous Time and Linear Discrete Time systems, Diagonalization, Solution of State Equations (for both Continuous and Discrete Time systems), Relevant problems.	
Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos
MODULE-3	
State Feedback Systems: Concepts of Controllability and Observability (for both Continuous and Discrete Time systems),Pole Placement by State Feedback(for both continuous and discrete Time systems), Observer System (Full order and Reduced order observers for both Continuous and Discrete Time systems),Relevant problems	
Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos
MODULE-4	
Regulators: Dead beat Control by State Feedback, Optimal control problems using State Variable approach, State regulator and Output regulator, Concepts ofModel Reference Adaptive Control(MRAC).	
Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos
MODULE 5	
Nonlinear Control Systems: Behavior of Nonlinear Systems, Common Physical Nonlinearities, Describing Function Method, Stability Analysis by Describing Function Method, Phase Plane Method, Stability Analysis by Phase Plane Method.	
Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

PRACTICAL COMPONENT OF IPCC

Sl. NO	Experiments
1	Study and verification of step response of standard second order system (both analog and digital system), (MATLAB), for the cases of undamped, under damped and critically damped cases.

2	To design a Lag-Lead compensator and to obtain the characteristics by simulation using MATLAB. Verify the performance using experiments with the compensator circuit made of passive elements
3	Steady state error analysis for Type-0, Type-1, Type-2 digital control system using MATLAB by applying standard reference inputs of step , ramp and parabola.
4	Design a digital controller with output feedback to control the speed of a DC motor; simulate the design using Simulink.
5	Design a digital controller with state variable feedback to control the speed of a DC motor; simulate the design using Simulink.
6	Design a digital controller with output feedback to control the position of the metallic ball in Magnetic levitation experiment and simulate the design using Simulink
7	Design a digital controller with state variable feedback to control the position of the metallic ball in Magnetic levitation experiment.
8	Implement an on-off temperature controller to control lamp using a temperature sensor and dspace DS1104 hardware interface
9	Design a digital controller with output feedback to control the speed of a DC motor; Control the DC motor using dspace DS1104 hardware interface
10	Design a digital controller with state variable feedback to control the speed of a DC motor; Control the DC motor using dspace DS1104 hardware interface

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together

CIE for the theory component of IPCC

1. Two Tests each of **20 Marks**
2. Two assignments each of **10 Marks/One Skill Development Activity of 20 marks**
3. Total Marks of two tests and two assignments/one Skill Development Activity added will be CIE for 60 marks, marks scored will be proportionally scaled down to **30 marks**.

CIE for the practical component of IPCC

1. On completion of every experiment/program in the laboratory, the students shall be evaluated and marks shall be awarded on the same day. The**15 marks** are for conducting the experiment and preparation of the laboratory record, the other **05 marks shall be for the test** conducted at the end of the semester.
2. The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to 15 marks.
3. The laboratory test at the end /after completion of all the experimentsshall be conducted for 50 marks and scaled down to 05 marks**.**

Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **20 marks**.

.

SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (duration 03 hours)

1. The question paper will be set for 100 marks and marks scored will be scaled down proportionately to 50 marks.

2. The question paper will have ten questions. Each question is set for 20 marks.
3. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
4. The students have to answer 5 full questions, selecting one full question from each module.

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper shall include questions from the practical component).

1. The minimum marks to be secured in CIE to appear for SEE shall be the 15 (50% of maximum marks-30) in the theory component and 10 (50% of maximum marks -20) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included**.** The maximum of 04/05 questions to be set from the practical component of IPCC, the total marks of all questions should not be more than the 20 marks.
2. SEE will be conducted for 100 marks and students shall secure 40% of the maximum marks to qualify in the SEE. Marks secured will be scaled down to 50. (Student has to secure an aggregate of 50% of maximum marks of the course(CIE+SEE)

Suggested Learning Resources:

Text Books

1. 'Control Systems Engineering', IJ Nagrath& MGopal, New AgeInternational Publishers, Fifth edition, 2007.
2. 'Discrete Time Control Systems', K Ogata, 2nd edition, PHI, 2009.

Reference Books

1. 'Modern Control Engineering', K Ogata, PHI, 5th Edition, 2010.
2. 'Modern Control System Theory', M Gopal,New Age International, 2012.
3. 'Digital Control and State Variable methods', M Gopal, Tata McGraw Hill, 4thedition, 2012.
4. 'Advanced Control Theory', A Nagoorkani, RBA publications, 2006.

Web links and Video Lectures (e-Resources):

www.nptel.ac.in

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1		L3
CO2		L3
CO3		L4
CO4		L4
CO5	Explain the behaviour of nonlinear systems, nonlinearities, Stability Analysis by Describing Function Method, Phase Plane Method.	L3

ADVANCED D S P			
Course Code	22LIE13	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:0:2	SEE Marks	50
Total Hours of Pedagogy	50	Total Marks	100
Credits	04	Exam Hours	03

Course Learning objectives:

1. To understand multirate signal processing fundamentals and design of practical sampling rate converters and applications.
2. To study linear prediction filters and adaptive filters using LMS and RLS algorithms.
3. To explore various methods for power spectrum estimation of the signals.
4. To study wavelet transforms and digital filter implementation of wavelets and its applications.

Module-1

Multirate Digital Signal Processing: Introduction, decimation by a factor 'D', Interpolation by a factor 'I', sampling rate conversion by a factor 'I/D', Implementation of sampling rate conversion, Multistage implementation of sampling rate conversion, Applications of multirate signal processing, Digital filter banks, two channel quadrature mirror filter banks, M-channel QMF bank.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-2

Linear prediction and Optimum Linear Filters: Random signals, Correlation Functions and Power Spectra, Innovations Representation of a Stationary Random Process. Forward and Backward Linear Prediction. Solution of the Normal Equations. The Levinson-Durbin Algorithm. Properties of the Linear Prediction-Error Filters.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-3

Adaptive filters: Applications of Adaptive Filters-Adaptive Channel Equalization, Adaptive noise cancellation, Linear Predictive coding of Speech Signals, Adaptive direct form FIR filters-The LMS algorithm, Properties of LMS algorithm. Adaptive direct form filters- RLS algorithm.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-4

Power Spectrum Estimation: Non parametric Methods for Power Spectrum Estimation - Bartlett Method, Welch Method, Blackman and Tukey Methods.
Parametric Methods for Power Spectrum Estimation: Relationship between the auto correlation and the model parameters, Yule and Walker methods for the AR Model Parameters, Burg Method for the AR Model parameters, Unconstrained least-squares method for the AR Model parameters, Sequential estimation methods for the AR Model parameters, ARMA Model for Power Spectrum Estimation.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-5

WAVELET TRANSFORMS: The Age of Wavelets, The origin of Wavelets, Wavelets and other reality transforms, History of wavelets, Wavelets of the future.
Continuous Wavelet and Short Time Fourier Transform: Wavelet Transform, Mathematical preliminaries, Properties of wavelets.
Discrete Wavelet Transform: Haar scaling functions, Haar wavelet function, Daubechies Wavelets.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks**

to attain the COs and POs

3. The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Text Books

1. 'Digital Signal Processing, Principles, Algorithms and Applications', John G. Proakis, Dimitris G.Manolakis, Pearson, Fourth edition, 2007
2. 'Insight into Wavelets- from Theory to Practice', K P Soman, Ramachandran, Resmi, PHI, Third Edition, 2010

Web links and Video Lectures (e-Resources):

www.nptel.ac.in

Skill Development Activities Suggested

1) Interact with industry (small, medium, and large.
2) Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3) Involve in case studies and field visits/ fieldwork.
4) Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5) Handle advanced instruments to enhance technical talent.
6) Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7) Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Apply theory of multirate digital signal processing and design of sampling rate converters.	L4
CO2	Design adaptive filters using LMS and RLS algorithms and linear prediction filters.	L4
CO3	Design prediction filters and understand the solution of normal equation.	L4
CO4	Estimate the power spectrum of signals using different methods.	L4
CO5	Apply theory of wavelet transform and capable of designing wavelet filters.	L4

ADVANCED EMBEDDED SYSTEMS			
Course Code	22LIE14	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	2:0:2	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives:

1. To understand the difference between Embedded Systems and General Computing Systems
2. To understand the Classification of Embedded Systems based on Performance, Complexity along with the Domains and Areas of Applications of Embedded Systems
3. Analysis of a Real Life example on the bonding of Embedded Technology with Human Life
4. To understand the difference between Microcontrollers and ARM Cortex processors.
5. To learn Programming using assembly and C language, CMSIS for variety of End Applications.

Module-1	
Embedded System: Embedded vs General computing system, classification, application and purpose of ES. Core of an Embedded System, Memory, Sensors, Actuators, LED, Opto coupler, Communication Interface, Reset circuits, RTC, WDT, Characteristics and Quality Attributes of Embedded Systems.	
Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-2	
Hardware Software Co-Design, embedded firmware design approaches, computational models, embedded firmware development languages, Integration and testing of Embedded Hardware and firmware, Components in embedded system development environment (IDE), Files generated during compilation, simulators, emulators and debugging.	
Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-3	
ARM-32 bit Microcontroller: Thumb-2 technology and applications of ARM, Architecture of ARM Cortex M3, Various Units in the architecture, General Purpose Registers, Special Registers, exceptions, interrupts, stack operation, reset sequence.	
Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-4	
Instruction Sets: Assembly basics, Instruction list and description, useful instructions, Memory Systems, Memory maps, Cortex M3 implementation overview, pipeline and bus interface.	
Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-5	
Exceptions, Nested Vector interrupt controller design, Systick Timer, Cortex- M3 Programming using assembly and C language, CMSIS.	
Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks**

to attain the COs and POs

3. The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Text Books

1. 'Introduction to embedded systems', K. V. Shibu, TMH education Pvt.Ltd., 2009.
2. 'The Definitive Guide to the ARM Cortex-M3', Joseph Yiu, Newnes,(Elsevier), 2nd edn, 2010.

Reference Books

1. 'Embedded systems - A contemporary design tool', James K. Peckol, JohnWiley, 2008

Web links and Video Lectures (e-Resources):

www.nptel.ac.in

Skill Development Activities Suggested

1) Interact with industry (small, medium, and large.
2) Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3) Involve in case studies and field visits/ fieldwork.
4) Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5) Handle advanced instruments to enhance technical talent.
6) Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7) Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Understand the basic hardware components and their selection methods based on the attributes of Embedded Systems	L1
CO2	Describe the code design process and firmware design approaches	L2
CO3	Acquaint the knowledge of ARM Cortex M3 Processor and its salient features.	L2
CO4	Apply and use Programming Techniques for different End Uses	L3

MULTIMEDIA COMMUNICATION			
Course Code	22LIE15	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	2:0:2	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives:

1. To learn the several multimedia networks and applications.
2. To learn about the MPEG 4 systems.
3. To study the multimedia communication across network.

Module-1

Multimedia Communications: Multimedia information representation, multimedia networks, multimedia applications, network QoS and application of QoS. (Text 1 Chap. 1)

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-2

Information representation: Text, images, audio and video. Text and image compression,, compression principles, text compression, image compression, Audio and video compression, audio compression, video compression, video compression principles, video compression standards:H.261,H.263,P1.323,MPEG1,MPEG2, other coding formats text, speech, image and video. (Text 1 Chap. 3&4)

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-3

Detailed Study of MPEG4: coding of audiovisual objects, MPEG4 systems, MPEG4 audio and video, profiles and levels, MPEG 7 standardization process of multimedia content description, MPEG21 multimedia framework, Significant features of JPEG 2000, MPEG 4 transport across the internet. (Text 2 Chap. 5)

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-4

Synchronization: Notion of synchronization, presentation requirements, reference model for synchronization, Synchronization specification, Multimedia operating systems, Resource management, process management techniques. (Ref. 1 Chap. 9 & 11)

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-5

Multimedia Communication Across Networks: Layered video coding, error resilient video coding techniques, multimedia transport across IP networks and relevant protocols such as RSVP, RTP, RTCP, DVMRP, multimedia in mobile networks, multimedia in broadcast networks.(Text 2 Chap.6)

Assignments /Practicals can be given on writing the programs to encode and decode the various kinds of data by using the algorithms. Students can collect several papers from journal/conferences/Internet on a specific area of multimedia communications and write a review paper and make a presentation.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks**

to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Text Books

1. Fred Halsall, "Multimedia Communications", Pearson Education, 2001
2. K. R Rao, Zoran S. Bojkovic, Dragorad A. Milovanovic, "Multimedia Communication Systems", Pearson Education, 2004.

Reference Books

1. Raifsteinmetz, Klara Nahrstedt, "Multimedia: Computing, Communications and Applications", Pearson Education, 2002
2. John Billamil, Louis Molina, "Multimedia An introduction", PHI 2002.

Web links and Video Lectures (e-Resources):

www.nptel.ac.in

Skill Development Activities Suggested

1) Interact with industry (small, medium, and large.
2) Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3) Involve in case studies and field visits/ fieldwork.
4) Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5) Handle advanced instruments to enhance technical talent.
6) Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7) Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Explain the basics of different multimedia networks and applications	L2
CO2	Explain different compression techniques to compress audio and video.	L2
CO3	Describe the MPEG4 and other systems	L3
CO4	Explore synchronization and multimedia operating system	L2
CO5	Describe multimedia Communication across Networks.	L3

RESEARCH METHODOLOGY AND IPR			
Course Code	22RMI16	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40 Hours	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives:

Module-1	
Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-2	
Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-3	
Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-4

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-5

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks**

to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Text Books

Reference Books

Web links and Video Lectures (e-Resources):

Skill Development Activities Suggested

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1		
CO2		
CO3		
CO4		
CO5		

Program Outcome of this course

Sl. No.	Description	POs

Mapping of COS and POs

EMBEDDED AND SIGNAL PROCESSING LAB			
Course Code	22LIEL17	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	1:2:0	SEE Marks	50
Credits	02	Exam Hours	03

Course objectives:

1. To implement different techniques of message passing.
2. To develop and test programs.
3. To compare DFT and DCT using MatLab.
4. To design digital filters using suitable techniques.

Sl.NO	Experiments
	PART-A: Following RTOS experiments to be done using Linux.
1	Develop and test programs to (a) create child process and display its ID and (b) Execute child process function using switch structure.
2	Develop and test the program for a multithreaded application, where communication is through a buffer for the conversion of lowercasetext to uppercase text, using semaphore concept.
3	Develop and test the program for a multithreaded application, wherecommunication is through shared memory for the conversion of lowercase text to uppercase text.
4	Develop program for inter-thread communication using message queue. Data is to be input from the keyboard for the chosenapplication.
5	Create 'n' number of child threads. Each thread prints the message "I'm in thread number …" andsleeps for 50 ms and then quits. The main thread waits for complete execution of all the childthreads and then quits. Compile and execute in Linux.
6	Implement the multi-thread application satisfying the following: a) Two child threads are created with normal priority. b) Thread 1 receives and prints its priority and sleeps for 50ms and then quits. c) Thread 2 prints the priority of the thread 1 and rises its priority to above normal and retrieves the new priority of thread 1, prints it and then quits. d) The main thread waits for the child thread to complete its job and quits.
7	Implement the usage of anonymous pipe with 512bytes for data sharing between parent and child processes using handle inheritance mechanism.
	PART-B: Digital Signal Processing using MATLAB
1	Comparison of DFT and DCT (in terms of energy compactness)Generate the sequence x[n] = n-64 for n=0,…,127. (a) Let X[k]=DFT{x[n]}. For various values of L, set to zero the "high frequency coefficients" X [64-L]=….X[64]=…….= X[64+L]=0. Take the inverse DFT and plot the results. (b) Let X_{DCT}[k]=DCT(x[n]). For the same values of L, set to zero the high frequency coefficients X_{DCT} [127-L]=…..X_{DCT}[127]. Take the inverse DCT for each case and compare the reconstruction with the previous case.
2	Design digital FIR LPF and HPF using the following windowstechniques. i) Hamming window function ii) Kaiser window function
3	Design digital IIR Butterworth low pass and high pass filter usingbilinear transformation. Compare FIR and IIR filter in terms of performance(accuracy in meeting specifications) and computational complexity.
4	Compute Fourier Transform & its inverse Fourier Transform of an image.
5	Compute FFT when N is not a power of 2.
6	Design an equi ripple filter for the given specification.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

1. Select a suitable task switching technique in a multithreaded application.
2. Implement different techniques of message passing and Inter task/threadcommunication.
3. Implement different data structures such as pipes, queues, shared memory,semaphores, buffers in multithreaded programming.
4. Implement DCT, DFT, FFT and IFFT for the given input data.
5. Implement the appropriate design method for FIR and IIR filters.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 40%of maximum marks in the semester-end examination(SEE). In total of CIE and SEE student has to secure 50% maximum marks of the course.

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of the semester and the second test shall be conducted after the 14th week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of **scaled-down** marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University.

- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.
- Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.
- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.
- General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

• Change of experiment is allowed only once and 10% Marks allotted to the procedure part to be made zero. The duration of SEE is 03 hours
Suggested Learning Resources: • www.nptel.ac.in

Semester II

PROCESS CONTROL INSTRUMENTATION			
Course Code	22LIE21	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	2:0:2	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives:

1. To understand the interface between process and control subsystem, manual interaction with the processes, process industrial automation system.
2. To learn about latest hardware and software modules for realizing the Data Acquisition and Control Unit.
3. To understand inter and intra systems data exchange in process industrial automation systems.
4. To understand the structure of field bus I/O and the management of safety in process plants.
5. To understand the manufacturing, utility in industrial processes and also to give the Integration of operational technology and Information Technology to derive operational and business excellence.

Module-1	
Automation – Need and Benefit: Instrumentation subsystems- Structure, Signal Interface Standards, Input data reliability enhancement, Isolation and Protection, human interface subsystems - Operation panel, Construction, control subsystems – Structure, interfacing, automation strategies-Basic and advanced strategies.	
Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-2	
Data Acquisition and Control Unit: Hardware and Software- Basic modules, functional modules, DACU capacity expansion, system cables, Integrated assemblies, DACU construction, Data exchange on bus, Softwarestructure, application programming, Programmable control subsystems.	
Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-3	
Data Communication and Networking: Communication network, signal and data transmission, Data communication protocol, Inter process communication, cyber security, Safe and redundant network.	
Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-4	
Fieldbus Technology & Safety Systems: Centralized, remote- input-output, Field bus- input-output, communication, device integration, Other networks. Safety systems introduction, Process and Machine safety management.	
Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-5	
Management and Information Technology in Industrial Processes: Introduction, Classification of industrial processes, Manufacturing and utility processes, industrial robotics, operation technology and IT, before and after convergence, ISA 95 standard, new developments.	
Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks**

to attain the COs and POs

3. The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Text Books

1. 'Overview of Industrial Process Automation', KLS Sharma,2nd edition, ELSEVIER, 2016.

Web links and Video Lectures (e-Resources):

www.nptel.ac.in

Skill Development Activities Suggested

1) Interact with industry (small, medium, and large.
2) Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3) Involve in case studies and field visits/ fieldwork.
4) Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5) Handle advanced instruments to enhance technical talent.
6) Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7) Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.		Blooms Level
CO1	Understand the safety requirements in process plants.	L2
CO2	Understand the use of information technology and standards in process control operation	L2
CO3	Describe the hardware and software modules for realizing the Data Acquisition and Control Modules	L2
CO4	Explain the techniques of Automation in industries and describe the networking requirements.	L2

DESIGN of POWER CONVERTERS			
Course Code	22LIE22	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:2:0	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory + 10-12 Lab slots	Total Marks	100
Credits	04	Exam Hours	03

Course objectives:

1. Acquire knowledge about various power semiconductor devices.
2. Analyze and design different power converter circuits.
3. Analyze various single phase and three phase power converter circuits and understand their applications.
4. Identify the basic requirements for power electronics based design application.
5. Develop skills to build, and troubleshoot power electronics circuits.
   Understand the use of power converters in commercial and industrial applications.

MODULE-1	
Introduction to Control characteristics of power semiconductor devices: SCR, BJT, MOSFET, GTO, MCT, SITH, IGBT. Comparison of controllable switches. **AC to Controlled DC Converter**: Thyristor circuits and their control, Gate Triggering, Single phase converters, Three phase converters.	
Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

MODULE-2	
DC to DC converters: Introduction, control of DC-DC converters, Buck, Boost,Buck-Boost, Cuk converter. **Inverters**: Introduction, principle of operation, single phase inverters, three phase inverters-120 and 180 modes of operation.	
Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

MODULE-3	
Switching DC power supplies: linear power supply, overview of switching power supply, DC - DC converters with electrical isolation, flyback converter, forward converter, push-pull converter, Half and Full bridge converter, current mode control, power supply protection.	
Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

MODULE-4	
Magnetics for Switched Mode Converters: Power Handling capacity of a transformer, Area product, window utilization factor. **Transformer designs** – forward converter, half and Full Bridge converter, Push-pull converter, Flyback converter. Design of Inductors, problems.	
Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

MODULE 5	
PWM controlling Techniques: single PWM, Multiple, sinusoidal, modified,phase displacement control. **Power electronic applications**: UPS, control of motor drives, criteria forselecting drive components, High frequency fluorescent lighting. **Industrial applications**: Induction heating, Electric welding	
Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

PRACTICAL COMPONENT OF IPCC

Sl. NO	Experiments
	P-Spice Simulation of following
1	Experimental study for characteristics of DC-DC Buck converter.
2	Experimental study for characteristics of DC-DC Boost converter.
3	Experimental study for characteristics of DC-DC Buck-Boost converter.
4	Experimental study for characteristics of single phase fully controlled Full Bridge converter.
5	Experimental study for characteristics of single phase semi controlled Full Bridge converter.
6	Experimental study for Flyback and Push pull Converter.
7	Generation of gating signals using single, Multiple, sinusoidal and modified PWM techniques.
8	Experimental study for characteristics of three phase semi controlled Full Bridge converter.
9	Experimental study for characteristics of three phase fully controlled Full Bridge converter.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together

CIE for the theory component of IPCC

1. Two Tests each of **20 Marks**
2. Two assignments each of **10 Marks/One Skill Development Activity of 20 marks**
3. Total Marks of two tests and two assignments/one Skill Development Activity added will be CIE for 60 marks, marks scored will be proportionally scaled down to **30 marks**.

CIE for the practical component of IPCC

1. On completion of every experiment/program in the laboratory, the students shall be evaluated and marks shall be awarded on the same day. The**15 marks** are for conducting the experiment and preparation of the laboratory record, the other **05 marks shall be for the test** conducted at the end of the semester.
2. The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to 15 marks.
3. The laboratory test at the end /after completion of all the experiments shall be conducted for 50 marks and scaled down to 05 marks**.**

Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **20 marks**.

.

SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (duration 03 hours)

1. The question paper will be set for 100 marks and marks scored will be scaled down proportionately to 50 marks.
2. The question paper will have ten questions. Each question is set for 20 marks.
3. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), should have a mix of topics under that module.
4. The students have to answer 5 full questions, selecting one full question from each module.

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper shall include questions from the practical component).

1. The minimum marks to be secured in CIE to appear for SEE shall be the 15 (50% of maximum marks-30) in the theory component and 10 (50% of maximum marks -20) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included**.** The maximum of 04/05 questions to be set from the practical component of IPCC, the total marks of all questions should not be more than the 20 marks.
2. SEE will be conducted for 100 marks and students shall secure 40% of the maximum marks to qualify in the SEE. Marks secured will be scaled down to 50. (Student has to secure an aggregate of 50% of maximum marks of the course(CIE+SEE)

Suggested Learning Resources:

Text Books

1. 'Power Electronics: Converters, Applications and Design', Ned Mohan Tore, Undeland and William P Robbins, 3rdEdition, John Wiley and Sons, 2007
2. 'Design of Magnetic Components for Switched Mode Power Converters', Umanand L & S R Bhat, New Age International (P) Ltd., Publishers 2017.

Reference Books

1. 'Power Electronics', M H Rashid, 3rdedition, PHI / Pearson Publisher, 2004.

Web links and Video Lectures (e-Resources):

www.nptel.ac.in

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Describe the various power semiconductor devices and techniques used in power electronics.	L2
CO2	Analyze and design different power converter circuits	L4
CO3	Analyze and design different 1∅ and 3∅ power converter circuits and understand their applications	L4
CO4	Explain the use of power converters in commercial and industrialapplications	L2
CO5	Troubleshoot power electronics circuits and fix the design problems.	L4

WIRELESS SENSOR NETWORKS			
Course Code	22LIE231	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	2:0:2	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives:

1. To understand the hardware details of different types of sensors and select right type of sensor for various applications.
2. To understand conversion of sensor information into digital data and packetize to a specific protocol for transmission
3. To understand radio standards and communication protocols to be used for wireless sensor.
4. To understand the issues involved in synchronization and security.

Module-1

Introduction: Sensor Mote Platforms, WSN Architecture and Protocol Stack.
WSN Applications: Military Applications, Environmental Applications, HealthApplications, Home Applications, Industrial Applications.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-2

Factors Influencing WSN Design: Hardware Constraints Fault Tolerance Scalability Production Costs WSN Topology, Transmission Media, Power Consumption.
Physical Layer: Physical Layer Technologies, Overview of RF Wireless Communication, Channel Coding (Error Control Coding), Modulation, Wireless Channel Effects, PHY Layer Standards.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-3

Medium Access Control: Challenges for MAC, CSMA Mechanism, Contention-Based Medium Access, Reservation-Based Medium Access, HybridMedium Access.
Network Layer: Challenges for Routing, Data-centric and Flat Architecture Protocols, Hierarchical Protocols, Geographical Routing Protocols.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-4

Transport Layer: Challenges for Transport Layer, Reliable Multi Segment Transport (RMST) Protocol, Pump Slowly, Fetch Quickly (PSFQ) Protocol, Congestion Detection and Avoidance (CODA) Protocol, Event-to-Sink ReliableTransport (ESRT) Protocol, GARUDA.
Application Layer: Source Coding (Data Compression), Query Processing,Network Management.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-5

Time Synchronization: Challenges for Time Synchronization, Network Time Protocol, Timing-Sync Protocol for Sensor Networks (TPSN), Reference- Broadcast Synchronization (RBS), Adaptive Clock Synchronization (ACS)
Localization: Challenges in Localization, Ranging Techniques, Range-Based Localization Protocols, Range-Free Localization Protocols.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks**

to attain the COs and POs

3. The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Text Books

1. Wireless Sensor Networks', Ian F. Akyildiz and Mehmet Can Vuran, John Wiley & Sons Ltd. ISBN 978-0-470-03601-3 (H/B), 2010
2. 'Wireless Sensor Networks:Signal Processing and Communications Perspectives', Ananthram Swami, et. al., John Wiley & Sons Ltd., ISBN 978-0470-03557-3, 2007.

Web links and Video Lectures (e-Resources):

www.nptel.ac.in

Skill Development Activities Suggested

1) Interact with industry (small, medium, and large.
2) Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3) Involve in case studies and field visits/ fieldwork.
4) Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5) Handle advanced instruments to enhance technical talent.
6) Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7) Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Explain the concepts of sensors and conversion to digitally formatted signal for transmission.	L2
CO2	Evaluate the capacity and degradation in performance of various wireless MAC protocols in a transmission environment.	L2
CO3	Analyze schemes to transport sensor data to a server in a power efficient and time efficient manner.	L2
CO4	Develop and evaluate the performance of a sensor network including localization of sensor faults.	L2

NANOELECTRONICS AND NANOSENSORS			
Course Code	22LIE232	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	2:0:2	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives:

1. To understand basic building blocks of digital electronics.
2. To understand the operations of semiconductor nano-devices.
3. To understand the operation and applications of photonic materials.
4. To understand the operation and applications of nano-sensors.

Module-1	
Digital Electronics: OP-Amp, RS Flip Flops, J-K Master Slave Flip Flops, Types of registers, D/A and A/D Counters, Bipolar Junction Transistor, FET, MOSFET, Single Electron Tunnelling.	
Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos
Module-2	
Semiconductor Nanodevices: Single-Electron Devices, Nano scale MOSFET – Resonant Tunnelling Transistor - SingleElectron Transistors; Single-Electron Dynamics; Nanorobotics and Nanomanipulation; Molecular nanowires-Organic LED, Organic FETs- CNT and Graphene FTE, SiNW FET.	
Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos
Module-3	
Electronic and Photonic Materials: Single Electron Tunnelling phenomena- Coulomb blockade-Coulomb staircase - RSD and Resonant tunnelling transistor- Quantum structures based LEDs - OLED and photo detectors Magnetic quantum dots and their applications.	
Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos
Module-4	
Nano sensors: Micro and nano-sensors, Fundamentals of sensors, biosensor, micro fluids, MEMS and NEMS, Packaging and characterization of sensors, Method of packaging at zero level, dye level and first level.-Thermal energy sensors -temperature sensors, heat sensors Electromagnetic sensors- electrical resistance sensors, electrical current sensors, electrical voltage sensors, electrical power sensors, magnetism sensors.	
Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos
Module-5	
Nanosensors (contd): Mechanical sensors -pressure sensors, gas and liquid flow sensors, position sensors - Chemical sensors - Optical and radiation sensors- Gas Sensor-Bio Sensors- DNA based biosensors-Packaging and method of packaging.	
Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks**

to attain the COs and POs

3. The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Text Books

1. W. Ranier, "Nano Electronics and Information Technology", 3rd Edition Wiley, (2012).
2. K.E. Drexler, "Nano systems", Wiley, (1992).

Reference Books

1. M.C. Petty, "Introduction to Molecular Electronics". Oxford University Press 1995.
2. Frank J. Owens and Charles P. Poole Jr., The physics and chemistry of nanosolids, Wiley Interscience Publishers, 2008.
3. Kouroush Kalantar – Zadeh, Benjamin Fry, Nanotechnology enabled sensors, Springer Verlag New York, (2008) ISBN-13: 9780387324739

Web links and Video Lectures (e-Resources):

www.nptel.ac.in

Skill Development Activities Suggested

1) Interact with industry (small, medium, and large.
2) Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3) Involve in case studies and field visits/ fieldwork.
4) Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5) Handle advanced instruments to enhance technical talent.
6) Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7) Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Explain the operation and applications of basic building blocks of digital electronics.	L3
CO2	Explain the operations and applications of semiconductor nano-devices.	L4
CO3	Explain the operation and applications of photonic materials.	L4
C04	Explain the operation and applications of nano-sensors.	L4

CRYPTOGRAPHY AND NETWORK SECURITY			
Course Code	22LIE233	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	2:0:2	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives:

1. Enable students to understand the basics of symmetric key and public key cryptography
2. Equip students wirh basic mathematical concepts and their use in cryptographic algorithms
3. Enable students to Understand pseudorandom number generation and one way hash functions
4. Equip students with techniques and features of Email, IP and Web security

Module-1

Foundations: Terminology, Steganography, substitution ciphers and transpositions ciphers, Simple XOR,One-Time Pads, computer algorithms.
Symmetric ciphers: Traditional Block Cipher structure, Data encryption standard (DES), The AES Cipher.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-2

Introduction to modular arithmetic, Prime Numbers, Fermat's and Euler's theorem, primality testing, Chinese Remainder theorem, discrete logarithm.
Principles of Public-Key Cryptosystems, The RSA algorithm, Diffie - Hellman Key Exchange, Elliptic Curve Arithmetic, Elliptic Curve Cryptography.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-3

Pseudo-Random-Sequence Generators and Stream Ciphers: Linear Congruential Generators, Linear Feedback Shift Registers, Design and analysis of stream ciphers, Stream ciphers using LFSRs, A5, Hughes XPD/KPD, Nanoteq, Rambutan, Additive generators, Gifford, Algorithm M, PKZIP.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-4

One-Way Hash Functions: Background, Snefru, N-Hash, MD4, MD5, Secure Hash Algorithm [SHA], One way hash functions using symmetric block algorithms, Using public key algorithms, Choosing a one-way hash functions, Message Authentication Codes. Digital Signature Algorithm, Discrete Logarithm Signature Scheme.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-5

E-mail Security: Pretty Good Privacy-S/MIME.
IP Security: IP Security Overview, IP Security Policy, Encapsulation Security Payload (ESP), Combining security Associations.
Web Security: Web Security Considerations, SSL.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks**

to attain the COs and POs

3. The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Text Books

1. 'Cryptography and Network Security Principles and Practice', William Stallings, Pearson Education Inc., ISBN: 978-93325-1877-3, 6th Edition, 2014
2. 'Applied Cryptography Protocols, Algorithms, and Source code in C', Bruce Schneier, Wiley Publications ISBN: 9971-51348-X, 2nd Edition.

Reference Books

1. 'Cryptography and Network Security', Behrouz A. Forouzan, 1st Edition TMH, 2008
2. 'Cryptography and Network Security', Atul Kahate, TMH, 2013

Web links and Video Lectures (e-Resources):

www.nptel.ac.in

Skill Development Activities Suggested

1) Interact with industry (small, medium, and large.
2) Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3) Involve in case studies and field visits/ fieldwork.
4) Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5) Handle advanced instruments to enhance technical talent.
6) Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7) Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Understand the basics of symmetric key and public key cryptography.	L2
CO2	Use basic cryptographic algorithms to encrypt the data.	L2
CO3	Provide authentication and protection for encrypted data.	L2
CO4	Understand the techniques and features of Email, IP and Web security	L2

RECONFIGURABLE COMPUTING			
Course Code	22LIE234	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	2:0:2	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives:

1. To understand the fundamental principles and practices in reconfigurablearchitecture.
2. To Simulate and synthesize the reconfigurable computing architectures.
3. To understand the FPGA design principles, and logic synthesis
4. To learn the integration of hardware and software technologies for reconfiguration computingfocusing on partial reconfiguration design.
5. To understand the design of digital systems for a variety of applications on signal processing andsystem on chip configurations.

Module-1	
Introduction: History, Reconfigurable vs Processor based system, RCArchitecture. **Reconfigurable Logic Devices**: Field Programmable Gate Array, CoarseGrained Reconfigurable Arrays. **Reconfigurable Computing System**: Parallel Processing on Reconfigurable Computers, A survey of Reconfigurable Computing System.	
Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-2	
Languages and Compilation: Design Cycle, Languages, HDL, High Level Compilation, Low level Design flow, Debugging Reconfigurable Computing Applications.	
Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-3	
Implementation: Integration, FPGA Design flow, Logic Synthesis. **High Level Synthesis for Reconfigurable Devices:** Modelling, Temporal Partitioning Algorithms.	
Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-4	
Partial Reconfiguration Design: Partial Reconfiguration Design, Bitstream Manipulation with JBits, The modular Design flow, The Early Access Design Flow, Creating Partially Reconfigurable Designs, Partial Reconfiguration using Hansel-C Designs, Platform Design.	
Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-5	
Signal Processing Applications: Reconfigurable computing for DSP, DSP application building blocks, Examples: Beamforming, Software Radio, Image and video processing, Local Neighbourhood functions, Convolution. **System on a Programmable Chip**: Introduction to SoPC, Adaptive Multiprocessing on Chip.	
Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks**

to attain the COs and POs

3. The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Text Books

1. 'Reconfigurable Computing:Accelerating Computation with Field- Programmable Gate Arrays', M. Gokhale and P. Graham, Springer, ISBN: 978-0-387-26105-8, 2005.
2. 'Introduction to Reconfigurable Computing: Architectures, Algorithms and Applications', C. Bobda, Springer, ISBN: 978-1-4020-6088-5, 2007.

Reference Books

1. "Practical FPGA Programming in C', D. Pellerin and S. Thibault,Prentice-Hall, 2005.
2. "FPGA Based System Design', W. Wolf, Prentice-Hall, 2004.
3. 'Rapid System Prototyping with FPGAs: Accelerating the Design Process', R. Cofer and B. Harding, Newnes, 2005.

Web links and Video Lectures (e-Resources):

www.nptel.ac.in

Skill Development Activities Suggested

1) Interact with industry (small, medium, and large.
2) Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3) Involve in case studies and field visits/ fieldwork.
4) Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5) Handle advanced instruments to enhance technical talent.
6) Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7) Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Explain the fundamental principles and practices in reconfigurablearchitecture.	L2
CO2	Simulate and synthesize the reconfigurable computing architectures.	L3
CO3	Discuss the FPGA design principles, and logic synthesis	L3
CO4	Integrate hardware and software technologies for reconfiguration computingfocusing on partial reconfiguration design.	L4
CO5	Design digital systems for a variety of applications on signal processing andsystem on chip configurations.	L3

SWITCHED MODE POWER CONVERTERS			
Course Code	22LIE235	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	2:0:2	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives:

1. To understand the operation of various types of switched mode converters.
2. To understand the operation of various types of Cuk converter.
3. To understand the operation of different modes of operation of various types of flyback converter.
4. To understand the operation of various types of Switched Mode DC to AC converter.
5. To understand the operation of Resonant Converters.

Module-1	
Switched Mode DC-to-DC Converter - buck converters – boost Converter – buck-boost converter - continuous Conduction mode – design of filter inductance & capacitance - boundary between continuous and discontinuous conduction – critical values of inductance/load resistance - discontinuous conduction mode with constant output voltage – Output voltage ripple.	
Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-2	
Cuk converter – Full-ridge dc-dc Converter – PWM with bipolar voltage and unipolar voltage switching – comparison of dc-dc converters – Linear Power Supply – disadvantages of linear power supply – switched mode power supply – dc-dc converters with electrical isolation –unidirectional core excitation & bidirectional core excitation.	
Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-3	
Fly back converter – continuous & discontinuous conduction mode - double ended fly back converter – forward converters – basic forward converter – practical forward converter – continuous conduction mode only - double ended forward converter – push pull converter – half bridge converter – full bridge converter – continuous conduction mode – current source dc-dc converter.	
Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-4	
Switched Mode DC to AC converter – 1-phase square wave full-bridge inverter – square wave switching scheme - sine PWM switching scheme – PWM with bipolar & unipolar voltage switching - harmonic analysis of output voltage – output control by voltage cancellation - 3-phase voltage source inverter – 3-phase sine PWM inverter – RMS line to line voltage & RMS fundamental line-to-line voltage – square wave operation - Switching utilisation ratio of 1-phase & 3-phase full-bridge inverters.	
Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-5	
Resonant Converters - Basic resonant circuit concepts – series resonant circuit – parallel resonant circuit – load resonant converter - ZCS resonant converter - L type & M type - ZVS resonant converter – comparison of ZCS & ZVS Resonant Converters.	
Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks**

to attain the COs and POs

3. The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Text Books

1. Mohan, Undeland, Robbins, Power Electronics – Converters Application and Design, Wiley-India
2. Muhammad H. Rashid, Power Electronics – Circuits, Devices and Applications, Pearson Education

Reference Books

1. Abraham Pressman, Switching Power supply Design, McGraw Hill

Web links and Video Lectures (e-Resources):

www.nptel.ac.in

Skill Development Activities Suggested

1) Interact with industry (small, medium, and large.
2) Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3) Involve in case studies and field visits/ fieldwork.
4) Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5) Handle advanced instruments to enhance technical talent.
6) Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7) Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Explain the operation of various types of switched mode converters.	L3
CO2	Explain the operation of various types of Cuk converter.	L3
CO3	Explain the operation of different modes of operation of various types of flyback converter.	L3
CO4	Explain the operation of various types of Switched Mode DC to AC converter.	L3
CO5	Explain the operation of Resonant Converters.	L3

ADVANCES IN VLSI			
Course Code	22LIE241	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	2:0:2	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives:

1. To learn the Arrays and Reconfigurable computing system
2. To learn the hardware design implementation models.
3. To learn the signal processing applications using reconfigurable computing system

Module-1

Introduction: History, Reconfigurable vs Processor based system, RCArchitecture.
Reconfigurable Logic Devices: Field Programmable Gate Array, CoarseGrained Reconfigurable Arrays.
Reconfigurable Computing System: Parallel Processing on Reconfigurable Computers, A survey of Reconfigurable Computing System.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-2

Languages and Compilation: Design Cycle, Languages, HDL, High Level Compilation, Low level Design flow, Debugging Reconfigurable Computing Applications.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-3

Implementation: Integration, FPGA Design flow, Logic Synthesis.
High Level Synthesis for Reconfigurable Devices: Modelling, Temporal Partitioning Algorithms.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-4

Partial Reconfiguration Design: Partial Reconfiguration Design, Bitstream Manipulation with JBits, The modular Design flow, The Early Access Design Flow, Creating Partially Reconfigurable Designs, Partial Reconfiguration using Hansel-C Designs, Platform Design.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-5

Signal Processing Applications: Reconfigurable computing for DSP, DSP application building blocks, Examples: Beam forming, Software Radio, Image and video processing, Local Neighbourhood functions, Convolution.
System on a Programmable Chip: Introduction to SoPC, Adaptive Multiprocessing on Chip.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks**

to attain the COs and POs

3. The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Text Books

1. 'Reconfigurable Computing:Accelerating Computation with Field- Programmable Gate Arrays', M. Gokhale and P. Graham, Springer, ISBN: 978-0-387-26105-8, 2005.
2. 'Introduction to Reconfigurable Computing: Architectures, Algorithms and Applications', C. Bobda, Springer, ISBN: 978-1-4020-6088-5, 2007.

Reference Books

1. 'Practical FPGA Programming in C', D. Pellerin and S. Thibault,Prentice-Hall, 2005.
2. 'FPGA Based System Design',W. Wolf, Prentice-Hall, 2004.
3. 'Rapid System Prototyping with FPGAs: Accelerating the Design Process', R. Cofer and B. Harding, Newnes, 2005.

Web links and Video Lectures (e-Resources):

www.nptel.ac.in

Skill Development Activities Suggested

1) Interact with industry (small, medium, and large.
2) Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3) Involve in case studies and field visits/ fieldwork.
4) Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5) Handle advanced instruments to enhance technical talent.
6) Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7) Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Understand the Reconfigurable computing system	L2
CO2	Apply the hardware design flow concepts	L2
CO3	Implement complex circuits using FPGA	L3
CO4	Explore the reconfigurable design methods	L2
CO5	Apply Reconfigurable computing for DSP applications	L3

MICRO ELECTRO MECHANICAL SYSTEMS			
Course Code	22LIE242	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	2:0:2	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives:

1. To understand the basics of MEMS systems.
2. To understand the operation and design of Microsystems and its components.
3. To understand the engineering mechanics for micro systems design.
4. To understand scaling and laws as applied to miniaturization.
5. To understand the basics of micro-manufacturing and design of Microsystems.

Module-1

Overview of MEMS and Microsystems: MEMS and Microsystem, Typical MEMS and Microsystems Products, Evolution of Microfabrication, Microsystems and Microelectronics, Multidisciplinary Nature of Microsystems, Miniaturization. Applications and Markets.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-2

Working Principles of Microsystems: Introduction, Micro sensors, Micro actuation, MEMS with Micro actuators, Micro accelerometers, Micro fluidics.

Engineering Science for Microsystems Design and Fabrication: Introduction, Atomic Structure of Matters, Ions and Ionization, Molecular Theory of Matter and Inter-molecular Forces, Doping of Semiconductors, The Diffusion Process, Plasma Physics, Electrochemistry.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-3

Engineering Mechanics for Microsystems Design: Introduction, Static Bending of Thin Plates, Mechanical Vibration, Thermomechanics, Fracture Mechanics, Thin Film Mechanics, Overview on Finite Element Stress Analysis.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-4

Scaling Laws in Miniaturization:
Introduction, Scaling in Geometry, Scaling in Rigid-Body Dynamics, Scaling in Electrostatic Forces, Scaling of Electromagnetic Forces, Scaling in Electricity, Scaling in Fluid Mechanics, Scaling in Heat Transfer.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-5

Overview of Micro-manufacturing: Introduction, Bulk Micro-manufacturing, Surface Micromachining, The LIGA Process, Summary on Micromanufacturing.

Microsystem Design: Introduction, Design Considerations, Process Design, Mechanical Design, Using Finite Element Method.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks**

to attain the COs and POs

3. The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Text Books

1. 'Design and Implementation of Micro Mechatronic Systems' Ren-Jung Chang, IntechOpen, 2017
2. 'Mechatronics: Integrated Mechanical Electronic Systems', M.S.Balasundaram K.P. Ramachandran, G.K. Vijayaraghavan, WILEY, 2008

Reference Books

1. 'Micro Mechatronics' Kenji Uchino, CRC Press, 2nd Edition 2019.
2. 'Mechatronic Systems Analysis, Design and Implementation', El-Kébir Boukas, Fouad M. AL-Sunni, Springer, 2012.

Web links and Video Lectures (e-Resources):

www.nptel.ac.in

Skill Development Activities Suggested

1) Interact with industry (small, medium, and large.
2) Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3) Involve in case studies and field visits/ fieldwork.
4) Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5) Handle advanced instruments to enhance technical talent.
6) Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7) Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Explain and discuss the basics of MEMS systems.	L2
CO2	Explain the operation and design of Microsystems and its components.	L2
CO3	Explain the engineering mechanics for micro systems design.	L2
CO4	Explain the scaling and its laws as applied to miniaturization.	L2
CO5	Explain and discuss the basics of micro-manufacturing and design of Microsystems.	L3

MECHATRONICS			
Course Code	22LIE243	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	2:0:2	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives:

1. To understand the basics of Mechatronics and its design approach.
2. To understand the operation and applications of various sensors.
3. To understand the operation of various actuators and their applications in systems.
4. To understand the concepts of logic design, computer communication networks and Fault diagnosis and Analysis in Mechatronic Systems.
5. To understand the concepts of data acquisition, software design and development.

Module-1

Overview of mechatronics: What is Mechatronics? Integrated Mechatronic Design Approach, System Interfacing, Embedded Systems, Instrumentation and Control Systems, Open and closed loop systems, importance of feedback systems, Transfer function, Microprocessor Based Controllers and Microelectronics. An Introduction to Micro-technology and Nanotechnology, Mechatronics: Miniaturized, Examples and applications

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-2

Sensors and application: Introduction to Sensors , Classification of sensors, Sensor – Static and Dynamic Characteristics, Sensors, Linear and Rotational Sensors, Acceleration Sensors, Force Measurement, Torque and Power Measurement, Flow Measurement, Temperature Measurements, Distance Measuring and Proximity Sensors, Light Detection, Use of RF, Infra-Red sensors in automobiles, Image, and Vision Systems, Integrated, Micro-sensors, Selection Criteria.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-3

Actuators: Introduction to Actuators – Mechanical, Electrical and combinational actuators, Electro-mechanical Actuators, Electrical Machines, Piezoelectric Actuators, Hydraulic and Pneumatic Actuation Systems, Applications of few types of actuators in automobiles.

Electrical Actuation Systems: Importance of actuators, classification of Actuators, Mechanical Switches, Bouncing and De-bouncing in Mechanical Switches, Principles of Solenoids and relays, Classification of motors, Application of various motors - Block Diagram - Spindle motors – basic principles, DC motors with field applications, brushless permanent magnet DC motors, Stepper motors, Solid State Switches: transistors, Darling ton pair, Thyristors, Triacs.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-4

Computers and Logic Systems: Introduction to Computers and Logic Systems, Logic design concepts and Design, System Interfaces, Communication and Computer Networks, Fault diagnosis and Analysis in Mechatronic Systems, Logic System Design, Synchronous and Asynchronous Systems, Sequential Systems, Control System Architecture, Control with Embedded Computers and Programmable Logic Control, Digital Signal Processing for Mechatronic Applications, Adaptive and Nonlinear Control System Features, Neural Networks and Fuzzy Systems, Artificial Intelligence and Expert System Approach to control System design, Design Optimization of Mechatronic Systems.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-5

Data Acquisition and Software Development: Introduction to Data Acquisition, Measurement, Techniques, Data Acquisition systems, Importance of data acquisition in automobiles. Computer-Based Instrumentation Systems, Software Design and Development, Data Recording and Data Logging, DAQ for automotive engine system and other Measurements, Electronic Control Unit (ECU), Features of design and system logic in multiple signal measurements.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs
3. The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Text Books

1. Mechatronics – W.Bolton, Longman, 2Ed, Pearson Publications, 2007
2. Microprocessor Architecture, Programming & Applications With 8085/8085A – R.S. Ganokar, Wiley Eastern, 2008

Reference Books

1. Mechatronics – Principles,Concepts and Applications – Nitiagour and Premchand Mohalik – Tata McGraw Hill – 2003.
2. Measurement, Instrumentation, and Sensors Handbook - John G. Webster. Editor-inchief, CRC Press. 1999. 0-8493-2145-X. PDF files online available at www.engnetbase.com
3. Mechatronics Principles & Applications by Godfrey C. Onwubolu, Elsevier.
4. Introduction Mechatronics & Measurement Systems, David.G. Aliciatore

Web links and Video Lectures (e-Resources):

www.nptel.ac.in

Skill Development Activities Suggested

1) Interact with industry (small, medium, and large.
2) Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3) Involve in case studies and field visits/ fieldwork.
4) Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5) Handle advanced instruments to enhance technical talent.
6) Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7) Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Explain the basics of Mechatronics and its design approach.	L2
CO2	Explain the operation and applications of various sensors.	L2
CO3	Explain and discuss the operation of various actuators and their applications in systems.	L3
CO4	Explain and discuss the concepts of logic design, computer communication networks and Fault diagnosis and Analysis in Mechatronic Systems.	L3
CO5	Explain and discuss the concepts of data acquisition, software design and development.	L3

SYNTHESIS AND OPTIMIZATION OF DIGITAL CIRCUITS			
Course Code	22LIE244	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	2:0:2	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives:

4. Understand the need for optimization and dimensions of optimization for digital circuits
5. Understand the basic optimization techniques used in circuits design
6. Understand advanced tools and techniques in digital systems design including Hardware Modelling and Compilation Techniques.
7. Explain the details of Logic level Synthesis and optimization techniques for combinational and sequential circuits
8. Explain the concept of scheduling and resource binding for optimization

Module-1

Introduction to Synthesis and Optimization: Design of Microelectronics circuits, Computer aided Synthesis and Optimization.
Hardware Modeling: HDLs for Synthesis, Abstract models, Compilation and Behavioral Optimization.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-2

Graph theory for CAD for VLSI: Graphs, Combinatorial Optimization, Graph Optimization problems and Algorithms, Boolean Algebra and Applications.
Architectural Synthesis and Optimization: Fundamental Architectural Synthesis problems, Area and Performance Estimation, Strategies for Architectural Optimization, Data path Synthesis, Control Path Synthesis.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-3

Two level Combinational Logic Optimization: Introduction, Logic Optimizations, Operations on Two level Logic Covers, Algorithms for Logic Minimization, Symbolic Minimization and Encoding Problems.
Multiple Level Combinational Logic Optimization: Introduction, Models and Transformations for Combinational Networks, The Algebraic Model, The Boolean Model.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-4

Sequential Logic Optimization: Introduction, Sequential Logic Optimization using State based Models, Sequential Logic Optimization using Network Models, Implicit FSM Traversal Methods, Testability concerns for Synchronous Circuits.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-5

Scheduling Algorithms: Introduction, A Model for Scheduling problems, Scheduling with Resource Constraints, Scheduling without Resource Constraints, Scheduling Algorithms for Extended Sequencing Models, Scheduling Pipelined Circuits.
Resource Sharing and Binding: Sharing and Binding for Resource dominated circuits, Sharing and Binding for General Circuits, Concurrent Binding and Scheduling.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks**

to attain the COs and POs

3. The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Text Books

1. 'Synthesis and Optimization of Digital Circuits', Giovanni De Micheli, Tata McGraw-Hill, ISBN: 780070582781, 2003.

Reference Books

1. 'Automatic Logic synthesis Techniques for Digital Systems', Edwars M.D,Macmillan New Electronic Series, 1992.

Web links and Video Lectures (e-Resources):

www.nptel.ac.in

Skill Development Activities Suggested

1) Interact with industry (small, medium, and large.
2) Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3) Involve in case studies and field visits/ fieldwork.
4) Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5) Handle advanced instruments to enhance technical talent.
6) Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7) Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Explain the process of synthesis and optimization in a top down approach for digital circuits models using HDLs	L2
CO2	Explain the terminologies of graph theory and its algorithms to optimize a Boolean equation	L2
CO3	Apply the different two level and multilevel optimization algorithms for combinational circuits	L3
CO4	Apply different sequential circuits optimization methods using state models and network models	L2
CO5	Apply different scheduling algorithms with resource binding and without resource binding for pipelined sequential circuits and extended sequencing models	L3

MEDICAL ELECTRONICS			
Course Code	22LIE245	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	2:0:2	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives:

1. To understand sources of biomedical signals, medical instrumentation system.
2. To understand biomedical instruments and their working.
3. To learn about patient monitoring systems.
4. To understand medical imaging systems.

Module-1

Bioelectric Signals and Electrodes : Sources of biomedical signals, Basic medical instrumentation system, General constraints in design of medical instrumentation systems, Origin of bioelectric signals, Electrocardiogram (ECG), Electroencephalogram (EEG), Electromyogram (EMG), Electrooculogram (EOG), Electroretinogram (ERG), Electrodes – Electrode-tissue interface, Polarization, Skin contact impedance, Motion artifacts, Silver-Silver Chloride electrodes, Electrical conductivity of electrode jellies and creams.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-2

Acquisition of Bioelectrical signals and Pacemakers: Electrodes for ECG, ECG leads, Effects of artifacts, Multi-channel ECG machine, Vectorcardiograph, Phonocardiograph, Electrodes of EMG, Electrodes for EEG, 10-20 electrode systems, computerized analysis of EEG, Pacemakers & Defibrillator: Need for cardiac pacemaker, External pacemaker, Implantable pacemakerstypes, Need for defibrillator, DC defibrillator, Automatic external defibrillator, Implantable defibrillators.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-3

Diagnosis and Therapeutic Instruments: Spirometry: Basic spirometer, Ultrasonic spirometer, Ventilators, types, Modern ventilators, High frequency ventilators, Nebulizers, Artificial Kidney: Introduction, Dialyzers, Membranes for Hemodialysis, Hemodialysis machine, Oximetry, Blood flow measurement by Doppler imaging, Nuclear Magnetic Resonance& Laser Doppler flow meter.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-4

Patient Monitoring Systems and Telemedicine: Cardiac monitor, Bedside patient monitoring system, measurement of heart rate-average and instantaneous heart rate meters, Measurement of pulse rate, Blood pressure measurement: Direct method, Indirect method-automatic pressure measurement using Korotkoff's method, Single channel telemetry systems, Multichannel wireless telemetry systems, Multi-patient telemetry, Telemedicine applications, Essential parameters for telemedicine, Telemedicine technology.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-5

Medical Imaging Systems: Basic components and working principle of X-rays, Ultrasound, Computed Tomography (CT), Magnetic Resonance Imaging (MRI)& Radionuclide Imaging.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks**

to attain the COs and POs

3. The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Text Books

1. 'R. S. Khandpur, Handbook of Biomedical Instrumentation, 2nd Edition, Tata McGraw Hill, 2003.
2. Kirk Shung, Michael Smith and Benjamin M.W Tsui, 'Principles of Medical Imaging', Academic Press limited, 1992
3. Biomedical Instrumentation and Measurement Leslie Cromwell, Fred J Weibell and Erich A. Pfeiffer, 2nd Edition, Prentice-Hall India

Reference Books

1. Guyton & Hall, 'Text Book Of Medical Physiology',11th edition, Saunders/Elsevier
2. ZhongHicho and Manbirsingh, **Fundamentals of medical imaging**, John Wiley

Web links and Video Lectures (e-Resources):

www.nptel.ac.in

Skill Development Activities Suggested

1) Interact with industry (small, medium, and large.
2) Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3) Involve in case studies and field visits/ fieldwork.
4) Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5) Handle advanced instruments to enhance technical talent.
6) Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7) Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Discuss the various sources of biomedical signals, medical instrumentation system.	L2
CO2	Explain the working of biomedical instruments.	L2
CO3	Discuss patient monitoring systems.	L2
CO4	Explain medical imaging systems.	L2

POWER ELECTRONICS LAB			
Course Code	22LIEL26	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	1:2:0	SEE Marks	50
Credits	02	Exam Hours	03

Course objectives:

5. To implement different techniques of message passing.
6. To develop and test programs.
7. To compare DFT and DCT using MatLab.
8. To design digital filters using suitable techniques.

Sl.NO	Experiments
1	Analysis of static and dynamic characteristic of MOSFET and IGBT.
2	Performance of single phase fully controlled and semi-controlled converter for RL load for continuous and discontinuous current mode operation.
3	Study of effect of source inductance on the performance of single phase fully controlled converter.
4	Performance analysis of three phase fully controlled and semi-controlled converter for RL load for Continuous and discontinuous current mode operation.
5	Performance analysis of single phase bridge inverter for RL load and voltage control by single pulse width modulation.
6	Performance analysis of two quadrant chopper.
7	Performance analysis of Diode clamped multilevel inverter.
8	ZVS operation of a Synchronous buck converter.
9	Simulation study of buck, boost and buck- boost converter (basic topologies) and analysis of wave formsfor continuous current mode (CCM).
10	Simulation study of forward converter and fly back converter and performance analysis of various waveforms.
11	Closed loop operation of a buck and boost converter.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

1. Analyze the static and dynamic characteristics of various semiconductor devices.
2. Apply the knowledge of converters in assessing the performance of single phase and three phase fully controlled and semi controlled converters for RL load for continuous current modes.
3. Apply the knowledge of converters in assessing the performance of single phase and three phase fully controlled and semi controlled converters for RL load for discontinuous current modes.
4. Assess the performance of single phase bridge inverter for RL load and control the voltage by pulse width modulation.
5. Apply the knowledge of power electronics in performance analysis of chopper and synchronous buck converter.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 40%of maximum marks in the semester-end examination(SEE). In total of CIE and SEE student has to secure 50% maximum marks of the course.

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of the semester and the second test shall be conducted after the 14th week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of **scaled-down** marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University.

- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.
- Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.
- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.
- General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

- Change of experiment is allowed only once and 10% Marks allotted to the procedure part to be made zero.
  The duration of SEE is 03 hours

III Semester

PLCs AND INDUSTRIAL AUTOMATION			
Course Code	22LIE31	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:0:2	SEE Marks	50
Total Hours of Pedagogy	50	Total Marks	100
Credits	04	Exam Hours	03

Course Learning objectives:

1. To understand the Programmable Logic Controllers.
2. To understand different types of Devices to which PLC input and outputmodules are connected.
3. To understand the ladder diagrams from process control descriptions.
4. To understand the PLC timers and counters for the control of industrial processes.
5. To understand the Knowledge of Networking in Industrial automation.

Module-1

Introduction to PLCs: Technical Definition, Advantages, Characteristic Functions, Chronological Evolution, Types, Unitary PLC, Modular PLC, SMEEl PLC, Medium PLC, Large PLC, Block Diagram Of PLC, Input / Output Section, Processor Section, Power Supply, Memory, Central Processing Unit, Processor Software / Executive Software, Multitasking, Languages, Ladder Language.

Bit Logic Instructions: Introduction, Input and Output Contact Program, Symbols, Numbering System of Inputs and Outputs, Program Format, Introduction to Logic, Equivalent Ladder Diagram of - AND Gate, OR Gate, NOT Gate, XOR Gate, NAND Gate, NOR Gate, Equivalent Ladder Diagram to Demonstrate De Morgan Theorem, Ladder Design.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-2

PLC Timers and Counters: Timer and its Classification, Characteristics of PLC Timer, Functions in Timer, Resetting – Retentive and Non-Retentive, Classification of PLC Timer, On Delay, and Off Delay Timers, Timer-On Delay, Timer Off Delay, Retentive And Non-Retentive Timers, Format of a Timer Instruction. PLC Counter, Operation of PLC Counter, Counter Parameters, Counter Instructions. Overview, Count Up (CTU), Count Down (CTD).

Advanced Instructions: Comparison Instructions, Addressing Data Files, Format of Logical Address, Addressing Format for Micrologic System, Different Addressing Types. Data Movement Instructions.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-3

Logical Instructions: Mathematical Instructions and its Features, Special Mathematical Instructions, Scale with Parameters or SCP Instruction. Data Handling Instructions and its Features, Program Flow Control Instructions, Proportional Integral Derivative (PID) Instruction.

PLC I/O Modules and Power Supply: Classification of I/O, I/O SystemOverview, Practical I/O System and its mapping, Addressing Local and Expansion I/O, Input-Output Systems, Direct I/O Parallel I/O Systems Serial I/O Systems, Sinking and Sourcing, Sourcing and Sinking in PLC Interfacing, Discrete Input Module, Discrete DC Input Module, Discrete AC Input Module, Rectifier with Filter, Threshold Detection, Isolation, Logic Section, Discrete Output Modules, Advantages and Disadvantages of Output Modules, Types of Analog Input Module.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-4

Industrial Communication: Introduction, Evolution of Industrial Control Process, Types of Communication Interface, Types of Networking Channels, Parallel Communication Interface. Serial Communication Interface, communication mode, Synchronous and Asynchronous Transmissions, Standard interface RS 232C, RS 422, EIA 485, Comparison, Software Protocol, Industrial Network. Network Topology, Media Access Methods.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-5	
Industrial Networking: Open System Interconnection (OSI), Network Model, Network Components, Control Network Issues, Advantage of Standardized Industrial Network, Intelligent Devices, Industrial Network Bus Network, Device Bus Network vs. Process Bus Network, Controller Area Network(CAN), Devicenet, Controlnet, Ethernet Protocol, AS-I Interface, FOUNDATION FIELDBUS, Application of Profibus for Real PLC Communication. **Industrial Automation:** Introduction, Utility of Automation, General Structure of an Automated Process, Examples of Simple Automated Systems, Selection ofPLC.	
Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs
3. The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Text Books

1. 'Programmable LogicControllers and Industrial Automation', Madhuchhanda Mitra and Samarjit Sengupta,Penram International Publishing (India)Pvt. Ltd., 2007. ISBN: 81-87972-17-3.

Reference Books

1. 'Introduction to Programmable Logic Controllers', Garry Dunning, 2nd Edition, Delmar Thomson Learning, 2001. ISBN: 981-240-625-5.
2. 'Computer Control of Processes',M. Chidambaram, CRC Press, 2002.

Web links and Video Lectures (e-Resources):

www.nptel.ac.in

Skill Development Activities Suggested

1) Interact with industry (small, medium, and large.
2) Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3) Involve in case studies and field visits/ fieldwork.
4) Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5) Handle advanced instruments to enhance technical talent.
6) Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7) Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Explain and discuss the Programmable Logic Controllers.	L3
CO2	Explain different types of Devices to which PLC input and output modules are connected.	L2
CO3	Draw ladder diagrams from process control descriptions.	L3
CO4	Apply PLC timers and counters for the control of industrial processes.	L4
CO5	Discuss Networking in Industrial automation.	L3

III Semester

AUTOMATIVE ELECTRONICS			
Course Code	22LIE321	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives:

1. To understand various control requirements in the automotive system.
2. To understand the dashboard electronics and engine system electronics.
3. To understand various physical parameters that are to be sensed and monitored for maintaining the stability of the vehicle under dynamic conditions.
4. To understand and implement the controls and actuator system pertaining to the comfort and safety of commuters.
5. To understand sensor network for mechanical fault diagnostics in anautomotive vehicle.

Module-1

Automotive Fundamentals, the Systems Approach to Control and Instrumentation: Use of Electronics in the Automobile, Antilock Brake Systems(ABS), Electronic steering control, Power steering, Traction control, Electronically controlled suspension (Chap.1 and 2 of Text).

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-2

Automotive instrumentation Control: Operational amplifiers, Digital circuits,Logic circuits, Microcomputer fundamentals, Microcomputer operations, Microprocessor architecture, digital to analog converter, analog to digital converter, Microcomputer applications in automotive systems, Instrumentation applications of microcomputers, Microcomputer in control systems (Chap.3 and4 of Text).

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-3

The basics of Electronic Engine control: Integrated body: Climate controls, Motivation for Electronic Engine Control, Concept of An Electronic Engine Control System, Definition of General Terms, Definition of Engine Performance Terms, Electronic fuel control system, Engine control sequence, Electronic Ignition, Sensors and Actuators, Applications of sensorsand actuators, air flow rate sensor, Indirect measurement of mass air flow, Engine crankshaft angular position sensor, Automotive engine control actuators, Digital engine control, Engine speed sensor, Timing sensor for ignition and fuel delivery, Electronic ignition control systems, Safety systems, Interior safety, Lighting, Entertainment systems (Chap. 5 and 6 of Text).

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-4

Vehicle Motion Control and Automotive diagnostics: Cruise control system, Digital cruise control, Timing light, Engine analyzer, On-board and off-board diagnostics, Expert systems. Stepper motor-based actuator, Cruise control electronics, Vacuum - antilock braking system, Electronic suspension system, Electronic steering control, Computer-based instrumentation system, Sampling and Input\output signal conversion, Fuel quantity measurement, Coolant temperature measurement, Oil pressure measurement, Vehicle speed measurement, Display devices, Trip-Information-Computer, Occupant protection systems (Chap. 8 and 10 of Text).

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-5

Future automotive electronic systems: Alternative Fuel Engines, Collision Wide Range Air/Fuel Sensor, Alternative Engine, Low Tire Pressure Warning System, Collision avoidance Radar Warning Systems, Low Tire Pressure Warning System, Radio Navigation, Advance Driver information System. Alternative-Fuel Engines, Transmission Control, Collision Avoidance Radar Warning System, Low Tire Pressure Warning System, Speech Synthesis Multiplexing in Automobiles, Control Signal Multiplexing, Navigation Sensors, Radio Navigation, Signpost Navigation, Dead Reckoning Navigation Future Technology, Voice Recognition Cell

Phone Dialing Advanced Driver information System, Automatic Driving Control (Chap. 11 of Text).	
Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs
3. The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Text Books

1. 'Understanding Automotive Electronics', William B.Ribbens,SAMS/Elsevier publishing, 6thEdition, 1997.

Reference Books

1. 'Automotive Electrics and Automotive Electronics-Systems and Components, Networking and Hybrid Drive', Robert Bosch Gmbh, Springer Verlag,5thEdition, 2007.

Web links and Video Lectures (e-Resources):

www.nptel.ac.in

Skill Development Activities Suggested

1) Interact with industry (small, medium, and large.
2) Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3) Involve in case studies and field visits/ fieldwork.
4) Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5) Handle advanced instruments to enhance technical talent.
6) Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7) Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Implement various control requirements in the automotive system.	L3
CO2	Comprehend dashboard electronics and engine system electronics.	L2
CO3	Identify various physical parameters that are to be sensed and monitored for maintaining the stability of the vehicle under dynamic conditions.	L2
CO4	Understand and implement the controls and actuator system pertaining to the comfort and safety of commuters.	L4
CO5	Design sensor network for mechanical fault diagnostics in anautomotive vehicle.	L4

III Semester

Advanced Power Electronic Converters and Applications			
Course Code	22LIE322	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives:

1. To understand the dynamics of power electronic converters
2. To understand the sustainable energy generation technologies.
3. To model and analysis of power electronic systems andequipment using computational software.
4. To Simulate and analyze resonant converters.
5. To apply the knowledge of mathematics to converter/machine dynamics inElectrical engineering.

Module-1

Introduction to power electronics: Introduction to Power Processing, Several Applications of Power Electronics, Elements of Power Electronics.
Principles of Steady State Converter Analysis: Inductor Volt- Second Balance, Capacitor Charge Balance, and the Small- Ripple Approximation, Boost Converter Example, Cuk Converter Example Estimating the Output voltage ripple and inductor current ripple in converters Containing Two-Pole Low-Pass Filter(Text 1).

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-2

Converter Dynamics and Control: AC Equivalent Circuit Modeling, TheBasic AC Modeling Approach, State-Space Averaging, Circuit Averaging and Averaged Switch Modeling, The Canonical Circuit Model, Modeling the Pulse- Width Modulator, Analysis of Converter Transfer Functions, Graphical Construction of Impedances and Transfer Functions(Text 1).

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-3

Controller Design: Introduction, Effect of Negative Feedback on the Network Transfer Functions, Construction of the Important Quantities 1/(1 + T) and T/(1+ T) and the Closed-Loop Transfer Functions, Stability, The Phase Margin Test, The Relationship Between Phase Margin and Closed-Loop Damping Factor, Transient Response vs. Damping Factor, Regulator Design, Measurementof Loop Gains (Text 1).

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-4

Modern Rectifiers and Power System Harmonics: Power and Harmonics in Non-sinusoidal Systems, Pulse-Width Modulated Rectifiers.
Resonant Converters: Sinusoidal Analysis of Resonant Converters withexamples (Text 1).

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-5

Power supply applications: Switching DC Power Supplies, Motor drive applications: Introduction to Motor Drives, DC-Motor Drives, Residential and Industrial Applications, Electric Utility Applications (Text 2).

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs
3. The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Text Books

1. 'Fundamentals of Power Electronics', Erickson and Maksimovic, 2nd Edition, Kluwer Academic Publishers, 2001.
2. 'Power Electronics converters, Applications and Design', MNed Mohan, Tore Undeland and William P Robbins, John Wiley and Sons, 3rd Edition, 2002.

Reference Books

1. 'Switching Power Supply Design', Abraham Pressman, McGraw-Hill Publishers, 1998.
2. 'Power Electronics Handbook', Muhammad H.Rashid, 2nd Edition, Academic Press, 2007.

Web links and Video Lectures (e-Resources):

www.nptel.ac.in

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Estimate and analyze the dynamics of power electronic converters	L3
CO2	Explain the sustainable energy generation technologies.	L2
CO3	Perform Modelling and analysis of power electronic systems andequipment using computational software.	L4
CO4	Simulate and analyze resonant converters.	L4
CO5	Apply the knowledge of mathematics to converter/machine dynamics in Electrical engineering.	L4

III Semester

Pattern Recognition & Machine Learning			
Course Code	22LIE323	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives:

1. To understand the areas where Pattern Recognition and Machine Learning can offer a solution.
2. To understand the strength and limitations of some techniques used in computational Machine Learning for classification, regression and density estimation problems.
3. To understand and model data.
4. To solve problems in Regression and Classification.
5. To understand the main and modern concepts for model selection and parameter estimation in recognition, decision making and statistical learning problems.

Module-1

Introduction: Probability Theory, Model Selection, The Curse of Dimensionality, Decision Theory, information Theory.
Distributions: Binary and Multinomial Variables, The Gaussian Distribution,The Exponential Family, Nonparametric Methods (Ch. 1,2).

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-2

Supervised Learning
Linear Regression Models: Linear Basis Function Models, The Bias-VarianceDecomposition, Bayesian Linear Regression, Bayesian Model Comparison.
Classification & Linear Discriminant Analysis: Discriminant Functions,Probabilistic Generative Models, Probabilistic Discriminative Mode (Ch. 3,4).

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-3

Supervised Learning
Kernels: Dual Representations, Constructing Kernels, Radial Basis FunctionNetwork, Gaussian Processes
Support Vector Machines: Maximum Margin Classifiers, Relevance Vector Machines.
Neural Networks: Feed-forward Network, Network Training, ErrorBack propagation (Ch. 5,6,7).

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-4

Unsupervised Learning
Mixture Models: K-means Clustering, Mixtures of Gaussians, Maximumlikelihood, EM for Gaussian mixtures, Alternative View of EM. **Dimensionality Reduction:** Principal Component Analysis, Factor/ComponentAnalysis, Probabilistic PCA, Kernel PCA, Nonlinear Latent Variable Models(Ch. 9,12).

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-5

Probabilistic Graphical Models: Bayesian Networks, Conditional Independence, Markov Random Fields, Inference in Graphical Models, MarkovModel, Hidden Markov Models (Ch.8,13).

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs
3. The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Text Books

1. 'Pattern Recognition and Machine Learning', Christopher Bishop, Springer,2006.

Web links and Video Lectures (e-Resources):

www.nptel.ac.in

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Identify areas where Pattern Recognition and Machine Learning can offer a solution.	L2
CO2	Describe the strength and limitations of some techniques used in computational Machine Learning for classification, regression and density estimation problems.	L2
CO3	Describe and model data.	L2
CO4	Solve problems in Regression and Classification.	L4
CO5	Discuss main and modern concepts for model selection and parameter estimation in recognition, decision making and statistical learning problems.	L3

III Semester

COMMUNICATION SYSTEM DESIGN USING DSP ALGORITHMS			
Course Code	22LIE324	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives:

1. To understand communication systems, including algorithms that are particularlysuited to DSP implementation.
2. To learn DSP algorithms on TI DSP processors
3. To learn FIR, IIR digital filtering and FFT methods
4. To learn modulators and demodulators for AM, DSBSC-AM, SSB andFM
5. To learn the design of digital communication methods leading to the implementation of aline communication system.

Module-1

Introduction to the course: Digital filters, Discrete time convolution and frequency responses, FIR filters - Using circular buffers to implement FIR filters in C and using DSP hardware, Interfacing C and assembly functions, Linear assembly code and the assembly optimizer. IIR filters - realization and implementation, FFT and power spectrum estimation: DTFT window function, DFT and IDFT, FFT, Using FFT to implement power spectrum.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-2

Analog modulation scheme: Amplitude Modulation - Theory, generation and demodulation of AM, Spectrum of AM signal, Envelope detection and square law detection, Hilbert transform and complex envelope, DSP implementation ofamplitude modulation and demodulation.
DSBSC: Theory generation of DSBSC, Demodulation, and demodulation using coherent detection and Costas loop. Implementation of DSBSC using DSPhardware.
SSB: Theory, SSB modulators, Coherent demodulator, Frequency translation, Implementation using DSP hardware.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-3

Frequency modulation: Theory, Single tone FM, Narrow band FM, FM bandwidth, FM demodulation, Discrimination and PLL methods,Implementation using DSP hardware.
Digital Modulation scheme: PRBS, and data scramblers: Generation of PRBS, Self-synchronizing data scramblers, Implementation of PRBS and data scramblers. RS-232C protocol and BER tester: The protocol, error rate for binary signaling on the Gaussian noise channels, Three-bit error rate tester and implementation.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-4

PAM and QAM: PAM theory, baseband pulse shaping and ISI, Implementation of transmit filter and interpolation filter bank. Simulation and theoretical exercises for PAM, Hardware exercises for PAM.

QAM fundamentals: Basic QAM transmitter, 2 constellation examples, QAM structures using pass-band shaping filters, Ideal QAM demodulation, QAM experiment. QAM receivers-Clock recovery and other frontend sub-systems. Equalizers and carrier recovery systems.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-5

Experiment for QAM receiver frontend, Adaptive equalizer, Phase splitting,Fractionally spaced equalizer. Decision directed carrier tracking, Blindequalization, Complex cross coupled equalizer and carrier tracking experiment. Echo cancellation for full duplex modems: Multicarrier modulation, ADSLarchitecture, Components of simplified ADSL transmitter, A simplified ADSLreceiver, Implementing simple ADSL Transmitter and Receiver.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs
3. The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Text Book:

'Communication System Design using DSP Algorithms with Laboratory Experiments for the TMS320C6713 DSK', Steven A Tretter, Springer, 2008.

Web links and Video Lectures (e-Resources):

www.nptel.ac.in

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Realize communication systems, including algorithms that are particularlysuited to DSP implementation	L2
CO2	Implement DSP algorithms on TI DSP processors	L3
CO3	Implement FIR, IIR digital filtering and FFT methods	L3
CO4	Implement modulators and demodulators for AM, DSBSC-AM, SSB andFM	L3
CO5	Design digital communication methods leading to the implementation of aline communication system.	L4

III Semester

ADVANCED SENSORS			
Course Code	22LIE325	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives:

1. To understand working of various chemical sensors, materials for sensors.
2. To understand process involved, thin and thick film.
3. To understand working of biosensors.
4. To understand integrated magnetic sensors.
5. To understand the applications of various sensors.

Module-1

Chemical Sensors: Amperometry-Potentiometry-Conductivity sensors- Semi conductive sensors-MEMSsensors. Materials for Sensors-Electrical conducting materials- Ionic conductors zirconia-alumina-NASICON. Semiconductor materials-titania-tinoxide-zinc oxide. Insulating materials- Ferroelectric Materials-Negative temperature ceramic thermistors.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-2

Thin and Thick film sensors: Thick film Processes-Thin film processes- Thin film deposition methods- thin film characterization methods-thin film delineation techniques-compatibility issues- Longmuir-Blodgett films for sensor materials-film forming apparatus-dipping-ion sensors-gas sensors. Applications of thin and thick film sensors.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-3

Biosensors: Colorimetric- Optical- Potentiometric- Amperometic- Conductometric Semiconductor-Mechanical and Molecular electronic based sensors. Chemiluminescence based biosensors. Applications of biosensors in medical and health care- food and agricultural Industrial process and environmental monitoring.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-4

Integrated Magnetic Sensors: Overview of magnetic field sensor Technology-AMR-GMRSQUIDS-Optoelectronic MFS- Semiconductor magnetic effects-materials and figure of merit Standard MFS technologies-limitations and applications.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-5

Sensor Applications: Automotive Sensors-Environmental Sensors-Sensors for Medical Diagnosis and patient monitoring-Aerospace sensors.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs
3. The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Text Books:

1. Sensors- A Comprehensive study-W.Gopal, J Hesse, J N Zemel –VHC Press, 1989.
2. Sensors Handbook-Sabree Soloman—McGraw Hill Publishers-1998
3. Electro Optical Instrumentation- SilvanoDonati, Pearson Education 2005.
4. Introduction to Medical Equipment Technology: Carr and Brown- Addison Weseley2001.

Web links and Video Lectures (e-Resources):

www.nptel.ac.in

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Explain the working of various chemical sensors, materials for sensors.	L2
CO2	Explain the process involved, thin and thick film.	L2
CO3	Explain the working of biosensors.	L2
CO4	Explain the integrated magnetic sensors.	L2
CO5	Discuss the applications of various sensors.	L3

III Semester

ADVANCES IN IMAGE PROCESSING			
Course Code	22LIE331	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives:

1. To acquire fundamental knowledge in understanding the representation of the digital image and its properties
2. To equip with some pre-processing techniques required to enhance the image for further analysis purpose.
3. To select the region of interest in the image using segmentation techniques.
4. To represent the image based on its shape and edge information.
5. To describe the objects present in the image based on its properties and structure.

Module-1

The image, its representations and properties: Image representations a few concepts, Image digitization, Digital image properties, Color images.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-2

Image Pre-processing: Pixel brightness transformations, geometric transformations, local pre-processing.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-3

Segmentation: Thresholding; Edge-based segmentation – Edge image thresholding, Edge relaxation, Border tracing, Hough transforms; Region – based segmentation – Region merging, Region splitting, Splitting and merging, Watershed segmentation, Region growing post-processing.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-4

Shape representation and description: Region identification; Contour-based shape representation and description – Chain codes, Simple geometric border representation, Fourier transforms of boundaries, Boundary description using segment sequences, B-spline representation; Region-based shape representation and description – Simple scalar region descriptors, Moments, Convex hull.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-5

Mathematical Morphology: Basic morphological concepts, Four morphological principles, Binary dilation and erosion, Skeletons and object marking, Morphological segmentations and water sheds.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs
3. The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Text Book:

1. Milan Sonka, Vaclav Hlavac, Roger Boyle, "Image Processing, Analysis, and Machine Vision", Cengage Learning, 2013, ISBN: 978-81-315- 1883-0

Reference Books:

1. Geoff Doughertry, Digital Image Processing for Medical Applications, Cambridge university Press, 2010
2. S.Jayaraman, S Esakkirajan, T.Veerakumar, Digital Image Processing, Tata McGraw Hill, 2011.

Web links and Video Lectures (e-Resources):

www.nptel.ac.in

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Understand the representation of the digital image and its properties.	L2
CO2	Apply pre-processing techniques required to enhance the image for its further analysis.	L3
CO3	Use segmentation techniques to select the region of interest in the image for analysis	L4
CO4	Represent the image based on its shape and edge information.	L3
CO5	Describe the objects present in the image based on its properties and structure.	L3
CO6	Use morphological operations to simplify images, and quantify and preserve the main shape characteristics of the objects.	L3

III Semester

MEDICAL IMAGING			
Course Code	22LIE332	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives:

1. To acquire the knowledge of all currently available imaging procedures such as X-Ray Imaging, X-Ray Tomography, Radio Nuclide Imaging and Ultrasonic Imaging.
2. To understand the characteristics of X-ray, MRI and Radio Nuclide images.
3. To learn the Biological effects of X-Rays and Ultrasound.
4. To acquire the knowledge of some of the recent developments in the field of medical imaging.
5. To learn the procedures used for the generation and detection of X-rays, MRI and Ultrasound.

Module-1

Generation and Detection of X-Rays: X-Ray generation and X-Ray generators, Filters, Beam Restrictors and Grids, Screens, X-Ray Detectors.
X-Ray Diagnostic Methods: Conventional X-Ray Radiography, Fluoroscopy, Angiography, Mammography, Xeroradiography, Image Subtraction.
X-Ray Image Characteristics: Spatial Resolution, Image Noise, Image contrast.
Biological Effects of Ionizing Radiation: Determination of biological effects, Short term and Long term effects.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-2

X-Ray Tomography: Conventional Tomography, Computed Tomography - Projection function, Algorithms for Image Reconstruction, CT number, Image Artifacts.
Digital Radiography: Digital Subtraction Angiography (DSA), Dual Energy Subtraction, K-Edge subtraction, 3-D Reconstruction.
Recent Developments: Dynamic Spatial Reconstructor (DSR), Imatron or Fastrac Electron Beam CT.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-3

Generation and Detection of Ultrasound: Piezoelectric effect, Ultrasonic Transducers, Transducer Beam Characteristics, Axial and Lateral resolution, Focussing and Arrays.

Ultrasonic Diagnostic Methods: Pulse Echo systems - A mode, B mode, M mode and C mode, Transmission Methods, Doppler methods, Duplex Imaging.

Biological Effects of Ultrasound: Acoustic phenomena at high intensity levels, Ultrasound Bioeffects.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-4

Generation and Detection of Nuclear Emission: Nuclear Sources, Radionuclide Generators, Nuclear Radiation Detectors, Collimators.

Diagnostic methods using Radiation Detector Probes: Thyroid Function test, Renal function test, Blood volume measurement.

New Radio Nuclide Imaging methods: Longitudinal Section Tomography, SPECT and PET.

Characteristics of Radionuclide Images: Spatial Resolution, Image contrast, Image Noise.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-5

Generation and Detection of NMR signal: The NMR Coil/Probe, The transmitter and the Receiver, Data acquisition.

Magnetic Resonance Imaging methods: Spin Echo Imaging, Gradient Echo Imaging, Blood flow Imaging.

Characteristics of MRI images: Spatial Resolution, Image Contrast.

Imaging Safety

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs
3. The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Text Book:

1. Kirk Shung, Michael B, Smith, Benjamin M W Tsui, "Principles of Medical Imaging", Academic Press, 2012.

Reference Books:

1. Zhong Hicho and Manbir Singh "Fundamentals of Medical Imaging", John Wiley, 1993.
2. Peter Josefell & Edward Sudney "Nuclear Medicine Introductory Text", William Blackwell Scientific Publishers, London.

Web links and Video Lectures (e-Resources):

www.nptel.ac.in

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Understand the Generation and Detection of X-Rays, the Diagnostic Methods, Characteristics of X-ray images and Biological effects of X-rays.	L3
CO2	Analyze Computed tomography and Digital Radiography.	L3
CO3	Learn the techniques of Generation and Detection of Ultrasound, Pulse Echo Systems and Ultrasonic Diagnostic Methods.	L4
CO4	Understand the principles of various radiological imaging techniques such as SPECT and PET.	L3
CO5	Understand the principles of Magnetic Resonance Imaging, the concepts of Radionuclide Generation and Detection.	L3

III Semester

INTERNET OF THINGS			
Course Code	22LIE333	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives:

1. To understand the basic concepts IoT Architecture and devices employed.
2. To understand and analyze the sensor data generated and map it to IoT protocol stack for transport.
3. To understand and apply communication knowledge to facilitate transport of IoT data over various available communications media.
4. To understand a use case for a typical application in real life ranging from sensing devices to analyzing the data available on a server to perform tasks on the device.
5. To understand and apply the knowledge of Information technology to design of IoT applications (Operational Technology).

Module-1

What is IoT ?
Genesis, Digitization, Impact, Connected Roadways, Buildings, Challenges
IoT Network Architecture and Design
Drivers behind new network Architectures, Comparing IoT Architectures, M2M architecture, IoT world forum standard, IoT Reference Model, Simplified IoT Architecture.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-2

IoT Network Architecture and Design
Core IoT Functional Stack, Layer1 (Sensors and Actuators), Layer 2 (Communications Sublayer), Access network sublayer, Gateways and backhaul sublayer, Network transport sublayer, IoT Network management. Layer 3 (Applications and Analytics) – Analytics vs Control, Data vs Network Analytics, IoT Data Management and Compute Stack.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-3

Engineering IoT Networks
Things in IoT – Sensors, Actuators, MEMS and smart objects. Sensor networks, WSN, Communication protocols for WSN
Communications Criteria, Range, Frequency bands, power consumption, Topology, Constrained Devices, Constrained Node Networks
IoT Access Technologies, IEEE 802.15.4
Competitive Technologies – Overview only of IEEE 802.15.4g, 4e, IEEE1901.2a
Standard Alliances – LTE Cat 0, LTE-M, NB-IoT.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-4

Engineering IoT Networks
IP as IoT network layer, Key Advantages, Adoption, Optimization, Constrained Nodes, Constrained Networks, IP versions, Optimizing IP for IoT.

Application Protocols for IoT – Transport Layer, Application Transport layer, Background only of SCADA, Generic web based protocols, IoT Application Layer
Data and Analytics for IoT – Introduction, Structured and Unstructured data, IoT Data Analytics overview and Challenges.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-5

IoT in Industry (Three Use cases)
IoT Strategy for Connected manufacturing, Architecture for Connected Factory Utilities – Power utility, IT/OT divide, Grid blocks reference model, ReferenceArchitecture, Primary substation grid block and automation. Smart and Connected cities –Strategy, Smart city network Architecture, Street layer, city layer, Data center layer, services layer, Smart city security architecture, Smart street lighting.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs
3. The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Text Book:

1. 'CISCO, IoT Fundamentals – Networking Technologies, Protocols, Use Cases for IoT', David Hanes, Gonzalo Salgueiro, Patrick Grossetete, Robert Barton, Jerome Henry, Pearson Education, ISBN: 978-9386873743, First edition, 2017

Reference Books:

1. 'Internet of Things – A Hands on Approach', ArshdeepBahga and Vijay Madisetti, Orient Blackswan Private Limited - New Delhi, First edition,2015

Web links and Video Lectures (e-Resources):

www.nptel.ac.in

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Explain the basic concepts IoT Architecture and devices employed.	L2
CO2	Analyze the sensor data generated and map it to IoT protocol stack for transport.	L4
CO3	Apply communications knowledge to facilitate transport of IoT data over various available communications media.	L3
CO4	Design a use case for a typical application in real life ranging from sensing devices to analyzing the data available on a server to perform tasks on the device.	L3
CO5	Apply knowledge of Information technology to design of IoT applications (Operational Technology).	L3

III Semester

REAL TIME SYSTEMS			
Course Code	22LIE334	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives:

1. To understand basics of Real Time systems.
2. To distinguish a real-time system with other systems.
3. To identify the functions of operating system.
4. To evaluate the need for Real time operating system.
5. To design and develop embedded applications by means of real-time operating systems.

Module-1

Introduction to Real-Time Embedded Systems: Brief history of Real Time Systems, A brief history of Embedded Systems.
System Resources: Resource Analysis, Real-Time Service Utility, Scheduling Classes, The Cyclic Executive, Scheduler Concepts, Preemptive Fixed Priority Scheduling Policies, Real-Time OS, Thread Safe Re-entrant Functions.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-2

Processing: Preemptive Fixed-Priority Policy, Feasibility, Rate Montonic least upper bound, Necessary and Sufficient feasibility, Deadline – Monotonic Policy, Dynamic priority policies.
I/O Resources: Worst-case Execution time, Intermediate I/O, Execution efficiency, I/O Architecture.
Memory: Physical hierarchy, Capacity and allocation, Shared Memory, ECC Memory, Flash file systems.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-3

Multi-resource Services: Blocking, Deadlock and livestock, Critical sections to protect shared resources, priority inversion.
Soft Real-Time Services: Missed Deadlines, QoS, Alternatives to rate monotonic policy, Mixed hard and soft real-time services.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-4

Embedded System Components: Firmware components, RTOS system software mechanisms, Software application components.
Debugging Components: Exceptions assert, Checking return codes, Single-step debugging, kernel scheduler traces, Test access ports, Trace ports, Power-On self test and diagnostics.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-5

Performance Tuning: Basic concepts of drill-down tuning, hardware – supported profiling and tracing, Building performance monitoring into software, Path length.
High availability and Reliability Design: Reliability and Availability, Similarities and differences, Reliability, Reliable software, Available software, Design tradeoffs, Hierarchical applications for Fail-safe design.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs
3. The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Text Book:

Sam Siewert, "Real-Time Embedded Systems and Components", Cengage Learning India Edition, 2007.

Reference Books:

1. Krishna CM and Kang Singh G, "Real time systems", Tata McGraw Hill, 2003, ISBN: 0-07-114243-64
2. Qing Li and Carolyn Yao, "Real-Time Concepts for Embedded Systems", CMP Books, 2003, ISBN:1578201241
3. Jane W. S. Liu, "Real Time Systems", Prentice Hall, 2000, ISBN: 0130996513
4. Phillip A. Laplante, "Real-Time Systems Design and Analysis", John Wiley & Sons, 2004.

Web links and Video Lectures (e-Resources):

www.nptel.ac.in

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Analyze Real time operating systems.	L3
CO2	Describe the functions of Real time operating systems.	L3
CO3	Demonstrate embedded system applications.	L3
CO4	Design a Real Time operating system.	L4

III Semester

SMART MATERIALS			
Course Code	22LIE335	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives:

1. To understand various smart materials, their physical properties.
2. To understand and working of smart sensors, actuators and transducers.
3. To understand the working of signal conditioning devices, measuring and control techniques in signals processing.
4. To understand the design, analysis, manufacturing and application issues involved in integrating smart materials and devices with the help of case studies.
5. To apply Engineering Smart Structures and Products for automation and precision manufacturing equipment, automotives and consumer products.

Module-1

Overview of Smart Materials, Structures and Products Technologies. Physical Properties of Piezoelectric Materials, Electrostrictive Materials, Magnetostrictive Materials, Magneto electric Materials. Magnetorheological Fluids, Electrorheological Fluids, Shape Memory Materials, Fiber-Optic Sensors.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-2

Smart Sensors: Accelerometers; Force Sensors; Load Cells; Torque Sensors; Pressure Sensors; Microphones; Impact Hammers; MEMS Sensors; Sensor Arrays.
Smart Actuators: Displacement Actuators; Force Actuators; Power Actuators; Vibration Dampers; Shakers; Fluidic Pumps; Motors.
Smart Transducers: Ultrasonic Transducers; Sonic Transducers; Air Transducers

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-3

Measurement, Signal Processing, Drive and Control Techniques in Quasi-Static and Dynamic Measurement Methods; Signal-Conditioning Devices; Constant Voltage, Constant Current and Pulse Drive Methods; Calibration Methods; Structural Dynamics and Identification Techniques; Passive, Semi-Active and Active Control; Feedback and Feed forward Control Strategies.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-4

Design, Analysis, Manufacturing: Case studies incorporating design, analysis, manufacturing and application issues involved in integrating smart materials and devices with signal processing and control capabilities to engineering applications.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Module-5

Applications of Engineering Smart Structures and Products. Emphasis on structures, automation and precision manufacturing equipment, automotives, consumer products, sporting products, computer and telecommunications products, as well as medical and dental tools and equipment.

Teaching-Learning Process	1. Chalk & Talk 2. PPT 3. Videos

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs
3. The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Text Book:

1. M. V. Gandhi and B. So Thompson, Smart Materials and Structures, Chapman & Hall, London; New York, 1992 (ISBN: 0412370107).
2. B. Culshaw, Smart Structures and Materials, Artech House, Boston, 1996 (ISBN: 0890066817).

Reference Books:

1. A. V. Srinivasan, Smart Structures: Analysis and Design, Cambridge University Press, Cambridge; New York, 2001 (ISBN: 0521650267).
2. A. J. Molson and J. M. Herbert, Electro ceramics: Materials, Properties, Applications, 2nd Edition, John Wiley & Sons, Chichester, West Sussex; New York, 2003 (ISBN: 0471497479).
3. G. Gautschi, Piezoelectric Sensorics: Force, Strain, Pressure, Acceleration and Acoustic Emission Sensors. Materials and Amplifiers, Springer, Berlin; New York, 2002 (ISBN: 3540422595).
4. K. Uchino, Piezoelectric Actuators and Wtrasonic Motors, Kluwer Academic Publishers, Boston, 1997 (ISBN: 0792398114).

Web links and Video Lectures (e-Resources):

www.nptel.ac.in

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Explain various smart materials, their physical properties.	L3
CO2	Explain working of smart sensors, actuators and transducers.	L3
CO3	Explain the working of signal conditioning devices, measuring and control techniques in signals processing.	L3
CO4	Design, analysis, manufacturing and application issues involved in integrating smart materials and devices with the help of case studies.	L4
CO5	Apply Engineering Smart Structures and Products to automation and precision manufacturing equipment, automotives and consumer products.	L4