**Semester - 1**

| ICT-1 (IPCC) | | | |
|---|---|---|---|
| Course Code | 22EMS12 | CIE Marks | 50 |
| Teaching Hours/Week (L:P:SDA) | 03:02:00 | SEE Marks | 50 |
| Total Hours of Pedagogy | 40 hours Theory + 10-12 Lab slots | Total Marks | 100 |
| Credits | 04 | Exam Hours | 03 |

**Course objectives:**

- . To remember the basics of process control and understand the basic concepts of Industrial Automation.
- To apply the control system concepts to Special Intelligent control strategies.
- To analyze and evaluate the concepts of DCS to different types of Industries.
- Comprehensive coverage of communication protocols that are used in automation systems.

| MODULE-1 | |
|---|---|
| **Industrial Control Systems:** Embedded Control Systems, Real-Time Control Systems, Distributed Control System.<br>**Industrial Control Engineering:** Industrial Process Controls,Industrial Motion Controls, Industrial Production Automation | |
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

| MODULE-2 | |
|---|---|
| **Sensors and Actuators:** Industrial Optical Sensors, Industrial Physical Sensors,Industrial Measurement Sensors, Industrial Actuators. | |
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

| MODULE-3 | |
|---|---|
| **Transducers and Valves:** Industrial Switches, Industrial Transducers, Industrial Valves | |
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

| MODULE-4 | |
|---|---|
| **Microprocessors:** Single-Core Microprocessor Units, Multicore Microprocessor Units. | |
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

| MODULE 5 | |
|---|---|
| **Programmable-Logic and Application-Specific Integrated Circuits (PLASIC):** Fabrication Technologies and Design Issues, Field-Programmable-Logic Devices, Peripheral ProgrammableLogic Devices. ■ | |
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

**PRACTICAL COMPONENT OF IPCC** *(May cover all / major modules)*

| Sl.NO | Experiments |
|---|---|
| 1 | Program to toggle all the bits of port P1 continuously with a desired time delay. |
| 2 | Program to interface LCD data pins to port P1 and display a message on it |
| 3 | To study a Linear Variable Differential Transformer (LVDT) and use it in a simple experimental set up to measure a small displacement. |
| 4 | To measure static/dynamic pressure of fluid in pipe/tube using pressure transducer/pressure cell. |
| 5 | To obtain the characteristics of control valve. |
| 6 | Design and Develop an Assembly Program to sort a given set of 'n' 16-bit numbers in ascending order. |
| 7 | Develop an assembly language program to reverse a given string and verify whether it is a palindrome or not. |
| 8 | Program to read data from temperature sensor and display the temperature value. |
| 9 | Program to interface Stepper Motor to rotate the motor in clockwise and anticlockwise Directions. |

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together

**CIE for the theory component of IPCC**

1. Two Tests each of **20 Marks**
2. Two assignments each of **10 Marks/One Skill Development Activity of 20 marks**
3. Total Marks of two tests and two assignments/one Skill Development Activity added will be CIE for 60 marks, marks scored will be proportionally scaled down to **30 marks**.

**CIE for the practical component of IPCC**

- On completion of every experiment/program in the laboratory, the students shall be evaluated and marks shall be awarded on the same day. The**15 marks** are for conducting the experiment and preparation of the laboratory record, the other **05 marks shall be for the test** conducted at the end of the semester.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to 15 marks.
- The laboratory test at the end /after completion of all the experiments shall be conducted for 50 marks and scaled down to 05 marks**.**

Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **20 marks**.

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**SEE for IPCC**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (duration 03 hours)

1. The question paper will be set for 100 marks and marks scored will be scaled down proportionately to 50 marks.
2. The question paper will have ten questions. Each question is set for 20 marks.

3. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
4. The students have to answer 5 full questions, selecting one full question from each module.

**The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper shall include questions from the practical component**).

- The minimum marks to be secured in CIE to appear for SEE shall be the 15 (50% of maximum marks-30) in the theory component and 10 (50% of maximum marks -20) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included**.** The maximum of 04/05 questions to be set from the practical component of IPCC, the total marks of all questions should not be more than the 20 marks.
- SEE will be conducted for 100 marks and students shall secure 40% of the maximum marks to qualify in the SEE. Marks secured will be scaled down to 50. (Student has to secure an aggregate of 50% of maximum marks of the course(CIE+SEE)

**Suggested Learning Resources:**

**Books**

**1.** Advanced Industrial Control Technology, Peng Zhang, Elsevier, 2010.

**Course outcome (Course Skill Set)**

At the end of the course the student will be able to :

| Sl. No. | Description | Blooms Level |
|---|---|---|
| CO1 | Differentiate between different types of industrial control systems; embedded control systems, real time control systems and distributed control systems and to explain three types of industrial control engineering; process control, motion control and production automation. | BL1 |
| CO2 | Explain the need of sensors and actuators used in industrial control systems and to explain the working of transducers and valves used in industrial control systems. | BL2 |
| CO3 | Explain the use of multi-core microprocessors in industrial control systems and to describe programmable peripheral I/O ports, programmable interrupt controllers, programmable timers, and CMOS and DMA controllers, the application specific integrated circuits used in industrial control systems | BL2 |

**Semester- 1**

| Analysis of Linear Systems | | | |
|---|---|---|---|
| Course Code | **22EMS13** | CIE Marks | 50 |
| Teaching Hours/Week (L:P:SDA) | 02:00:02 | SEE Marks | 50 |
| Total Hours of Pedagogy | 40 hours Theory | Total Marks | 100 |
| Credits | 04 | Exam Hours | 03 |

**Course Learning objectives:**

- To model Continuous and Discrete time system in state space
- To solve the continuous and discrete time system state space models.
- To assess the controllability and observability of state space models in the continuous and discrete time domains.
- Understand the concepts of state feedback techniques

**Module-1**

**State space Representation of Continuous Time Systems:** Introduction, concepts of state, consistency conditions, State space representation using physical variables, phase variables, canonical variables. Eigen values, Eigen vectors, state equations for dynamic systems, Non-uniqueness of state model, state diagrams- state diagrams for continuous time state models

| | |
|---|---|
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

**Module-2**

**State Space Representation of Discrete Time Systems**: Digital control system, quantizing and quantization error, Data acquisition and conversion, Impulse sampling and data hold, pulse transfer function, State space representation of discrete time systems, State diagrams - state diagrams for discrete time state models

| | |
|---|---|
| **Teaching-Learning Process** | .<br>Chalk and talk, power point presentation and video lecture. |

**Module-3**

**Solution of State Equations**: Introduction, Existence and Uniqueness of solution to continuous time state equations, Solution of Linear time invariant continuous time state equations – Evaluation of matrix exponential, series evaluation, Evaluation using symmetry transformation, Evaluation using Cayley- Hamilton technique, Evaluation using Inverse Laplace transformation. Solution of Discrete time state equations – Z transform approach, Pulse transfer function matrix, Discretization of continuous time state space equations

| | |
|---|---|
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

**Module-4**

**Controllability and Observability of Systems**: Introduction, General Concept of Controllability, General Concept of Observability, Controllability Tests For Continuous Time Systems – Time Invariant Case, Observability Tests For Continuous Time Systems – Time Invariant Case, Controllability and Observability of Discrete Time Systems – Time Invariant Case Controllability and Observability of State Model in Jordan Canonical Form. Loss of Controllability and Observability due to Sampling

| | |
|---|---|
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

**Module-5**

Model Control: Introduction, Controllable and Observable Companion Forms – Single Input /Single Output Systems, Effect of State feedback on Controllability and Observability, Pole Placement by State Feedback- Single Input Systems, Stabilizability, Full Oder Observer, Reduced Order Observer, Deadbeat Observer. ■

| | |
|---|---|
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous Internal Evaluation:**

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

**CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester End Examination:**

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

**Suggested Learning Resources:**

**Books**

1. Modern Control System Theory, M Gopal, New Age International, 2012 Reprint.
2. Discrete Time Control Systems, Ogata K, PHI, 2nd Edition, 2016.

**Web links and Video Lectures (e-Resources):**

**Course outcome (Course Skill Set)**

At the end of the course the student will be able to :

| Sl. No. | Description | Blooms Level |
|---|---|---|
| CO1 | Provide a state variable models for Continuous and discrete time systems | BL1,2 |
| CO2 | Solve the State equations to provide a solution and analyze them in both continuous and discrete time domains | BL1,2,3 |
| CO3 | Assess the controllability and observability of state space models developed. | BL3 |
| CO4 | Apply the concepts of state feedback techniques in controlling the systems | BL3 |

**Semester- 1**

| VLSI Design | | | |
|---|---|---|---|
| Course Code | **22EMS14** | CIE Marks | 50 |
| Teaching Hours/Week (L:P:SDA) | 02:00:02 | SEE Marks | 50 |
| Total Hours of Pedagogy | 40 hours Theory | Total Marks | 100 |
| Credits | 03 | Exam Hours | 03 |

**Course Learning objectives:**

- To learn basic CMOS Circuits.
- To learn CMOS process technology.
- To learn techniques of chip design using programmable devices.
- To learn the concepts of designing VLSI Subsystems.

**Module-1**

**MOS Transistor Theory:** MOS Transistors, CMOS Fabrication and Layout,Long – Channel I-V Characteristics,C-V Characteristics, Non-ideal I-V Effects, DC Transfer Characteristics, Pitfalls and Fallacies.
**CMOS Processing Technology:** Introduction, CMOS Technologies, Layout Design Rules, CMOS Process Enhancements. ■

| | |
|---|---|
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

**Module-2**

**Combinational Circuit Design:** Introduction, Circuit Families, Circuit Pitfalls, More Circuit Families, Silicon-on-Insulator Circuit Design, Sub-threshold Design, Pitfalls and Fallacies, Historical Perspective. ■

| | |
|---|---|
| **Teaching-Learning Process** | .<br>Chalk and talk, power point presentation and video lecture. |

**Module-3**

**Sequential Circuit Design:** Introduction, Sequencing Static Circuits, Circuit Design of Latches and Flip-flops,Static Sequencing Element Methodology, Sequencing Dynamic Circuits, Synchronizers, Wave Pipelining, Pitfalls and Fallacies, Case study■

| | |
|---|---|
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

**Module-4**

**Single Stage Amplifiers:** Basic Concepts, Common – Source Stage, Source Follower, Common – Gate Stage, Cascode Stage, Choice of Device Models.
**Differential Amplifiers:** Single – Ended and Differential Operations, Basic Differential Pair, Common – Mode Response, Differential Pair with MOS Loads, Gilbert Cell.■

| | |
|---|---|
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

**Module-5**

**Passive and Active Current Mirrors:** Basic Current Mirrors, Cascode Current Mirrors, Active Current Mirrors. **Operational Amplifiers:** General Considerations, One – Stage Op Amps, Two – Stage Op Amps, Gain Boosting, Comparison, Common – Mode Feedback, Input Range Limitations, Slew Rate, Power Supply Rejection, Noise in Op Amps.■

| | |
|---|---|
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous Internal Evaluation:**

3. Three Unit Tests each of **20 Marks**
4. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

**CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester End Examination:**

6. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
7. The question paper will have ten full questions carrying equal marks.
8. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
9. Each full question will have a sub-question covering all the topics under a module.
10. The students will have to answer five full questions, selecting one full question from each module

**Suggested Learning Resources:**

**Books**

**1.** CMOS VLSI Design: A Circuits and Systems Perspective, Neil H. E. Weste, David Money Harris, Pearson, 4th

2. Design of Analog CMOS Integrated Circuits, Behzad Razavi, Mc Graw Hill, 31st Reprint, 2015.

**Web links and Video Lectures (e-Resources):**

**Course outcome (Course Skill Set)**

At the end of the course the student will be able to :

| Sl. No. | Description | Blooms Level |
|---|---|---|
| CO1 | Explain in detail the basic processing details and the characteristics of MOS transistors. | BL1,2 |
| CO2 | Optimize combinational circuits for lower delay, discuss alternate CMOS circuit families. | BL1,2,3 |
| CO3 | Design both static and dynamic sequential circuits. | BL3 |
| CO4 | Design and analyze CMOS power and differential amplifiers. | BL3 |
| CO5 | Design and analyze the current mirrors as both bias elements and signal processing components andCMOS Op Amps. | BL3 |

**Semester- 1**

| Embedded System | | | |
|---|---|---|---|
| Course Code | **22EMS15** | CIE Marks | 50 |
| Teaching Hours/Week (L:P:SDA) | 3:0:2 | SEE Marks | 50 |
| Total Hours of Pedagogy | 40 hours Theory | Total Marks | 100 |
| Credits | 04 | Exam Hours | 03 |

**Course Learning objectives:**

- To impart knowledge of embedded systems with suitable examples, explanation of process, classification of embedded systems.
- To explain the processor architecture, memory organization, communication with processor and interrupt services.
- To explain the program modeling concepts, inter-process communication and synchronization of processes.

**Module-1**

**Introduction to Embedded Systems:** Embedded Systems, Processor Embedded into a System, Embedded Hardware Units and Devices in a System, Embedded Software in a System, Examples of Embedded Systems, Embedded Systems – on –chip (Soc) and Use of VLSI Circuit Design Technology, Complex Systems Design and Processors, Design of Process in Embedded System, Formulation of System Design, Design Process and Design Examples, Classification of Embedded Systems, Skill required for an Embedded System Designer.

| | |
|---|---|
| **Teaching-Learning Process** | L1 – Remembering, L2 – Understanding. |

**Module-2**

**Processor Architecture and Memory Organisation:** 8051 Architecture, Real world Interfacing, Introduction to Advanced Architecture, Processor and Memory Organization, Instruction Level Parallelism, Performance Metrics, Memory – Types, Memory – Maps and Addresses, Processor Selection, Memory Selection.

| | |
|---|---|
| **Teaching-Learning Process** | L1 – Remembering, L2 – Understanding. |

**Module-3**

**Devices and Communication Buses, Interrupt Services:** IO Types and Examples, Serial Communication Devices, Parallel Device Ports, Sophisticated Interfacing Features in Device Ports, Wireless Devices, Timer and Counting Devices, Watchdog Timer, Real Time Clock, Networked Embedded Systems, Serial Bus Device Protocols – Parallel Communication Network Using ISA,PCI, PCI –X and Advanced Protocols.

**Device Drivers and Interrupts Service Mechanisms:** Programmed – I/O Busy – wait Approach without Interrupt Service Mechanism, ISR Concept, Interrupt Sources, Interrupt Servicing Mechanism, Direct Memory Access.

| | |
|---|---|
| **Teaching-Learning Process** | L1 – Remembering, L2 – Understanding |

**Module-4**

**Interprocess Communication and Synchronization of Processes, Threads and Tasks:** Multiple Processes in an Application, Multiple Threads in an Application, Tasks, Task Status, Task and Data, Clear – cut Distention Between Functions, ISRS and Tasks by their Characteristics, Concept of Semaphores, Shared Data, Interprocess Communication, Signal Function, Semaphore Functions, Message Queue Functions, Mailbox Functions, Pipe Functions, Socket Functions, RPC Functions.

| | |
|---|---|
| **Teaching-Learning Process** | L1 – Remembering, L2 – Understanding. |

**Module-5**

**Real - Time Operating Systems:** OS Services, Process Management, Timer Functions, Event Functions, Memory management, Device, File and IO Subsystems Management , Interrupt Routines in RTOS Environment and Handling of Interrupt Source Calls, Real – time Operating Systems, Basic Design Using an RTOS, Rtos Task Scheduling Models, Interrupt Latency and Response of the task as performance Metrics, OS Security Issues.

| | |
|---|---|
| **Teaching-Learning Process** | L1 – Remembering, L2 – Understanding |

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous Internal Evaluation:**

5. Three Unit Tests each of **20 Marks**
6. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

**CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester End Examination:**

11. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
12. The question paper will have ten full questions carrying equal marks.
13. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
14. Each full question will have a sub-question covering all the topics under a module.
15. The students will have to answer five full questions, selecting one full question from each module

**Suggested Learning Resources:**

**Books**

1. Embedded Systems: Architecture, Programming and Design, Raj Kamal, Mc Graw Hill, 2nd Edition, 2014.

**Web links and Video Lectures (e-Resources):**

**Skill Development Activities Suggested**

- Hardware Interfacing
- Embedded C Programming

**Course outcome (Course Skill Set)**

At the end of the course the student will be able to :

| Sl. No. | Description | Blooms Level |
|---|---|---|
| CO1 | Describe embedded system, recognize the classification of embedded systems and design process in embedded system. | L1 & L2 |
| CO2 | Describe processor architecture and memory organization. | L1 & L2 |
| CO3 | Communicate with processor using serial and parallel devices with the processor and explain interrupt services mechanism. | L1 & L2 |
| CO4 | Explain basics of interrupts and different architectures like Round Robin. Describe the Real – Time Operating System architecture. | L1 & L2 |
| CO5 | Explain semaphores. Clarify about. message queues, mailboxes, and pipes. Describe the process of effective memory management. | L1 & L2 |

| MICROELECTRONICS AND CONTROL LABORATORY - 1 | | | |
|---|---|---|---|
| Course Code | **22EMSL17** | CIE Marks | 50 |
| Teaching Hours/Week (L:T:P: S) | 00:01:02:00 | SEE Marks | 50 |
| Credits | 02 | Exam Hours | 100 |

**Course objectives:**

- . Understand mathematical models of electrical and mechanical systems.
- Analysis of control system stability using digital simulation.
- Demonstrate the time domain and frequency domain analysis for linear time invariant systems.
- Apply programmable logic controllers to demonstrate industrial controls in the laboratory

| Sl.NO | Experiments |
|---|---|
| 1 | Simulation of a typical second order system. |
| 2 | Study of system stability by using root locus, Bode plot and Nyquist plot. |
| 3 | Performance characteristics of P, PI, PID controller. |
| 4 | Study of MALAB FIS Tool box. |
| 5 | Verification of Sampling Theorem. |
| 6 | Design and verification of FIR filter. |
| 7 | State estimation using Pole placement method. |
| | **Demonstration Experiments ( For CIE ) if any** |
| 8 | DC and AC Servo motor characteristic s. |
| 9 | Frequency response of lag, lead and lag-lead network. |

**Course outcomes (Course Skill Set):**

At the end of the course the student will be able to:

- At the end of the course the student will be able to:
- Use MATLAB/Scilab to simulate a second order system to study the output and perform state estimation by pole placement method.
- Analyze the stability of the systems in time and frequency domains
- Design and verify the frequency response of different compensators.
- Evaluate the performance of different controllers in enhancing the system performance
- Verify the sampling theorem, design and analyze the FIR filter
- Gain knowledge on FIS toolbox for control system applications.

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 40% of maximum marks in the semester-end examination(SEE). In total of CIE and SEE student has to secure 50% maximum marks of the course.

**Continuous Internal Evaluation (CIE):**

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the $8^{th}$ week of the semester and the second test shall be conducted after the $14^{th}$ week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of **scaled-down** marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

**Semester End Evaluation (SEE):**

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University.

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 10% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours

**Semester- 2**

| INDUSTRIAL CONTROL TECHNOLOGY - 2 | | | |
|---|---|---|---|
| Course Code | **22EMS21** | CIE Marks | 50 |
| Teaching Hours/Week (L:P:SDA) | 02:00:02 | SEE Marks | 50 |
| Total Hours of Pedagogy | 40 hours Theory | Total Marks | 100 |
| Credits | 03 | Exam Hours | 3 Hrs |

**Course Learning objectives:**

- To learn the fundamental of control of most process variables and how these measuredquantities are transformed and transmitted.
- To learn the concepts of process control, including principles of industrial practices and computer control.
- To apply these concepts to the control system for typical chemical processes.
- To gain knowledge and actions of various types of control system, including analog and digital types, online and real time.

**Module-1**

**Industrial Intelligent Controllers:** PLC (Programmable Logic Control) Controllers, CNC (Computer Numerical Control) Controllers, FLC (Fuzzy Logic Control) Controllers. ■

| | |
|---|---|
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

**Module-2**

**Industrial Process Controllers:** PID (Proportional-Integral-Derivative) Controllers,BPC (Batch Process Control) Controllers,SMC (Servo Motion Control) Controllers.
**Industrial Computers:** Introduction, Industrial Computer Classes and Configurations,Industrial Computer Peripherals

| | |
|---|---|
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

**Module-3**

**Industrial Control Networks:** Controller Area Network (CAN), Supervisory Control and Data Acquisition (SCADA) Network, Industrial Ethernet Network, Industrial Enterprise Networks.■

| | |
|---|---|
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

**Module-4**

**Networking Devices:** Hubs and Switches, Network Routers, Bridges, Gateways and Repeaters.■

| | |
|---|---|
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

**Module-5**

**Human–machine interfaces:** Human–Machine Interactions, User–Machine Interfaces, Industrial Application Examples.
**Data Transmission Interfaces:** Data Transmission Basics, Data Transmission I/O Devices,Data TransmissionControl Devices. ■

| | |
|---|---|
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous Internal Evaluation:**

7. Three Unit Tests each of **20 Marks**
8. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

**CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester End Examination:**

16. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
17. The question paper will have ten full questions carrying equal marks.
18. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
19. Each full question will have a sub-question covering all the topics under a module.
20. The students will have to answer five full questions, selecting one full question from each module

**Suggested Learning Resources:**

**Books**

1. Advanced Industrial Control Technology, Peng Zhang, Elsevier, 2010.

**Course outcome (Course Skill Set)**

At the end of the course the student will be able to :

| Sl. No. | Description | Blooms Level |
|---|---|---|
| CO1 | Explain the industrial intelligent controllers necessary for both industrial production control andindustrial process control, PID controllers, batch process controllers and servo motion controllers. | L1, L2 |
| CO2 | Discuss the layer model, architectures, components, functions. | L1, L2 & L3 |
| CO3 | Describe interfaces existing in industrial control systems namely human machine interfaces and data transmission interfaces. | L1, L2 & L3 |
| CO4 | Discuss applications of several primary industrial control networks: CAN, SCADA, Ethernet, DeviceNet, LAN, and other enterprise networks. | L1, L2 & L3 |
| CO5 | Explain networking devices, including networking hubs, switches, routers, bridges, gateways, repeaters and key techniques used in these networking devices. | L1, L2 |

**Semester- 2**

| HIGH Speed VLSI Design (IPCC) | | | |
|---|---|---|---|
| Course Code | **22EMS22** | CIE Marks | 50 |
| Teaching Hours/Week (L:P:SDA) | 03:02:00 | SEE Marks | 50 |
| Total Hours of Pedagogy | 40 hours Theory + 10-12 Lab slots | Total Marks | 100 |
| Credits | 04 | Exam Hours | 03 |

**Course objectives:**

- To discuss various issues, that include parasitic capacitances and inductances, propagation delays, crosstalk, and electro migration-induced failure associated with VLSI interconnections used for high-speed applications.
- To learn about Green's Function Method: Using Method of Images, Green's Function Method Lumped Capacitance Approximation, Coupled Multiconductor MIS Microstrip line Model of Single-Level Interconnections.

**MODULE-1**

**Preliminary Concepts:** Interconnections for VLSI Applications, Copper Interconnections, Method of Images, Method of Moments, Even- and Odd-Mode Capacitances, Transmission Line Equations, Miller's Theorem, Inverse Laplace Transformation, Resistive Interconnection as Ladder Network, Propagation Modes in Micro strip Interconnection, Slow-Wave Mode Propagation, Propagation Delays.

**Parasitic Resistances, Capacitances, and Inductances:** Parasitic Resistances: General Considerations, Parasitic Capacitances: General Considerations, Parasitic Inductances: General Considerations, Approximate Formulas for Capacitances.

| | |
|---|---|
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

**MODULE-2**

**Parasitic Resistances, Capacitances, and Inductances (continued):** Green's Function Method: Using Method of Images, Green's Function Method: Fourier Integral Approach, Network Analog Method, Simplified Formulas for Interconnection Capacitances and Inductances on Silicon and GaAs Substrates, Inductance Extraction Using FastHenry, Copper Interconnections: Resistance Modeling, Electrode Capacitances in GaAsMESFET:Application of Program IPCSGV.

| | |
|---|---|
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

**MODULE-3**

**Interconnection Delays:** Metal–Insulator–Semiconductor Microstripline Model of an Interconnection, Transmission Line Analysis of Single-Level Interconnections, Transmission Line Analysis of Parallel Multilevel Interconnections, Analysis of Crossing Interconnections, Parallel Interconnections Modelled as Multiple Coupled Microstrips.

| | |
|---|---|
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

**MODULE-4**

**Interconnection Delays (continued):** Modelling of Lossy Parallel and Crossing Interconnections as Coupled Lumped Distributed Systems, Very High Frequency Losses in Microstrip Interconnection, Compact Expressions for Interconnection Delays, Interconnection Delays in Multilayer Integrated Circuits, Active Interconnections.

**Crosstalk Analysis:** Lumped-Capacitance Approximation, Coupled Multiconductor MIS Microstrip line Model of Single-Level Interconnections, Frequency-Domain Modal Analysis of Single-Level Interconnections.

| | |
|---|---|
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

**MODULE 5**

**Crosstalk Analysis:** Transmission Line Analysis of Parallel Multilevel Interconnections,Analysis of Crossing Interconnections,Compact Expressions for Crosstalk Analysis,Multiconductor Buses in GaAs High-Speed Logic Circuits.

**Electromigration-Induced Failure Analysis:**Electromigration in VLSI Interconnection Metallizations: Overview.

| | |
|---|---|
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

**PRACTICAL COMPONENT OF IPCC***(May cover all / major modules)*

| Sl.NO | Experiments |
|---|---|
| 1 | Design of CMOS Inverter |
| 2 | Design of AND gate |
| 3 | Design of OR gate |
| 4 | Design of NAND gate |
| 5 | Design of NOR gate |
| 6 | Design of XOR gate |
| 7 | Design of X-NOR gate |
| 8 | Design of transmission gate |
| 9 | Design of Half-Adder, |
| 10 | Design of Full Adder, |

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together

**CIE for the theory component of IPCC**

4. Two Tests each of **20 Marks**
5. Two assignments each of **10 Marks/One Skill Development Activity of 20 marks**
6. Total Marks of two tests and two assignments/one Skill Development Activity added will be CIE for 60 marks, marks scored will be proportionally scaled down to **30 marks**.

**CIE for the practical component of IPCC**

- On completion of every experiment/program in the laboratory, the students shall be evaluated and marks shall be awarded on the same day. The**15 marks** are for conducting the experiment and preparation of the laboratory record, the other **05 marks shall be for the test** conducted at the end of the semester.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to 15 marks.
- The laboratory test at the end /after completion of all the experimentsshall be conducted for 50 marks and scaled down to 05 marks**.**

Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **20 marks**.

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**SEE for IPCC**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (duration 03 hours)

5. The question paper will be set for 100 marks and marks scored will be scaled down proportionately to 50 marks.
6. The question paper will have ten questions. Each question is set for 20 marks.
7. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
8. The students have to answer 5 full questions, selecting one full question from each module.

**The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper shall include questions from the practical component**).

- The minimum marks to be secured in CIE to appear for SEE shall be the 15 (50% of maximum marks-30) in the theory component and 10 (50% of maximum marks -20) in the practical component. The laboratory component

of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included**.** The maximum of 04/05 questions to be set from the practical component of IPCC, the total marks of all questions should not be more than the 20 marks.

- SEE will be conducted for 100 marks and students shall secure 40% of the maximum marks to qualify in the SEE. Marks secured will be scaled down to 50. (Student has to secure an aggregate of 50% of maximum marks of the course(CIE+SEE)

**Suggested Learning Resources:**

**Books**

1. High-Speed VLSI Interconnections, Ashok K. Goel, Wiley, 2007.

**Course outcome (Course Skill Set)**

**At the end of the course the student will be able to :**

| Sl. No. | Description | Blooms Level |
|---|---|---|
| CO1 | Discuss basic techniques and advanced concepts regarding wave propagation in an interconnection, multilevel, multilayer, and multipath interconnections employed in VLSI applications | BL1,2 |
| CO2 | Discuss copper interconnections and their fabrication techniques and to explain numerical techniques that can be used to determine the interconnection resistances, capacitances, and inductances on a high-density VLSI chip. | BL1,2 |
| CO3 | Calculate the propagation delays in the single and multilevel parallel and crossing interconnections using numerical algorithms and to explain the crosstalk effects in the single and multilevel parallel and crossing interconnections. | BL1,2 |
| CO4 | Develop a model of very high speed VLSI circuits for the crosstalk analysis | BL4 |
| CO5 | Discuss the degradation of the reliability of an interconnection due to electromigration. | BL1,2 |

**Semester- 2**

| Nonlinear Systems | | | |
|---|---|---|---|
| Course Code | **22EMS241** | CIE Marks | 50 |
| Teaching Hours/Week (L:P:SDA) | 2:0:2 | SEE Marks | 50 |
| Total Hours of Pedagogy | | Total Marks | 100 |
| Credits | 3 | Exam Hours | 03 |

**Course Learning objectives:**

- To introduce the need and concept of nonlinear system.
- To impart knowledge about different strategies adopted in the analysis of nonlinear systems.
- To familiarize with the design of different types of nonlinear controllers.

**Module-1**

**Nonlinear Systems:** Introduction to Nonlinear systems, Behavior of Nonlinear Systems- Frequency –Amplitude dependence, Jump resonance, Sub- harmonic oscillations, Frequency entrainment, Limit Cycles, Asynchronous quenching. Common Physical Non-linearities, Classification of nonlinearities, methods of analysis of nonlinear systems Definition of describing function, Linearization of nonlinear system. ■

| | |
|---|---|
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

**Module-2**

**Describing Function Method:** Introduction, assumptions and definition, evaluation of describing function for functions like x2, x3,|x|x and common nonlinearities like relay, saturation, dead zone, hysteresis, backlash and a combination of these, Analysis of nonlinear systems – Concept of enclosure, stable and unstable limit cycles, Review of polar plot and Nichols Plot, Evaluation of existence of limit cycle and calculation of magnitude and frequency of oscillation. ■

| | |
|---|---|
| **Teaching-Learning Process** | .<br>Chalk and talk, power point presentation and video lecture. |

**Module-3**

**Phase-Plane Analysis:** Introduction to phase plane and phase trajectory, Singular points –evaluation, classification and trajectories, Stability analysis of nonlinear system using phase trajectories, Limit cycles in phase portrait, Construction of phase trajectories - Analytical method, Isocline method, Delta method, and Pell's method.■

| | |
|---|---|
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

**Module-4**

**Lyapunov Stability:** Stability Definitions, Some Preliminaries, Lyapunov's Direct Method, Stability of Linear Systems, Lyapunov's Linearization Method, The Lur'e Problem, Krasovskii;s method of stability assessment, Variable gradient method of stability assessment. Stability assessment of discrete time systems.■

| | |
|---|---|
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

**Module-5**

**Stability Assessment in the Frequency Domain:**Circle criteria and its application, Popov's method**.**
**Sliding mode control:** Introduction An overview of classical sliding mode control, introductory example, Dynamics in sliding mode – Linear Systems, Nonlinear Systems, Chattering Problems, Reachability Condition, Applications of Sliding mode control.■

| | |
|---|---|
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous Internal Evaluation:**

9. Three Unit Tests each of **20 Marks**
10. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

**CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester End Examination:**

21. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
22. The question paper will have ten full questions carrying equal marks.
23. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
24. Each full question will have a sub-question covering all the topics under a module.
25. The students will have to answer five full questions, selecting one full question from each module

**Suggested Learning Resources:**

**Books**


1. 1. Advanced Control Theory, A.NagoorKani, RBA Publications, 2nd Edition, 2009.
2. Nonlinear Systems Analysis, M. Vidyasagar, PHI, 2ndEdition. 2002.
3. Non Linear Systems, H. K. Khalil, Pearson, 2015.
4. Sliding Mode Control in Engineering, Wilfrid Perruquetti & Jean Pierre Barbot, Marcel Dekker, 2002.


**Course outcome (Course Skill Set)**

At the end of the course the student will be able to :

| Sl. No. | Description | Blooms Level |
|---|---|---|
| CO1 | Identify the nonlinearity present in a system and explain the behavior of nonlinear system. | BL1,2 |
| CO2 | Evaluate the describing function for the nonlinearity present in the system and assess the performance ofthe system using it. | BL1,2 |
| CO3 | Analyze the nonlinear system using the Phase Plane Analysis. | BL3 |
| CO4 | Define the stability of a system and assess the stability using Lyapunov Stability method. | BL2 |
| CO5 | Assess the stability of nonlinear system using circle criterion and Popov's stability criterion and applysliding mode control to the linear and nonlinear systems. | BL2 |

**Semester- 2**

| PROCESS CONTROL AND INSTRUMENTATION | | | |
|---|---|---|---|
| Course Code | **22EMS242** | CIE Marks | 50 |
| Teaching Hours/Week (L:P:SDA) | 2:0:2 | SEE Marks | 50 |
| Total Hours of Pedagogy | | Total Marks | 100 |
| Credits | 3 | Exam Hours | 3 |

**Course Learning objectives:**

- Understand the basic principles & importance of process control in industrial process plants;
- Understand the importance and application of good instrumentation for the efficient design of process control loops for process engineering plants;
- Specify the required instrumentation and final elements to ensure that well-tuned control is achieved;
- Understand the use of block diagrams & the mathematical basis for the design of control systems;
- Understand the PLC Documentation and PID controller drawings;
- Understand the experimental implementation of advanced process control schemes and the methods for process monitoring and diagnosis;

| **Module-1** | |
|---|---|
| **Introduction to Process Control:** Introduction, Process Control, Definition of the Elements in a Control Loop, Instrumentation and Sensors, Control System Evaluation, Analog and Digital Data, Process Facility Considerations. **Units and Standards:** Introduction, Basic Units, Units Derived from Base Units, Standard Prefixes, Standards. **Basic Electrical Components:** Introduction, Circuits with R, L, and C, RC Filters, Bridge Circuits. **Analog Electronics:** Introduction, Analog Circuits, Types of Amplifiers, Amplifier Applications. **10 Hours** | |
| **Teaching-Learning Process** | Chalk and Board, Power Point Presentation. |
| **Module-2** | |
| **Digital Electronics:** Introduction, Digital Building Blocks, Converters, Data Acquisition Devices, Basic Processor. **Microelectromechanical Devices and Smart Sensors:** Introduction, Basic Sensors, Piezoelectric Devices, Microelectromechanical Devices, Smart Sensors Introduction. **Pressure:** Introduction, Pressure Measurement, Measuring Instruments, Application Considerations. **Level:** Introduction, Level Measurement, Application Considerations. **10 Hours** | |
| **Teaching-Learning Process** | Chalk and Board, Power Point Presentation. |
| **Module-3** | |
| **Flow:** Introduction, Fluid Flow, Flow Measuring Instruments, Application Considerations. **Temperature and Heat:** Introduction, Temperature and Heat, Temperature Measuring Devices, Application Considerations. **Position, Force, and Light:** Introduction, Position and Motion Sensing, Force, Torque, and Load Cells, Light. **10 Hours** | |
| **Teaching-Learning Process** | Chalk and Board, Power Point Presentation. |
| **Module-4** | |
| **Humidity and Other Sensors:** Humidity, Density and Specific Gravity, Viscosity, Sound, pH Measurements, Smoke and Chemical Sensors. **Regulators, Valves, and Motors:** Introduction, Pressure Controllers, Flow Control Valves, Power Control, Motors, Application Considerations. **Programmable Logic Controllers:** Introduction, Programmable Controller System, Controller Operation, Input/output Modules, Ladder Diagrams. **10 Hours** | |
| **Teaching-Learning Process** | Chalk and Board, Power Point Presentation. |
| **Module-5** | |
| **Signal Conditioning and Transmission:** Introduction, General Sensor Conditioning, Conditioning Considerations for Specific Types of Devices, Digital Conditioning, Pneumatic Transmission, Analog Transmission, Digital Transmission, Wireless Transmission. **Process Control:** Introduction, Sequential Control, Discontinuous Control, Continuous Control, Process Control Tuning, Implementation of Control Loops. **Documentation and P&ID:** Introduction, Alarm and Trip Systems, PLC Documentation, Pipe and Instrumentation Symbols, P&ID Drawings. **10 Hours** | |
| **Teaching-Learning Process** | Chalk and Board, Power Point Presentation. |

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous Internal Evaluation:**

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

**CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester End Examination:**

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

**Suggested Learning Resources:**

**Books**

1. Introduction to Instrumentation, Sensors, and Process Control, William C. Dunn, Artech House, 2006.

**Skill Development Activities Suggested**

- Workshop on Process Control and Instrumentation that introduces control in process industries, explains why control is important, different ways in which precise control is ensured, different measuring instruments, sensors and PLC.
- Visit to process industries to illustrate different types of instrumentation used to perform measuring tasks for temperature, pressure, flow and level, etc.

**Course outcome (Course Skill Set)**

At the end of the course the student will be able to :

| Sl. No. | Description | Blooms Level |
|---|---|---|
| CO1 | Explain the concepts of process control, the elements in the building blocks, the units for physical measurements, use of basic electrical and analog electronic circuits. | L2 |
| CO2 | Explain the use of digital concepts to their applications, measurement of pressure and level in process control. | L2 |
| CO3 | Explain the use of instruments and sensors for measurement of flow of fluids, temperature and heat, position, force and light. | L3 |
| CO4 | Explain use of Humidity measuring devices, regulators, valves, motors and the use of PLC for sequential logic control and continuous control. | L3 |
| CO5 | Discuss various methods of analog and digital signal conditioning, process control, the terminology used, and the various methods of implementation of the controller functions and the documentation for alarm and trip systems. | L3 |

**Semester- 2**

| Optimal Control Theory | | | |
|---|---|---|---|
| Course Code | **22EMS243** | CIE Marks | 50 |
| Teaching Hours/Week (L:P:SDA) | 2:0:2 | SEE Marks | 50 |
| Total Hours of Pedagogy | | Total Marks | 100 |
| Credits | 3 | Exam Hours | 03 |

**Course Learning objectives:**

- To discuss modeling of systems. To discuss state and control constraints.
- To discuss the performance measures used in control problems.
- To explain determination of control function that minimizes the performance measure.
- To explain development of a dynamic program applicable to a class of control problems.
- To explain some basic ideas of the calculus of variations and to relate the analogy of results in calculus and the results of calculus of variations
- To explain application of variational method to optimal control problems.
- To explain Pontryagin's minimum principle

| **Module-1** | |
|---|---|
| **Introduction:** Problem Formulation, State Variable Representation of a System. **The Performance Measure:** Performance Measure for Optimal Control Problems, Selecting a Performance Measure, Selection of a Performance Measure. **Dynamic Programming:** The optimal Control Law, the Principle of Optimality, Application of the principle of Optimality to Decision- Making, Dynamic Programming applied to a Routing Problem, An Optimal Control System, Interpolation. 10 Hours | |
| **Teaching-Learning Process** | Chalk and Board, Power Point Presentation. |
| **Module-2** | |
| **Dynamic Programming (continued):** A Recurrence Relation of Dynamic Programming, Computational Procedure for Solving Control Problems, Characteristics of Dynamic Programming Solution, Analytical Results – Linear Regulator Problems, The Hamilton- Jacobi-Bellman Equation, Continuous Linear Regulator Problem, The Hamilton- Jacobi-Bellman Equation – Some Observations. **The Calculus Of Variations:** Fundamental Concepts, Functions of a Single Function. 10 Hours | |
| **Teaching-Learning Process** | . Chalk and Board, Power Point Presentation. |
| **Module-3** | |
| **The Calculus of Variations (continued):** Functionals involving several independent Functions, Piecewise – smooth Externals, Constrained Extrema. **The Variational Approach to Optimal Control Problems:** Necessary Conditions for Optimal Control. 10 Hours | |
| **Teaching-Learning Process** | Chalk and Board, Power Point Presentation. |
| **Module-4** | |
| **The Variational Approach to Optimal Control Problems (continued):** Linear regulator problem, Pontryagin's Minimum Principle and state Inequality Constraints, Minimum –Time problems. 10 Hours | |
| **Teaching-Learning Process** | Chalk and Board, Power Point Presentation. |
| **Module-5** | |
| **The Variational Approach to Optimal Control Problems (continued):** Minimum Control-Effort Problems, Singular Intervals in Optimal Control Problems. 10 Hours | |
| **Teaching-Learning Process** | Chalk and Board, Power Point Presentation. |

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous Internal Evaluation:**

3. Three Unit Tests each of **20 Marks**
4. Two assignments each of **20 Marks**or**oneSkill Development Activity of 40 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

**CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester End Examination:**

6. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
7. The question paper will have ten full questions carrying equal marks.
8. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
9. Each full question will have a sub-question covering all the topics under a module.
10. The students will have to answer five full questions, selecting one full question from each module

**Suggested Learning Resources:**

**Books**

1. Optimal Control Theory An Introduction, Donal E Kirk, Dover Publication, 2004.

**Course outcome (Course Skill Set)**

At the end of the course the student will be able to :

| Sl. No. | Description | Blooms Level |
|---|---|---|
| CO1 | Develop mathematical models for systems using state variables. | 1,2,3 |
| CO2 | Formulate an optimal control problem with constraints and discuss performance, performance measures used in control problems. | 1,2,3,6 |
| CO3 | Evaluate control function that minimizes the performance measure and explain dynamic programming applicable to a class of control problems. | 1,2,3 |
| CO4 | Explain basic ideas of the calculus of variations and explain application of variational method to optimal control problems. | 1,2,3 |
| CO5 | Construct Pontryagin's minimum principle used for optimal control systems. | 1,2,3 |

**Semester- 2**

| Neural and Fuzzy Logic Control of Drives | | | |
|---|---|---|---|
| Course Code | **22EMS244** | CIE Marks | 50 |
| Teaching Hours/Week (L:P:SDA) | 2:0:2 | SEE Marks | 50 |
| Total Hours of Pedagogy | | Total Marks | 100 |
| Credits | 3 | Exam Hours | 03 |

**Course Learning objectives:**

- This course introduces the basics of Neural Networks and essentials of Artificial Neural Networks with Single Layer and Multilayer Feed Forward Networks.
- It deals with Associate Memories and introduces Fuzzy sets and Fuzzy Logic system components.
- The Neural Network and Fuzzy Network system application to Electrical Engineering is also presented. This subject is very important and useful for doing Project Work.
- The main objective of this course is to provide the student with the basic understanding of neural networks and fuzzy logic fundamentals.

**Module-1**

**Modern control systems design using CAD techniques:** Introduction, Control systems for AC drives, Electronic design automation (EDA), Application specific integrated circuit (ASIC) basics, Field programmable gate arrays (FPGAs), ASICs for power systems and drives, Electric motors.
**Electric motors:** Motors, Pulse width modulation, The space vector in electrical systems, Induction motor control. ■

| | |
|---|---|
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

**Module-2**

**Elements of neural control:** Neurone types, Artificial neural networks architectures, Training algorithms, Control applications of ANNs, Neural network implementation.
**Neural FPGA implementation**: Neural networks design and implementation strategy, Universal programs FFANN, hardware implementation, Hardware implementation complexity analysis. ■

| | |
|---|---|
| **Teaching-Learning Process** | .<br>Chalk and talk, power point presentation and video lecture. |

**Module-3**

**Fuzzy logic fundamentals:** Introduction, Fuzzy sets and fuzzy logic, Types of membership functions, Linguistic variables, Fuzzy logic operators, Fuzzy control systems, Fuzzy logic in power and control, Applications.
**VHDL fundamentals**: Introduction, VHDL design units, Libraries, visibility and state system in VHDL, Sequential statements, Concurrent statements, Functions and procedures, Advanced features in VHDL. ■

| | |
|---|---|
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

**Module-4**

**Neural current and speed control of induction motors:** The induction motor equivalent circuit, The currentcontrol algorithm, The new sensorless motor control Strategy. .■

| | |
|---|---|
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

**Module-5**

**Neural current and speed control of induction motors (continued):** Induction motor controller VHDLDesign, FPGA controller experimental results.■

| | |
|---|---|
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous Internal Evaluation:**

5. Three Unit Tests each of **20 Marks**
6. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

**CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester End Examination:**

11. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
12. The question paper will have ten full questions carrying equal marks.
13. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
14. Each full question will have a sub-question covering all the topics under a module.
15. The students will have to answer five full questions, selecting one full question from each module

**Suggested Learning Resources:**

**Books**

**1.** Neural and Fuzzy Logic Control of Drives and Power Systems, M.N. Cirstea, et al, Newnes, 2002.

**Course outcome (Course Skill Set)**

At the end of the course the student will be able to :

| Sl. No. | Description | Blooms Level |
|---|---|---|
| CO1 | Discuss control strategies for electric drives/power systems. | BL1,2 |
| CO2 | Understand the complex features of control strategies, EDA. | BL1,2 |
| CO3 | Understand the features of neural networks, fuzzy logic, electricmachines and drives, power systems and VHDL. | BL1,2 |

**Semester- 2**

| CAD Tools for VLSI Design | | | |
|---|---|---|---|
| Course Code | **22EMS245** | CIE Marks | 50 |
| Teaching Hours/Week (L:P:SDA) | 2:0:2 | SEE Marks | 50 |
| Total Hours of Pedagogy | | Total Marks | 100 |
| Credits | 3 | Exam Hours | 03 |

**Course Learning objectives:**

- To provide an introduction to the fundamentals of Computer-Aided Design tools for the modeling, design, analysis, test, and verification of digital Very Large Scale Integration (VLSI) systems. ·
- To learn Physical design of VLSI Circuits ·
- To learn the Basics of Graph Theory Algorithms ·
- To understand the concept of CAD Tools. · To Learn the Physical Design of FPGA and MCMS

**Module-1**

**VLSI Physical Design Automation:** VLSI Design Cycle, New Trends in VLSI Design Cycle, Physical Design Cycle, New Trends in Physical Design Cycle, Design Styles, System Packaging Styles.
**Design and Fabrication of VLSI Devices:** Fabrication Materials, Transistor Fundamentals, Fabrication of VLSI Circuits, Design Rules, Layout of Basic Devices. ■

| | |
|---|---|
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

**Module-2**

**Data Structures and Basic Algorithms:** Basic Terminology, Complexity Issues and NP-hardness, Basic Algorithms, Basic Data Structures, Graph Algorithms for Physical design.■

| | |
|---|---|
| **Teaching-Learning Process** | .<br>Chalk and talk, power point presentation and video lecture. |

**Module-3**

**Partitioning:** Problem Formulation, Classification of Partitioning Algorithms, Group Migration Algorithms, Simulated Annealing and Evolution, Other Partitioning Algorithms, Performance Driven Partitioning.
**Floor planning and Pin Assignment:** Floor planning, Chip planning, Pin Assignment, Integrated Approach. ■

| | |
|---|---|
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

**Module-4**

**Placement:** Problem Formulation, Classification of Placement Algorithms, Simulation Based Placement Algorithms, Partitioning Based Placement Algorithms, Other Placement Algorithms, Performance Driven Placement.
**Global Routing:** Problem Formulation, Classification of Global Routing Algorithms, Maze Routing Algorithms, Line-Probe Algorithms, Shortest Path Based Algorithms, Steiner Tree based Algorithms, Integer Programming Based Approach, Performance Driven Routing. ■

| | |
|---|---|
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

**Module-5**

**Detailed Routing:** Problem Formulation, Classification of Routing Algorithms, Single-Layer Routing Algorithms,Two-Layer Channel Routing Algorithms, Three-Layer Channel Routing Algorithms, Multi-Layer Channel Routing Algorithms, Switchbox Routing Algorithms. ■

| | |
|---|---|
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous Internal Evaluation:**

7. Three Unit Tests each of **20 Marks**
8. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

**CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester End Examination:**

16. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
17. The question paper will have ten full questions carrying equal marks.
18. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
19. Each full question will have a sub-question covering all the topics under a module.
20. The students will have to answer five full questions, selecting one full question from each module

**Suggested Learning Resources:**

**Books**

**1.** Algorithms for VLSI Physical Design Automation, Naveed A. Sherwani, Kluwer Academic Publishers, 3rd Edition, 2002.

**Course outcome (Course Skill Set)**

At the end of the course the student will be able to :

| Sl. No. | Description | Blooms Level |
|---|---|---|
| CO1 | Discuss design automation field including the VLSI design cycle, physical design cycle, design styles, packaging styles and the fabrication process for VLSI devices, process innovations, design rules and costs involved in fabrication process. | BL1,2 |
| CO2 | Explain data structures for layout and algorithms involved in the physical design, and graphs used to model problems in VLSI design and algorithms for the graphs. | BL1,2 |
| CO3 | Explain partitioning, partitioning algorithms, their classification and the factors that must be considered in partitioning the VLSI circuits and discuss algorithms for floorplanning and pin assignment and techniques for placement. | BL1,2 |
| CO4 | Discuss global routing, routing algorithms and routing of multi-terminal nets writing. | BL1,2 |
| CO5 | Discuss design automation field including the VLSI design cycle, physical design cycle, design styles, packaging styles and the fabrication process for VLSI devices, process | BL1,2 |

**Semester- 2**

| Reset Control Systems | | | |
|---|---|---|---|
| Course Code | **22EMS251** | CIE Marks | 50 |
| Teaching Hours/Week (L:P:SDA) | 2:0:2 | SEE Marks | 50 |
| Total Hours of Pedagogy | | Total Marks | 100 |
| Credits | 3 | Exam Hours | 03 |

**Course Learning objectives:**

- To provide an introduction to the fundamentals of Reset control, concepts of RCSs, Fundamental theory of traditional reset. ·
- To learn Sinusoid input response, Describing function, Application to HDD systems ·
- To learn the Quadratic stability, Affine quadratic stability, Robust stability of RCS with time-delay ·
- To understand the concept of Stability analysis, A heuristic design method, Application to track-seeking control of HDD systems

| **Module-1** | |
|---|---|
| **Introduction:** Motivation of reset control, Basic concepts of RCSs, Fundamental theory of traditional reset design. ■ | |
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

| **Module-2** | |
|---|---|
| **Describing function analysis of reset systems:** Sinusoid input response, Describing function, Application to HDD systems.■ | |
| **Teaching-Learning Process** | . Chalk and talk, power point presentation and video lecture. |

| **Module-3** | |
|---|---|
| **Stability of reset control systems:** Preliminaries, Quadratic stability, Stability of RCSs with time-delay, Resettimes-dependent stability, Passivity of RCSs.■ | |
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

| **Module-4** | |
|---|---|
| **Robust stability of reset control systems:** Definitions and assumptions, Quadratic stability, Affine quadratic stability, Robust stability of RCS with time-delay, Examples. **RCSs with discrete-time reset conditions:** Preliminaries and problem setting, Stability analysis, A heuristicdesign method, Application to track-seeking control of HDD systems. ■ | |
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

| **Module-5** | |
|---|---|
| **Reset control systems with fixed reset instants:** Stability analysis, Moving horizon optimization, Optimal resetlaw design, Application to HDD systems, Application to PZT-positioning stage. **Reset control systems with conic jump sets:** Basic idea, L 2 -gain analysis. ■ | |
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous Internal Evaluation:**

9. Three Unit Tests each of **20 Marks**
10. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

**CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester End Examination:**

21. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
22. The question paper will have ten full questions carrying equal marks.
23. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
24. Each full question will have a sub-question covering all the topics under a module.
25. The students will have to answer five full questions, selecting one full question from each module

**Suggested Learning Resources:**

**Books**

**1.** Analysis and Design of Reset Control Systems, YuqianGuo et al, IET, 2015.

**Course outcome (Course Skill Set)**

At the end of the course the student will be able to :

| Sl. No. | Description | Blooms Level |
|---|---|---|
| CO1 | Explain design concepts of Reset Control Systems. | BL1,2 |
| CO2 | Explain the describing function of reset systems and the effects of reset matrix on the frequency domainproperty of HDD system. | BL1,2 |
| CO3 | Perform stability study stability of RCS with fixed reset time instants both moving horizon optimizationand fixed horizon optimization | BL1,2 |
| CO4 | Discuss the application of optimal reset law design to HDD systems and PZT-positioning stage. | BL1,2 |
| CO5 | Discuss passivity and finite $L_2$ gain stability of RCSs with conic jump sets | BL1,2 |

**Semester- 2**

| Robust Control Theory | | | |
|---|---|---|---|
| Course Code | **22EMS252** | CIE Marks | 50 |
| Teaching Hours/Week (L:P:SDA) | 2:0:2 | SEE Marks | 50 |
| Total Hours of Pedagogy | | Total Marks | 100 |
| Credits | 3 | Exam Hours | 03 |

**Course Learning objectives:**

- To provide an introduction to Systems and Control, Modern Control Theory, Stability, Optimal Control, Optimal Control Approach, Kharitonov Approach, H∞ and H 2 Control. ·
- To learn Sinusoid input response, Describing function, Application to HDD systems ·
- To learn the Quadratic stability, Affine quadratic stability, Robust stability of RCS with time-delay ·
- To understand the concept of Stability analysis, A heuristic design method, Application to track-seeking control of HDD systems.

**Module-1**

**Introduction:** Systems and Control, Modern Control Theory, Stability, Optimal Control, Optimal ControlApproach, Kharitonov Approach, H∞ and H 2 Control, Applications.
**Optimal Control and Optimal Observers:** Optimal Control Problem, Principle of Optimality, Hamilton–Jacobi–Bellman Equation, Linear Quadratic Regulator Problem, Kalman Filter. ■

| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |
|---|---|

**Module-2**

**Robust Control of Linear Systems:** Introduction, Matched Uncertainty, Unmatched Uncertainty, Uncertainty in the Input Matrix.■

| **Teaching-Learning Process** | .<br>Chalk and talk, power point presentation and video lecture. |
|---|---|

**Module-3**

**Robust Control of Nonlinear Systems:** Introduction, Matched Uncertainty, Unmatched Uncertainty, Uncertaintyin the Input Matrix.
**Kharitonov Approach:** Introduction, Preliminary Theorems, Kharitonov Theorem, Control Design Using Kharitonov Theorem. ■

| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |
|---|---|

**Module-4**

**H∞ and H 2Control:** Introduction, Function Space, Computation of H∞ and H 2 Norms, Robust Control Problem as H∞ and H 2 Control Problem, H∞ / H 2 Control Synthesis. ■

| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |
|---|---|

**Module-5**

**Robust Active Damping:** Introduction, Problem Formulation, Robust Active Damping Design, Active Vehicle Suspension System.
**Robust Control of Manipulators:** Robot Dynamics, Problem Formulation, Robust Control Design, Simulations.
**Aircraft Hovering Control:** Modelling and Problem Formulation, Control Design for Jet-borne Hovering, Simulation.■

| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |
|---|---|

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous Internal Evaluation:**

11. Three Unit Tests each of **20 Marks**
12. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

**CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester End Examination:**

26. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
27. The question paper will have ten full questions carrying equal marks.
28. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
29. Each full question will have a sub-question covering all the topics under a module.
30. The students will have to answer five full questions, selecting one full question from each module

**Suggested Learning Resources:**

**Books**

**1.** Robust Control Design; An Optimal Control Approach, Feng Lin, Wiley, 2007.

**Course outcome (Course Skill Set)**

At the end of the course the student will be able to :

| Sl. No. | Description | Blooms Level |
|---|---|---|
| CO1 | Explain properties of linear time-invariant systems including controllability, observability, stability,stabilizability, and detectability. | BL1,2 |
| CO2 | Synthesize linear time-invariant systems by pole placement and observer design. | BL1,2,3 |
| CO3 | Discuss optimal control and the Kalman filter. | BL1,2 |
| CO4 | Design robust active damper for vibration systems, robust controller for robot manipulators. | BL1,2 |
| CO5 | Design controller for Jet-borne Hovering | BL1,2 |

**Semester- 2**

| Digital System Design with VHFL | | | |
|---|---|---|---|
| Course Code | **22EMS253** | CIE Marks | 50 |
| Teaching Hours/Week (L:P:SDA) | 2:0:2 | SEE Marks | 50 |
| Total Hours of Pedagogy | | Total Marks | 100 |
| Credits | 3 | Exam Hours | 03 |

**Course Learning objectives:**

- To discuss the design of digital systems, CMO technology, programmable logic and engineering problems of noise margins and fan-out.
- To discuss the principles of Boolean algebra, combinational logic design, timing diagrams and basic number systems.
- To explain modeling of combinational logic and synchronous sequential logic systems in VHDL.
- To explain modeling of sequential logic blocks and complex sequential systems in VHDL.
- To describes event-driven simulation and specific features of a VHDL simulator.
- To discuss synthesis tool for RTL synthesis, fault modeling and design-for-test principles.
- To explain the designing of asynchronous sequential circuits.
- To explain simulation of digital to analog and analog to digital converters using VHDL-AMS simulator.

| **Module-1** | |
|---|---|
| **Introduction**: Modern digital design, CMOS technology, Programmable logic, Electrical properties. **Combinational logic design:** Boolean algebra, Logic gates, Combinational logic design, Timing, Number codes. **Combinational logic using VHDL gate models:** Entities and architectures, Identifiers, spaces and comments, Netlists, Signal assignments, Generics, Constant and open ports, Testbenches, Configurations. | |
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

| **Module-2** | |
|---|---|
| **Combinational building blocks:** Three-state buffers, Decoders, Multiplexers, Priority encoder, Adders, Parity checker, Testbenches for combinational blocks. **Synchronous sequential design:** Synchronous sequential systems, Models of synchronous sequential systems, Algorithmic state machines, Synthesis from ASM charts, State machines in VHDL, VHDL testbenches for state machines. | |
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

| **Module-3** | |
|---|---|
| **VHDL models of sequential logic blocks:** Latches, Flip-flops, JK and T flip-flops, Registers and shift registers, Counters, Memory, Sequential multiplier, Testbenches for sequential building blocks. **Complex sequential systems:** Linked state machines, Datapath /controller partitioning, Instructions, A simple microprocessor, VHDL model of a simple microprocessor. | |
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

| **Module-4** | |
|---|---|
| **VHDL simulation:** Event-driven simulation, Simulation of VHDL models, Simulation modelling issues, File operations. **VHDL synthesis:** RTL synthesis, Constraints, Synthesis for FPGAs, Behavioural synthesis, Verifying synthesis results. **Testing digital systems:** The need for testing, Fault models, Fault-oriented test pattern generation, Fault simulation, Fault simulation in VHDL. | |
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

| **Module-5** | |
|---|---|
| **Asynchronous sequential design:** Asynchronous circuits, Analysis of asynchronous circuits, Design of asynchronous sequential circuits, Asynchronous state machines, Setup and hold times and metastability. **Interfacing with the analogue world:** Digital to analogue converters, Analogue to digital converters, VHDL-AMS, Phase-locked loops, VHDL-AMS simulators. | |
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous Internal Evaluation:**

13. Three Unit Tests each of **20 Marks**
14. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

**CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester End Examination:**

31. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
32. The question paper will have ten full questions carrying equal marks.
33. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
34. Each full question will have a sub-question covering all the topics under a module.
35. The students will have to answer five full questions, selecting one full question from each module

**Suggested Learning Resources:**

**Books**

1. Digital System Design with VHDL, Mark Zwoli´nski, Pearson, 2nd Edition, 2004.

**Course outcome (Course Skill Set)**

At the end of the course the student will be able to :

| Sl. No. | Description | Blooms Level |
|---|---|---|
| CO1 | Discuss the design digital systems using VHDL, the technology of CMO integrated circuits programmable logic, engineering problems of noise margins and fan-out. | L1 & L2 |
| CO2 | Explain the principles of Boolean algebra, combinational logic design, timing, hazards and basic number systems. | L1 & L2 |
| CO3 | Model combinational logic and synchronous sequential logic systems in VHDL. | L1 & L2 |
| CO4 | Develop models for sequential logic blocks and complex sequential systems in VHDL. | L1 & L2 |
| CO5 | Describes idea of event-driven simulation and specific features of a VHDL simulator. And discuss synthesis tool for RTL synthesis, fault modeling and design-for-test principles. | L1 & L2 |
| CO6 | Design asynchronous sequential circuits and Explain simulation of digital to analog and analog to digital converters using VHDL-AMS simulator. | L1 & L2 |

**Semester- 2**

| Internet Based Control Systems | | | |
|---|---|---|---|
| Course Code | **22EMS254** | CIE Marks | 50 |
| Teaching Hours/Week (L:P:SDA) | 2:0:2 | SEE Marks | 50 |
| Total Hours of Pedagogy | | Total Marks | 100 |
| Credits | 03 | Exam Hours | 03 |

**Course Learning objectives:**

- To provide an introduction to the Internet-based Control Systems (ICS), Challenges of NCS/ICS.
- To learn Traditional Bilateral Tele-operation Systems, Remote Control over the Internet, Canonical Internet-based Control System Structures.
- To learn the Network Infrastructure for Internet-based Control, Features of Internet Communication, Comparison of TCP and UDP.
- To understand the concept of Similarity of Safety and Security, Framework of Security Checking, Control Command Transmission Security.

**Module-1**

**Introduction:** Networked Control Systems (NCS), Internet-based Control Systems (ICS), Challenges of NCS/ICS. **Requirements Specification for Internet-based Control Systems:** Introduction, Requirements Specification, Functional Modelling of Internet-based Control Systems, Information Hierarchy, Possible Implementation of Information Architecture.
**Internet-based Control System Architecture Design:** Introduction, Traditional Bilateral Tele-operation Systems, Remote Control over the Internet, Canonical Internet-based Control System Structures.
**Web-based User Interface Design:** Features of Web-based User Interface, Multimedia User Interface Design, Case Study. ■

| | |
|---|---|
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

**Module-2**

**Real-time Data Transfer over the Internet:** Real-time Data Processing, Data Wrapped with XML, Real-time Data Transfer Mechanism, Case Study.
**Dealing with Internet Transmission Delay and Data Loss from the Network View:** Requirements of Network Infrastructure for Internet-based Control, Features of Internet Communication, Comparison of TCP and UDP, Network Infrastructure for Internet-based Control, Typical Implementation for Internet-based Control. ■

| | |
|---|---|
| **Teaching-Learning Process** | . Chalk and talk, power point presentation and video lecture. |

**Module-3**

**Dealing with Internet Transmission Delay and Data Loss from the Control Perspective:** Overcoming the Internet Transmission Delay, Control Structure with the Operator Located Remotely, Internet-based Control with a Variable Sampling Time, Multi-rate Control, Time Delay Compensator Design, Simulation Studies, Experimental Studies.
**Design of Multi-rate SISO Internet-based Control Systems:** Introduction, Discrete-time Multi-rate Control Scheme, Design Method, Stability Analysis, Simulation Studies, Real-time Implementation. ■

| | |
|---|---|
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

**Module-4**

**Design of Multi-rate MIMO Internet-based Control Systems:** Introduction, System Modeling, Controller Design, Stability Analysis, Design Procedure, Model-based Time Delay Compensation, Simulation Study.
**Safety and Security Checking:** Introduction, Similarity of Safety and Security, Framework of Security Checking, Control Command Transmission Security, Safety Checking, Case Study. ■

| | |
|---|---|
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

**Module-5**

**Remote Control Performance Monitoring and Maintenance over the Internet:** Introduction, Performance Monitoring, Performance Monitoring of Control Systems, Remote Control Performance Maintenance, Case Study.
**Remote Control System Design and Implementation over the Internet:** Introduction, Real-time Control System Life Cycle, Integrated Environments, A Typical Implementation of the General Integrated Environment, Case Study. ■

| | |
|---|---|
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous Internal Evaluation:**

15. Three Unit Tests each of **20 Marks**
16. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

**CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester End Examination:**

36. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
37. The question paper will have ten full questions carrying equal marks.
38. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
39. Each full question will have a sub-question covering all the topics under a module.
40. The students will have to answer five full questions, selecting one full question from each module

**Suggested Learning Resources:**

**Books**

**1.** Algorithms for VLSI Physical Design Automation, Naveed A. Sherwani, Kluwer Academic Publishers, 3rd Edition, 2002.

**Course outcome (Course Skill Set)**

At the end of the course the student will be able to :

| Sl. No. | Description | Blooms Level |
|---|---|---|
| CO1 | Discuss requirements for Internet-based control systems and to building a functional model, traditionaltele-operation systems and Web-based user interface design. | BL1,2 |
| CO2 | Discuss Real-time Data Transfer over the Internet dealing with Internet Transmission Delay and Data Lossfrom the Network View and Control perspective. | BL1,2 |
| CO3 | Discuss design of Multi-rate SISO and MIMO Internet-based Control Systems and Safety and SecurityChecking. | BL1,2 |
| CO4 | Explain the basic concepts and general guidelines of control system performance monitoring, remotelydesigning, testing, and updating real-time control software through the Internet | BL1,2 |

**Semester- 2**

| Nanotechnology for microelectronics and optoelectronics | | | |
|---|---|---|---|
| Course Code | **22EMS255** | CIE Marks | 50 |
| Teaching Hours/Week (L:P:SDA) | 2:0:2 | SEE Marks | 50 |
| Total Hours of Pedagogy | | Total Marks | 100 |
| Credits | 03 | Exam Hours | 03 |

**Course Learning objectives:**

- To provide an introduction to nanoelectronics and Optoelectronics, Quantum mechanical coherence, Quantum wells, wires, and dots, Density of states and dimensionality, Semiconductor heterostructures, Quantum transport.
- To learn Energy bands in typical semiconductors, Intrinsic and extrinsic semiconductors, Electron and hole concentrations in semiconductors.
- To learn the , MOSFET structures, Heterojunctions, Quantum wells, Superlattices.
- To understand the concept of Effect of a magnetic field on a crystal, Low-dimensional systems in magnetic fields, Density of states of a 2D system in a magnetic field.

**Module-1**

**Mesoscopic Physics and Nanotechnologies:** Trends in nanoelectronics and Optoelectronics, Characteristic lengths in mesoscopic systems, Quantum mechanical coherence, Quantum wells, wires, and dots, Density of states and dimensionality, Semiconductor heterostructures, Quantum transport.
**Survey of Solid State Physics:** Introduction, review of quantum mechanics, free electron model of a solid. Densityof states function, Bloch theorem, Electrons in crystalline solids, Dynamics of electrons in bands, Lattice vibrations, Phonons.■

| | |
|---|---|
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

**Module-2**

**Review of Semiconductor Physics:** Introduction, Energy bands in typical semiconductors, Intrinsic and extrinsic semiconductors, Electron and hole concentrations in semiconductors, Elementary transport in semiconductors, Degenerate semiconductors, Optical properties of semiconductors.
**The Physics of Low-Dimensional Semiconductors:** Introduction, Basic properties of two-dimensional semiconductor nanostructures, Square quantum well of finite depth, Parabolic and triangular quantum wells, Quantum wires, Quantum dots, Strained layers, Effect of strain on valence bands, Band structure in quantum wells, Excitonic effects in quantum.■

| | |
|---|---|
| **Teaching-Learning Process** | . Chalk and talk, power point presentation and video lecture. |

**Module-3**

**Semiconductor Quantum Nanostructures and Superlattices:** Introduction, MOSFET structures, Heterojunctions, Quantum wells, Superlattices.
**Electric Field Transport in Nanostructures:** Introduction, Parallel transport, Perpendicular transport, Quantum transport in nanostructures.■

| | |
|---|---|
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

**Module-4**

**Transport in Magnetic Fields and the Quantum Hall Effect:** Introduction, Effect of a magnetic field on a crystal,Low-dimensional systems in magnetic fields, Density of states of a 2D system in a magnetic field, The Aharonov–Bohm effect, The Shubnikov–de Haas effect, The quantum Hall Effect.
**Optical and Electro-optical Processes in Quantum Heterostructures:** Introduction,
Optical properties of quantum wells and superlattices, Optical properties of quantum dots and nanocrystals, Electro-optical effects in quantum wells. Quantum confined Stark Effect, Electro-optical effects in superlattices. Stark ladders and Bloch Oscillations. ■

| | |
|---|---|
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

**Module-5**

**Electronic Devices Based on Nanostructures:** Introduction, MODFETs, Heterojunction bipolar transistors,Resonant tunnel effect, Hot electron transistors, Resonant tunneling transistor, Single electron transistor.
**Optoelectronic Devices Based on Nanostructures:** Introduction, Heterostructure semiconductor lasers, Quantumwell semiconductor lasers, Vertical cavity surface emitting lasers (VCSELs), Strained quantum well lasers, Quantum dot lasers, Quantum well and superlattice photodetectors, Quantum well modulators. ■

| | |
|---|---|
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous Internal Evaluation:**

17. Three Unit Tests each of **20 Marks**
18. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

**CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester End Examination:**

41. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
42. The question paper will have ten full questions carrying equal marks.
43. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
44. Each full question will have a sub-question covering all the topics under a module.
45. The students will have to answer five full questions, selecting one full question from each module

**Suggested Learning Resources:**

**Books**

**1.** Algorithms for VLSI Physical Design Automation, Naveed A. Sherwani, Kluwer Academic Publishers, 3rd Edition, 2002.

**Course outcome (Course Skill Set)**

At the end of the course the student will be able to :

| Sl. No. | Description | Blooms Level |
|---|---|---|
| CO1 | Explain the present trends in microelectronic and optoelectronic devices, solid state and semiconductorphysics and define nanostructures. | BL1,2 |
| CO2 | Explain behavior of electrons in nanostructures and the transport and optical properties of nanostructures. | BL1,2 |
| CO3 | Discuss the transport properties of electrons in magnetic field and integral and fractional quantum Halleffect. | BL1,2 |
| CO4 | Discuss advanced semiconductor devices based on nanostructures and advanced optoelectronic andphotonic devices based on quantum heterostructures. | BL1,2 |

**Semester- 2**

| MICROELECTRONICS AND CONTROL LABORATORY - 2 | | | |
|---|---|---|---|
| Course Code | **22EMSL27** | CIE Marks | 50 |
| Teaching Hours/Week (L:T:P: S) | 00:01:02:00 | SEE Marks | 50 |
| Credits | 02 | Exam Hours | 100 |

**Course objectives:**

- . Apply the concepts of basic combinational logic circuits, sequential circuit elements, and programmable logic in the laboratory setting.
- To develop familiarity and confidence with designing, building and testing digital circuits, including the use of CAD tools.
- Behavioural, register- transfer, logic, and physical-level structured VLSI design using CAD tools and hardware description languages

| Sl.NO | Experiments |
|---|---|
| 1 | Design a 16 bit parallel adder (carry select, carry look ahead adder and ripple carry adder) using Verilog code and verify its functionality. Compare the area and power utilisation. |
| 2 | Write a Verilog code for a 3 input Boolean expression using 8:1 multiplexor and verify its functionality. |
| 3 | Design the following Flip flops using Verilog code and verify the functionality: SR flip flop, D flip flop, T flip flop, JK flip-flop. |
| 4 | Write a Verilog code for a universal shift register and verify its functionality. |
| 5 | Design a MOD-16 Synchronous counter using synchronous reset. Draw the truth table and waveform diagram. |
| 6 | Design a MOD-16 Asynchronous counter using T-flip flop. Draw the truth table and waveform diagram. |
| 7 | Using the Verilog code verify the functionality of a Boolean expression using Basic gates like NAND, NOR, AND, XOR. |
| | **Demonstration Experiments ( For CIE ) if any** |
| 8 | Verify the function of CMOS inverter by Verilog code. |
| 9 | Write a Verilog code for a buffer and verify its functionality. |
| 10 | Write a Verilog code for a Transmission gate and verify its functionality. |

**Course outcomes (Course Skill Set):**

At the end of the course the student will be able to:

- Write Verilog code to verify the functionality of CMOS inverter and buffer.
- Write Verilog code to verify the functionality of Basic gates, transmission gates and universal shift register.
- Write Verilog codes for verifying the functionality of 3 input Boolean expression using 8:1 multiplexer.
- Determine critical input and output voltages of CMOS inverter and noise margins of CMOS inverter.
- Use Verilog code to design a 16 bit parallel adder, flip flops.
- Design MOD -16 synchronous counter using synchronous set.
- Design MOD -16 asynchronous counter using T – flip flop.■

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 40% of maximum marks in the semester-end examination(SEE). In total of CIE and SEE student has to secure 50% maximum marks of the course.

**Continuous Internal Evaluation (CIE):**

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the $8^{th}$ week of the semester and the second test shall be conducted after the $14^{th}$ week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of **scaled-down** marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

**Semester End Evaluation (SEE):**

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University.

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 10% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours

**Semester- 3**

| CONTROL SYSTEMS FOR HVAC | | | |
|---|---|---|---|
| Course Code | 22EMS21 | CIE Marks | 50 |
| Teaching Hours/Week (L:P:SDA) | 02:00:02 | SEE Marks | 50 |
| Total Hours of Pedagogy | 40 hours Theory | Total Marks | 100 |
| Credits | 04 | Exam Hours | 3 Hrs |

**Course Learning objectives:**

- To learn HVAC control devices, control types/actions, and sensors.
- To learn control strategies based on temperature set point, PMV control, CO2 set-point, and equipment used to reduce the amount of energy consumed by heating, ventilating, and air conditioning (HVAC) systems.
- To learn various control schemes encountered in HVAC systems and assess monitoring and control strategies over life cycle costs.
- To develop the model and formulate optimization problem of any HVAC system operation to minimize energy consumption based on a control strategy.
- To design/select appropriate HVAC control systems for acceptable comfort and IAQ

**Module-1**

**Control Theory and Terminology:** Introduction, Elementary Control System, Purposes of Control, Control action, Energy Sources for Control, Systems, Measurement, Symbols and Abbreviations, Psychrometrics, Relationships.
**Pneumatic Control Devices:** Introduction, Pneumatic Control Devices, Control Cabinets, Air Supply.
**Electric and Electronic Control:** Devices, Electric Control Devices, Electronic Control Devices. ■

| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |
|---|---|

**Module-2**

**Fluidic Control Devices:** Introduction, Wall Attachment Devices, Turbulence Amplifiers, Vortex Amplifiers, Radial Jet Amplifier, Fluidic Transducers, Manual Switches.
**Flow Control Devices**: Dampers, Steam and Water Flow, Control Valves.
**Elementary Control Systems:** Introduction, Outside Air Controls, Air Stratification, Heating, Cooling Coils, Humidity Control, Dehumidifiers, Static Pressure Control, Electric Heat, Gas-Fired Heaters, Oil-Fired Heaters, Refrigeration Equipment, Fire and Smoke Control, Electrical Interlocks, Location of Sensors.■and Accessories.■

| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |
|---|---|

**Module-3**

**Complete Control Systems:** Introduction, Single-Zone Systems, Multizone Air Handling Systems, Dual-Duct Systems, Variable-Volume Systems, Reheat Systems, Heat Reclaim, Fan-Coil Units, Induction Systems, Unit Ventilators, Packaged Equipment, Other Packaged Equipment, Radiant Heating and Cooling, Radiators and Convectors, Heat Exchangers, Solar Heating and Cooling Systems.■

| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |
|---|---|

**Module-4**

**Electric Control Systems:** Introduction, Electric Control Diagrams, Electrical Control of a Chiller, Electrical Control of an Air Handling Unit, Example: A Typical Small Air- Conditioning System, Electric Heaters, Reduced- Voltage Starters, Multispeed Starters, Variable Speed Controllers.
**Special Control:** Introduction, Close Temperature and/or Humidity Control, Controlled Environment, Rooms for Testing.
**Digital and Supervisory Control Systems:** Introduction, Hard-Wired Systems, Multiplexing Systems, Computer-Based Systems for Monitoring and Control, Benefits of the Computer System, Training for Maintenance and Operation. ■

| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |
|---|---|

**Module-5**

**Psychrometrics:** Introduction, Psychrometric Properties, Psychrometric Tables, Psychrometric Charts, Processes on the Psychrometric Chart, HVAC Cycles on the Chart, Impossible Processes, Effects of Altitude.
**Central Plant Pumping and Distribution Systems:** Introduction, Diversity, Constant Flow Systems, Variable Flow Systems, Distribution Systems, Building Interfaces.

| | |
|---|---|
| **Retrofit of Existing Control Systems:** Introduction, Economic Analysis, Discriminators, Control Modes, Economy Cycle Controls, Single-Zone systems, Reheat Systems, Multizone Systems, Dual-Duct Systems, Systems with Humidity Control, Control Valves and Pumping Arrangements.<br>**Dynamic Response And Tuning:** Introduction, Dynamic Response, Tuning HVAC Control Loops. ■ | |
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

## Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

### Continuous Internal Evaluation:

19. Three Unit Tests each of **20 Marks**
20. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

**CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

### Semester End Examination:

46. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
47. The question paper will have ten full questions carrying equal marks.
48. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
49. Each full question will have a sub-question covering all the topics under a module.
50. The students will have to answer five full questions, selecting one full question from each module

**Suggested Learning Resources:**

**Books**

2. Control Systems For Heating, Ventilating, and Air Conditioning, Roger W. Haines, Springer, 6th Edition,2006.

**Course outcome (Course Skill Set)**

At the end of the course the student will be able to :

| Sl. No. | Description | Blooms Level |
|---|---|---|
| CO1 | Discuss the elements of a control system, the basic types of control action, and the energy sources usedfor controls and various types of control elements. | L1, L2 |
| CO2 | Discuss formation of combinations control elements used for control of HVAC. | L1, L2 |
| CO3 | Discuss formation and analysis of complete control system for specific application. | L1, L2 |
| CO4 | Explain and solve the electrical problems inherent in the design of control diagrams, stability of and thedigital control of HVAC control systems. | L1, L2 |
| CO5 | Use Psychrometric chart to control design, to study central plant pumping and distribution systems,existing HVAC systems and the tuning of HVAC control loops.■ | L1, L2 |

**Semester- 3**

| Industrial Control - Software And Routines | | | |
|---|---|---|---|
| Course Code | 22EMS321 | CIE Marks | 50 |
| Teaching Hours/Week (L:P:SDA) | 2:0:2 | SEE Marks | 50 |
| Total Hours of Pedagogy | | Total Marks | 100 |
| Credits | 3 | Exam Hours | 03 |

**Course Learning objectives:**

- To learn about code Structures, Single-Processor Boot Sequences, Multiprocessor Boot Sequences, Task Controls, Input /Output Device Drivers.
- To learn about interrupts, Memory Management, Event Brokers, Message Queue,Semaphores, Timer.
- To learn multiprocessor Operating Systems, multicomputer operating systems,distributed and parallel facilities, modelling and identification, simulation and control, softwareand simulator.

**Module-1**

**Microprocessor Boot Code:** Code Structures, Single-Processor Boot Sequences, Multiprocessor Boot Sequences.
**Real-Time Operating Systems:** Introduction, Task Controls, Input /Output Device Drivers.■

| | |
|---|---|
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

**Module-2**

**Real-Time Operating Systems (continued):** Interrupts, Memory Management, Event Brokers, Message Queue, Semaphores, Timer.■

| | |
|---|---|
| **Teaching-Learning Process** | . Chalk and talk, power point presentation and video lecture. |

**Module-3**

**Distributed Operating Systems:** Multiprocessor Operating Systems,Multicomputer Operating Systems, Distributed and Parallel Facilities.■

| | |
|---|---|
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

**Module-4**

**Industrial Control System Operation Routines:** Self-Test Routines, Install and Configure Routines, DiagnosisRoutines, Calibration Routines.■

| | |
|---|---|
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

**Module-5**

**Industrial Control System Simulation Routines:** Modelling and Identification, Simulation and Control, Software and Simulator.■

| | |
|---|---|
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

## Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

### Continuous Internal Evaluation:

21. Three Unit Tests each of **20 Marks**
22. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

**CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

### Semester End Examination:

51. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
52. The question paper will have ten full questions carrying equal marks.
53. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
54. Each full question will have a sub-question covering all the topics under a module.
55. The students will have to answer five full questions, selecting one full question from each module

**Suggested Learning Resources:**

**Books**

1. Advanced Industrial Control Technology, Peng Zhang, Elsevier, 2010.

**Course outcome (Course Skill Set)**

At the end of the course the student will be able to :

| Sl. No. | Description | Blooms Level |
|---|---|---|
| CO1 | Explain the Microprocessor boot code, one of the key component of Embedded software for controlpurpose. | BL1,2 |
| CO2 | Explain in detail the real-time operating systems, which are the platforms needed for a control system tosatisfy real-time criteria. | BL1,2 |
| CO3 | Explain the distributed operating system, the necessary platform for distributed control systems. | BL2 |
| CO4 | Explain industrial system operation routines, including the self-test routines at power-on and power-down, installation and configuration routines, diagnostic routines, and calibration routines. | BL2 |
| CO5 | Discuss the identification principles and techniques for model-based control.■ | BL2 |

**Semester- 3**

| DIGITAL SYSTEM DESIGN WITH FPGA | | | |
|---|---|---|---|
| Course Code | **22EMS322** | CIE Marks | 50 |
| Teaching Hours/Week (L:P:SDA) | 3:0:0 | SEE Marks | 50 |
| Total Hours of Pedagogy | | Total Marks | 100 |
| Credits | 03 | Exam Hours | 3 |

**Course Learning objectives:**

- To learn about electronic Circuits, Programmable Logic versus Discrete Logic, Types , Methods and Tools, Technology Trends.
- To learn about Software Programming Languages, Hardware Description Languages, SPICE, System C $^{R}$, System Verilog, Mathematical Modelling Tools.
- To learn about designing with HDLs, Design Entry Methods, Logic Synthesis. Entities, Architectures, Packages, and Configurations, Sequential Logic Design, Memories Unsignedversus Signed Arithmetic.
- To learn about Integrated Circuit Testing, Printed Circuit Board Testing, Boundary Scan Testing, Software Testing, Digital-to-Analogue Conversion, Analogue-to-Digital Conversion, Power Electronics, Heat Dissipation and Heat sinks. Operational Amplifier Circuits.

**Module-1**

**Programmable Logic:** Introduction, Electronic Circuits: Analogue and Digital, Programmable Logic versus Discrete Logic, Programmable Logic versus Processors, Types of Programmable Logic, PLD Configuration Technologies, Programmable Logic Vendors, Programmable Logic Design Methods and Tools, Technology Trends.
**Design Languages:** Introduction, Software Programming Languages, Hardware Description Languages, SPICE, System C $^{R}$, System Verilog, Mathematical Modelling Tools. ■

| **Teaching-Learning Process** | Chalk and Board, Power Point Presentation. |
|---|---|

**Module-2**

**Electronic Systems Design:** Introduction, Sequential Product Development Process versus Concurrent Engineering Process, Flowcharts, Block Diagrams, Gajski-Kuhn Chart, Hardware-Software Co-Design, Formal Verification, Embedded Systems and Real-Time Operating Systems, Electronic System-Level Design, Creating a Design Specification, Unified Modelling Language, Reading a Component Data Sheet, Digital Input/Output, Parallel and Serial Interfacing, System Reset, System Clock, Power Supplies, Power Management, Printed Circuit Boards and Multichip Modules, System on a Chip and System in a Package, Mechatronic Systems, Intellectual Property, CE and FCC Markings. ■

| **Teaching-Learning Process** | Chalk and Board, Power Point Presentation. |
|---|---|

**Module-3**

**Introduction to Digital Logic Design with VHDL:** Introduction, Designing with HDLs, Design Entry Methods, Logic Synthesis. Entities, Architectures, Packages, and Configurations, A First Design, Signals versus Variables, Generics, Reserved Words, Data Types, Concurrent versus Sequential Statements, Loops and Program Control, Coding Styles for VHDL, Combinational Logic Design. ■

| **Teaching-Learning Process** | Chalk and Board, Power Point Presentation. |
|---|---|

**Module-4**

**Introduction to Digital Logic Design with VHDL (continued):** Sequential Logic Design, Memories Unsignedversus Signed Arithmetic - Adder Example. Multiplier Example.
**Testing the Design:** Introduction, Integrated Circuit Testing, Printed Circuit Board Testing, Boundary Scan Testing, Software Testing. ■

| **Teaching-Learning Process** | Chalk and Board, Power Point Presentation. |
|---|---|

**Module-5**

**Digital-to-Analogue Conversion, and Power Electronics:** Introduction, Digital-to-Analogue Conversion, Analogue-to-Digital Conversion, Power Electronics, Heat Dissipation and Heat sinks. Operational Amplifier Circuits.
**System-Level Design:** Introduction, Case Study-DC Motor Control. ■

| **Teaching-Learning Process** | Chalk and Board, Power Point Presentation. |
|---|---|

## Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

### Continuous Internal Evaluation:

23. Three Unit Tests each of **20 Marks**
24. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

**CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

### Semester End Examination:

56. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
57. The question paper will have ten full questions carrying equal marks.
58. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
59. Each full question will have a sub-question covering all the topics under a module.
60. The students will have to answer five full questions, selecting one full question from each module

**Suggested Learning Resources:**

**Books**

3. Digital Systems Design with FPGAs and CPLDs, Ian Grout, Elsevier, 2008..

**Course outcome (Course Skill Set)**

At the end of the course the student will be able to :

| Sl. No. | Description | Blooms Level |
|---|---|---|
| CO1 | Discuss programmable logic devices that are available today, their architectures, their use within electronic system design and the terminology used. | L2 |
| CO2 | Discuss different programming languages that are used to develop digital designs for implementation ineither a processor or in programmable logic. | L2 |
| CO3 | Explain designing of electronic systems, the types of solutions that can be developed, and the decisions that will need to be made in order to identify the right technology choice for the design implementation. | L3 |
| CO4 | Describe digital circuit and system designs in an ASCII text-based format using VHDL.Test the electronic systems for failure mechanisms in hardware and software. Interface programmable logic devices to the analogue world. | L3 |
| CO5 | Explain with a case study the necessity to develop programmable logic–based designs at a high level ofabstraction using behavioral descriptions of the system functionality.■ | L3 |

**Semester- 3**

| REAL TIME APPROACH TO PROCESS CONTROL | | | |
|---|---|---|---|
| Course Code | **22EMS323** | CIE Marks | 50 |
| Teaching Hours/Week (L:P:SDA) | 3:0:0 | SEE Marks | 50 |
| Total Hours of Pedagogy | | Total Marks | 100 |
| Credits | 3 | Exam Hours | 03 |

**Course Learning objectives:**

- To learn about Control Simulation, Control system components, Primary elements, Final control elements, open-loop control, Disturbances, Feedback controloverview, Feedback control.
- To learn about On−off control, Proportional (P-only) control, Integral (I-only) control, Proportional plus integral (PI) control, Derivative action, Proportional plus derivative (PD) controller, Proportional integral derivative(PID) control, Choosing the correct controller, Controller hardware.
- To learn about Cascade control, Feed forward control, Ratio control, Overridecontrol (auto selectors). Flow loops, Liquid pressure loops, Liquid level control, Gas pressure loops, Temperature control loops, Pump control, Compressor control, Boiler control.

**Module-1**

**Control, simulation, and Process control hardware fundamentals:** Control, Simulation, Control system components, Primary elements, Final control elements. ■

| | |
|---|---|
| **Teaching-Learning Process** | Chalk and Board, Power Point Presentation. |

**Module-2**

**Fundamentals of single input−single output systems**: Open-loop control, Disturbances, Feedback controloverview, Feedback control: a closer look, Process attributes: capacitance and dead time, Process dynamic response, Process modeling and simulation.■

| | |
|---|---|
| **Teaching-Learning Process** | . Chalk and Board, Power Point Presentation. |

**Module-3**

**Basic control modes:** On−off control, Proportional (P-only) control, Integral (I-only) control, Proportional plus integral (PI) control, Derivative action, Proportional plus derivative (PD) controller, Proportional integral derivative(PID) control, Choosing the correct controller, Controller hardware.
**Tuning feedback controllers:** Quality of control and optimisation, Tuning methods. ■

| | |
|---|---|
| **Teaching-Learning Process** | Chalk and Board, Power Point Presentation. |

**Module-4**

**Advanced topics in classical automatic control:** Cascade control, Feedforward control, Ratio control, Overridecontrol (auto selectors).
**Common control loops:** Flow loops, Liquid pressure loops, Liquid level control, Gas pressure loops, Temperature control loops, Pump control, Compressor control, Boiler control. ■

| | |
|---|---|
| **Teaching-Learning Process** | Chalk and Board, Power Point Presentation. |

**Module-5**

**Distillation column control:** Basic terms, Steady-state and dynamic degrees of freedom, Control system objectives and design considerations, Methodology for selection of a controller structure, Level, pressure, temperature and composition control, Optimizing control, Distillation control scheme design using steady-state models, Distillation control scheme design using dynamic models.
**Using steady-state methods in a multi-loop control scheme:** Variable pairing, The relative gain array,Niederlinski index, Decoupling control loops, Tuning the controllers for multi-loop systems, Practical examples. **Plant-wide control:** Short-term versus long-term control focus, Cascaded units, Recycle streams, General considerations for plant-wide control. ■

| | |
|---|---|
| **Teaching-Learning Process** | Chalk and Board, Power Point Presentation. |

## Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

### Continuous Internal Evaluation:

25. Three Unit Tests each of **20 Marks**
26. Two assignments each of **20 Marks**or**oneSkill Development Activity of 40 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

**CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

### Semester End Examination:

61. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
62. The question paper will have ten full questions carrying equal marks.
63. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
64. Each full question will have a sub-question covering all the topics under a module.
65. The students will have to answer five full questions, selecting one full question from each module

**Suggested Learning Resources:**

**Books**

1. A Real-Time Approach to Process Control, William Y. Svrcek, Wiley, 2nd Edition, 2006.

**Course outcome (Course Skill Set)**

At the end of the course the student will be able to :

| Sl. No. | Description | Blooms Level |
|---|---|---|
| CO1 | Discuss process control and the instruments used in the process control | 1,2 |
| CO2 | Explain basics of single input – single output systems, Feedback control, elements of control loops,system dynamics including capacitance and dead time, and system modeling. | 1,2 |
| CO3 | Discuss various PID control modes, control-loop design and tuning. and advanced control configurations including feed-forward, cascade, and override control. | 1,2,3 |
| CO4 | Explain thumb rules for designing and tuning the more common control loops found in industry Control distillation columns. | 1,2,3 |
| CO5 | Explain the concept of multiple loop controllers and issues relating to the plant-wide control problem. ■ | 1,2,3 |

**Semester- 3**

| DATA ANALYTICS FOR THE SMART GRID | | | |
|---|---|---|---|
| Course Code | **22EMS324** | CIE Marks | 50 |
| Teaching Hours/Week (L:P:SDA) | 3:0:0 | SEE Marks | 50 |
| Total Hours of Pedagogy | | Total Marks | 100 |
| Credits | 3 | Exam Hours | 03 |

**Course Learning objectives:**

- To learn about the Imperative for the Data-Driven Utility, Big Data, Building the Analytical Architecture, Algorithms, Seeing Intelligence, Assessing the Business Issues.
- To learn about Analytical Models, Using Descriptive Models for Analytics, Using Diagnostic Models for Analytics, Predictive Analytics, Prescriptive Analytics.
- To learn about Cybersecurity in the Utility Industry, The Role of Big Data Cybersecurity Analytics.

**Module-1**

**Putting the Smarts in the Smart Grid:** Goal, The Imperative for the Data-Driven Utility, Big Data: We'll Know It When We See It, What Are Data Analytics? Starting from Scratch, Finding Opportunity with Smart Grid Data Analytics.
**Building the Foundation for Data Analytics:** Chapter Goal, Perseverance Is the Most Important Tool, Building the Analytical Architecture.
**Transforming Big Data for High-Value Action**: Goal, The Utility as a Data Company, Algorithms, Seeing Intelligence, Assessing the Business Issues. ■

| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |
|---|---|

**Module-2**

**Applying Analytical Models in the Utility:** Goal, Understanding Analytical Models, Using Descriptive Models for Analytics, Using Diagnostic Models for Analytics, Predictive Analytics, Prescriptive Analytics, An Optimization Model for the Utility, Toward Situational Intelligence.
**Enterprise Analytics**: Goal, Moving Beyond Business Intelligence.
**Operational Analytics:** Goal, Aligning the Forces for Improved Decision-Making, The Opportunity for Insight, Focus on Effectiveness, Distributed Generation Operations: Managing the Mix-Up, Grid Management, Resiliency Analytics, Extracting Value from Operational Data Analytics. ■

| **Teaching-Learning Process** | . Chalk and talk, power point presentation and video lecture. |
|---|---|

**Module-3**

**Customer Operations and Engagement Analytics**: Goal, Increasing Customer Value, What's in It for the Customer?
**Analytics for Cybersecurity**: Goal, Cybersecurity in the Utility Industry, The Role of Big Data Cybersecurity Analytics.
**Sourcing Data:** Goal, Sourcing the Data, Working with a Variety of Data Sources. ■

| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |
|---|---|

**Module-4**

**Big Data Integration, Frameworks, and Databases:** Goal, This Is Going to Cost, Storage Modalities, Data Integration, The Costs of Low-Risk Approaches, Let the Data Flow, Other Big Data Databases, The Curse of Abundance.
**Extracting Value:** Goal, We Need Some Answers Here, Mining Data for Information and Knowledge, The Process of Data Extraction, Stream Processing, Avoid Irrational Exuberance. ■

| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |
|---|---|

**Module-5**

**Envisioning the Utility:** Goal, Big Data Comprehension, Why Humans Need Visualization, The Role of Human Perception, The Utility Visualized, Making Sense of It All.
**A Partnership for Change:** Goal, With Big Data Comes Big Responsibility, Privacy, Not Promises, Privacy Enhancement, The Utility of the Future Is a Good Partner. ■

| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |
|---|---|

## Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

### Continuous Internal Evaluation:

27. Three Unit Tests each of **20 Marks**
28. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

**CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

### Semester End Examination:

66. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
67. The question paper will have ten full questions carrying equal marks.
68. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
69. Each full question will have a sub-question covering all the topics under a module.
70. The students will have to answer five full questions, selecting one full question from each module

**Suggested Learning Resources:**

**Books**

**1.** Big Data Analytics Strategies for the Smart Grid, Carol L. Stimmel, CRC Press, 2015.

**Course outcome (Course Skill Set)**

At the end of the course the student will be able to :

| Sl. No. | Description | Blooms Level |
|---|---|---|
| CO1 | Discuss the key role of data analytics; its architecture and the challenges of creating and implementingthem. | BL1,2 |
| CO2 | Discuss useful analytical models, traditional business functions and issues affecting how analytics areused in the control room. | BL1,2 |
| CO3 | Discuss the methods to increase residential customer lifetime value, vulnerabilities, threats, and analyticapproaches to responding to cyber warfare against the utility, | BL1,2 |
| CO4 | Discuss the elements of big data infrastructure, their difficulties and benefits in adapting to the needs ofhigh-volume and varied data types, | BL1,2 |
| CO5 | Explain the basic concepts of data visualization and the importance of utility becoming trusted stewardof big data. ■ | BL1,2 |

| IoT-Internet of Things | | | |
|---|---|---|---|
| Course Code | **22EMS325** | CIE Marks | 50 |
| Teaching Hours/Week (L:P:SDA) | 3:0:0 | SEE Marks | 50 |
| Total Hours of Pedagogy | | Total Marks | 100 |
| Credits | 3 | Exam Hours | 03 |

**Course Learning objectives:**

- To learn about the IoT and Digitization, IoT Impact, Convergence of IT and IoT, IoT Challenges, IoT Network Architecture and Design, Drivers Behind New Network Architectures.
- To learn about Sensors, Actuators, and Smart Objects, Sensor Networks, Connecting Smart Objects, Communications Criteria.
- To learn about Data Analytics for IoT, Machine Learning, Big Data Analytics Tools and Technology, Edge Streaming Analytics.
- To learn about RaspberryPi, Programming RaspberryPi with Python, Wireless Temperature Monitoring System Using Pi, DS18B20 Temperature Sensor.

**Module-1**

What is IoT, Genesis of IoT, IoT and Digitization, IoT Impact, Convergence of IT and IoT, IoT Challenges, IoT Network Architecture and Design, Drivers Behind New Network Architectures, Comparing IoT Architectures, A Simplified IoT Architecture, The Core IoT Functional Stack, IoT Data Management and Compute Stack. ■

| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |
|---|---|

**Module-2**

Smart Objects: The "Things" in IoT, Sensors, Actuators, and Smart Objects, Sensor Networks, Connecting Smart Objects, Communications Criteria, IoT Access Technologies.■

| **Teaching-Learning Process** | . Chalk and talk, power point presentation and video lecture. |
|---|---|

**Module-3**

IP as the IoT Network Layer, The Business Case for IP, The need for Optimization, Optimizing IP for IoT, Profiles and Compliances, Application Protocols for IoT, The Transport Layer, IoT Application Transport Methods.■

| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |
|---|---|

**Module-4**

**Data and Analytics for IoT**, An Introduction to Data Analytics for IoT, Machine Learning, Big Data Analytics Tools and Technology, Edge Streaming Analytics, Network Analytics, Securing IoT, A Brief History of OT Security, Common Challenges in OT Security, How IT and OT Security Practices and Systems Vary, Formal Risk.
**Analysis Structures:** OCTAVE and FAIR, The Phased Application of Security in an Operational Environment. ■

| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |
|---|---|

**Module-5**

IoT Physical Devices and Endpoints - Arduino UNO: Introduction to Arduino, Arduino UNO, Installing the Software, Fundamentals of Arduino Programming. IoT Physical Devices and Endpoints - RaspberryPi: Introduction to RaspberryPi, About the RaspberryPi Board: Hardware Layout, Operating Systems on RaspberryPi, Configuring RaspberryPi, Programming RaspberryPi with Python, Wireless Temperature Monitoring System Using Pi, DS18B20 Temperature Sensor, Connecting Raspberry Pi via SSH, Accessing Temperature from DS18B20 sensors, Remote access to RaspberryPi, Smart and Connected Cities, An IoT Strategy for Smarter Cities, Smart City IoT Architecture, 10 Hours Smart City Security Architecture, Smart City Use-Case Examples.■

| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |
|---|---|

## Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

### Continuous Internal Evaluation:

29. Three Unit Tests each of **20 Marks**
30. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

**CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

### Semester End Examination:

71. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
72. The question paper will have ten full questions carrying equal marks.
73. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
74. Each full question will have a sub-question covering all the topics under a module.
75. The students will have to answer five full questions, selecting one full question from each module

**Suggested Learning Resources:**

**Text Book:**

**1. David Hanes, Gonzalo Salgueiro, Patrick Grossetete, Robert Barton, Jerome Henry**,"IoT Fundamentals: Networking Technologies, Protocols, and Use Cases for the Internet of Things", 1 stEdition, Pearson Education (Cisco Press Indian Reprint). (ISBN: 978- 9386873743) 2. Srinivasa K G, "Internet of Things",CENGAGE Leaning India, 2017.

**Reference Book:**

1. **Vijay Madisetti and ArshdeepBahga,** "Internet of Things (A Hands-on-Approach)", 1 stEdition, VPT, 2014. (ISBN: 978-8173719547) 2. Raj Kamal, "Internet of Things: Architecture and Design Principles", 1st Edition, McGraw Hill Education, 2017. (ISBN: 978-9352605224)

**Course outcome (Course Skill Set)**

At the end of the course the student will be able to :

| Sl. No. | Description | Blooms Level |
|---|---|---|
| CO1 | Interpret the impact and challenges posed by IoT networks leading to new architectural models. | BL1,2 |
| CO2 | Compare and contrast the deployment of smart objects and the technologies to connect them to network. | BL1,2 |
| CO3 | Appraise the role of IoT protocols for efficient network communication. | BL1,2 |
| CO4 | Elaborate the need for Data Analytics and Security in IoT. | BL1,2 |
| CO5 | Illustrate different sensor technologies for sensing real world entities and identify the applications of IoT in Industry.■ | BL1,2 |

**Semester- 3**

| Microelectronic Fabrication | | | |
|---|---|---|---|
| 3:0:0 | **22EMS331** | CIE Marks | 50 |
| Teaching Hours/Week (L:P:SDA) | 3:0:0 | SEE Marks | 50 |
| Total Hours of Pedagogy | | Total Marks | 100 |
| Credits | 3 | Exam Hours | 03 |

**Course Learning objectives:**

- To learn about , Metal – Oxide Semiconductor (MOS) Process, Photolithographic Process, Etching Techniques, Photomask Fabrication, Exposure Systems, Exposure Sources, Optical and Electron Microscopy.
- To lear about Diffusion Coefficient, Successive Diffusions, Solid – Solubility Limits, Junction Formation and Characterization, Sheet Resistance.
- To learn about Testing, Water Thinning and Die Separation, Die Attachment, Wire Bonding, Packages, Mechanical Properties of Silicon, Bulk Micromachining.

**Module-1**

**Introduction:** Historical Perspective, Overview of Monolithic Fabrication, Metal – Oxide Semiconductor (MOS) Process, Basic Bipolar Process, Safety.
**Lithography:** The Photolithographic Process, Etching Techniques, Photomask Fabrication, Exposure Systems, Exposure Sources, Optical and Electron Microscopy.
**Thermal Oxidation of Silicon:** The Oxidation Process, Modelling Oxidation, Factors Influencing Oxidation Rate, Dopant Redistribution during Oxidation, Masking Properties of Silicon Dioxide, Technology of Oxidation, Oxide Quality, Selective Oxidation and Shallow Trench Formation, Oxide Thickness Characterization, Process Simulation. ■

| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |
|---|---|

**Module-2**

**Diffusion:** The Diffusion Process, Mathematical Model for Diffusion, The Diffusion Coefficient, Successive Diffusions, Solid – Solubility Limits, Junction Formation and Characterization, Sheet Resistance, Generation – Depth and Impurity Profile Measurement, Diffusion Simulation, Diffusion Systems, Gettering. ■

| **Teaching-Learning Process** | . Chalk and talk, power point presentation and video lecture. |
|---|---|

**Module-3**

**Ion Implantation:** Implantation Technology, Mathematical Model for Ion Implantation, Selective Implantation, Junction Depth and Sheet Resistance, Channeling, Lattice, Damage and Annealing, Shallow Implantations.
**Film Deposition:** Evaporation, Sputtering, Chemical Vapour Deposition, Epitaxy.
**Interconnections and Contacts:** Interconnections in Integrated Circuits, Metal Interconnections and Contact Technology, Diffused Interconnections, Polysilicon Interconnections and Buried Contacts, Silicides and Multilayer – Contact Technology, The Liftoff Process, Multilevel Metallization, Copper Interconnects and Damascene Process. ■

| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |
|---|---|

**Module-4**

**Packaging and Yield:** Testing, Water Thinning and Die Separation, Die Attachment, Wire Bonding, Packages, Flip – Chip and tape – Automated – Bonding Process, Yield.
**MOS Process Integration:** Basic MOS Device Considerations, MOS Transistor Layout and Design Rules, Complementary MOS (CMOS) Technology, Silicon on Insulator. ■

| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |
|---|---|

**Module-5**

**Bipolar Process Integration:** The Junction – Isolated Structure, Current Gain, Transit Time, Base Width, Breakdown Voltages, Other Elements in SBC Technology, Layout Considerations, Advanced Bipolar Structure, Other Bipolar Insulation Techniques, BICMOS.
**Process for Microelectromechanical Systems (MEMS):** Mechanical Properties of Silicon, Bulk Micromachining, Silicon Etchants, Surface Micromachining, High – Aspect – Ratio Micromachining, Silicon Wafer Bonding, IC Process Compatibility. ■

| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |
|---|---|

## Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

### Continuous Internal Evaluation:

31. Three Unit Tests each of **20 Marks**
32. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

**CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

### Semester End Examination:

76. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
77. The question paper will have ten full questions carrying equal marks.
78. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
79. Each full question will have a sub-question covering all the topics under a module.
80. The students will have to answer five full questions, selecting one full question from each module

**Suggested Learning Resources:**

**Text Book**

1. Introduction to Microelectronic Fabrication, Richard C Jaeger, Prentice Hall, 2nd Edition, 2002.

**Course outcome (Course Skill Set)**

At the end of the course the student will be able to :

| Sl. No. | Description | Blooms Level |
|---|---|---|
| CO1 | Explain the basic processes of fabrication of monolithic integrated –circuit and basic steps in lithographic process. | BL1,2 |
| CO2 | Discuss the theory of oxide growth, oxide growth processes, factors affecting the growth rate, impurity redistribution during oxidation. | BL1,2 |
| CO3 | Discuss ion implementation technology, mathematical modelling of the impurity distributions, and the removal of crystal damage due to implantation process. | BL1,2 |
| CO4 | Discuss packaging and associated processes with integrated circuits and MOS process integration. | BL1,2 |
| CO5 | Discuss bipolar process integration and processes for fabrication of microelectromechanical elements in silicon. | BL1,2 |

**Semester- 3**

| Real Time Operating System | | | |
|---|---|---|---|
| Course Code | **22EMS332** | CIE Marks | 50 |
| Teaching Hours/Week (L:P:SDA) | 3:0:0 | SEE Marks | 50 |
| Total Hours of Pedagogy | | Total Marks | 100 |
| Credits | 3 | Exam Hours | 03 |

**Course Learning objectives:**

- To learn about Elements of a Computer Control System, RTS- Definition, Classification of Real-time Systems, Time Constraints, Sequence Control, Loop Control, Supervisory Control.
- To learn about Introduction, Syntax Layout and Readability, Declaration and Initialization of Variables and Constants, Cutlass, Modularity and Variables, Data types, Control Structures.
- To learn about Real-Time Multi-Tasking OS, Scheduling Strategies, Priority Structures, Task Management, Scheduler and Real-Time Clock Interrupt Handler

**Module-1**

**Introduction to Real-Time Systems:** Historical background, Elements of a Computer Control System, RTS- Definition, Classification of Real-time Systems, Time Constraints, Classification of Programs.
**Concepts of Computer Control:** Introduction, Sequence Control, Loop Control, Supervisory Control, Centralized Computer Control, Hierarchical Systems. ■

| | |
|---|---|
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

**Module-2**

**Computer Hardware Requirements for Real-Time Applications:** Introduction, General Purpose Computer, Single Chip Microcomputers and Microcontrollers, Specialized Processors, Process-Related Interfaces, Data Transfer Techniques, Communications, Standard Interface.■

| | |
|---|---|
| **Teaching-Learning Process** | . Chalk and talk, power point presentation and video lecture. |

**Module-3**

**Languages for Real-Time Applications:** Introduction, Syntax Layout and Readability, Declaration and Initialization of Variables and Constants, Cutlass, Modularity and Variables, Compilation of Modular Programs, Data types, Control Structures, Exception Handling, Low-level facilities, Co-routines, Interrupts and Device Handling, Concurrency, Real-Time Support, Overview of Real-Time Languages. ■

| | |
|---|---|
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

**Module-4**

**Operating Systems:** Introduction, Real-Time Multi-Tasking OS, Scheduling Strategies, Priority Structures, Task Management, Scheduler and Real-Time Clock Interrupt Handler, Memory Management, Code Sharing, Resource Control, Task Co-Operation and Communication, Mutual Exclusion.■

| | |
|---|---|
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

**Module-5**

**Design of RTS- General Introduction:** Introduction, Specification Document, Preliminary Design. Single-Program Approach, Foreground/Background System.
**RTS Development Methodologies:** Introduction, Yow-don Methodology, Ward and Mellor Method, Hately and Pirbhai Method.■

| | |
|---|---|
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

## Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

### Continuous Internal Evaluation:

33. Three Unit Tests each of **20 Marks**
34. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

**CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

### Semester End Examination:

81. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
82. The question paper will have ten full questions carrying equal marks.
83. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
84. Each full question will have a sub-question covering all the topics under a module.
85. The students will have to answer five full questions, selecting one full question from each module

**Suggested Learning Resources:**

**Text Book**

**1.** Real-Time Computer Control, Stuart Bennet, 2nd Edn. Pearson Education. 2008

**Reference Books**

**1.** "Real-Time Systems", C.M. Krishna, Kang G Shin, McGraw-Hill International Editions, 1997.
**2** Real-Time Systems Design and Analysis, Phillip. A. Laplante, second edition, PHI, 2005.
**3.** Embedded Systems, Raj Kamal, Tata McGraw Hill, India, third edition, 2005.

**Course outcome (Course Skill Set)**

At the end of the course the student will be able to :

| Sl. No. | Description | Blooms Level |
|---|---|---|
| CO1 | Explain the fundamentals of Real time systems and its classifications. | BL1,2 |
| CO2 | Understand the concepts of computer control and the suitable computer hardware requirements for real-time applications. | BL1,2,3 |
| CO3 | Describe the operating system concepts and techniques required for real time systems. | BL1,2 |
| CO4 | Develop the software algorithms using suitable languages to meet Real time applications. | BL1,2 |
| CO5 | Apply suitable methodologies to design and develop Real-Time Systems.. ■ | BL1,2 |

**Semester- 3**

| LOW POWER VLSI DESIGN | | | |
|---|---|---|---|
| Course Code | **22EMS333** | CIE Marks | 50 |
| Teaching Hours/Week (L:P:SDA) | 3:0:0 | SEE Marks | 50 |
| Total Hours of Pedagogy | | Total Marks | 100 |
| Credits | 3 | Exam Hours | 03 |

**Course Learning objectives:**

- To learn about Needs for Low Power VLSI Chips, Charging and Discharging Capacitance, Short-circuit Current in CMOS Circuit, CMOS Leakage Current, Static Current.
- To learn about Transistor and Gate Sizing, Equivalent Pin Ordering, Network Restructuring and Reorganization,Special Latches and Flip-flops, Low Power Digital Cell Library.
- To learn about Gate Reorganization, Signal Gating, Logic Encoding, Adiabatic Computation, Pass Transistor Logic Synthesis, Asynchronous Circuits

**Module-1**

**Low Power VLSI Chips:** Introduction, Needs for Low Power VLSI Chips, Charging and Discharging Capacitance, Short-circuit Current in CMOS Circuit, CMOS Leakage Current, Static Current, Basic Principles of Low Power Design, Low Power Figure of Merits.
**Simulation Power Analysis:** SPICE Circuit Simulation, Discrete Transistor Modelling and Analysis, Gate-level Logic Simulation, Architecture-level Analysis, Data Correlation Analysis in DSP Systems, Monte Carlo Simulation. ■

| | |
|---|---|
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

**Module-2**

**Probabilistic Power Analysis:** Random Logic Signals, Probability and Frequency, Probabilistic Power Analysis Techniques, Signal Entropy. ■

| | |
|---|---|
| **Teaching-Learning Process** | . Chalk and talk, power point presentation and video lecture. |

**Module-3**

**Circuit:** Transistor and Gate Sizing, Equivalent Pin Ordering, Network Restructuring and Reorganization, Special Latches and Flip-flops, Low Power Digital Cell Library, Adjustable Device Threshold Voltage.■

| | |
|---|---|
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

**Module-4**

**Logic:** Gate Reorganization, Signal Gating, Logic Encoding, State Machine Encoding, Precomputation Logic.
**Special Techniques**: Power Reduction in Clock Networks, CMOS Floating Node, Low Power Bus, Delay Balancing, Low Power Techniques for SRAM. ■

| | |
|---|---|
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

**Module-5**

**Architecture and System:** Power and Performance Management, Switching Activity Reduction, ParallelArchitecture with Voltage Reduction, Flow Graph Transformation.
**Advanced Techniques:** Adiabatic Computation, Pass Transistor Logic Synthesis, Asynchronous Circuits. ■

| | |
|---|---|
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

## Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

### Continuous Internal Evaluation:

35. Three Unit Tests each of **20 Marks**
36. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

**CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

### Semester End Examination:

86. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
87. The question paper will have ten full questions carrying equal marks.
88. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
89. Each full question will have a sub-question covering all the topics under a module.
90. The students will have to answer five full questions, selecting one full question from each module

**Suggested Learning Resources:**

**Books**

**1.** Practical Low Power Digital VLSI Design, Gary Yeap, Springer, 1998.

**Course outcome (Course Skill Set)**

At the end of the course the student will be able to :

| Sl. No. | Description | Blooms Level |
|---|---|---|
| CO1 | Explain the needs for low power VLSI, the charging and discharging capacitances, short circuit andleakage currents in CMOS circuits and basic principles of low power design. | BL1,2 |
| CO2 | Simulate VLSI chips using modeling techniques to estimate power dissipation, probabilistic power analysis for VLSI circuits. | BL1,2 |
| CO3 | Discuss the optimization and trade-off techniques that involve power dissipation for digital circuits. | BL1,2 |
| CO4 | Explain gate reorganization, signal gating, logic encoding and low power techniques for reduction inpower consumption in VLSI circuits. | BL1,2 |
| CO5 | Explain power and performance management switching activity reduction and the architecture forreduction in the power consumption of VLSI circuits, adiabatic computation, pass transistorlogic synthesis and asynchronous circuits. ■ | BL1,2 |

**Semester- 3**

| Linear Control System | | | |
|---|---|---|---|
| Course Code | **22EMS334** | CIE Marks | 50 |
| Teaching Hours/Week (L:P:SDA) | 3:0:0 | SEE Marks | 50 |
| Total Hours of Pedagogy | | Total Marks | 100 |
| Credits | 03 | Exam Hours | 03 |

**Course Learning objectives:**

- To learn about Transfer function of LTI systems- Mechanical and Electromechanical systems – Force voltage and force current analogy, DC and AC servo motors – synchro -gyroscope - stepper motor - Tacho generator.
- To learn about Transient and steady state responses - time domain specifications, - steady state error analysis - static error coefficient of type 0,1, 2 systems - Dynamic error coefficients.
- To learn about Root locus, - Analysis based on Bode plot - Log magnitude vs. phase plot, - Nyquist stability criterion-Nichols chart.

**Module-1**

**Open loop-and closed loop control systems:** Transfer function of LTI systems- Mechanical and Electromechanical systems – Force voltage and force current analogy - block diagram representation - block diagram reduction - signal flow graph - Mason's gain formula – characteristic equation. ■

| | |
|---|---|
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

**Module-2**

**Control system components:** DC and AC servo motors – synchro -gyroscope - stepper motor - Tacho generator.
**Time domain analysis of control systems**: Transient and steady state responses - time domain specifications - first and second order systems - step responses of first and second order systems ■

| | |
|---|---|
| **Teaching-Learning Process** | . Chalk and talk, power point presentation and video lecture. |

**Module-3**

**Error analysis -** steady state error analysis - static error coefficient of type 0,1, 2 systems - Dynamic error coefficients.
**Concept of stability:** Time response for various pole locations - stability of feedback system - Routh's stability criterion. ■

| | |
|---|---|
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

**Module-4**

Root locus - General rules for constructing Root loci – stability from root loci - effect of addition of poles and zeros. ■

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|---|---|
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

**Module-5**

**Frequency domain analysis:** Frequency domain specifications- Analysis based on Bode plot - Log magnitude vs. phase plot,
**Polar plot-** Nyquist stability criterion-Nichols chart - Non-minimum phase system - transportation lag. ■

| | |
|---|---|
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

## Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

### Continuous Internal Evaluation:

37. Three Unit Tests each of **20 Marks**
38. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

**CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

### Semester End Examination:

91. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
92. The question paper will have ten full questions carrying equal marks.
93. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
94. Each full question will have a sub-question covering all the topics under a module.
95. The students will have to answer five full questions, selecting one full question from each module

**Suggested Learning Resources:**

**Text Books**

1) Dorf R. C. and R. H. Bishop, Modern Control Systems, Pearson Education, 2011.
2) Nagarath I. J. and Gopal M., Control System Engineering, Wiley Eastern, 2008.
3) Nise N. S., Control Systems Engineering, 6/e, Wiley Eastern, 2010.
4) Ogata K., Modern Control Engineering, Prentice Hall of India, New Delhi, 2010.

**Reference Books**

1) Gibson J. E., F. B. Tuteur and J. R. Ragazzini, Control System Components, Tata McGraw Hill, 2013
2) Gopal M., Control Systems Principles and Design, Tata McGraw Hill, 2008.
3) Imthias Ahamed T P, Control Systems, Phasor Books, 2016
4) Kuo B. C., Automatic Control Systems, Prentice Hall of India, New Delhi, 2002.

**Course outcome (Course Skill Set)**

At the end of the course the student will be able to :

| Sl. No. | Description | Blooms Level |
|---|---|---|
| CO1 | Analyze and model electrical and mechanical system using analogous. | BL1,2 |
| CO2 | Formulate transfer functions using block diagram and signal flow graphs. | BL1,2 |
| CO3 | Analyze the stability of control system, ability to determine transient and steady state time response. | BL1,2 |
| CO4 | Illustrate the performance of a given system in time and frequency domains, stability analysis using Root locus and Bode plots. | BL1,2 |
| CO5 | Discuss stability analysis using Nyquist plots, Design controller and compensator for a given specification.. ■ | BL1,2 |

**Semester- 3**

| Computer Architecture | | | |
|---|---|---|---|
| Course Code | **22EMS335** | CIE Marks | 50 |
| Teaching Hours/Week (L:P:SDA) | 3:0:0 | SEE Marks | 50 |
| Total Hours of Pedagogy | | Total Marks | 100 |
| Credits | 03 | Exam Hours | 03 |

**Course Learning objectives:**

- To learn about state o f computing, Classification of parallel computers, Multiprocessors and multicomputer, Multivectors and SIMD computers.
- To learn about Control flow versus data flow, Data flow Architecture, Demand driven mechanisms, Comparisons of flow mechanisms.
- To learn about Linear pipeline processor, nonlinear pipeline processor, Instruction pipeline Design, Mechanisms for instruction pipelining.
- To learn about Symmetric shared memory architectures, distributed shared memory architectures, models of memory consistency, cache coherence protocols.

**Module-1**

**Parallel Computer Models:** The state o f computing, Classification of parallel computers, Multiprocessors and multicomputer, Multivectors and SIMD computers.
**Program and Network Properties:** Conditions of parallelism, Data and resource Dependences, Hardware and software parallelism, Program partitioning and scheduling, Grain Size and latency. ■

| | |
|---|---|
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

**Module-2**

**Program flow mechanisms:** Control flow versus data flow, Data flow Architecture, Demand driven mechanisms, Comparisons of flow mechanisms.
**Principles of Scalable Performance:** Performance Metrics and Measures, Parallel Processing Applications, Speedup Performance Laws, Scalability Analysis and Approaches. ■

| | |
|---|---|
| **Teaching-Learning Process** | . Chalk and talk, power point presentation and video lecture. |

**Module-3**

**Speedup Performance Laws:** Amdhal's law, Gustafson's law, Memory bounded speed up model, Scalability Analysis and Approaches.
**Advanced Processors:** Advanced processor technology, Instruction-set Architectures, CISC Scalar Processors, RISC Scalar Processors, Superscalar Processors, VLIW Architectures. ■

| | |
|---|---|
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

**Module-4**

**Pipelining:** Linear pipeline processor, nonlinear pipeline processor, Instruction pipeline Design, Mechanisms for instruction pipelining, Dynamic instruction scheduling, Branch Handling techniques, branch prediction, Arithmetic Pipeline Design.
**Memory Hierarchy Design:** Cache basics & cache performance, reducing miss rate and miss penalty, multilevel cache hierarchies, main memory organizations, design of memory hierarchies. ■

| | |
|---|---|
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

**Module-5**

**Multiprocessor Architectures:** Symmetric shared memory architectures, distributed shared memory architectures, models of memory consistency, cache coherence protocols (MSI, MESI, MOESI), scalable cache coherence, overview of directory based approaches, design challenges of directory protocols, memory based directory protocols, cache based directory protocols. ■

| | |
|---|---|
| **Teaching-Learning Process** | Chalk and talk, power point presentation and video lecture. |

## Assessment Details (both CIE and SEE)

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### Continuous Internal Evaluation:

39. Three Unit Tests each of **20 Marks**
40. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

**CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

### Semester End Examination:

96. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
97. The question paper will have ten full questions carrying equal marks.
98. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
99. Each full question will have a sub-question covering all the topics under a module.
100. The students will have to answer five full questions, selecting one full question from each module

**Suggested Learning Resources:**

**Text Book**

**1. Kai Hwang,** —Advanced computer architecture‖; TMH.

**Reference Books**

1. Kai Hwang and Zu, —Scalable Parallel Computers Architecture‖; MGH.
2. M.J Flynn, —Computer Architecture, Pipelined and Parallel Processor Design‖; Narosa Publishing.
3. D.A.Patterson, J.L.Hennessy, —Computer Architecture :A quantitative approach‖; Morgan Kauffmann Feb, 2002.

**Course outcome (Course Skill Set)**

At the end of the course the student will be able to :

| Sl. No. | Description | Blooms Level |
|---|---|---|
| CO1 | Explain parallel computer models and conditions of parallelism | BL1,2 |
| CO2 | Differentiate control flow, dataflow, demand driven mechanisms | BL1,2 |
| CO3 | Explain the principle of scalable performance | BL1,2 |
| CO4 | Discuss advanced processors architectures like CISC, RISC, superscalar and VLIW | BL1,2 |
| CO5 | Understand the basics of instruction pipelining and memory technologies<br>Explain the issues in multiprocessor architectures.■ | BL1,2 |

**Semester- 3**

| PROJECT WORK PHASE – 1 | | | |
|---|---|---|---|
| Course Code | **22EMS34** | CIE Marks | 100 |
| Number of contact Hours/Week | 2 | SEE Marks | -- |
| Credits | 02 | Exam Hours | -- |

**Course objectives:**

- Support independent learning.
- Guide to select and utilize adequate information from varied resources maintaining ethics.
- Guide to organize the work in the appropriate manner and present information (acknowledging the sources) clearly.
- Develop interactive, communication, organisation, time management, and presentation skills.
- Impart flexibility and adaptability.
- Inspire independent and team working.
- Expand intellectual capacity, credibility, judgement, intuition.
- Adhere to punctuality, setting, and meeting deadlines.
- Instil responsibilities to oneself and others.
- Train students to present the topic of project work in a seminar without any fear, face audience confidently, enhance communication skill, involve in group discussion to present and exchange ideas. ■

**Project Phase-1** Students in consultation with the guide/s shall carry out literature survey/ visit industries to finalize the topic of the Project. Subsequently, the students shall collect the material required for the selected project, prepare synopsis and narrate the methodology to carry out the project work.

**Seminar:** Each student, under the guidance of a Faculty, is required to

- Present the seminar on the selected project orally and/or through power point slides.
- Answer the queries and involve in debate/discussion.
- Submit two copies of the typed report with a list of references.

The participants shall take part in discussion to foster friendly and stimulating environment in which the students are motivated to reach high standards and become self-confident. ■

**Course outcomes:**

At the end of the course the student will be able to:

- Demonstrate a sound technical knowledge of their selected project topic.
- Undertake problem identification, formulation and solution.
- Design engineering solutions to complex problems utilising a systems approach.
- Communicate with engineers and the community at large in written an oral forms.
- Demonstrate the knowledge, skills and attitudes of a professional engineer.■

**Continuous Internal Evaluation**

CIE marks for the project report (50 marks), seminar (30 marks) and question and answer (20 marks) shall be awarded (based on the quality of report and presentation skill, participation in the question and answer session by the student) by the committee constituted for the purpose by the Head of the Department. The committee shall consist of three faculty from the department with the senior most acting as the Chairperson. ■

**Semester- 3**

| MINI PROJECT | | | |
|---|---|---|---|
| Course Code | **22EMS35** | CIE Marks | 40 |
| Number of contact Hours/Week | 2 | SEE Marks | 60 |
| Credits | 02 | Exam Hours/Batch | 03 |

**Course objectives:**

- To support independent learning and innovative attitude.
- To guide to select and utilize adequate information from varied resources upholding ethics.
- To guide to organize the work in the appropriate manner and present information (acknowledging the sources) clearly.
- To develop interactive, communication, organisation, time management, and presentation skills.
- To impart flexibility and adaptability.
- To inspire independent and team working.
- To expand intellectual capacity, credibility, judgement, intuition.
- To adhere to punctuality, setting and meeting deadlines.
- To instil responsibilities to oneself and others.
- To train students to present the topic of project work in a seminar without any fear, face audience confidently, enhance communication skill, involve in group discussion to present and exchange ideas. ■

**Mini-Project:** Each student of the project batch shall involve in carrying out the project work jointly in constant consultation with internal guide, co-guide, and external guide and prepare the project report as per the norms avoiding plagiarism. ■

**Course outcomes:**

At the end of the course the student will be able to:

- Present the mini-project and be able to defend it.
- Make links across different areas of knowledge and to generate, develop and evaluate ideas and information so as to apply these skills to the project task.
- Habituated to critical thinking and use problem solving skills.
- Communicate effectively and to present ideas clearly and coherently in both the written and oral forms.
- Work in a team to achieve common goal.
- Learn on their own, reflect on their learning and take appropriate actions to improve it. ■

**CIE procedure for Mini - Project:**

The CIE marks awarded for Mini - Project, shall be based on the evaluation of Mini - Project Report, Project Presentation skill and Question and Answer session in the ratio 50:25:25.The marks awarded for Mini - Project report shall be the same for all the batch mates.

**Semester End Examination**

SEE marks for the mini-project shall be awarded based on the evaluation of Mini-Project Report, Presentation skill and Question and Answer session in the ratio 50:25:25 by the examiners appointed by the University. ■

**Semester- 4**

| PROJECT WORK PHASE -2 | | | |
|---|---|---|---|
| Course Code | **22EMS41** | CIE Marks | 100 |
| Number of contact Hours/Week | 4 | SEE Marks | 100 |
| Credits | 18 | Exam Hours | 03 |

**Course objectives:**

- To support independent learning.
- To guide to select and utilize adequate information from varied resources maintaining ethics.
- To guide to organize the work in the appropriate manner and present information (acknowledging the sources) clearly.
- To develop interactive, communication, organisation, time management, and presentation skills.
- To impart flexibility and adaptability.
- To inspire independent and team working.
- To expand intellectual capacity, credibility, judgement, intuition.
- To adhere to punctuality, setting and meeting deadlines.
- To instil responsibilities to oneself and others.
- To train students to present the topic of project work in a seminar without any fear, face audience confidently, enhance communication skill, involve in group discussion to present and exchange ideas. ■

**Project Work Phase - II:** Each student of the project batch shall involve in carrying out the project work jointly in constant consultation with internal guide, co-guide, and external guide and prepare the project report as per the norms avoiding plagiarism. ■

**Course outcomes:**

At the end of the course the student will be able to:

- Present the project and be able to defend it.
- Make links across different areas of knowledge and to generate, develop and evaluate ideas and information so as to apply these skills to the project task.
- Habituated to critical thinking and use problem solving skills
- Communicate effectively and to present ideas clearly and coherently in both the written and oral forms.
- Work in a team to achieve common goal.
- Learn on their own, reflect on their learning and take appropriate actions to improve it. ■

**Continuous Internal Evaluation:**

**Project Report:** 20 marks. The basis for awarding the marks shall be the involvement of the student in the project and in the preparation of project report. To be awarded by the internal guide in consultation with external guide if any.

**Project Presentation:** 10 marks.

The Project Presentation marks of the Project Work Phase -II shall be awarded by the committee constituted for the purpose by the Head of the Department. The committee shall consist of three faculty from the department with the senior most acting as the Chairperson.

**Question and Answer:** 10 marks.

The student shall be evaluated based on the ability in the Question and Answer session for 10 marks.

**Semester End Examination**

SEE marks for the project report (30 marks), seminar (20 marks) and question and answer session (10 marks) shall be awarded (based on the quality of report and presentation skill, participation in the question and answer session) by the examiners appointed by the University. ■