VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI.

Semester–I

Scheme and Syllabus of Teaching and Examinations and Syllabus

M.Tech.VLSI Design & Embedded Systems ULV)

Applicable to VTU Departments-UNIVERSITY

(Effective from the Academic year 2022-23)

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VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI
Scheme of Teaching and Examinations – – 2022
M.Tech. VLSI Design & Embedded Systems (ULV)
Choice Based Credit System (CBCS) and Outcome-Based Education(OBE)

I SEMESTER

Sl. No	Course	Course Code	Course Title	Teaching Hours per Week			Examination				Credits
				Theory	Practical/Seminar	Tutorial/ Skill Development Activities	Duration in hours	CIE Marks	SEE Marks	Total Marks	
				L	P	T/SDA					
1	BSC	22ULV11	Advanced Engineering Mathematics	03	00	00	03	50	50	100	3
2	IPCC	22ULV12	Advanced Digital Design with Verilog HDL	03	02	00	03	50	50	100	4
3	PCC	22ULV13	Advanced Embedded System	03	00	02	03	50	50	100	4
4	PCC	22ULV14	Digital VLSI Design	02	00	02	03	50	50	100	3
5	PCC	22ULV15	VLSI Testing & Verification	02	00	02	03	50	50	100	3
6	MCC	22RMI16	Research Methodology and IPR	03	00	00	03	50	50	100	3
7	PCCL	22ULVL17	VLSI Design & Embedded Systems Lab-I	01	02	00	03	50	50	100	2
8	AUD/AEC	22AUD18/ 22AEC18	BOS recommended ONLINE courses	Classes and evaluation procedures are as per the policy of the online course providers.							PP
			TOTAL	**17**	**04**	**06**	**21**	**350**	**350**	**700**	**22**

Note: BSC-Basic Science Courses, PCC: Professional core. IPCC-Integrated Professional Core Courses, MCC- Mandatory Credit Course, AUD/AEC –Audit Course / Ability Enhancement Course(A pass in AUD/AEC is mandatory for the award of the degree), PCCL-Professional Core Course lab, **L-Lecture, P-Practical, T/SDA-Tutorial / Skill Development Activities**(Hours are for Interaction between faculty and students)

Integrated Professional Core Course (IPCC): **Integrated Professional Core Course (IPCC)**: Refers to Professional Theory Core Course Integrated with practical of the same course. The theory part of the IPCC shall be evaluated both by CIE and SEE. The practical part shall be evaluated by only CIE (no SEE). However, questions from the practical part of IPCC shall be included in the SEE question paper.

Audit Courses /Ability Enhancement Courses Suggested by BOS (ONLINE courses): Audit Courses: These are prerequisite courses suggested by the concerned Board of Studies. Ability Enhancement Courses will be suggested by the BoS if prerequisite courses are not required for the programs. **Ability Enhancement Courses**:

- These courses are prescribed to help students to enhance their skills in in fields connected to the field of specialisation as well allied fields that leads to employable skills. Involving in learning such courses is impetus to lifelong learning.
- The courses under this category are online courses published in advance and approved by the concerned Board of Studies.
- Registration to Audit /Ability Enhancement Course shall be done in consultation with the mentor and is compulsory during the concerned semester.
- In case a candidate fails to appear for the proctored examination or fails to pass the selected online course, he/she can register and appear for the same course if offered during the next session or register for a new course offered during that session, in consultation with the mentor.
- The Audit Ability Enhancement Course carries no credit and is not counted for vertical progression. However, a pass in such a course is mandatory for the award of the degree.

Skill development activities: Under Skill development activities in a concerning course, the students should

1. Interact with industry (small, medium, and large).
2. Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3. Involve in case studies and field visits/ fieldwork.
4. Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5. Handle advanced instruments to enhance technical talent.
6. Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7. Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc.

Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical –activities which will enhance their skill. The prepared report shall be evaluated for CIE marks.

Semester - I

Advanced Digital Design with Verilog HDL			
Course Code	22ULV12	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:2:0	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory + 10-12 Lab slots	Total Marks	100
Credits	04	Exam Hours	03

Course Learning Objectives:

- To understand the concepts of advanced digital design and role of Verilog in designing.
- To understand the Synthesis of Combinational and Sequential Logic.
- To know the Design and Synthesis of Datapath Controllers.
- To get the insight of Post synthesis Design Tasks.

MODULE-1	
Introduction to Digital Design Methodology: Design Methodology-An Introduction**,** IC Technology Options **Introduction to Logic Design with Verilog**: Structural Models of Combinational Logic, Logic System, Design Verification and Test Methodology, Propagation Delay, Truth Table Models of Combinational and Sequential Logic with Verilog.	
Teaching-Learning Process	Chalk and Talk / Power Point Presentations
MODULE-2	
Logic Design with Behavioral Models of Combinational and Sequential Logic: Behavioral Modeling, A Brief Look at Data Types for Behavioral Modeling, Boolean Equation-Based Behavioral Models of Combinational Logic, Propagation Delay and Continuous Assignments, Latches and Level-Sensitive Circuits in Verilog, Cyclic Behavioral Models of Flip-Flops and Latches, Cyclic Behavior and Edge Detection, A Comparison of Styles for Behavioral Modeling, Behavioral Models of Multiplexers, Encoders, and Decoders, Dataflow Models of a Linear-Feedback Shift Register, Modeling Digital Machines with Repetitive Algorithms, Machines with Multicycle Operations, Design Documentation with Functions and Tasks: Legacy or Lunacy?, Algorithmic State Machine Charts for Behavioral Modeling, ASMD Charts, Behavioral Models of Counters, Shift Registers and	
Teaching-Learning Process	Chalk and Talk / Power Point Presentations
MODULE-3	
Synthesis of Combinational and Sequential Logic: Introduction to Synthesis, Synthesis of Combinational Logic, Synthesis of Sequential Logic with Latches, Synthesis of Three-state Devices and Bus Interfaces, Synthesis of Sequential Logic with Flip-Flops, Synthesis of Explicit State Machines.	
Teaching-Learning Process	Chalk and Talk / Power Point Presentations
MODULE-4	
Synthesis of Combinational and Sequential Logic: Registered Logic, State Encoding, Synthesis of Implicit State Machines, Registers and Counters, Resets, Synthesis of Gated Clocks and Clock Enables, Anticipating the Results of Synthesis, Synthesis of Loops, Design Traps to Avoid, Divide and Conquer: Partitioning a Design.	
Teaching-Learning Process	Chalk and Talk / Power Point Presentations
MODULE 5	
Design and Synthesis of Despatch Controllers: Partitioned Sequential Machines, Design Example: Binary Counter, Design and Synthesis of a RISC Stored-Program Machine. **Postsynthcsis Design Tasks**: Post synthesis Design Validation, Post synthesis Timing Verification, Elimination of ASIC Timing Violations, False Paths, System Tasks for Timing Verification.	
Teaching-Learning Process	Chalk and Talk / Power Point Presentations

PRACTICAL COMPONENT OF IPCC *(May cover all / major modules)*

Sl.No.	Experiments
	Write a Verilog Description and Simulate
1)	Half Adder, AOI Circuit And Binary Full Adder Circuit.
2)	16-Bil Ripple-Carry Adder
3)	D Flip Flop, Transparent Latch, 32-Bit Comparator, 4-Bit Serial Shift Register
4)	Four-Channel 32-Bit Multiplexer, 8:3 Priority Encoder.
5)	3:8 Decoder, Seven-Segment Light-Emitting Diode (LED) Display.
6)	4-Bit Counter which can Count Up, Count Down or Hold the Count, 4·Bit Universal Shift Register

7)	Design a ALU with Default Output Assignment as 'Zero' and 'Don't Cares'. Synthesize both the codes and compare the result.
8)	Design and Synthesize a BCD-To-Excess-3 Code Converter
9)	UART Transmitter
10)	UART Receiver

Demonstration Experiments

1)	Implementation Of Verilog Description on FPGA Boards
2)	Implementation Of Verilog Description on FPGA Boards

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together

CIE for the theory component of IPCC

1) Two Tests each of **20 Marks**
2) Two assignments each of **10 Marks/One Skill Development Activity of 20 marks**
3) Total Marks of two tests and two assignments/one Skill Development Activity added will be CIE for 60 marks, marks scored will be proportionally scaled down to **30 marks**.

CIE for the practical component of IPCC

- On completion of every experiment/program in the laboratory, the students shall be evaluated and marks shall be awarded on the same day. The**15 marks** are for conducting the experiment and preparation of the laboratory record, the other **05 marks shall be for the test** conducted at the end of the semester.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to 15 marks.
- The laboratory test at the end /after completion of all the experiments shall be conducted for 50 marks and scaled down to 05 marks**.**

Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **20 marks**.

SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (duration 03 hours)

1) The question paper will be set for 100 marks and marks scored will be scaled down proportionately to 50 marks.
2) The question paper will have ten questions. Each question is set for 20 marks.
3) There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
4) The students have to answer 5 full questions, selecting one full question from each module.

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper shall include questions from the practical component).

- The minimum marks to be secured in CIE to appear for SEE shall be the 15 (50% of maximum marks-30) in the theory component and 10 (50% of maximum marks -20) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included**.** The maximum of 04/05 questions to be set from the practical component of IPCC, the total marks of all questions should not be more than the 20 marks.
- SEE will be conducted for 100 marks and students shall secure 40% of the maximum marks to qualify in the SEE. Marks secured will be scaled down to 50. (Student has to secure an aggregate of 50% of maximum marks of the course(CIE+SEE)

Suggested Learning Resources:

Books

1) Michael D. Ciletti, "Advanced Digital Design with Verilog HDL", Pearson, Second Edition.
2) John Michael Williams, "Digital VLSI Design with Verilog", A Textbook from Silicon Valley Polytechnic Institute, Second Edition.

Web links and Video Lectures (e-Resources):

- **https://www.youtube.com/watch?v=FWE0-FOoE4s&list=PLUtfVcb-iqn-EkuBs3arreilxa2UKIChl**
- **https://www.youtube.com/watch?v=zok4iU9YJiE&list=PLUtfVcb-iqn8ff92DJ0SZqwsX4W1s_oab**
- **https://www.youtube.com/watch?v=Y8FvvzcocT4&list=PLD2350A83B752C861**

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

1) Real world Problem Solving: Applying the digital design and Verilog HDL concepts

Course Outcomes (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Design the Digital Circuits and write the Verilog Description.	L2, L3
CO2	Synthesize the Combinational and Sequential Logic Circuits.	L2, L3
CO3	Analyse Postsynthesis Design Tasks.	L4

Program Outcomes of this course

Sl. No.	Description	POs
1)	Independently carry out research /investigation and development work to solve practical problems related to VLSI Design and embedded systems.	PO1
2)	Demonstrate a degree of mastery over the areas of VLSI Design and embedded systems. The mastery should be at a level higher than the requirements in the bachelor's in Electronics & Communication Engineering.	PO3
3)	Apply appropriate methodology and modern engineering/IT tools to meet the international standards in the area of VLSI design and embedded systems.	PO4
4)	Acquire competency in areas of VLSI and Embedded Systems, IC Fabrication, Design, Testing, Verification and Integrate multiple sub-systems to develop System on Chip to optimize its performance and excel in industry sectors related to VLSI / Embedded domain.	PO5
5)	Understand impact of professional engineering solutions in societal and environmental contexts and demonstrate the knowledge for sustainable development.	PO6

Mapping of COS and POs

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	×		×	×	×	×
CO2			×	×	×	
CO3	×		×			×

Semester - I

Advanced Embedded System			
Course Code	22ULV13	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:0:2	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory + 10-12 slots for Skill Development Activities	Total Marks	100
Credits	4	Exam Hours	3

Course Learning Objectives:

- To understand the concepts of embedded system design.
- To learn real design challenges of the system under development.
- To gain the essential knowledge required to design practical real-time embedded systems and appropriate real-time operating system (RTOS) product to be used.
- To know networking aspects of the embedded systems and Hardware-Software Co-design.

Module-1

Introduction of Embedded System: Embedded System: Embedded vs General computing system, classification, application and purpose of ES.
Typical of Embedded System: Communication Interface
The Strategy: Definition, Common Characteristics, Some Quality Metrics in ES Design, Versatility Factors for ES Product, Technologies Involved (Processors, Platforms, Devices-IC Technology), Hardware/Software Co-design
Use Cases: What Are Use Cases, Casual Versus Structured Version, Black Box Versus White Box, Hub and Spoke Model,
Details of the Use Case Model Entities (Actor, Stakeholder, Primary Actor, Supporting Actor, Scope, Scenarios, Levels, Use Case Entities and Their Relation, When Are We Done, Standard Use Case Template)

Teaching-Learning Process	Chalk and Talk / Power Point Presentations

Module-2

Models and Architectures: Representation of a Design, Model Taxonomy, Finite-State Machine (Mealy) Model, Petri Nets, Hierarchical Concurrent FSMs, Activity-Oriented Data Flow Graphs, Control Flow Graphs (Flowchart), Structure-Oriented Models, Data-Oriented Entity-Relationship Model, Jackson's Structured Programming Model, Heterogeneous Models

Teaching-Learning Process	Chalk and Talk / Power Point Presentations

Module-3

Specification Languages: SystemC: Characteristics of ESL for Embedded Systems, SystemC, Processes.
UML for Embedded Systems: Motivation, Typical Tasks and Roles in System Engineering, UML Diagrams, Structural Diagrams, Behavioural Diagrams

Teaching-Learning Process	Chalk and Talk / Power Point Presentations

Module-4

Real-Time Systems: Definition and Examples, Broad Classification of RTS, Terms in RT Systems, Periodic Schedule, Precedence Constraints and Dependencies, Scheduling Algorithms–Classification, Clock-Driven Scheduling, Priority-Driven Periodic Tasks, Dynamic Priority Algorithms, Scheduling Sporadic Jobs, Resource Access and Contention.
Real-Time Operating Systems (RTOS): Introduction, RTOS Concepts, Basic Design Using RTOS Case Study 1, Concept-Process and Threads.

Teaching-Learning Process	Chalk and Talk / Power Point Presentations

Module-5

Real-Time Operating Systems (RTOS): Posix, pThreads, Thread Synchronization, Design Strategies
Networked Embedded Systems (NES): Introduction, Characteristics, Broad Segments of NES, Automotive NES, CAN (Controller Area Network).
HW-SW Co-design: Introduction, Factors Driving Co-design, Co-design Problems, Conventional Model for HW-SW Design Process, Integrated Co-design Process, System Partitioning, Partitioning Algorithms.

Teaching-Learning Process	Chalk and Talk / Power Point Presentations

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1) Three Unit Tests each of **20 Marks**
2) Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1) The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2) The question paper will have ten full questions carrying equal marks.
3) Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4) Each full question will have a sub-question covering all the topics under a module.
5) The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Books

1) (Transactions on computer systems and networks) k. c. s. murti - design principles for embedded systems-springer (2022)
2) Introduction to embedded systems K. V. Shibu TMH education Pvt. Ltd. 2009
3) Embedded systems - A contemporary design tool James K. Peckol John Wiley 2008
4) The Definitive Guide to the ARM Cortex-M3 Joseph Yiu Newnes, (Elsevier) 2 ndedn, 2010.

Web links and Video Lectures (e-Resources):

- https://youtu.be/GaZBpY9Ys1Y
- https://youtu.be/SUusup7FfJo
- https://youtu.be/dHsHP9RrXBw?list=PLJ5C_6qdAvBH-JNRIlupFb44miyx9M8JD
- https://youtu.be/vn7aT9-cYzQ
- https://youtu.be/-rWGzFDLnAY

Skill Development Activities Suggested:

1) Interact with industry (small, medium, and large).
2) Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3) Involve in case studies and field visits/ fieldwork.
4) Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5) Handle advanced instruments to enhance technical talent.
6) Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7) Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc.

Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical – activities which will enhance their skill. The prepared report shall be evaluated for CIE marks.

Course Outcomes

At the end of the course the student will be able to:

Sl. No.	Description	Blooms Level
CO1	Design and Develop Embedded Systems with hardware software co-design.	L3
CO2	Analyze different models and architecture of the Embedded Systems and Networked Embedded Systems	L4
CO3	Verify the performance of RTS and RTOS	L3, L4

Program Outcomes of this course

Sl. No.	Description	POs
1)	Independently carry out research /investigation and development work to solve practical problems related to VLSI Design and embedded systems.	PO1
2)	Demonstrate a degree of mastery over the areas of VLSI Design and embedded systems. The mastery should be at a level higher than the requirements in the bachelor's in Electronics & Communication Engineering.	PO3
3)	Apply appropriate methodology and modern engineering/IT tools to meet the international standards in	PO4

	the area of VLSI design and embedded systems.	
4)	Acquire competency in areas of VLSI and Embedded Systems, IC Fabrication, Design, Testing, Verification and Integrate multiple sub-systems to develop System On Chip to optimize its performance and excel in industry sectors related to VLSI / Embedded domain.	PO5
5)	Understand impact of professional engineering solutions in societal and environmental contexts and demonstrate the knowledge for sustainable development.	PO6

Mapping of COS and POs

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	×					×
CO2			×			
CO3				×	×	

Semester - I

Digital VLSI Design			
Course Code	22ULV14	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	2:0:2	SEE Marks	50
Total Hours of Pedagogy	25 Hours Theory + 10 -12 slots for Skill Development Activities	Total Marks	100
Credits	04	Exam Hours	03

Course Learning Objectives:

- To understand the operation of MOS transistor, Scaling and Small Geometry Effects.
- To study Static Characteristics, Switching Characteristics and Interconnect Effect of MOS Inverter.
- To provide the insight of Semiconductor Memories, Dynamic Logic Circuits and BiCMOS Logic Circuits.
- To know Chip Input and Output Circuits, Clock Generation and Distribution Circuits, Design for Manufacturability.

Module-1

MOS Transistor: The Metal Oxide Semiconductor (MOS) Structure, The MOS System under External Bias, Structure and Operation of MOS Transistor, MOSFET Current-Voltage Characteristics, MOSFET Scaling and Small-Geometry Effects.

Teaching-Learning Process	Chalk and Talk, Power Point Presentations.

Module-2

MOS Inverters-Static Characteristics: Introduction, Resistive-Load Inverter, Inverters with n_Type MOSFET Load, CMOS Inverter.

Teaching-Learning Process	Chalk and Talk / Power Point Presentations.

Module-3

Dynamic Logic Circuits: Introduction, Basic Principles of Pass Transistor Circuits, Voltage Bootstrapping, Synchronous Dynamic Circuit Techniques, Dynamic CMOS Circuit Techniques, High Performance Dynamic CMOS circuits.

Teaching-Learning Process	Chalk and Talk / Power Point Presentations.

Module-4

Semiconductor Memories: Introduction, Dynamic Random Access Memory (DRAM), Static Random Access Memory (SRAM).

Teaching-Learning Process	Chalk and Talk / Power Point Presentations.

Module-5

BiCMOS Logic Circuits: Introduction, BiCMOS Applications.
Chip Input and Output (I/O) Circuits: Introduction, ESD Protection, On-Chip Clock Generation and Distribution, Latch-Up and Its Prevention.

Teaching-Learning Process	Chalk and Talk / Power Point Presentations.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1) Three Unit Tests each of **20 Marks**
2) Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1) The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2) The question paper will have ten full questions carrying equal marks.
3) Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4) Each full question will have a sub-question covering all the topics under a module.
5) The students will have to answer five full questions, selecting one full question from each module

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Suggested Learning Resources:

Books

1) "Sung Mo Kang & Yusuf Leblebici", CMOS Digital Integrated Circuits: Analysis and Design, Tata McGraw-Hill, Third Edition.
2) "Neil Weste and K. Eshraghian", Principles of CMOS VLSI Design: A System Perspective Pearson Education (Asia) Pvt. Ltd. Second Edition, 2000.
3) "Wayne, Wolf", Modern VLSI Design: System on Silicon, Prentice Hall PTR/ Pearson Education Second Edition, 1998
4) "Douglas A Pucknell& Kamran Eshraghian", Basic VLSI Design PHI 3rd Edition

Web links and Video Lectures (e-Resources):

- https://www.youtube.com/watch?v=57uTCtSQV50&list=PLHO2NKv71TvsSqYwVvUCZwNkY-jUyUHdS
- https://www.youtube.com/watch?v=oL8SKNxEaHs&list=PLLy_2iUCG87Bdulp9brz9AcvW_TnFCUmM

Skill Development Activities Suggested

1) Interact with industry (small, medium, and large).
2) Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3) Involve in case studies and field visits/ fieldwork.
4) Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5) Handle advanced instruments to enhance technical talent.
6) Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7) Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc.

Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical – activities which will enhance their skill. The prepared report shall be evaluated for CIE marks.

Course Outcomes:

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Analyse issues of On-chip interconnect Modelling and Interconnect delay calculation.	
CO2	Analyse the Switching Characteristics in Digital Integrated Circuits.	
CO3	Use the Dynamic Logic circuits in state-of-the-art VLSI chips.	
CO4	Study critical issues such as ESD protection, Clock distribution, Clock buffering, and Latch phenomenon	
CO5	Use Bipolar and Bi-CMOS circuits in very high speed design.	

Program Outcome of this course

Sl. No.	Description	POs
1)	Independently carry out research /investigation and development work to solve practical problems related to VLSI Design and embedded systems.	PO1
2)	Demonstrate a degree of mastery over the areas of VLSI Design and embedded systems. The mastery should be at a level higher than the requirements in the bachelor's in Electronics & Communication Engineering.	PO3
3)	Apply appropriate methodology and modern engineering/IT tools to meet the international standards in the area of VLSI design and embedded systems.	PO4
4)	Acquire competency in areas of VLSI and Embedded Systems, IC Fabrication, Design, Testing, Verification and Integrate multiple sub-systems to develop System On Chip to optimize its performance and excel in industry sectors related to VLSI / Embedded domain.	PO5
5)	Understand impact of professional engineering solutions in societal and environmental contexts and demonstrate the knowledge for sustainable development.	PO6

Mapping of COs and POs

	PO1	PO2	PO3	PO4	PO5	PO6
CO1			×	×		
CO2			×	×		
CO3	×				×	×
CO4	×				×	
CO5			×			×

Semester - I

VLSI Testing & Verification			
Course Code	22ULV15	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	2:0:2	SEE Marks	50
Total Hours of Pedagogy	25 Hours of Theory+ 10-12 sessions of Skill Development Activities.	Total Marks	100
Credits	03	Exam Hours	03

Course Learning Objectives:

- To study Faults in digital circuits.
- To learn various algorithms for test generation of Combinational Logic Circuits.
- To study the approach to deal with the testing problems at the chip level (BIST).
- To know about Design Verification Concepts, Simulator Architectures and Operations.

Module-1

Faults in digital circuits: Failures and Faults, Modeling of faults, Temporary Faults.
Test generation for Combinational Logic circuits: Fault Diagnosis of digital circuits, Test generation techniques for combinational circuits (One-Dimensional Path Sensitization, Boolean Difference, D-Algorithm,)

Teaching-Learning Process	Chalk and Talk / Power Point Presentations.

Module-2

Test generation for Combinational Logic circuits: Test generation techniques for combinational circuits (PODEM, FAN, Delay Fault Detection), Detection of multiple faults in Combinational logic circuits.
Design of testable sequential circuits: Controllability and Observability, Ad-Hoc design rules for improving testability, design of diagnosable sequential circuits, the scan-path technique for testable sequential circuit design, Boundary Scan.

Teaching-Learning Process	Chalk and Talk / Power Point Presentations.

Module-3

Built-In Self Test: Test pattern generation for BIST, Output response analysis, Circular BIST, BIST Architectures.

Teaching-Learning Process	Chalk and Talk / Power Point Presentations.

Module-4

An Invitation to Design Verification: What is design verification? The basic verification principle, Verification methodology, Simulation-based verification versus formal verification, Limitations of formal verification, A quick overview of Verilog schedulingand execution semantics.
Coding for Verification: Functional correctness, Timing correctness.

Teaching-Learning Process	Chalk and Talk / Power Point Presentations.

Module-5

Simulator Architectures and Operations: The compilers, The simulators, Simulator taxonomy and comparison, Simulator operations and applications.

Teaching-Learning Process	Chalk and Talk / Power Point Presentations.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1) Three Unit Tests each of **20 Marks**
2) Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1) The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2) The question paper will have ten full questions carrying equal marks.

3) Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4) Each full question will have a sub-question covering all the topics under a module.
5) The students will have to answer five full questions, selecting one full question from each module

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Suggested Learning Resources:

Books

1) Lala Parag K, "Digital Circuit Testing and Testability", New York, Academic Press 1997.
2) Abramovici M, Breuer M A, "Digital Systems Testing and Testable Design and Friedman A D", Wiley 1994.
3) William K. Lam, "Hardware Design Verification: Simulation and Formal Method-Based Approaches", Prentice Hall PTR, 2005.
4) Vishwani D Agarwal, "Essential of Electronic Testing for Digital, Memory and Mixed Signal Circuits", Springer 2002

Web links and Video Lectures (e-Resources):

- https://www.youtube.com/watch?v=O5lyBoWR-PA&list=PLx98Qgh5zPjh6oWI73QfQHZAmAiyt8Wkf
- https://www.youtube.com/watch?v=Abld-fSxjNM&list=PLbMVogVj5nJTClnafWQ9FK2nt3cGG8kCF
- https://www.youtube.com/watch?v=MEaMm423t0w&list=PLZjlBaHNchvOFBWBAtAP9exwQgYpKqsO4&index=1
- VTU e-learning Resources.

Skill Development Activities Suggested:

1) Interact with industry (small, medium, and large).
2) Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3) Involve in case studies and field visits/ fieldwork.
4) Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5) Handle advanced instruments to enhance technical talent.
6) Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7) Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc.
Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical – activities which will enhance their skill. The prepared report shall be evaluated for CIE marks.

Course Outcomes

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Analyze the need for fault modeling and testing of digital circuits	L3
CO2	Generate fault lists for digital circuits and compress the tests for efficiency	L2, L3
CO3	Apply boundary scan technique to validate the performance of digital circuits	L3, L4
CO4	Design built-in self tests for complex digital circuits	L3
CO5	Apply the Verification Concepts to Digital Circuits.	L3

Program Outcome of this course

Sl. No.	Description	POs
1)	Independently carry out research /investigation and development work to solve practical problems related to VLSI Design and embedded systems.	PO1
2)	Demonstrate a degree of mastery over the areas of VLSI Design and embedded systems. The mastery should be at a level higher than the requirements in the bachelor's in Electronics & Communication Engineering.	PO3
3)	Apply appropriate methodology and modern engineering/IT tools to meet the international standards in the area of VLSI design and embedded systems.	PO4
4)	Acquire competency in areas of VLSI and Embedded Systems, IC Fabrication, Design, Testing, Verification and Integrate multiple sub-systems to develop System On Chip to optimize its performance and excel in industry sectors related to VLSI / Embedded domain.	PO5
5)	Understand impact of professional engineering solutions in societal and environmental contexts and demonstrate the knowledge for sustainable development.	PO6

Mapping of COS and POs

	PO1	PO2	PO3	PO4	PO5	PO6
CO1			×			
CO2			×	×		
CO3	×			×	×	
CO4	×			×	×	×
CO5			×	×		×

Semester - I

VLSI Design & Embedded Systems Lab-1			
Course Code	22ULVL17	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	1:2:0	SEE Marks	50
Credits	2	Exam Hours	3

Course objectives:

- To study Digital VLSI Design Flow and analyses the performance parameters.
- To learn RTOS programming using C.

PART A
VLSI Design
Experiments to be conducted using suitable CAD tool

Design the following circuit with given specifications, completing the design flow mentioned below:

a. Draw the schematic and verify DC Analysis and Transient Analysis.
b. Draw the Layout and verify the DRC, ERC and Check for LVS.
c. Extract RC Parasitic and back annotate the same and verify the Design.
d. Optimize for Time, Power and Area to the given constraint and verify.

1	Inverter
2	Two input NAND and NOR gates
3	XOR and XNOR gate using Transmission gates
4	Full Adder
5	4:1 multiplexer using pass transistor logic
6	4x4 NOR based ROM array

PART B
RTOS programs using C language in LINUX OS

1	Develop programs to (a) create child process and display its id (b) Execute child process function using switch structure
2	Develop and test program for a multithreaded application, where communication is through a buffer for the conversion of lowercase text to uppercase text, using semaphore concept.
3	Develop and test program for a multithreaded application, where communication is through shared memory for the conversion of lowercase text to uppercase text.
4	Develop program for inter-thread communication using message queue. Data is to be input from the keyboard for the chosen application.
5	Create 'n' number of child threads. Each thread prints the message "I'm in thread number …" and sleeps for 50 ms and then quits. The main thread waits for complete execution of all the child threads and then quits. Compile and execute in Linux.
6	Implement the usage of anonymous pipe with 512 bytes for data sharing between parent and child processes using handle inheritance mechanism.

Course Outcomes

At the end of the course the student will be able to:

- Design, implement and analyse digital VLSI circuits.
- Implement different techniques of message passing and Inter task communication.
- Implement different data structures such as pipes, queues and buffers in multithreaded programming and also select a suitable task switching technique in a multithreaded application.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 40% of maximum marks in the semester-end examination(SEE). In total of CIE and SEE student has to secure 50% maximum marks of the course.

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.

- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of the semester and the second test shall be conducted after the 14th week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of **scaled-down** marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University.

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 10% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours

Suggested Learning Resources:

- https://youtu.be/VdCkrykPy_k
- https://youtu.be/gASfjBP1Mdw