ವಿಶ್ವೇಶ್ವರಯ್ಯ ತಾಂತ್ರಿಕ ವಿಶ್ವವಿದ್ಯಾಲಯ
ವಿಟಿಯು ಅಧಿನಿಯಮ ೧೯೯೪ರ ಅಡಿಯಲ್ಲಿ ಕರ್ನಾಟಕ ಸರ್ಕಾರದಿಂದ ಸ್ಥಾಪಿತವಾದ ರಾಜ್ಯವಿಶ್ವವಿದ್ಯಾಲಯ
**VISVESVARAYA TECHNOLOGICAL UNIVERSITY**
State University of Government of Karnataka Established as per the VTU Act, 1994"JnanaSangama" Belagavi-590018

**Prof. B. E. Rangaswamy**, Ph.D
REGISTRAR

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REF: VTU/BGM/BoS/BCSL404-CE/684/2024-25/ 5522 DATE: 27 JAN 2025

## CIRCULAR

**Subject**: Additional Professional Elective Courses added under 1st semester of ECE stream PG programs regarding.

**Reference**:

1. Chairpersons' approval Dated: 21.01.2025
2. The Hon'ble Vice-Chancellor's approval Dated: 27.01.2025

Madam/Sir

This is with reference to the subject mentioned above. Additional courses/subjects have been incorporated into the **first-semester syllabus** of the **Electronics and Communication Engineering (ECE)** streams' Postgraduate programs to meet the requirements of the **Microelectronics and Control Systems** program. This is also made available @ https://vtu.ac.in/pdf/cbcs/pg/2024/commsysscheme.pdf, https://vtu.ac.in/pdf/cbcs/pg/2024/commsylee1syll.pdf (Serial number 16 Micro Electronics and Control System)

You are requested to bring the contents of this circular to the notice of all concerned stakeholders for their information and necessary action.

**Enclosure:** Details of the updated syllabus.

Sd/-
REGISTRAR

**Copy to,**

- The Hon'ble Vice-Chancellor through the secretary to Vice-Chancellor for information
- Registrar (Evaluation) VTU Belagavi for information and needful
- The Director, ITI SMU, VTU Belagavi for information
- The Principal BLDE College of Engineering Bijapur for needful
- The Special Officer, QPDS Section, VTU Belagavi for information.
- Office copy

27/01/25
REGISTRAR

# VISVESVARAYA TECHNOLOGICAL UNIVERSITY

## BELAGAVI


# Scheme of Teaching and Examinations

## M.Tech. in Electronics and Communication Engineering

## (Specialization in)

Choice Based Credit System (CBCS) and Outcome Based Education (OBE)

| I SEMESTER (Core Courses related to main Engineering Stream) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Sl. No. | Course Type | Course Code | Course Title | Teaching Hours per Week | | | Examination | | | | Credits |
| | | | | Theory | Practical/ Seminar | Tutorial/SDA | Duration in hours | CIE Marks | SEE Marks | Total Marks | |
| | | | | L | P | T/SDA | | | | | |
| 1 | PCC | MEC101 | Advanced Machine Learning and Deep Learning | 3 | 0 | 0 | 03 | 50 | 50 | 100 | 3 |
| 2 | IPCC | MEC102 | Advanced Embedded Systems | 3 | 2 | 0 | 03 | 50 | 50 | 100 | 4 |
| 3 | PCC | MEC103 | Digital Circuits & Logic Design | 3 | 0 | 0 | 03 | 50 | 50 | 100 | 3 |
| 4 | PEC | MEC114 | Professional Elective I | 3 | 0 | 0 | 03 | 50 | 50 | 100 | 3 |
| 5 | PEC | MEC115 | Professional Elective II | 3 | 0 | 0 | 03 | 50 | 50 | 100 | 3 |
| 6 | PECL | MECL116x | Lab Elective | 0 | 4 | 0 | 03 | 50 | 50 | 100 | 2 |
| 7 | NCMC | MRMI107 | Research Methodology and IPR (Online) | Online Courses (online.vtu.ac.in) | | | | | | | PP |
| | | | | | | | | 300 | 300 | 600 | 18 |

| Professional Elective I | | Professional Elective II | |
|---|---|---|---|
| MEC114A | ASIC Design | MEC115A | System Verilog |
| MEC114B | Advanced Computer Networking | MEC115B | Advanced Wireless Communication |
| MEC114C | Advanced Signal Processing | MEC115C | Multimedia & Applications |
| MEC114D | Power Converters | MEC115D | Process Control |
| MEC114E | Digital System Design with FPGA | MEC115E | Real Time Operating Systems |
| **Lab Elective** | | | |
| MECL116A | Advanced Machine Learning and Deep Learning Lab | MECL116B | Electronics and Communication Lab |
| | | | |

Note: **BSC**-Basic Science Courses, **PCC**: Professional core. **IPCC**-Integrated Professional Core Courses, **PCC(PB):** Professional Core Courses (Project Based), **PCCL**-Professional Core Course lab, **NCMC**- None Credit Mandatory Course, **L**-Lecture, **P**-Practical, **T/SDA**-Tutorial / Skill Development Activities(Hours are for Interaction between faculty and students) **MRMI107** - Research Methodology and IPR (**Online**) for the students who have **not studied** this course in the Undergraduate level. This course is not counted for vertical progression, Students have to qualify for the award of the master's degree.

**M**- Master program **xx** – **ME** for Mechanical Engineering Stream, **CV** for Civil Engineering Stream, **EE** – Electrical & Electronics Engineering Stream, **EC**- Electronics and Communication Engineering Stream, **CS**- Computer Science and Engineering, **BA**-Business Administration **AR**- Architecture- etc.

**BSC: Basic Science Courses:** Courses like Mathematics/ Science are the prerequisite courses that the concerned engineering stream board of Studies will decide. **PCC: Professional Core Course:** Courses related to the stream of engineering, which will

**Semester- 1**

| Digital System Design with FPGA | | | |
|---|---|---|---|
| Course Code | **MEC114E** | CIE Marks | 50 |
| Teaching Hours/Week (L:P:SDA) | 3:0:0 | SEE Marks | 50 |
| Total Hours of Pedagogy | 40 | Total Marks | 100 |
| Credits | 03 | Exam Hours | 03 |

**Course Learning objectives:**

- To learn about electronic Circuits, Programmable Logic versus Discrete Logic, Types , Methods and Tools, Technology Trends.
- To learn about Software Programming Languages, Hardware Description Languages, SPICE, System C R , System Verilog, Mathematical Modelling Tools.
- To learn about designing with HDLs, Design Entry Methods, Logic Synthesis. Entities, Architectures, Packages, and Configurations, Sequential Logic Design, Memories Unsigned versus Signed Arithmetic.
- To learn about Integrated Circuit Testing, Printed Circuit Board Testing, Boundary Scan Testing, Software Testing, Digital-to-Analogue Conversion, Analogue-to-Digital Conversion, Power Electronics, Heat Dissipation and Heat sinks. Operational Amplifier Circuits.

**Module-1**

**Programmable Logic:** Introduction, Electronic Circuits: Analogue and Digital, Programmable Logic versus Discrete Logic, Programmable Logic versus Processors, Types of Programmable Logic, PLD Configuration Technologies, Programmable Logic Vendors, Programmable Logic Design Methods and Tools, Technology Trends.
**Design Languages:** Introduction, Software Programming Languages, Hardware Description Languages, SPICE, System C R, System Verilog, Mathematical Modelling Tools.

**RBT Levels:** L3

**Module-2**

**Electronic Systems Design:** Introduction, Sequential Product Development Process versus Concurrent Engineering Process, Flowcharts, Block Diagrams, Gajski-Kuhn Chart, Hardware-Software Co-Design, Formal Verification, Embedded Systems and Real-Time Operating Systems, Electronic System-Level Design, Creating a Design Specification, Unified Modelling Language, Reading a Component Data Sheet, Digital Input/Output, Parallel and Serial Interfacing, System Reset, System Clock, Power Supplies, Power Management, Printed Circuit Boards and Multichip Modules, System on a Chip and System in a Package, Mechatronic Systems.

**RBT Levels:** L3

**Module-3**

**Introduction to Digital Logic Design with VHDL:** Introduction, Designing with HDLs, Design Entry Methods, Logic Synthesis. Entities, Architectures, Packages, and Configurations, A First Design, Signals versus Variables, Generics, Reserved Words, Data Types, Concurrent versus Sequential Statements, Loops and Program Control, Coding Styles for VHDL, Combinational Logic Design

**RBT Levels:** L3, L4

**Module-4**

**Introduction to Digital Logic Design with VHDL (continued):** Sequential Logic Design, Memories Unsigned versus Signed Arithmetic - Adder Example. Multiplier Example.
**Testing the Design:** Introduction, Integrated Circuit Testing, Printed Circuit Board Testing, Boundary Scan Testing, Software Testing.

**RBT Levels:** L3

**Module-5**

**Digital-to-Analogue Conversion, and Power Electronics:** Introduction, Digital-to-Analogue Conversion, Analogueto-Digital Conversion, Power Electronics, Heat Dissipation and Heat sinks. Operational Amplifier Circuits. System-Level Design: Introduction, Case Study-DC Motor Control.

**RBT Levels:** L3

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous Internal Evaluation:**

3. Two Unit Tests each of **25 Marks**
4. Two assignments each of **25 Marks** or **one Skill Development Activity of 50 marks** to attain the COs and Pos.

The sum of two tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

**CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester-End Examination:**

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module.

**Suggested Learning Resources:**

**Books**

1. Digital Systems Design with FPGAs and CPLDs, Ian Grout, Elsevier, 2008..

**Web links and Video Lectures (e-Resources):**

- https://nptel.ac.in/

**Course outcome (Course Skill Set)**

At the end of the course the student will be able to :

| Sl. No. | Description | Blooms Level |
|---|---|---|
| CO1 | Discuss programmable logic devices that are available today, their architectures, their use within electronic system design and the terminology used. | L3 |
| CO2 | Discuss different programming languages that are used to develop digital designs for implementation in either a processor or in programmable logic. | L3 |
| CO3 | Explain designing of electronic systems, the types of solutions that can be developed, and the decisions that will need to be made in order to identify the right technology choice for the design implementation. | L3, L4 |
| CO4 | Describe digital circuit and system designs in an ASCII text-based format using VHDL.Test the electronic systems for failure mechanisms in hardware and software. Interface programmable logic devices to the analogue world. | L3 |
| CO5 | Explain with a case study the necessity to develop programmable logic–based designs at a high level of abstraction using behavioral descriptions of the system functionality | L3 |

**Semester- I**

| Real Time Operating Systems | | | |
|---|---|---|---|
| Course Code | **MEC115E** | CIE Marks | 50 |
| Teaching Hours/Week (L:P:SDA) | 3:0:0 | SEE Marks | 50 |
| Total Hours of Pedagogy | 40 | Total Marks | 100 |
| Credits | 03 | Exam Hours | 03 |

**Course Learning objectives:**

- To learn about Elements of a Computer Control System, RTS- Definition, Classification of Realtime Systems, Time Constraints, Sequence Control, Loop Control, Supervisory Control.
- To learn about Introduction, Syntax Layout and Readability, Declaration and Initialization of Variables and Constants, Cutlass, Modularity and Variables, Data types, Control Structures.
- To learn about Real-Time Multi-Tasking OS, Scheduling Strategies, Priority Structures, Task Management, Scheduler and Real-Time Clock Interrupt Handler

**Module-1**

**Introduction to Real-Time Systems:** Historical background, Elements of a Computer Control System, RTS-Definition, Classification of Real-time Systems, Time Constraints, Classification of Programs.
**Concepts of Computer Control:** Introduction, Sequence Control, Loop Control, Supervisory Control, Centralized Computer Control, Hierarchical Systems.

**RBT Levels:** L2

**Module-2**

**Computer Hardware Requirements for Real-Time Applications:** Introduction, General Purpose Computer, Single Chip Microcomputers and Microcontrollers, Specialized Processors, Process-Related Interfaces, Data Transfer Techniques, Communications, Standard Interface.

**RBT Levels:** L2, L3

**Module-3**

**Languages for Real-Time Applications:** Introduction, Syntax Layout and Readability, Declaration and Initialization of Variables and Constants, Cutlass, Modularity and Variables, Compilation of Modular Programs, Data types, Control Structures, Exception Handling, Low-level facilities, Co-routines, Interrupts and Device Handling, Concurrency, Real-Time Support, Overview of Real-Time Languages.

**RBT Levels:** L2, L3

**Module-4**

**Operating Systems:** Introduction, Real-Time Multi-Tasking OS, Scheduling Strategies, Priority Structures, Task Management, Scheduler and Real-Time Clock Interrupt Handler, Memory Management, Code Sharing, Resource Control, Task Co-Operation and Communication, Mutual Exclusion.

**RBT Levels:** L3, L4

**Module-5**

**Design of RTS- General Introduction:** Introduction, Specification Document, Preliminary Design. Single-Program Approach, Foreground/Background System. RTS Development Methodologies: Introduction, Yow-don Methodology, Ward and Mellor Method, Hately and Pirbhai Method.

**RBT Levels:** L3, L4

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

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**CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester-End Examination:**

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.

**Suggested Learning Resources:**

**Books**

1. Real-Time Computer Control, Stuart Bennet, 2nd Edn. Pearson Education. 2008

**Reference Books**

1. "Real-Time Systems", C.M. Krishna, Kang G Shin, McGraw-Hill International Editions, 1997.
2. Real-Time Systems Design and Analysis, Phillip. A. Laplante, second edition, PHI, 2005.
3. Embedded Systems, Raj Kamal, Tata McGraw Hill, India, third edition, 2005.

**Web links and Video Lectures (e-Resources):**

- https://nptel.ac.in/

**Course outcome (Course Skill Set)**

At the end of the course the student will be able to :

| Sl. No. | Description | Blooms Level |
|---|---|---|
| CO1 | Explain the fundamentals of Real time systems and its classifications. | L2, L3 |
| CO2 | Understand the concepts of computer control and the suitable computer hardware requirements for real-time applications. | L2 |
| CO3 | Describe the operating system concepts and techniques required for real time systems. | L3 |
| CO4 | Develop the software algorithms using suitable languages to meet Real time applications. | L2, L3, L4 |
| CO5 | Apply suitable methodologies to design and develop Real-Time Systems.. | L3 |