Semester- 1

Digital System Design with FPGA			
Course Code	**MEC114E**	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives:

- To learn about electronic Circuits, Programmable Logic versus Discrete Logic, Types , Methods and Tools, Technology Trends.
- To learn about Software Programming Languages, Hardware Description Languages, SPICE, System C R , System Verilog, Mathematical Modelling Tools.
- To learn about designing with HDLs, Design Entry Methods, Logic Synthesis. Entities, Architectures, Packages, and Configurations, Sequential Logic Design, Memories Unsigned versus Signed Arithmetic.
- To learn about Integrated Circuit Testing, Printed Circuit Board Testing, Boundary Scan Testing, Software Testing, Digital-to-Analogue Conversion, Analogue-to-Digital Conversion, Power Electronics, Heat Dissipation and Heat sinks. Operational Amplifier Circuits.

Module-1

Programmable Logic: Introduction, Electronic Circuits: Analogue and Digital, Programmable Logic versus Discrete Logic, Programmable Logic versus Processors, Types of Programmable Logic, PLD Configuration Technologies, Programmable Logic Vendors, Programmable Logic Design Methods and Tools, Technology Trends.
Design Languages: Introduction, Software Programming Languages, Hardware Description Languages, SPICE, System C R, System Verilog, Mathematical Modelling Tools.

RBT Levels: L3

Module-2

Electronic Systems Design: Introduction, Sequential Product Development Process versus Concurrent Engineering Process, Flowcharts, Block Diagrams, Gajski-Kuhn Chart, Hardware-Software Co-Design, Formal Verification, Embedded Systems and Real-Time Operating Systems, Electronic System-Level Design, Creating a Design Specification, Unified Modelling Language, Reading a Component Data Sheet, Digital Input/Output, Parallel and Serial Interfacing, System Reset, System Clock, Power Supplies, Power Management, Printed Circuit Boards and Multichip Modules, System on a Chip and System in a Package, Mechatronic Systems.

RBT Levels: L3

Module-3

Introduction to Digital Logic Design with VHDL: Introduction, Designing with HDLs, Design Entry Methods, Logic Synthesis. Entities, Architectures, Packages, and Configurations, A First Design, Signals versus Variables, Generics, Reserved Words, Data Types, Concurrent versus Sequential Statements, Loops and Program Control, Coding Styles for VHDL, Combinational Logic Design

RBT Levels: L3, L4

Module-4

Introduction to Digital Logic Design with VHDL (continued): Sequential Logic Design, Memories Unsigned versus Signed Arithmetic - Adder Example. Multiplier Example.
Testing the Design: Introduction, Integrated Circuit Testing, Printed Circuit Board Testing, Boundary Scan Testing, Software Testing.

RBT Levels: L3

Module-5

Digital-to-Analogue Conversion, and Power Electronics: Introduction, Digital-to-Analogue Conversion, Analogueto-Digital Conversion, Power Electronics, Heat Dissipation and Heat sinks. Operational Amplifier Circuits. System-Level Design: Introduction, Case Study-DC Motor Control.

RBT Levels: L3

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

3. Two Unit Tests each of **25 Marks**
4. Two assignments each of **25 Marks** or **one Skill Development Activity of 50 marks** to attain the COs and Pos.

The sum of two tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module.

Suggested Learning Resources:

Books

1. Digital Systems Design with FPGAs and CPLDs, Ian Grout, Elsevier, 2008..

Web links and Video Lectures (e-Resources):

- https://nptel.ac.in/

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Discuss programmable logic devices that are available today, their architectures, their use within electronic system design and the terminology used.	L3
CO2	Discuss different programming languages that are used to develop digital designs for implementation in either a processor or in programmable logic.	L3
CO3	Explain designing of electronic systems, the types of solutions that can be developed, and the decisions that will need to be made in order to identify the right technology choice for the design implementation.	L3, L4
CO4	Describe digital circuit and system designs in an ASCII text-based format using VHDL.Test the electronic systems for failure mechanisms in hardware and software. Interface programmable logic devices to the analogue world.	L3
CO5	Explain with a case study the necessity to develop programmable logic–based designs at a high level of abstraction using behavioral descriptions of the system functionality	L3