Semester- I

ADVANCED MACHINE LEARNING AND DEEP LEARNING			
Course Code	**MEC101**	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives:

- To understand the fundamental concepts of machine learning and its applications
- To master the concepts of classification and clustering techniques.
- To develop a deep understanding of convolutional neural networks (CNNs) and their architecture.
- To apply deep learning techniques to large-scale datasets and real-world problems.

Module-1

Introduction to Machine Learning: Introduction, Training, Rote Learning, Learning Concepts, General-to-Specific Ordering, Version Spaces, Candidate Elimination, Inductive Bias, Decision-Tree Induction, The Problem of Overfitting, The Nearest Neighbor Algorithm, Learning Neural Networks, Supervised Learning, Unsupervised Learning, Reinforcement Learning.

RBT Levels: L2, L3

Module-2

Neural Networks: Introduction, Neurons, Perceptrons, Multilayer Neural Networks, Recurrent Networks, Unsupervised Learning Networks, Evolving Neural Networks.

RBT Levels: L3

Module-3

Convolutional Neural Networks: The operation, Pooling, Convolution and Pooling as an infinitely strong prior, Variants of the basic functions, efficient algorithms, Random or Unsupervised Features, Neuroscientific Basis for Convolutional Networks.

RBT Levels: L3

Module-4

Recurrent Neural Networks: RNN, Bidirectional RNN, Encoder-Decoder Sequence to sequence architecture, Deep Recurrent Networks, Recursive Neural Networks, The Long Short Term Memory and other Gated RNNs, Optimization for Long Term Dependencies.

RBT Levels: L3

Module-5

Applications: Large-Scale Deep Learning, Computer Vision, Speech Recognition, Natural Language Processing, Other Applications.

RBT Levels: L3, L4

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Two Unit Tests each of **25 Marks**
2. Two assignments each of **25 Marks** or **one Skill Development Activity of 50 marks** to attain the COs and POs

The sum of two tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.

4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Books

1. Artificial Intelligence Illuminated - Ben Coppin
2. Deep Learning - Ian Goodfellow, Yoshua Bengio, Aaron Courville
3. Fundamentals of Deep Learning – Nikhil Budama
4. Neural Networks and Deep Learning – Charu Aggarwal
5. Hands-on Deep Learning Algorithms with Python – Sudharsan Ravichandran

Web links and Video Lectures (e-Resources):

- https://nptel.ac.in/

Skill Development Activities Suggested

- Individual or group projects to apply learned concepts to real-world problems.
- Regular coding assignments to reinforce theoretical concepts.
- Experimentation with different libraries and frameworks (e.g., TensorFlow, PyTorch, Scikit-learn).
- Guest lectures from industry experts to provide insights into current trends.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	**Demonstrate** a comprehensive understanding of machine learning and deep learning fundamentals and their applications.	L2
CO2	**Apply** various machine learning algorithms and deep learning architectures to solve complex problems.	L3
CO3	**Develop** and implement machine learning models using appropriate programming languages and tools.	L4

Semester- I

ADVANCED EMBEDDED SYSTEMS			
Course Code	**MEC102**	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:2:0	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory +10 hours Lab	Total Marks	100
Credits	04	Exam Hours	03

Course Learning Objectives:

1. To understand the difference between Embedded Systems and General Computing Systems
2. To understand the Classification of Embedded Systems based on Performance, Complexity along with the Domains and Areas of Applications of Embedded Systems
3. Analysis of a Real Life example on the bonding of Embedded Technology with Human Life
4. To understand the difference between Microcontrollers and ARM Cortex processors.
5. To learn Programming using assembly and C language, CMSIS for variety of End Applications.

Module - 1

Embedded System: Embedded v/s General Computing System, classification, application and purpose ofES. Core of an Embedded System, Memory, Sensors, Actuators, LED, Optocoupler, Communication Interface, Reset circuits, RTC, WDT, Characteristics and Quality Attributes of Embedded Systems.

RBT Levels: L2, L3

Module - 2

Hardware Software Co-Design: Embedded firmware design approaches, computational models, embeddedfirmware development languages, Integration and testing of Embedded Hardware and firmware, Components inembedded system development environment(IDE),Files generated during compilation, simulators, emulators and debugging.

RBT Levels: L3

Module - 3

ARM - 32 bit Microcontroller: Thumb-2 technology and applications of ARM, Architecture of ARM Cortex M3, Various Units in the architecture, General Purpose Registers, Special Registers, exceptions, interrupts, stack operation, reset sequence.

RBT Levels: L3

Module - 4

Instruction Sets: Assembly basics, Instruction list and description, useful instructions,MemorySystems, Memory maps, Cortex M3 implementation overview, pipeline and bus interface, Exceptions, Nested Vector interrupt controller design, Systick Timer, Cortex- M3 Programming using assembly and C language, CMSIS.

RBT Levels: L3

Module - 5

Introduction to RISC - V: Operations of the Computer Hardware, Operands of the Computer Hardware, Signed and Unsigned Numbers, Representing Instructions in the Computer, Logical Operations, Instructions for Making Decisions, RISC-V Addressing for Wide Immediate and Addresses, Parallelism and Instructions: Synchronization

RBT Levels: L3, L4

PRACTICAL COMPONENT OF IPCC Using suitable simulation software in Linux Develop and test Assembly Language Program (ALP) using ARM/RISC Processor.	
1.	Develop and test programs: a) To create child process and display it's ID. b) Execute child process function using switch structure.
2.	Develop and test the program for a multi-threaded application, where communication is through shared memory for the conversion of lowercase text touppercase text.
3.	Develop program for inter-thread communication using message queue. Data is to be input from the keyboard for the chosen application.
4.	Create 'n' number of child threads. Each thread prints the message "I'm in thread number …" and sleeps for 50 ms and then quits. The main thread waits for complete execution of all the child threads and then quits. Compile and execute in Linux.
5.	Implement the multi-thread application satisfying the following: a) Two child threads are created with normal priority. b) Thread 1 receives and prints its priority and sleeps for 50ms and then quits. c) Thread 2 prints the priority of the thread 1 and rises its priority to above normal and retrieves the new priority of thread 1, prints it and then quits. d) The main thread waits for the child thread to complete its job and quits.
6.	Write ALP to find the square of a number (1 to 10) using look-up table.
7.	Write an ALP to arrange a series of 32 bit numbers in ascending/descending order.
8.	Write an ALP to count the number of ones and zeros in two consecutive memory locations.
9.	Interface a simple Switch and display its status through Relay, Buzzer and LED. (Study Expt.)
10.	Implement a clock capable of displaying (and being set to the correct time). Include an alarm facility which can be set by the user and will 'go off' at the correct time.

Assessment Details (both CIE and SEE):

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester EndExam (SEE) is 50%. Theminimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks inSEE is 40% of themaximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than50% (50 marks out of 100) in the sum total oftheCIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

CIE for the theory component ofIPCC

1. Two Tests each of 20 Marks
2. Two assignments each of 10 Marks / One Skill Development Activity of 20 Marks
3. Total Marks of two tests and two assignments / One Skill Development Activity added will be CIE for 60 Marks, marks scored will be proportionally scaled down to 30 Marks.

CIE for the practical component of IPCC

1. On completion of every experiment / program in the laboratory, the students shall be evaluated and marks shall be awarded on the same day. The 15 Marks are for conducting the experiment and preparation of the laboratory record, the other 05 Marks shall be for the test conducted at the end of the semester.
2. The CIE marks awarded in the case of the Practical component shall be based on the continuousevaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments'write-ups are added and scaled down to15 marks.
3. The laboratory test at the end /after completion of all the experimentsshall be conducted for 50 Marks and scaled down to 05 Marks.

Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for 20marks.

SEEfor IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (duration 03hours)

1. The question paper will be set for 100 marks and marks scored will be scaled downproportionately to 50marks.
2. The question paper will have ten questions. Each question isset for 20marks.
3. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), should have a mixof topics under that module.
4. The students have toanswer 5 full questions, selecting one full question from each module.

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper shall include questions fromthe practical component.

1. The minimum marks to be secured in CIE to appear for SEE shall be the 15 (50% of maximum marks-30) in the theory component and 10 (50% of maximum marks -20) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included. The maximum of 04/05 questions to be set from the practical component of IPCC, the total marks of all questions should not be more than the 20marks.

2. SEE will beconducted for 100marks and students shall secure 40% ofthe maximum marks toqualify in the SEE. Marks secured will be scaled down to 50. (Student has to secure an aggregate of50% of maximum marks ofthe course(CIE+SEE)

Suggested Learning Resources:

Text Books

1. 'Introduction toembedded systems', K. V.Shibu, TMH education Pvt.Ltd., 2009.
2. 'The Definitive Guide tothe ARM Cortex-M3', Joseph Yiu, Newnes,(Elsevier), 2nd edn, 2010.
3. 'Computer Organization and Design RISC-V Edition', David A. Patterson, John L. Hennessy, Morgan Kaufmann, ISBN: 9780128122761.

Reference Books

1. 'Embedded systems - A contemporary design tool', James K.Peckol, JohnWiley, 2008

Web links and Video Lectures (e-Resources):

https://nptel.ac.in/

Skill Development Activities Suggested

1. Interact with industry (small, medium, and large).
2. Involve in research / testing / projects to understand their problems and help creative and innovative methods tosolve the problem.
3. Involve incase studies and field visits/ fieldwork.
4. Accustom tothe use ofstandards/codes etc., tonarrow the gap between academia and industry.
5. Handle advanced instruments toenhance technical talent.
6. Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7. Work ondifferent software/s (tools) tosimulate, analyze and authenticate the output tointerpret and conclude.

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

Sl. No	Course Outcomes	Blooms Level
CO 1	Understand the basic hardware components and their selection methods based onthe attributes ofEmbedded Systems	L2
CO 2	Describe the code design process and firmware design approaches	L2
CO 3	Acquaint the knowledge ofARM Cortex M3Processor anditssalient features.	L3
CO 4	Understand the basics of RISC – V Architecture.	L3
CO 5	Apply and use Programming Techniques for different End Uses	L3, L4

Semester- I

DIGITAL CIRCUITS & LOGIC DESIGN			
Course Code	**MEC103**	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives:

- Understand the concepts of sequential machines
- Design Sequential Machines/Circuits
- Analyze the faults in the design of circuits
- Apply fault detection experiments to sequential circuits

Module-1

Threshold Logic: Introductory Concepts, Synthesis of Threshold Networks

Capabilities, Minimization, and Transformation of Sequential Machines: The Finite- State Model, Further Definitions, Capabilities.

RBT Levels: L2, L3

Module-2

Fault detection by path sensitizing: Detection of multiple faults, Failure-Tolerant Design, Quadded Logic, Reliable Design and Fault Diagnosis Hazards: Fault Detection in Combinational Circuits.

RBT Levels: L3

Module-3

Fault-location experiments: Boolean Differences, Limitations of Finite – State Machines, State Equivalence and Machine Minimization, Simplification of Incompletely Specified Machines.

RBT Levels: L3

Module-4

Structure of Sequential Machines: Introductory Example, State Assignments Using Partitions, The Lattice of closed Partitions, Reductions of the Output Dependency, Input Independence and Autonomous Clocks, Covers and Generation of closed Partitions by state splitting, Information Flow in Sequential Machines, decompositions, Synthesis of Multiple Machines.

RBT Levels: L3

Module-5

State Identifications and Fault-Detection Experiments:

Homing Experiments, Distinguishing Experiments, Machine Identification, Fault Detection Experiments, Design of Diagnosable Machines, Second Algorithm for the Design of Fault Detection Experiments, Fault-Detection.

RBT Levels: L3, L4

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Two Unit Tests each of **25 Marks**
2. Two assignments each of **25 Marks** or **one Skill Development Activity of 50 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.

Suggested Learning Resources:

Textbook:

1. 'Switching and Finite Automata Theory', Zvi Kohavi, TMH, ISBN: 978_0_07_099387_7, 2nd Edition, 2008.

Reference Books:

1. 'Digital Circuits and logic Design', Charles Roth Jr., Cengage Learning, 7thedition, 2014.
2. 'Fault Tolerant and Fault Testable Hardware Design', Parag K Lala, Prentice Hall Inc. 1985.
3. 'Introductory Theory of Computer', E. V. Krishnamurthy, Macmillan Press Ltd, 1983
4. 'Theory of computer science – Automata, Languages and Computation', Mishra & Chandrasekaran, 2ndEdition, PHI, 2004.

Web links and Video Lectures (e-Resources):

https://nptel.ac.in/

Skill development activities: Under Skill development activities in a concerning course, the students should

1. Interact with industry (small, medium, and large).
2. Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3. Involve in case studies and field visits/ fieldwork.
4. Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5. Handle advanced instruments to enhance technical talent.
6. Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

CO	Description	Blooms Level
CO1	Able to understand the concepts of sequential machines.	L2
CO2	Able to understand the Sequential Machines/Circuits.	L2
CO3	Able to understand the structure of sequential machines.	L2
CO4	Able to analyse the faults in the design of circuits.	L3, L4
CO5	Able to analyse fault detection experiments to sequential circuits.	L3, L4

Semester- I

ASIC DESIGN			
Course Code	**MEC114A**	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	3

Course Learning objectives:

- To learn ASIC methodologies and programmable logic cells to implement a function on IC.
- To Analyse back-end physical design flow, including partitioning, floor-planning, placement, and routing.
- To Gain sufficient theoretical knowledge for carrying out FPGA and ASIC designs

Module-1

Introduction to ASICs: Full custom, Semi-custom and Programmable ASICs, ASIC Design flow, ASIC cell libraries. **CMOS Logic**: Data path Logic Cells: Data Path Elements, Adders: Carry skip, Carry bypass, Carry save, Carryselect, Conditional sum, Multiplier (Booth encoding), Data path Operators, I/O cells, Cell Compilers.

RBT Levels: L2

Module-2

ASIC Library Design: Logical effort: Predicting Delay, Logical area and logical efficiency, Logical paths, Multi-stage cells, Optimum delay and number of stages, library cell design.

Programmable ASIC Logic Cells: MUX as Boolean function generators, Acted ACT: ACT 1, ACT 2 and ACT 3 Logic Modules, Xilinx LCA:XC3000 CLB, Altera FLEX and MAX, Programmable ASIC I/O Cells: Xilinx and Altera I/O Block

RBT Levels: L2, L3

Module-3

Low-level design entry: Schematic entry: Hierarchical design, The cell library, Names, Schematic Icons & Symbols, Nets, Schematic Entry for ASICs, Connections, vectored instances & buses, Edit in place, attributes, Netlist screener.

ASIC Construction: Physical Design, CAD Tools System partitioning, Estimating ASIC size. **Partitioning:** Goals and objectives, Constructive Partitioning, Iterative Partitioning Improvement, KL, FM and Look Ahead algorithms.

RBT Levels: L2, L3

Module-4

Floor planning and placement: Goals and objectives, Measurement of delay in Floor planning, Floor planning tools, Channel definition, I/O and Power planning and Clock planning.

Placement: Goals and Objectives, Min-cut Placement algorithm, Iterative Placement Improvement, Time driven placement methods, Physical Design Flow.

RBT Levels: L2, L3

Module-5

Routing: Global Routing - Goals and objectives, Global Routing Methods, Global routing between blocks, Back-annotation. Detailed Routing - Goals and objectives, Measurement of Channel Density, Left-Edge Algorithm, Area-Routing Algorithms, Multilevel routing, Timing –Driven detailed routing, Final routing steps, Special Routing, Circuit extraction and DRC.

RBT Levels: L3, L4

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Two Unit Tests each of **25 Marks**
2. Two assignments each of **25 Marks**or **oneSkill Development Activity of 50 marks** to attain the COs and POs

The sum of two tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.

Suggested Learning Resources:

Books

1. Michael John Sebastian Smith, "Application - Specific Integrated Circuits", Addison- Wesley Professional, 2005
2. Neil H.E. Weste, David Harris, and Ayan Banerjee, "CMOS VLSI Design: A Circuits and Systems Perspective" , Addison Wesley/ Pearson education 3rdedition, 2011
3. Vikram Arkalgud Chandrasetty, "VLSI Design: A Practical Guide for FPGA and ASIC Implementations" Springer, ISBN: 978-1-4614-1119-2. 2011
4. Rakesh Chadha, Bhasker J, "An ASIC Low Power Primer", Springer, ISBN: 978-14614-4270-7.
5. Peter J. Ashenden Digital Design (Verilog): An Embedded Systems Approach Using Verilog,1st Edition, Kindle Edition.

Web links and Video Lectures (e-Resources):

- https://nptel.ac.in/

Skill Development Activities Suggested

- Activity Based Learning (Suggested Activities in Class)/ Practical Based learning
- Real world Problem Solving: Applying the ASIC front end and backend concepts.

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

Sl. No.	Description	Blooms Level
CO1	Describe the concepts of ASIC design methodology, data path elements, logical effort.	L2
CO2	Analyze the design of ASICs suitable for specific tasks, perform design entry and explain the physical design flow.	L3
CO3	Design data path elements for ASIC cell libraries and compute optimum path delay.	L3
CO4	Create floor plan including partition and routing with the use of CAD algorithms	L3,L4
CO5	Design CAD algorithms and explain how these concepts interact in ASIC design.	L3,L4

Semester 1

ADVANCED COMPUTER NETWORKING			
Course Code	**MEC114B**	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3

Course Learning objectives: This Course will enable students to

- Focus on advanced networking concepts for next generation network architecture and design.
- Acquire knowledge about SDN and virtualization for designing next generation networks.

Module-1

Medium Access Control Sub Layer: Wireless LANs, Broadband Wireless, Bluetooth, RFID.
The Network Layer: Network Layer Design Issues, Congestion Control Algorithms, Quality of Service, The Network Layer in the Internet.

RBT Levels: L2

Module-2

The Application Layer: The Domain Name System, Electronic Mail, The World Wide Web.

RBT Levels: L2, L3

Module-3

Software Defined Network (SDN): Evolution of Switches and Control Planes, Cost, SDN Implications for Research and Innovation
Genesis of SDN: The Evolution of Networking Technology, Forerunners of SDN, Software Defined Networking is Born, Sustaining SDN Interoperability, Open Source Contributions, Network Virtualization
How SDN Works: Fundamental Characteristics of SDN, SDN Operation, SDN Devices, SDN Controller, SDN Applications, Alternate SDN Methods

RBT Levels: L2, L3

Module-4

The Openflow Specification: OpenFlow Overview, OpenFlow 1.0 and OpenFlow Basics, OpenFlow Additions - 1.1, 1.2, 1.3, 1.4, 1.5, Improving OpenFlow Interoperability, Optical Transport Protocol Extensions, OpenFlow Limitations

RBT Levels: L2, L3

Module-5

Network Functions Virtualization: Definition of NFV, Virtualize, Standards, OPNFV, Leading NFV Vendors, SDN Vs NFV, In-Line Network Functions.
SDN Open Source: SDN Open Source Landscape, The OpenFlow Open Source Environment, Profiles of SDN Open Source Users, OpenFlow Source Code, Switch Implementations, Controller Implementations, SDN Applications, Orchestration and Network Virtualization, Simulation, Testing and Tools, Open Source Cloud Software, Example: Applying SDN Open Source.

RBT Levels: L3, L4

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Two Unit Tests each of **25 Marks**
2. Two assignments each of **25 Marks** or **one Skill Development Activity of 50 marks** to attain the COs and Pos.

The sum of two tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module.

Suggested Learning Resources:

Text Books:

1. Andrew S. Tanenbaum, David J. Wetherall, Computer Network, 5th Edition. Pearson Education.
2. Paul Goransson, Chuck Black and Timothy Culver, Software Defined Networks – A Comprehensive Approach, 2nd Edition, 2017, Morgan Kaufmann.

Reference books:

1. Behrouz A. Forouzan, Data Communications and Networking, Fourth Edition, Tata McGraw Hill, 2007.
2. James F Kurose, Keith W Ross, Computer Networking- A Top-down Approach Featuring the Internet, 7th Edition, 2017, Pearson Education.
3. Alberto Leon Garcia, Indra Widjaja, Communication Networks-Fundamental Concepts and Key Architectures, Fifth reprint 2002 , Tata McGraw Hill.

Web links and Video Lectures (e-Resources):

- https://nptel.ac.in/

Skill Development Activities Suggested

- The students with the help of the course teacher can take up relevant technical – activities which will enhance their skill.

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

Sl. No.	Description	Blooms Level
CO1	Understand advanced concepts and next generation networks.	L2
CO2	Analyze network Algorithms, Protocols and their functionalities.	L3
CO3	Comprehend features of SDN and its application to next generation systems.	L3
CO4	Analyze the performance of various server implementations.	L3, L4

Semester- 1

ADVANCED SIGNAL PROCESSING			
Course Code	**MEC114C**	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives:

- To know the analysis of discrete time signals.
- To study the modern digital signal processing algorithms and applications.
- To Have an in-depth knowledge of use of digital systems in real time applications
- To apply the algorithms for wide area of recent applications.

Module-1

Analysis of Discrete Time Signals: Basic elements of a DSP System – Review of Sampling and Quantisation – Sampling theorem for low pass and band pass signals, uniform and non-uniform quantization, Application of quantisation in lossy compression of signals – Lloyd Max quantizer; Fourier analysis of Continuous and Discrete time signals –Review of Fourier series and Fourier transform, Discrete Time Fourier Transform (DTFT), Discrete Fourier Transform (DFT), Interpretation of DFT Spectrum, Review of DFT properties – Convolution and correlation, Convolution of long sequences, Leakage effect, Windowing – Introduction to other transforms : Discrete Cosine Transform (DCT), Walsh Hadamard Transform (WHT), Karhunen Loeve Transform (KLT) – Applications.

RBT Levels: L2, L3

Module-2

Digital Filters and Implementation: Review of FIR and IIR filter design – Notch filter– Comb filter– All pass filters – Applications – Structures for digital filter realization: Signal flow graph and block diagram representations, FIR and IIR Filter structures, Lattice structures – Finite word length effects – Fixed-point and floating-point DSP arithmetic, Effects of quantization, Scaling, Limit cycles in fixed point realizations of IIR digital filters, Limit cycles due to overflow. Quantization effect in DFT and FFT computation.

RBT Levels: L3, L4

Module-3

Multirate Signals and Systems: Introduction to multirate signal processing with applications, Multirate System Fundamentals – Decimation and Interpolation, Transform domain analysis of Decimators and Interpolators, Decimation and Interpolation filters, Fractional sampling rate alteration, Practical sampling rate converter design.

RBT Levels: L3, L4

Module-4

Introduction to 2-D Signals and Systems: Polyphase decomposition and efficient structures – Introduction to digital filter banks – The DFT filter bank, Two Channel Quadrature Mirror Filter bank (QMF), Perfect Reconstruction.

RBT Levels: L3, L4

Module-5

Introduction to 2-D Signals and Systems: Elementary 2D signals – Linear shift Invariant systems – Separability – 2D convolution – Introduction to 2D transforms: 2D DFT, 2D DCT, Applications.

RBT Levels: L3, L4

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Two Unit Tests each of **25 Marks**
2. Two assignments each of **25 Marks** or **one Skill Development Activity of 50 marks** to attain the COs and POs

The sum of two tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module.

Suggested Learning Resources:

Books

1. John G. Proakis, Dimitris G. Manolakis, Digital Signal Processing: Principles, Algorithms and Applications, 4th Edition, Pearson India, 2007.
2. P.P. Vaidyanathan, Multirate systems and filter banks, 2nd Edition, Pearson Education India, 1992.
3. Lim J. S., Two-dimensional signal and image processing, Prentice Hall, 1990.
4. K Deergha Rao, M N S Swamy, Digital Signal Processing: Theory and Practice, Springer, 2018.
5. Steven W. Smith, The Scientist and Engineer's Guide to Digital Signal Processing, California, 1999.
6. Mitra S. K., Digital Signal Processing: A Computer Based Approach, McGraw-Hill Publishing Company, 2013

Web links and Video Lectures (e-Resources):

- https://nptel.ac.in/

Skill Development Activities Suggested

- Mini Project in the area Advanced signal processing using modern tools like MATLAB, Python etc.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Analyze the effect of sampling and quantisation of signals and appraise its relevance with reference to applications.	L2, L3
CO2	Formulate various transform domain representations of 1D and 2D signals and demonstrate their applications with reference to practical signals.	L3, L4
CO3	Examine finite word length effects and design practical filters for real life.	L3, L4
CO4	Demonstrate the effect of sampling rate converters and design distortion free digital filter banks illustrating their applications to process real life signals.	L3, L4
CO5	Analyze and choose architectures to efficiently implement the DSP systems for various applications taking into consideration the practical aspects.	L3, L4

Semester- 1

POWER CONVERTERS			
Course Code	**MEC114D**	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives:

- To analyse switched circuits.
- To analyse single phase and three phase AC to DC converters.
- To analyse and design DC to DC converters.
- To analyse DC to AC converters.
- To analyse AC to AC converters.

Module-1

Analysis of switched circuits: thyristor controlled half wave rectifier – R, L, RL, RC load circuits, classification and analysis of commutation.

RBT Levels: L3

Module-2

Single-Phase and Three-Phase AC to DC converters: half controlled configurations- operating domains of three phase full converters and semi-converters – Reactive power considerations.

RBT Levels: L3

Module-3

Analysis and design of DC to DC converters: Control of DC-DC converters, Buck converters, Boost converters, Buck-Boost converters, Cuk converters.

RBT Levels: L3, L4

Module-4

Single phase and Three phase inverters: Voltage source and Current source inverters, Voltage control and harmonic minimization in inverters.

RBT Levels: L3

Module-5

AC to AC power conversion using voltage regulators: choppers and cyclo-converters, consideration of harmonics.

RBT Levels: L3

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Two Unit Tests each of **25 Marks**
2. Two assignments each of **25 Marks** or **one Skill Development Activity of 50 marks** to attain the COs and Pos.

The sum of two tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module.

Suggested Learning Resources:

Books

1. Ned Mohan, Undeland and Robbin, 'Power Electronics: converters, Application and design', John Wiley and sons.Inc, Newyork, 1995.

2. Rashid M.H., 'Power Electronics Circuits, Devices and Applications ', Prentice Hall India, New Delhi, 1995.

3. P.C Sen.,' Modern Power Electronics ', Wheeler publishing Co, First Edition, New Delhi, 1998.

Web links and Video Lectures (e-Resources):

- https://nptel.ac.in/

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Analyse switched circuits.	L3
CO2	Analyse single phase and three phase AC to DC converters.	L3
CO3	Analyse and design DC to DC converters.	L3, L4
CO4	Analyse DC to AC converters.	L3
CO5	Analyse ACto AC converters.	L3

Semester- 1

SYSTEMVERILOG			
Course Code	**MEC115A**	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives: This course will enable students to:

- Understand Digital System Verification Using Object Oriented Methods
- Learn the System Verilog Language for Digital System Verification.
- Create/Build Test Benches for the Design/Methodology.
- Use Constrained Random Tests for Verification
- Understand Concepts of Functional Coverage

Module-1

Verification Guidelines: The Verification Process, Basic Test Bench Functionality, Directed Testing, Methodology Basics, Constrained Random Stimulus, Randomization, Functional Coverage, Test Bench Components, Layered Test Bench.

Data Types:Built-In Data Types, Fixed and Dynamic Arrays, Queues, Associative Arrays, Linked Lists, Array Methods, Choosing A Storage Type, Creating New Types With typedef, Creating User Defined Structures, Type Conversion, EnumeratedTypes, Constants and Strings, Expression Width.

RBT Levels: L2, L3

Module-2

Procedural Statements and Routines:Procedural Statements, Tasks, Functions and Void Functions, Task and Function Overview, Routine Arguments, Returning from a Routine, Local Data Storage, Time Values.

Connectingthe Test Bench and Design:Separating the Test Bench and Design, The Interface Construct, Stimulus Timing, Interface Driving and Sampling, System Verilog Assertions.

RBT Levels: L2, L3

Module-3

Randomization:Introduction, Randomization in System Verilog, Constraint Details, Solution Probabilities, Valid Constraints, InLine Constraints, Random Number Functions, Common Randomization Problems, Random Control, Random Number Generators.

RBT Levels: L3

Module-4

Threads and Inter process Communication:Working with Threads, Disabling Threads, Inter Process Communication, Events, Semaphores, Mailboxes, BuildingA Test Bench with Threads and InterProcess Communication.

RBT Levels: L3

Module-5

Functional Coverage: Coverage Types, Functional Coverage Strategies, Simple Functional Coverage Example, Anatomy of Cover Group, Triggeringa CoverGroup, Data Sampling, Cross Coverage, Generic Cover Groups, Coverage Options, Analyzing Coverage Data, MeasuringCoverage Statistics During Simulation.

RBT Levels: L3, L4

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Two Unit Tests each of **25 Marks**
2. Two assignments each of **25 Marks**or **oneSkill Development Activity of 50 marks** to attain the COs and POs

The sum of two tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.

Suggested Learning Resources:

Books

1. Chris Spear, "System Verilog for Verification – A guide to learning the Test bench language features", Springer Publications Second Edition, 2010.
2. Stuart Sutherland, Simon Davidmann, Peter Flake, "System Verilog for Design- A guide to using system Verilog for Hardware design and modelling", Springer Publications Second Edition, 2006.

Web links and Video Lectures (e-Resources):

- https://nptel.ac.in/

Skill Development Activities Suggested:

1) Interact with industry (small, medium, and large).
2) Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3) Involve in case studies and field visits/ fieldwork.
4) Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5) Handle advanced instruments to enhance technical talent.
6) Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7) Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc.
Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical –activities which will enhance their skill. The prepared report shall be

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Apply the SystemVerilog concepts to verify the design.	L3
CO2	Apply constrained random tests benches using SystemVerilog.	L3
CO3	Appreciate Functional Coverage.	L3, L4

Semester-I

ADVANCED WIRELESS COMMUNICATION			
Course Code	**MEC115B**	CIE Marks	50
Teaching Hours/Week(L:P:SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3

Course Learning objectives:

1. To enable students understand the various aspects of wireless communication
2. To understand the concept behind the capacity of channels.
3. Gain the information on Linear time-invariant Gaussian channels, Capacity of fading channels
4. Study uplink and downlink model of AWGN channel, fading channels
5. Describe different types of diversity, Understanding concept behind modeling of MIMO.

Module-1

Physical modeling for wireless channels, Input/output model of the wireless channel: Free space, fixed transmit and receive antennas, Free space, moving antenna, Reflecting wall, fixed antenna, Reflecting wall, moving antenna, Reflection from a ground plane, Power decay with distance and shadowing, Moving antenna, multiple reflectors, The wireless channel as a linear time-varying system, Baseband equivalent model, discrete-time baseband model, Additive white noise.

RBT Levels: L2

Module-2

Time and frequency coherence, AWGN channel capacity: Time and frequency coherence: Doppler spread and coherence time, delay spread and coherence bandwidth, Repetition coding, Packing spheres, Capacity-achieving AWGN channel codes, Reliable rate of communication and capacity, Resources of the AWGN channel-Continuous-time AWGN channel, Power and bandwidth, Bandwidth reuse in cellular systems.

RBT Levels: L2, L3

Module-3

Linear time-invariant Gaussian channels, Capacity of fading channels: Single input multiple output (SIMO) channel, Multiple input single output (MISO) channel, Frequency-selective channel, Slow fading channel, receive diversity, Transmit diversity, Transmit and receive diversity, Time and frequencydiversity,Outage forparallelchannels,Fastfadingchannel,Transmittersideinformation,Frequency-selectivefadingchannels.

RBT Levels: L2, L3

Module-4

Uplink and Downlink AWGN channel, Uplink and Downlink fading channel: Capacity via successive interference cancellation, Comparison with conventional CDMA, Comparison with orthogonal multiple access, General K-use ruplink capacity, Symmetric case: two capacity achieving schemes, General case: superposition coding achieves capacity, Slow fading channel, Fast fading channel, Full channel side information, Channel side information at receiver only, Full channel side information, Frequency selective fading channels.

RBT Levels: L2, L3

Module-5

Multiuser diversity, Physical Modeling of MIMO channels: Multiuser diversity gain, Multiuser versus classical diversity, Fair scheduling and multiuser diversity, Channel prediction and feedback, Opportunistic beam forming using dumb antennas, Multiuser diversity in multicell systems, Line-of- sight SIMO channel, Line-of-sight MISO channel, Antenna arrays with only a line-of-sight path, Geographically separated antennas, Line-of-sight plus one reflected path, MIMO multipath channel, Angular domain representation of signals, Angular domain representation of MIMO channels, Statistical modeling in the angular domain, Degrees of freedom and diversity, Dependency on antenna spacing.

RBT Levels: L3, L4

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE.A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Two Unit Tests each of **25 Marks.**
2. Two assignments each of **25 Marks** or **one Skill Development Activity of 50 marks** to attain the Cos and Pos.

The sum of two tests, two assignments/skill Development Activities, will be **scaled down to 50 marks CIE methods/question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

Semester-End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module.

Suggested Learning Resources:

Books

1. Andrea Goldsmith, Wireless Communications, Cambridge University Press, 2005.
2. David T, Pramod Viswanath, Fundamentals of Wireless Communications, Cambridge.

Weblinks and Video Lectures (e-Resources):

- https://nptel.ac.in/

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

Sl. No.	Description	Blooms Level
CO1	Implement physical models of wireless channels. Gain knowledge on communication links and physical model.	L3, L4
CO2	Gain knowledge of key concepts of wireless communication	L3
CO3	Measure capacity of AWGN channel, LTI Gaussian channels and various fading channels.	L3
C04	Study uplink and downlink model of AWGN channel, fading channels and multiuser diversity.	L2, L3

MULTIMEDIA AND APPLICATIONS			
Course Code	**MEC115C**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	3 Hours

Course objectives:

This course will enable students to:

- Understanding basics of multimedia including text, image, audio, video and multimedia networking terminology.
- Explore how multimedia is used in different applications like image compression and text compression.
- Understand various audio and video compression techniques.
- Comprehend the various video compression standards and Multimedia Networks with applications.

Module-1

Introduction: Multimedia information representation, Multimedia networks, Multimedia applications, Application and networking terminology, Network QoS and application QoS, Digitization principles, Text, images, audio and video.

RBT Levels: L2

Module-2

Text and image compression: Compression principles, Text compression- Run length, Huffman, LZW, Document Image compression using T2 and T3 coding, image compression- GIF, TIFF and JPEG.

RBT Levels: L3

Module-3

Audio and Video Compression: Audio compression – principles, DPCM, ADPCM, Adaptive and Linear Predictive coding, Code-Excited LPC, Perceptual coding, MPEG and Dolby coders video compression, Video compression principles.

RBT Levels: L3

Module-4

Video Compression Standards: H.261, H.263, MPEG, MPEG 1, MPEG 2, MPEG-4 and Reversible VLCs, MPEG-7 standardization process of multimedia content description, MPEG 21 multimedia framework.

RBT Levels: L3

Module-5

Multimedia Networks: Basics of Multimedia Networks, Communications and Applications: Quality of Multimedia Data Transmission, Multimedia over IP, Multimedia over ATM Networks, Transport of MPEG-4, Media on Demand (MoD).

RBT Levels: L3, L4

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Two Unit Tests each of **25 Marks**
2. Two assignments each of **25 Marks** or **one Skill Development Activity of 50 marks**

to attain the COs and POs

The sum of two tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.

The students will have to answer five full questions, selecting one full question from each module.

Suggested Learning Resources:

Text Books:

1. Fred Halsall, "Multimedia Communications: Applications, Networks, Protocols and Standards" Pearson Education Publishers, 2001, ISBN: 97802013981871.
2. Raif Steinmetz, Klara Nahrstedt, "Multimedia: Computing, Communications and Applications", Pearson education, 2002.

Reference Books:

1. K. R. Rao, Zoran S. Bojkovic, Dragorad A. Milovanovic, "Multimedia Communication Systems", Pearson education, 2004.
2. Hans. W. Barz, Gregory A. Bassett, "Multimedia Networks: Protocols, Design and Applications", John Wiley & Sons publications, 2016. ISBN: 9781119090137.
3. John Billamil, Louis Molina, "Multimedia: An Introduction", PHI, 2002.

Web links and Video Lectures (e-Resources):

- https://nptel.ac.in/

Semester Course outcome (Course Skill Set)

At the end of the course the student will be able to:

Sl. No.	Description	Blooms Level
CO1	Deploy the right multimedia communication models.	L3, L4
CO2	Apply QoS to multimedia network applications with efficient routing techniques.	L3
CO3	Discuss the various standards and quality aspects of digital video formats used for multimedia application.	L2
C04	Solve the security threats in the multimedia networks.	L3
C05	Develop the real-time multimedia network applications.	L4

Semester- I

PROCESS CONTROL			
Course Code	**MEC115D**	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives:

- To understand the need of process control, basic principles of various manufacturing processes and apply engineering knowledge to do problem analysis in process control.
- To define common dynamics of processes found in many industries and model them mathematically.
- To select the proper controller and apply the tuning rules to achieve optimum performance.
- To understand, interpret and implement tuning of the controllers using various methods and study about digital controllers.
- To select advanced control strategy to enhance the performance.

Module-1

Introduction: Introduction to Process Control. Control objectives, servo regulatory control, and classification of process variables.

Modeling of some Chemical Process Systems: Modeling basics, Degree of Freedom, Mass Balance, Energy Balance equations, linearization of nonlinear systems, Modeling of Level Tank System, Continuous Stirred Tank Heater, Continuous Stirred Tank Reactor, Transfer function.

RBT Levels: L2

Module-2

Elements of Process Control: Dead time, Interacting and non-interacting systems, self-regulation, inverse response, capacity of process, integrating systems, multi-capacity process.

Process Identification: Dynamic behavior of first and second order processes, Obtaining First Order Plus Time Delay (FOPTD) model with Process Reaction curve. Obtaining second order model of processes.

RBT Levels: L2, L3

Module-3

Common Controller Modes: Controller Modes, ON OFF, Multi position, time proportional controller, Theory Proportional, Integral and Derivative modes, PI, PD, PID Controller, Electronics Controller implementation, Dynamic Behavior of closed loop systems with P, I, D, PI , PID modes.

RBT Levels: L2, L3

Module-4

Discretisation and Implementation Issues: Discrete time control mode realization. Velocity and Position algorithm of PID control. Integral windup, anti-windup systems, controller bias, bumps less transfer.

Tuning of Controllers: Application and tuning, ZN Tuning (Open loop and Closed loop), Performance criteria, Integral criteria.

RBT Levels: L3, L4

Module-5

Some Advance Control Techniques: Cascade Control, Feed forward Control, ratio Control, Air Fuel Ratio Control for Drum Boilers. Level Control in Drum Boiler, Shrinking and Swelling, Inverse response of Drum Boiler.

RBT Levels:L3, L4

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Two Unit Tests each of **25 Marks**
2. Two assignments each of **25 Marks**or **oneSkill Development Activity of 50 marks** to attain the COs and POs

The sum of two tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.

Suggested Learning Resources:

Books

1. G. Stephanopolous, "Chemical Process Control An Introduction to Theory and Practice", Prentice Hall India, August 2000.
2. Surekha Bhanot, "Process Control Principles and Applications", Oxford, 2008
3. C.D. Johnson, "Process Control Instrumentation Technology", Prentice Hall India.
4. Thomas Marlin, "Process Control Designing Processes and Control for Dynamic Performance", Tata MC Graw Hill, 2012.
5. F.G. Shinskey, "Process Control Systems Application Design and Adjustment" 3rd editionn, McGraw Hill International, 6. D. E. Seborg, T.F. Edgar, D. A. Mellichamp, "Process Dynamics and Control", Wiley, 2004.

Web links and Video Lectures (e-Resources):

- https://nptel.ac.in/

Skill Development Activities Suggested

- To develop a simple control loop for a system using microcontroller or hardware circuit e.g. on off control of heaters/temperature control systems, displaying of the variables on computer screens or LCD screens etc.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Understand the need of process control, basic principles of various manufacturing processes and apply engineering knowledge to do problem analysis in process control.	L2, L3
CO2	Define common dynamics of processes found in many industries and model them mathematically.	L2
CO3	Select the proper controller and apply the tuning rules to achieve optimum performance.	L3
CO4	Understand, interpret and implement tuning of the controllers using various methods and study about digital controllers.	L2, L3, L4
CO5	Select advanced control strategy to enhance the performance.	L3

ADVANCED MACHINE LEARNING AND DEEP LEARNING LAB			
Course Code	**MECL116A**	CIE Marks	50
Teaching Hours/Week (L:P:T/SDA)	0:4:0	SEE Marks	50
Credits	02	Exam Hours	03

Course Objectives:

- To apply theoretical knowledge to practical scenarios.
- To gain proficiency in implementing machine learning algorithms.
- To analyse real-world problems and develop appropriate solutions.

Sl.No.	Experiments
1	Implement multivariate linear regression.
2	Implementing Decision tree Classification.
3	Implement K-means clustering algorithm.
4	Write a program for Gradient Descent Learning.
5	Implement Bidirectional Recurrent neural network.
6	Implementation of Natural Language Processing.
7	Implementation of Speech Recognition.
8	Case study- Convolutional Neural Networks.
	Demonstration Experiments (For CIE)
9	Visualizing linear regression: Use a physical model or software to demonstrate how a line fits to data points.
10	Overfitting and underfitting: Demonstrate the effects of overfitting and underfitting using simple datasets.
11	Convolution operation: Visualize the convolution process using image patches.
12	Language modelling: Generate text using a simple RNN model.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

1. Implement and apply machine learning techniques in prediction problems.
2. Implement suitable learning algorithms to solve a given problem.
3. Implement a model based on machine learning for an application.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 40% of maximum marks in the semester-end examination(SEE). In total of CIE and SEE student has to secure 50% maximum marks of the course.

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with an observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- **Total marks scored by the students are scaled down to 30 marks** (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 01 tests for 100 marks, test shall be conducted after the 14th week of the semester.
- In test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- **The test marks is scaled down to 20 marks** (40% of the maximum marks).

The Sum of **scaled-down** marks scored in the report write-up/journal and marks of test is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University.

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 10% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours

Suggested Learning Resources:

- Deep Learning - Goodfellow, Bengio and Courville
- Fundamentals of Deep Learning – Nikhil Budama
- Neural Networks and Deep Learning – CharuAggarwal
- Hands-on Deep Learning Algorithms with Python – SudharsanRavichandran

ELECTRONICS AND COMMUNICATIONLABORATORY			
Course Code	**MECL116B**	CIE Marks	50
Teaching Hours/Week (L:P:T/SDA)	0:4:0	SEE Marks	50
Credits	02	Exam Hours	03

Course Objectives:

- To apply theoretical knowledge to practical scenarios.
- To design and analyseanalog and mixed-signal circuits.
- To implement and evaluate timing and oscillation circuits.
- To analyse and implement communication systems.

Sl.No.	Experiments
	Part - A
1	Design a Two-Stage direct coupled Differential Amplifier with series voltage Negative Feedback of β=50.
2	Design a Voltage regulator using operational amplifier to produce output of 12V with maximum load current of 50mA.
3	Design a Two-stage CS Amplifier with overall gain of 100. Plot the frequency response and estimate the Bandwidth and Q factor.
4	Design a Darlington Emitter follower using MOSFET/BJT with and without bootstrap; plot the frequency response. Also calculate gain and bandwidth.
5	Design and realize:i) Four-bit weighted R – 2R ladder DAC. ii) Two-bit Flash ADC using Op-amp.
6	Design and verify an IC 555 timer-based pulse generator for the specified pulse of 2ms.
7	Using IC NE 566 Voltage Controlled Oscillator, design a circuit to generate square and triangular waveform with a time period of 0.2ms.
	Part - B
8	Design a radio receiver for a given frequency (88 to 108 MHz) and measure the sensitivity, selectivity, and fidelity of the same.
9	Generate PAM and PDM signals for a pulse duration of 10 msec using IC 555 Timer.
10	Implement an AM and FM systems and measure its noise figure.
11	Consider the bit sequence of length 10,000. Modulate it with BPSK, BASK, BFSK. Transmit the signal through AWGN channel. Vary the SNR. Compare the theoretical and simulated probability of error.
12	Design and implement the Adaptive delta modulation and demodulation.

Courseoutcomes(CourseSkillSet):

At theendofthecourse thestudent will beableto:

1. Analyze frequency response of BJT/ MOSFET circuits.
2. Design Analog circuits using OPAMPs and IC555 for different applications.
3. Design and test circuits for Analog and digital modulation/demodulation schemes.
4. Design and test circuits for Analog to digital signal conversion techniques.
5. Design and analysis of feedback circuits.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 40% of maximum marks in the semester-end examination (SEE). In total of CIE and SEE student has to secure 50% maximum marks of the course.

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with an observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- **Total marks scored by the students are scaled down to 30 marks** (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 01 tests for 100 marks, test shall be conducted after the 14th week of the semester.
- In test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- **The test marks is scaled down to 20 marks** (40% of the maximum marks).

The Sum of **scaled-down** marks scored in the report write-up/journal and marks of test is the total CIEmarks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

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All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

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General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 10% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours

Suggested Learning Resources:

- "Analog Integrated Circuit Design" by David A. Johns and Ken Martin.
- "Design of Analog CMOS Integrated Circuits" by Behzad Razavi.
- "Op-Amps and Linear Integrated Circuits" by Ramakant A. Gayakwad.
- "555 Timer IC: Operation and Application" by Michael T. R. R. Haskell.
- "Communication Systems" by Simon Haykin.
- "Digital Communications" by John G. Proakis and Masoud Salehi.