

Semester - II

Industrial Control System -I			
Course Code	MLMS201	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	03:02:00	SEE Marks	50
Total Hours of Pedagogy	40hoursTheory+10-12Labslots	Total Marks	100
Credits	04	Exam Hours	3
Course objectives: <ul style="list-style-type: none"> To remember the basics of process control and understand the basic concepts of Industrial Automation. To apply the control system concepts to Special Intelligent control strategies. To analyze and evaluate the concepts of DCS to different types of Industries. Comprehensive coverage of communication protocols that are used in automation systems 			
MODULE-1			
Industrial Control Systems: Embedded Control Systems, Real-Time Control Systems, DistributedControl System. Industrial Control Engineering: Industrial Process Controls,Industrial Motion Controls,IndustrialProduction Automation. <div style="text-align: right;">RBTLevel:L2,L3</div>			
MODULE-2			
Sensors and Actuators: Industrial Optical Sensors,Industrial Physical Sensors,Industrial Measurement Sensors, Industrial Actuators. <div style="text-align: right;">RBTLevel:L2,L3</div>			
MODULE-3			
Transducers and Valves: Industrial Switches, Industrial Transducers, Industrial Valves <div style="text-align: right;">RBTLevel:L2,L3</div>			
MODULE-4			
Microprocessors: Single-Core Microprocessor Units, Multicore Microprocessor Units <div style="text-align: right;">RBTLevel:L2,L3, L4</div>			
MODULE 5			
Programmable-Logic and Application-Specific Integrated Circuits (PLASIC): Fabrication Technologies and Design Issues, Field-Programmable-Logic Devices, Peripheral Programmable Logic Devices. <div style="text-align: right;">RBTLevel:L2,L3, L4</div>			

PRACTICAL COMPONENT OF IPCC(May cover all / major modules)

Sl.NO	Experiments
1	Program to toggle all the bits of portP1 continuously with a desired time delay.
2	Program to interface LCD datapins to portP1 and display a message on it
3	To study a Linear Variable Differential Transformer (LVDT) and use it in a simple experimental set up to measure a small displacement.
4	To measure static/dynamic pressure of fluid in pipe/tube using pressure transducer/pressure cell.
5	To obtain the characteristics of control valve.
6	Design and Develop an Assembly Program to sort a given set of 'n'16-bit numbers in ascending order.

7	Develop an assembly language program to reverse a given string and verify whether it is a palindrome or not.
8	Program to read data from temperature sensor and display the temperature value.
9	Program to interface Stepper Motor to rotate the motor in clockwise and anticlockwise Directions
10	Program to control the speed of stepper motor
11	Program to read the temperature data and control the devices
12	Program to find the largest of all.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together

CIE for the theory component of IPCC

1. Two Tests each of **25 Marks**
2. Two assignments each of **25 Marks/One Skill Development Activity of 50 marks**
3. Total Marks of two tests and two assignments/one Skill Development Activity added will be CIE for 60 marks, marks scored will be proportionally scaled down to **30 marks**.

CIE for the practical component of IPCC

- On completion of every experiment/program in the laboratory, the students shall be evaluated and marks shall be awarded on the same day. The **15 marks** are for conducting the experiment and preparation of the laboratory record, the other **05 marks shall be for the test** conducted at the end of the semester.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for **10 marks**. Marks of all experiments' write-ups are added and scaled down to **15 marks**.
- The laboratory test at the end /after completion of all the experiments shall be conducted for **50 marks** and scaled down to **05 marks**.

Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **20 marks**.

SEE for IPCC

Theory SEE will be conducted by the University as per the scheduled timetable, with common question papers for the course (duration 03 hours)

1. The question paper will be set for 100 marks and marks scored will be scaled down proportionately to 50 marks.
2. The question paper will have ten questions. Each question is set for 20 marks.
3. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
4. The students have to answer 5 full questions, selecting one full question from each module.

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper shall include questions from the practical component).

- The minimum marks to be secured in CIE to appear for SEE shall be the 15 (50% of maximum marks-30) in the theory component and 10 (50% of maximum marks -20) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included. The maximum of 04/05 questions to be set from the practical component of IPCC, the total marks of all questions should not be more than the 20 marks.
- SEE will be conducted for 100 marks and students shall secure 40% of the maximum marks to qualify in the SEE. Marks secured will be scaled down to 50. (Student has to secure an aggregate of 50% of maximum marks of the course (CIE+SEE))

Suggested Learning Resources:

Books

1. Advanced Industrial Control Technology, Peng Zhang, Elsevier, 2010.

Web links and Video Lectures (e-Resources):

<https://nptel.ac.in>

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Course outcome (Course Skill Set)

- Technical seminar on different types of industrial sensors.
- Assignments, quiz.

Sl. No.	Description	Blooms Level
CO1	Differentiate between different types of industrial control systems; embedded control systems, real time control systems and distributed control systems.	BL1,2
CO2	Explain the need of sensors and actuators.	BL1,2
CO3	Explain the use of multi core microprocessors in industrial control systems and to describe programmable peripheral I/O ports, etc.	BL1,2

Analysis of Linear System			
Course Code	MLMS202	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	03:00:0	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory	Total Marks	100
Credits	03	Exam Hours	3
<p>Course Learning objectives:</p> <ul style="list-style-type: none"> • To model Continuous and Discrete time system in state space • To solve the continuous and discrete time system state space models. • To assess the controllability and observability of state space models in the continuous and discrete time domains. • Understand the concepts of state feedback techniques. 			
Module-1			
<p>State space Representation of Continuous Time Systems: Introduction, concepts of state, consistency conditions, State space representation using physical variables, phase variables, canonical variables. Eigen values, Eigen vectors, state equations for dynamic systems, non-uniqueness of state model, state diagrams-state diagrams for continuous time statemodels.</p> <p style="text-align: right;">RBTLevel: L2, L3</p>			
Module-2			
<p>State Space Representation of Discrete Time Systems: Digital control system, quantizing and quantization error, Data acquisition and conversion, Impulse sampling and data hold, pulse transfer function, State space representation of discrete time systems, State diagrams - state diagrams for discrete time state models.</p> <p style="text-align: right;">RBTLevel: L2, L3</p>			
Module-3			
<p>Solution of State Equations: Introduction, Existence and Uniqueness of solution to continuous time state equations, Solution of Linear time invariant continuous time state equations – Evaluation of matrix exponential, series evaluation, Evaluation using symmetry transformation, Evaluation using Cayley- Hamilton technique, Evaluation using Inverse Laplace transformation. Solution of Discrete time state equations – Z transform approach, Pulse transfer function matrix, Discretization of continuous time state space equations.</p> <p style="text-align: right;">RBTLevel: L2, L3, L4</p>			
Module-4			
<p>Controllability and Observability of Systems: Introduction, General Concept of Controllability, General Concept of Observability, Controllability Tests for Continuous Time Systems – Time Invariant Case, Observability Tests for Continuous Time Systems – Time Invariant Case, Controllability and Observability of Discrete Time Systems – Time Invariant Case Controllability and Observability of State Model in Jordan Canonical Form. Loss of Controllability and Observability due to Sampling.</p> <p style="text-align: right;">RBTLevel: L2, L3, L4</p>			
Module-5			
<p>Model Control: Introduction, Controllable and Observable Companion Forms–Single Input/Single Output Systems, Effect of State feedback on Controllability and Observability, Pole Placement by State Feedback- Single Input Systems, Stabilizability, Full Order Observer, Reduced Order Observer, Deadbeat Observer</p> <p style="text-align: right;">RBTLevel: L2, L3, L4</p>			

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Two Unit Tests each of **25 Marks**
2. Two assignments each of **25Marks** or **one Skill Development Activity of 50 marks** to attain the COs and POs

The sum of two tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:**Books**

1. Modern Control System Theory, M Gopal, New Age International, 2012 Reprint.
2. Discrete Time Control Systems, Ogata K, PHI, 2nd Edition, 2016

Web links and Video Lectures (e-Resources):

<https://nptel.ac.in>

Skill Development Activities Suggested

- Quiz, technical seminar, assignments.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Provide a state variable models for Continuous and discrete time systems	BL1,2
CO2	Solve the State equations to provide a solution and analyze the min both continuous and Discrete time domains	BL1,2,3
CO3	Assess the controllability and observability of statespace models developed.	BL3

EMBEDDED SYSTEM			
Course Code	MLMS203	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory	Total Marks	100
Credits	03	Exam Hours	3
<p>Course Learning objectives:</p> <ul style="list-style-type: none"> • To impart knowledge of embedded systems with suitable examples, explanation of process, classification of embedded systems. • To explain the processor architecture, memory organization, communication with processor and interrupt services. • To explain the program modelling concepts, inter-process communication and synchronization of processes. 			
Module-1			
<p>Introduction to Embedded Systems: Embedded Systems, Processor Embedded into a System, Embedded Hardware Units and Devices in a System, Embedded Software in a System, Examples of Embedded Systems, Embedded Systems – on-chip(Soc) and Use of VLSI Circuit Design Technology, Complex Systems Design and Processors, Design of Process in Embedded System, Formulation of System Design, Design Process and Design Examples, Classification of Embedded Systems, Skill required for an Embedded System Designer.</p> <p style="text-align: right;">RBTLLevel:L2,L3</p>			
Module-2			
<p>Processor Architecture and Memory Organisation: 8051 Architecture, Real world Interfacing, Introduction to Advanced Architecture, Processor and Memory Organization, Instruction Level Parallelism, Performance Metrics, Memory – Types, Memory – Maps and Addresses, Processor Selection, Memory Selection.</p> <p style="text-align: right;">RBTLLevel:L2,L3</p>			
Module-3			
<p>Devices and Communication Buses, Interrupt Services: I/O Types and Examples, Serial Communication Devices, Parallel Device Ports, Sophisticated Interfacing Features in Device Ports, Wireless Devices, Timer and Counting Devices, Watchdog Timer, Real Time Clock, Networked Embedded Systems, Serial Bus Device Protocols – Parallel Communication Network Using ISA, PCI, PCI –X and Advanced Protocols.</p> <p>Device Drivers and Interrupts Service Mechanisms: Programmed-I/O Busy-wait Approach without Interrupt Service Mechanism, ISR Concept, Interrupt Sources, Interrupt Servicing Mechanism, Direct Memory Access</p> <p style="text-align: right;">RBTLLevel:L2,L3, L4</p>			
Module-4			
<p>Interprocess Communication and Synchronization of Processes, Threads and Tasks: Multiple Processes in an Application, Multiple Threads in an Application, Tasks, Task Status, Task and Data, Clear – cut Distention Between Functions, ISRS and Tasks by their Characteristics, Concept of Semaphores, Shared Data, Interprocess Communication, Signal Function, Semaphore Functions, Message Queue Functions, Mailbox Functions, Pipe Functions, Socket Functions, RPC Functions.</p> <p style="text-align: right;">RBTLLevel:L2,L3, L4</p>			
Module-5			
<p>Real - Time Operating Systems: OS Services, Process Management, Timer Functions, Event Functions, Memory management, Device, File and IO Subsystems Management, Interrupt Routines in RTOS Environment and Handling of Interrupt Source Calls, Real-time Operating Systems, Basic Design Using an RTOS, Rtos Task Scheduling Models, Interrupt Latency and Response of the task as performance Metrics, OS Security Issues.</p> <p style="text-align: right;">RBTLLevel:L2,L3, L4</p>			

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

3. Two Unit Tests each of **25 Marks**
4. Two assignments each of **25Marks** or **one Skill Development Activity of 50 marks** to attain the COs and POs

The sum of two tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

6. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
7. The question paper will have ten full questions carrying equal marks.
8. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
9. Each full question will have a sub-question covering all the topics under a module.
10. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:**Books**

1. Embedded Systems: Architecture, Programming and Design, Raj Kamal, McGrawHill, 2nd Edition, 2014.

Web links and Video Lectures (e-Resources):

<https://nptel.ac.in>

Skill Development Activities Suggested

- Quiz, technical seminar, assignments.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Explain embedded system, and 8051 architectures	L1,2
CO2	Analyse communication busses, and interrupt services.	L1,2
Co3	Explain Inter Process Communication, Real Time Operating System.	L1,2

VLSI TECHNOLOGY			
Course Code	MLMS204	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	03:0:0	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory	Total Marks	100
Credits	03	Exam Hours	3
Course Learning objectives: <ul style="list-style-type: none"> • To learn basic CMOS Circuits. • To describe CMOS process technology. • To explain techniques of chip design using programmable devices. • To learn the concepts of designing VLSI Subsystems 			
Module-1			
MOS Transistor Theory: MOS Transistors, CMOS Fabrication and Layout, Long-Channel I-V Characteristics, C-V Characteristics, Non-ideal I-V Effects, DC Transfer Characteristics, Pitfalls and Fallacies. CMOS Processing Technology: Introduction, CMOS Technologies, Layout Design Rules, CMOS Process Enhancements <div style="text-align: right;">RBTL Level: L2, L3</div>			
Module-2			
Combinational Circuit Design: Introduction, Circuit Families, Circuit Pitfalls, More Circuit Families, Silicon-on-Insulator Circuit Design, Sub-threshold Design, Pitfalls and Fallacies, Historical Perspective <div style="text-align: right;">RBTL Level: L2, L3</div>			
Module-3			
Sequential Circuit Design: Introduction, Sequencing Static Circuits, Circuit Design of Latches and Flip-flops, Static Sequencing Element Methodology, Sequencing Dynamic Circuits, Synchronizers, Wave Pipelining, Pitfalls and Fallacies, Case study <div style="text-align: right;">RBTL Level: L2, L3</div>			
Module-4			
Single Stage Amplifiers: Basic Concepts, Common – Source Stage, Source Follower, Common – Gate Stage, Cascode Stage, Choice of Device Models. Differential Amplifiers: Single-Ended and Differential Operations, Basic Differential Pair, Common-Mode Response, Differential Pair with MOS Loads, Gilbert Cell <div style="text-align: right;">RBTL Level: L2, L3, L4</div>			
Module-5			
Passive and Active Current Mirrors: Basic Current Mirrors, Cascode Current Mirrors, Active Current Mirrors. Operational Amplifiers: General Considerations, One – Stage Op Amps, Two – Stage Op Amps, Gain Boosting, Comparison, Common-Mode Feedback, Input Range Limitations, Slew Rate, Power Supply Rejection, Noise in Opamp. <div style="text-align: right;">RBTL Level: L2, L3, L4</div>			

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

5. Two Unit Tests each of **25 Marks**
6. Two assignments each of **25Marks** or **one Skill Development Activity of 50 marks** to attain the COs and POs

The sum of two tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

11. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
12. The question paper will have ten full questions carrying equal marks.
13. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
14. Each full question will have a sub-question covering all the topics under a module.
15. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:**Books**

1. CMOS VLSI Design: A Circuits and Systems Perspective, Neil H.E.Weste, David Money Harris, Pearson, 4th
2. Design of Analog CMOS Integrated Circuits, Behzad Razavi, McGrawHill, 31st Reprint, 2015

Web links and Video Lectures (e-Resources):

<https://nptel.ac.in>

Skill Development Activities Suggested

- Technical seminar on different types of Op-amps.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Describe MOS theory and Processing Technology.	BL1,2
CO2	Analyse sequential circuits, single stage and multistage amplifiers.	BL,2
CO3	Explain passive and active current mirrors, and operational amplifiers.	BL1,2

NON LINEAR SYSTEM			
Course Code	MLMS215A	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40 HOURS	Total Marks	100
Credits	3	Exam Hours	3
Course Learning objectives:			
<ul style="list-style-type: none"> • To introduce the need and concept of nonlinear system. • To impart knowledge about different strategies adopted in the analysis of nonlinear systems. • To familiarize with the design of different types of nonlinear controllers 			
Module-1			
Nonlinear Systems: Introduction to Nonlinear systems, Behavior of Nonlinear Systems- Frequency –Amplitude dependence, Jump resonance, Sub- harmonic oscillations, Frequency entrainment, Limit Cycles, Asynchronous quenching, Common Physical Non-linearities, Classification of nonlinearities, methods of analysis of nonlinear systems, Definition of describing function, Linearization of nonlinear system.			
RBTL Level: L2, L3			
Module-2			
Describing Function Method: Introduction, assumptions and definition, evaluation of describing function for functions like x^2 , x^3 , $ x $ and common nonlinearities like relay, saturation, dead zone, hysteresis, backlash and a combination of these, Analysis of nonlinear systems –Concept of enclosure, stable and unstable limit cycles, Review of polar plot and Nichols Plot, Evaluation of existence of limit cycle and calculation of magnitude and frequency of oscillation			
Module-3			
Phase-Plane Analysis: Introduction to phase plane and phase trajectory, Singular points –evaluation, classification and trajectories, Stability analysis of nonlinear system using phase trajectories, Limit cycles in phase portrait, Construction of phase trajectories- Analytical method, Isocline method, Delta method, and Pell's method.			
RBTL Level: L2, L3			
Module-4			
Lyapunov Stability: Stability Definitions, Some Preliminaries, Lyapunov's Direct Method, Stability of Linear Systems, Lyapunov's Linearization Method, The Lur'e Problem, Krasovskii's method of stability assessment, Variable gradient method of stability assessment. Stability assessment of discrete time systems			
RBTL Level: L2, L3, L4			
Module-5			
Stability Assessment in the Frequency Domain: Circle criteria and its application, Popov's method. Sliding mode control: Introduction An overview of classical sliding mode control, introductory example, Dynamics in sliding mode–Linear Systems, Nonlinear Systems, Chattering Problems, Reachability Condition, Applications of Sliding Mode control.			
RBTL Level: L2, L3, L4			

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

7. Two Unit Tests each of **25 Marks**
8. Two assignments each of **25Marks** or **one Skill Development Activity of 50 marks** to attain the COs and POs

The sum of two tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

16. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
17. The question paper will have ten full questions carrying equal marks.
18. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
19. Each full question will have a sub-question covering all the topics under a module.
20. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:**Books**

1. Advanced Control Theory, A. Nagoor Kani, RBA Publications, 2nd Edition, 2009.
2. Nonlinear Systems Analysis, M. Vidyasagar, PHI, 2nd Edition, 2002.
3. Non Linear Systems, H.K. Khalil, Pearson, 2015.
4. Sliding Mode Control in Engineering, Wilfrid Perruquetti & Jean Pierre Barbot, Marcel Dekker, 2002.

Web links and Video Lectures (e-Resources):

<https://nptel.ac.in>

Skill Development Activities Suggested

- Quiz, technical seminar, assignments.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Explain the need and concept of nonlinear system.	BL1,2
CO2	Explain about different strategies adopted in the analysis of nonlinear systems.	BL1,2
CO3	Describe with the design of different types of nonlinear controllers	BL1,2

PROCESS CONTROL AND INSTRUMENTATION			
Course Code	MLMS215B	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3
<p>Course Learning objectives:</p> <ul style="list-style-type: none"> • Understand the basic principles & importance of process control in industrial process plants; • Understand the importance and application of good instrumentation for the efficient design of process control loops for process engineering plants. • Specify the required instrumentation and final elements to ensure that well-tuned control is achieved. • Understand the use of block diagrams & the mathematical basis for the design of control systems. • Understand the PLC Documentation and PID controller drawings. • Understand the experimental implementation of advanced process control schemes and the methods for process monitoring and diagnosis. 			
Module-1			
<p>Introduction to Process Control: Introduction, Process Control, Definition of the Elements in a Control Loop, Instrumentation and Sensors, Control System Evaluation, Analog and Digital Data, Process Facility Considerations. Units and Standards: Introduction, Basic Units, Units Derived from Base Units, Standard Prefixes, Standards. Basic Electrical Components: Introduction, Circuits with R, L, and C, RC Filters, Bridge Circuits. Analog Electronics: Introduction, Analog Circuits, Types of Amplifiers, Amplifier Applications.</p> <p style="text-align: right;">RBT Level: L2, L3</p>			
Module-2			
<p>Digital Electronics: Introduction, Digital Building Blocks, Converters, Data Acquisition Devices, Basic Processor. Micro electromechanical Devices and Smart Sensors: Introduction, Basic Sensors, Piezoelectric Devices, Microelectromechanical Devices, Smart Sensors Introduction. Pressure: Introduction, Pressure Measurement, Measuring Instruments, Application Considerations. Level: Introduction, Level Measurement, Application Considerations.</p> <p style="text-align: right;">RBT Level: L2, L3</p>			
Module-3			
<p>Flow: Introduction, Fluid Flow, Flow Measuring Instruments, Application Considerations. Temperature and Heat: Introduction, Temperature and Heat, Temperature Measuring Devices, Application Considerations. Position, Force, and Light: Introduction, Position and Motion Sensing, Force, Torque, and Load Cells, Light.</p> <p style="text-align: right;">RBT Level: L2, L3, L4</p>			
Module-4			
<p>Humidity and Other Sensors: Humidity, Density and Specific Gravity, Viscosity, Sound, pH Measurements, Smoke and Chemical Sensors. Regulators, Valves, and Motors: Introduction, Pressure Controllers, Flow Control Valves, Power Control, Motors, Application Considerations. Programmable Logic Controllers: Introduction, Programmable Controller System, Controller Operation, Input/output Modules, Ladder Diagrams</p> <p style="text-align: right;">RBT Level: L2, L3, L4</p>			
Module-5			
<p>Signal Conditioning and Transmission: Introduction, General Sensor Conditioning, Conditioning Considerations for Specific Types of Devices, Digital Conditioning, Pneumatic Transmission, Analog Transmission, Digital Transmission, Wireless Transmission. Process Control: Introduction, Sequential Control, Discontinuous Control, Continuous Control, Process Control Tuning, Implementation of Control Loops. Documentation and P&ID: Introduction, Alarm and Trip Systems, PLC Documentation, Pipe and Instrumentation Symbols, P&ID Drawings.</p> <p style="text-align: right;">RBT Level: L2, L3, L4</p>			

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

9. Two Unit Tests each of **25 Marks**
10. Two assignments each of **25Marks** or **one Skill Development Activity of 50 marks** to attain the COs and POs

The sum of two tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom’s taxonomy as per the outcome defined for the course.

Semester-End Examination:

21. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
22. The question paper will have ten full questions carrying equal marks.
23. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
24. Each full question will have a sub-question covering all the topics under a module.
25. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:**Books**

- 1 Introduction to Instrumentation, Sensors, and Process Control, William C. Dunn, Artech House, 2006.

Web links and Video Lectures (e-Resources):

<https://nptel.ac.in>

Skill Development Activities Suggested

- Quiz, technical seminar, assignments.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Explain Process Control, Electrical Components and Analog Electronics	BL1,2
CO2	Describe the good instrumentation for the efficient design of process control loops for process engineering plants;	BL1,2
CO3	Explain the Mathematical basis for the design of Control Systems; PLC Documentation and PID controller drawings.	BL1,2

Optimal Control Theory			
Course Code	MLMS215C	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3
<p>Course Learning objectives:</p> <ul style="list-style-type: none"> • To discuss modeling of systems.To discuss state and control constraints. • To discuss the performance measures used in control problems. • To explain determination of control function that minimizes the performance measure. • To explain development of a dynamic program applicable to a class of control problems. • To explain some basic ideas of the calculus of variations and to relate the analogy of results in calculus and the results of calculus of variations. • To explain application of variational method to optimal control problems. 			
Module-1			
<p>Introduction: Problem Formulation, State Variable Representation of a System. The Performance Measure: Performance Measure for Optimal Control Problems, Selecting a Performance Measure, Selection of a Performance Measure. Dynamic Programming: The optimal Control Law, the Principle of Optimality, Application of the principle of Optimality to Decision- Making, Dynamic Programming applied to a Routing Problem, An Optimal Control System, Interpolation.</p> <p style="text-align: right;">RBTLLevel:L2,L3</p>			
Module-2			
<p>Dynamic Programming (continued): A Recurrence Relation of Dynamic Programming, Computational Procedure for Solving Control Problems, Characteristics of Dynamic Programming Solution, Analytical Results – Linear Regulator Problems, The Hamilton- Jacobi-Bellman Equation, Continuous Linear Regulator Problem, The Hamilton- Jacobi- Bellman Equation – Some Observations. The Calculus of Variations: Fundamental Concepts, Functions of a Single Function</p> <p style="text-align: right;">RBTLLevel:L2,L3</p>			
Module-3			
<p>The Calculus of Variations (continued): Functionals involving several independent Functions, Piecewise – smooth External, Constrained Extrema. The Variational Approach to Optimal Control Problems: Necessary Conditions for Optimal Control</p> <p style="text-align: right;">RBTLLevel:L2,L3, L4</p>			
Module-4			
<p>The Variational Approach to Optimal Control Problems (continued): Linear regulator problem, Pontryagin's Minimum Principle and state Inequality Constraints, Minimum –Time problems.</p> <p style="text-align: right;">RBTLLevel:L2,L3, L4</p>			
Module-5			
<p>The Variational Approach to Optimal Control Problems (continued): Minimum Control-Effort Problems, Singular Intervals in Optimal Control Problems</p> <p style="text-align: right;">RBTLLevel:L2,L3, L4</p>			

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

11. Two Unit Tests each of **25 Marks**
12. Two assignments each of **25Marks** or **one Skill Development Activity of 50 marks** to attain the COs and POs

The sum of two tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom’s taxonomy as per the outcome defined for the course.

Semester-End Examination:

26. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
27. The question paper will have ten full questions carrying equal marks.
28. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
29. Each full question will have a sub-question covering all the topics under a module.
30. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:**Books**

- Optimal Control Theory An Introduction, Donal E Kirk, Dover Publication, 2004

Web links and Video Lectures (e-Resources):

<https://nptel.ac.in>

Skill Development Activities Suggested

Quiz, technical seminar, assignments.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Explain the Modeling of systems., state and control constraints. And performance measures used in control problems.	BL1,2
CO2	Analyze the determination of control function that minimizes the performance measure. And dynamic program applicable to a class of control problems	BL1,2
CO3	Explain some basic ideas of the calculus of variations and to relate the analogy of	BL1,2

Neural and Fuzzy Logic Control of Drives			
Course Code	MLMS215D	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3
Course Learning objectives:			
<ul style="list-style-type: none"> • This course introduces the basics of Neural Networks and essentials of Artificial Neural Networks with Single Layer and Multilayer Feed Forward Networks. • It deals with Associate Memories and introduces Fuzzy sets and Fuzzy Logic system components. • The Neural Network and Fuzzy Network system application to Electrical Engineering is also presented. • This subject is very important and useful for doing Project Work. 			
Module-1			
Modern control systems design using CAD techniques: Introduction, Control systems for AC drives, electronic design automation (EDA), Application specific integrated circuit (ASIC) basics, Field programmable gate arrays (FPGAs), ASICs for power systems and drives, Electric motors. Electric motors: Motors, Pulse width modulation, The space vector in electrical systems, Induction motor control <b style="text-align: right;">RBTLevel:L2,L3			
Module-2			
Elements of neural control: Neurontypes, Artificial neural networks architectures, Training algorithms, Control applications of ANNs, Neural network implementation. Neural FPGA implementation: Neural networks design and implementation strategy, Universal programs FFANN, hardware implementation, Hardware implementation complexity analysis <b style="text-align: right;">RBTLevel:L2,L3			
Module-3			
Fuzzy logic fundamentals: Introduction, Fuzzy sets and fuzzy logic, Types of membership functions, Linguistic variables, Fuzzy logic operators, Fuzzy control systems, Fuzzy logic in power and control, Applications. VHDL fundamentals: Introduction, VHDL design units, Libraries, visibility and state system in VHDL, Sequential statements, Concurrent statements, Functions and procedures, Advanced features in VHDL <b style="text-align: right;">RBTLevel:L2,L3, L4			
Module-4			
Neural current and speed control of induction motors: The induction motor equivalent circuit, The current control algorithm, The new sensor less motor control Strategy <b style="text-align: right;">RBTLevel:L2,L3, L4			
Module-5			
Neural current and speed control of induction motors (continued): Induction motor controller VHDL Design, FPGA controller experimental results <b style="text-align: right;">RBTLevel:L2,L3, L4			

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

13. Two Unit Tests each of **25 Marks**

14. Two assignments each of **25 Marks** or **one Skill Development Activity of 50 marks** to attain the COs and POs

The sum of two tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

31. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.

32. The question paper will have ten full questions carrying equal marks.

33. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.

34. Each full question will have a sub-question covering all the topics under a module.

35. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:**Books**

1. Neural and Fuzzy Logic Control of Drives and Power Systems, M.N.Cirstea, et al, Newnes, 2002

Web links and Video Lectures (e-Resources):

<https://nptel.ac.in>

Skill Development Activities Suggested

Quiz, technical seminar, assignments.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Discuss control strategies for electric drives/power systems.	BL1,2
CO2	Understand the complex features of control strategies, EDA.	BL1,2
CO3	Understand the features of neural networks, fuzzy logic, electric machines and drives, Power systems and VHDL.	BL1,2

RESET CONTROL SYSTEMS			
Course Code	MLMS216A	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3
Course Learning objectives: <ul style="list-style-type: none"> To provide an introduction to the fundamentals of Reset control, concepts of RCSs, Fundamental theory of traditional reset. To learn Sinusoid input response, Describing function, Application to HDD systems. To learn the Quadratic stability, Affine quadratic stability, Robust stability of RCS with time-delay. To understand the concept of Stability analysis, A heuristic design method, Application to track-seeking control of HDD systems 			
Module-1			
Introduction: Motivation of reset control, Basic concepts of RCSs, Fundamental theory of traditional reset design. RBTLLevel: L2, L3			
Module-2			
Describing function analysis of reset systems: Sinusoid input response, Describing function, Application to HDD systems RBTLLevel: L2, L3			
Module-3			
Stability of reset control systems: Preliminaries, Quadratic stability, Stability of RCSs with time-delay, Reset times-dependent stability, Passivity of RCSs RBTLLevel: L2, L3, L4			
Module-4			
Robust stability of reset control systems: Definitions and assumptions, Quadratic stability, Affine quadratic stability, Robust stability of RCS with time-delay, Examples. RCSs with discrete-time reset conditions: Preliminaries and problem setting, Stability analysis, A heuristic design method, Application to track-seeking control of HDD systems RBTLLevel: L2, L3, L4			
Module-5			
Reset control systems with fixed reset instants: Stability analysis, Moving horizon optimization, Optimal reset law design, Application to HDD systems, Application to PZT-positioning stage. Reset control systems with conic jump sets: Basic idea, L2-gain analysis RBTLLevel: L2, L3, L4			

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

15. Two Unit Tests each of **25 Marks**

16. Two assignments each of **25Marks** or **one Skill Development Activity of 50 marks** to attain the COs and POs

The sum of two tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom’s taxonomy as per the outcome defined for the course.

Semester-End Examination:

2. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
3. The question paper will have ten full questions carrying equal marks.
4. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
5. Each full question will have a sub-question covering all the topics under a module.
6. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:**Books**

1. Analysis and Design of Reset Control Systems, YuqianGuo et al, IET, 2015.

Web links and Video Lectures (e-Resources):

<https://nptel.ac.in>

Skill Development Activities Suggested

- Quiz, technical seminar, assignments.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Explain fundamentals of Reset control, concepts of RCSs, Fundamental theory of traditional reset. Describing function, Application to HDD systems	BL1,2
CO2	Analyse Quadratic stability, Affine quadratic stability, Robust stability of RCS with time-delay	BL1,2
CO3	concept of Stability analysis. A heuristic design method. Application to track tracking	BL1,2

Digital System Design With VHDL			
Course Code	MLMS216B	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3
Course Learning objectives:			
<ul style="list-style-type: none"> • Enable students to analyse logic design circuits. • Able to build combinational and sequential circuits. • Able to model the sequential circuits using VHDL Module. 			
Module-1			
<p>Introduction: Modern digital design, CMOS technology, Programmable logic, Electrical properties. Combinational logic design: Boolean algebra, Logic gates, Combinational logic design, Timing, Number codes. Combinational logic using VHDL gate models: Entities and architectures, Identifiers, spaces and comments, Netlists, Signal assignments, Generics, Constant and open ports, Testbenches, Configurations.</p> <p style="text-align: right;">RBTLLevel:L2,L3</p>			
Module-2			
<p>Combinational building blocks: Three-state buffers, Decoders, Multiplexers, Priority encoder, Adders, Parity checker, Test benches for combinational blocks. Synchronous sequential design: Synchronous sequential systems, Models of synchronous sequential systems, Algorithmic state machines, Synthesis from ASM charts, State machines in VHDL, VHDL testbenches for state machines.</p> <p style="text-align: right;">RBTLLevel:L2,L3</p>			
Module-3			
<p>VHDL models of sequential logic blocks: Latches, Flip-flops, JK and T flip-flops, Registers and shift registers, Counters, Memory, Sequential multiplier, Test benches for sequential building blocks. Complex sequential systems: Linked state machines, Datapath /controller partitioning, Instructions, A simple microprocessor, VHDL model of a simple microprocessor.</p> <p style="text-align: right;">RBTLLevel:L2,L3</p>			
Module-4			
<p>VHDL simulation: Event-driven simulation, Simulation of VHDL models, Simulation modelling issues, File operations. VHDL synthesis: RTL synthesis, Constraints, Synthesis for FPGAs, Behavioral synthesis, Verifying synthesis results. Testing digital systems: The need for testing, Fault models, Fault-oriented test pattern generation, Fault simulation, Fault simulation in VHDL.</p> <p style="text-align: right;">RBTLLevel:L2,L3, L4</p>			
Module-5			
<p>Asynchronous sequential design: Asynchronous circuits, Analysis of asynchronous circuits, Design of asynchronous sequential circuits, Asynchronous state machines, Setup and hold times and metastability. Interfacing with the analog world: Digital to analogue converters, Analogue to digital converters, VHDL-AMS, Phase-locked loops, VHDL-AMS simulators.</p> <p style="text-align: right;">RBTLLevel:L2,L3, L4</p>			

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

17. Two Unit Tests each of **25 Marks**
18. Two assignments each of **25Marks** or **one Skill Development Activity of 50 marks** to attain the COs and POs

The sum of two tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom’s taxonomy as per the outcome defined for the course.

Semester-End Examination:

2. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
3. The question paper will have ten full questions carrying equal marks.
4. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
5. Each full question will have a sub-question covering all the topics under a module.
6. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:**Books**

- Digital System Design with VHDL, Mark Zwolinski, Pearson, 2nd Edition, 2004

Web links and Video Lectures (e-Resources):

<https://nptel.ac.in>

Skill Development Activities Suggested

- Quiz, technical seminar, assignments.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Analyse Logic Design Circuits.	L2
CO2	Build Combinational and Sequential Circuits.	L3
CO3	Model The Sequential Circuits Using VHDL Module	L3

Nanotechnology for Microelectronics and Optoelectronics			
Course Code	MLMS216C	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3
<p>Course Learning objectives:</p> <ul style="list-style-type: none"> To provide an introduction to nanoelectronics and Optoelectronics, Quantum mechanical coherence, Quantum wells, wires, and dots, Density of states and dimensionality, Semiconductor heterostructures, Quantum transport. To learn Energy bands in typical semiconductors, Intrinsic and extrinsic semiconductors, Electron and hole concentrations in semiconductors. To learn the, MOSFET structures, Heterojunctions, Quantum wells, Superlattices. To understand the concept of Effect of a magnetic field on a crystal, Low-dimensional systems in magnetic fields, Density of states of a 2D system in a magnetic field 			
Module-1			
<p>Mesoscopic Physics and Nanotechnologies: Trends in nanoelectronics and Optoelectronics, Characteristic lengths in mesoscopic systems, Quantum mechanical coherence, Quantum wells, wires, and dots, Density of states and dimensionality, Semiconductor heterostructures, Quantum transport.</p> <p>Survey of Solid-State Physics: Introduction, review of quantum mechanics, free electron model of a solid. Density of states function, Bloch theorem, Electron in crystalline solids, Dynamics of electrons in bands, Lattice vibrations, Phonons</p> <p style="text-align: right;">RBTL Level: L2, L3</p>			
Module-2			
<p>Review of Semiconductor Physics: Introduction, Energy bands in typical semiconductors, Intrinsic and extrinsic semiconductors, Electron and hole concentrations in semiconductors, Elementary transport in semiconductors, Degenerate semiconductors, Optical properties of semiconductors.</p> <p>The Physics of Low-Dimensional Semiconductors: Introduction, Basic properties of two-dimensional semiconductor nanostructures, square quantum well of finite depth, Parabolic and triangular quantum wells, Quantum wires, Quantum dots, Strained layers, Effect of strain on valence bands, Band structure in quantum wells, Excitonic effects in quantum</p> <p style="text-align: right;">RBTL Level: L2, L3</p>			
Module-3			
<p>Semiconductor Quantum Nanostructures and Superlattices: Introduction, MOSFET structures, Heterojunctions, Quantum wells, Superlattices.</p> <p>Electric Field Transport in Nanostructures: Introduction, Parallel transport, Perpendicular transport, Quantum Transport in nanostructures.</p> <p style="text-align: right;">RBTL Level: L2, L3</p>			
Module-4			
<p>Transport in Magnetic Fields and the Quantum Hall Effect: Introduction, Effect of a magnetic field on a crystal, Low-dimensional systems in magnetic fields, Density of states of a 2D system in a magnetic field, The Aharonov-Bohm effect, The Shubnikov-de Haas effect, The quantum Hall Effect.</p> <p>Optical and Electro-optical Processes in Quantum Heterostructures: Introduction, Optical properties of quantum wells and superlattices, Optical properties of quantum dots and nanocrystals, Electro-optical effects in quantum wells. Quantum confined Stark Effect, Electro-optical effects in superlattices. Stark Ladders and Bloch Oscillations.</p> <p style="text-align: right;">RBTL Level: L2, L3, L4</p>			
Module-5			
<p>Electronic Devices Based on Nanostructures: Introduction, MODFETs, Heterojunction bipolar transistors, Resonant tunnel effect, Hot electron transistors, Resonant tunneling transistor, Single electron transistor.</p> <p>Optoelectronic Devices Based on Nanostructures: Introduction, Heterostructure semiconductor lasers, Quantum well semiconductor lasers, Vertical cavity surface emitting lasers (VCSELs), Strained quantum well lasers, Quantum dot lasers, Quantum well and superlattice photodetectors, Quantum well modulators.</p> <p style="text-align: right;">RBTL Level: L2, L3, L4</p>			

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

19. Two Unit Tests each of **25 Marks**
20. Two assignments each of **25 Marks** or **one Skill Development Activity of 50 marks** to attain the COs and POs

The sum of two tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:**Books**

1. Algorithms for VLSI Physical Design Automation, Naveed A. Sherwani, Kluwer Academic Publishers, 3rd Edition, 2002.

Web links and Video Lectures (e-Resources):

<https://nptel.ac.in>

Skill Development Activities Suggested

- Quiz, technical seminar, assignments.

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

Sl. No.	Description	Blooms Level
CO1	To explain to Nano Electronics and Optoelectronics, Quantum mechanical coherence, Quantum wells, wires, and dots, Density of states and dimensionality, Semiconductor heterostructures, Quantum transport.	BL1,2
CO2	Explain the Physics of Low-Dimensional Semiconductors, Semiconductor Quantum Nanostructures and Superlattices	BL1,2
CO3	Explain Transport in Magnetic Fields and the Quantum Hall Effect, Optical and Electro-optical Processes in Quantum Heterostructures.	BL1,2

Internet Based Control Systems			
Course Code	MLMS216D	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3
<p>Course Learning objectives:</p> <ul style="list-style-type: none"> • Specifications of internet-based control system. • Real time data transfer over the internet. • Delay and losses from control perceptive. 			
Module-1			
<p>Introduction: Networked Control Systems (NCS), Internet-based Control Systems (ICS), Challenges of NCS/ICS. Requirements Specification for Internet-based Control Systems: Introduction, Requirements Specification, Functional Modelling of Internet-based Control Systems, Information Hierarchy, Possible Implementation of Information Architecture. Internet-based Control System Architecture Design: Introduction, Traditional Bilateral Tele-Operation Systems, Remote Control over the Internet, Canonical Internet-based Control System Structures. Web-based User Interface Design: Features of Web-based User Interface, Multimedia User Interface Design, CaseStudy.</p> <p style="text-align: right;">RBTLLevel:L2,L3</p>			
Module-2			
<p>Real-time Data Transfer over the Internet: Real-time Data Processing, Data Wrapped with XML, Real-time Data Transfer Mechanism, Case Study. Dealing with Internet Transmission Delay and Data Loss from the Network View: Requirements of Network Infrastructure for Internet-based Control, Features of Internet Communication, Comparison of TCP and UDP, Network Infrastructure for Internet-based Control, Typical Implementation for Internet-based Control.</p> <p style="text-align: right;">RBTLLevel:L2,L3</p>			
Module-3			
<p>Dealing with Internet Transmission Delay and Data Loss from the Control Perspective: Overcoming the Internet Transmission Delay, Control Structure with the Operator Located Remotely, Internet-based Control with a Variable SamplingTime, Multi-rate Control, Time Delay Compensator Design, Simulation Studies, Experimental Studies. Design of Multi-rate SISO Internet-based Control Systems: Introduction, Discrete-time Multi-rate Control Scheme, Design Method,StabilityAnalysis,SimulationStudies,Real-time Implementation.</p> <p style="text-align: right;">RBTLLevel:L2,L3</p>			
Module-4			
<p>Design of Multi-rate MIMO Internet-based Control Systems:Introduction, System Modeling,Controller Design, Stability Analysis, Design Procedure, Model-based Time Delay Compensation, Simulation Study. Safety and Security Checking: Introduction,Similarity of Safety and Security,Framework of Security Checking, Control Command Transmission Security, Safety Checking, Case Study.</p> <p style="text-align: right;">RBTLLevel:L2,L3, L4</p>			
Module-5			
<p>Remote Control Performance Monitoring and Maintenance over the Internet: Introduction, Performance Monitoring, Performance Monitoring of Control Systems, Remote Control Performance Maintenance, Case Study. Remote Control System Design and Implementation over the Internet: Introduction, Real-time Control System LifeCycle, Integrated Environments, A Typical Implementation of the General Integrated Environment, CaseStudy.</p> <p style="text-align: right;">RBTLLevel:L2,L3, L4</p>			

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

21. Two Unit Tests each of **25 Marks**
22. Two assignments each of **25Marks** or **one Skill Development Activity of 50 marks** to attain the COs and POs

The sum of two tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom’s taxonomy as per the outcome defined for the course.

Semester-End Examination:

2. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
3. The question paper will have ten full questions carrying equal marks.
4. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
5. Each full question will have a sub-question covering all the topics under a module.
6. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:**Books**

1. Algorithms for VLSI Physical Design Automation, Naveed A.Sherwani, Kluwer Academic Publishers, 3rd Edition, 2002.

Web links and Video Lectures (e-Resources):

<https://nptel.ac.in>

Skill Development Activities Suggested

- Quiz, technical seminar, assignments.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Explain the Specifications of internet-based control system.	BL 1,2
CO2	Describe Real time data transfer over the internet.	BL1,2
CO3	Explain Delay and losses from control perceptive.	BL1,2

MICROELECTRONICS AND CONTROL LABORATORY-1			
Course Code	MLMSL207	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	00:04:00	SEE Marks	50
Credits	02	Exam Hours	3
Course objectives:			
<ul style="list-style-type: none"> • Understand mathematical models of electrical and mechanical systems. • Analysis of control system stability using digital simulation. • Demonstrate the time domain and frequency domain analysis for linear time invariant systems. • Apply programmable logic controllers to demonstrate industrial controls in the laboratory 			
Sl.NO	Experiments		
1	Simulation of a typical second order system.		
2	Study of system stability by using root locus, Bode plot and Nyquist plot.		
3	Performance characteristics of P,PI,PIDcontroller.		
4	Study of MALABFIS Toolbox.		
5	Verification of Sampling Theorem.		
6	Design and verification of FIR filter.		
7	State estimation using Pole placement method.		
8	DC and AC Servo motor characteristics.		
Course outcomes (Course Skill Set):			
At the end of the course the student will be able to:			
<ul style="list-style-type: none"> • Use MATLAB/ Scilab to simulate a second order system to study the output and perform state estimation by pole placement method. • Analyze the stability of the system sin time and frequency domains • Design and verify the frequency response of different compensators. • Evaluate the performance of different controllers in enhancing the system performance • Verify the sampling theorem,design and analyze the FIR filter • Gain knowledge on FI Stool box for control system applications 			

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 40% of maximum marks in the semester-end examination(SEE). In total of CIE and SEE student has to secure 50% maximum marks of the course.

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with an observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- **Total marks scored by the students are scaled down to 30 marks** (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 01 tests for 100 marks, test shall be conducted after the 14th week of the semester.
- In test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- **The test marks is scaled down to 20 marks** (40% of the maximum marks).

The Sum of **scaled-down** marks scored in the report write-up/journal and marks of test is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University.

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 10% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours

Suggested Learning Resources:

<https://nptel.ac.in>