| Design of Analog and Mixed Mode VLSI Circuits | | | |
|---|---|---|---|
| Course Code | MLVS201 | CIE Marks | 50 |
| Teaching Hours/Week(L:P:SDA) | 3:2:0 | SEE Marks | 50 |
| Total Hours of Pedagogy | 40hoursTheory+10-12Labslots | Total Marks | 100 |
| Credits | 04 | Exam Hours | 3 |

**Courseobjectives:**

- TounderstandthebasicphysicsandoperationofMOSdevices.
- TostudySingle-StageandDifferentialAmplifiers.
- TolearnDataConverterSpecificationsandArchitectures.
- TounderstandSingleendedDifferentialAmplifierandoperations.
- TolearnarchitectureofDataconverterincludesADC(AnalogtoDigital)and DAC(DigitaltoAnalog) Converters.

**MODULE-1**

**BasicMOSDevicePhysics:**Generalconsiderations,MOS1/VCharacteristics,secondordereffects,MOSdeviceMod els.

**RBT Levels:** L2

**MODULE-2**

**SinglestageAmplifier:**BasicConcepts,CommonSourcestage,Sourcefollower.

**RBT Levels:** L2, L3

**MODULE-3**

**SinglestageAmplifier:**common-gatestage,CascadeStage,choiceofdevicemodels.

**RBT Levels:** L2, L3

**MODULE-4**

**DifferentialAmplifiers:**Singleendedanddifferentialoperation,Basicdifferentialpair,Commonmoderesponse,Dif ferentialpairwithMOSloads,Gilbertcell.

**RBT Levels:** L2, L3

**MODULE5**

**DataConverter Architectures :** DAC& ADCSpecifications,Current SteeringDAC,ChargeScalingDAC, Flash ADC,SuccessiveApproximationADC.

**RBT Levels:** L3, L4

**PRACTICALCOMPONENTOFIPCC***(Maycoverall/majormodules)*

| Sl.NO | Experiments |
|---|---|
| 1 | Designa SingleStagedifferentialamplifier |
| 2 | DesignaCommonsourceamplifier |
| 3 | Designanop-ampwithgivenspecification*usingdifferentialamplifierCommonsourceamplifierinlibrary. (ApplicableLibraryshouldbeadded&informationshouldbe giventotheDesigner.) |
| 4 | Designa4bitR-2RbasedDACforthegivenspecification(ApplicableLibraryshouldbeadded&information shouldbegiventotheDesigner.) |
| 5 | DesignanIntegratorusingOPAMP(FirstOrder) |
| 6 | DesignaDifferentiatorusingOPAMP(FirstOrder) |
| 7 | Designandcharacterizeabasic Sigma delta ADCfromtheavailabledesigns. |
| | |
| Note | 1. ExperimentstobeconductedusingsuitableCADtool<br>2. For 1-4 experiments draw the schematic and verify the following i) DC Analysis ii) AC Analysis iii)TransientAnalysisb.DrawtheLayoutandverifytheDRC,ERC,LVSc.CheckforXXd.ExtractRCandback annotatethesameandverifytheDesign |

**AssessmentDetails(bothCIEandSEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. Theminimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of themaximum marks of SEE.A student shall be deemed to have satisfied the academic requirements and earned thecredits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sumtotalof theCIE(ContinuousInternalEvaluation)andSEE(SemesterEndExamination)takentogether

**CIEforthetheorycomponentofIPCC**

1. TwoTestseachof**25 Marks**
2. Twoassignmentseachof**25Marks/OneSkillDevelopmentActivityof50marks**
3. TotalMarksoftwotestsand twoassignments/oneSkillDevelopmentActivityaddedwillbeCIEfor60marks,marks scoredwillbeproportionallyscaleddown to**30marks**.

**CIEforthepracticalcomponentofIPCC**

- Oncompletionofeveryexperiment/programinthelaboratory,thestudentsshallbeevaluatedandmarks shall be awarded on the same day.The **15 marks** are for conducting the experiment andpreparation of the laboratory record, the other **05 marks shall be for the test** conducted at theendof thesemester.
- The CIE marks awarded in the case of the Practical component shall be based on the continuousevaluationofthelaboratoryreport.Eachexperimentreportcanbeevaluatedfor**10marks**. Marksofallexperiments'write-upsareaddedandscaleddownto**15marks**.
- The laboratory test at the end /after completion of all the experiments shall be conducted for **50marks**andscaleddownto **05marks.**

Scaled-downmarksofwrite-upevaluationsandtestsaddedwillbeCIEmarksforthelaboratorycomponentofIPCC for **20marks**.

.

**SEEforIPCC**

TheorySEEwillbeconducted by theUniversityasperthescheduled timetable,withcommonquestionpapersforthecourse(duration03hours)

1. Thequestionpaperwillbesetfor100marksandmarksscoredwillbescaleddownproportionately to50marks.
2. Thequestionpaperwillhavetenquestions.Eachquestionisset for20marks.
3. Therewillbe2questionsfromeachmodule.Eachofthetwoquestionsunderamodule(withamaximumof3sub-questions),**shouldhavea mixoftopics**underthatmodule.
4. Thestudentshavetoanswer5fullquestions,selecting onefullquestionfromeachmodule.

**The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion willhaveaCIEcomponentonly.QuestionsmentionedintheSEEpapershallinclude questionsfromthepracticalcomponent**).

- The minimum marks to be secured in CIE to appear for SEE shall be the 15 (50% of maximummarks-30)inthetheorycomponentand10(50%ofmaximummarks-20)inthepracticalcomponent. The laboratory component of the IPCC shall be for CIE only. However, in SEE, thequestionsfromthelaboratorycomponentshallbeincluded.Themaximum

of04/05questionsto
besetfromthepracticalcomponentofIPCC,thetotalmarksofallquestionsshouldnotbemore

thanthe20marks.

- SEEwillbeconductedfor100marksandstudentsshallsecure40%ofthemaximummarksto qualifyintheSEE.Markssecuredwillbescaleddownto50.(Studenthasto secureanaggregateof50% of maximummarksof thecourse(CIE+SEE)

SuggestedLearningResources:

Books

1) "BehzadRazavi",DesignofAnalogCMOSIntegratedCircuits,TMH 2007.
2) "R.JacobBaker",CMOSCircuitDesign,Layout,andSimulation,WileySecondEdition

"PhillipE.Allen,Douglas R.Holberg",CMOSAnalogCircuitDesignOxfordUniversity PressSecondEdition.

**WeblinksandVideoLectures(e-Resources):**

VTUe-IearningResources.

**ActivityBasedLearning(SuggestedActivitiesinClass)/PracticalBasedlearning**

1. Interactwithindustry(small,medium,andlarge).
2. Involvein research/testing/projectsto understandtheirproblemsandhelpcreative andinnovativemethodstosolvetheproblem.
3. Involveincasestudies andfieldvisits/fieldwork
4. Accustomtotheuseofstandards/codesetc.,tonarrowthegapbetweenacademiaandindustry.
5. Handleadvancedinstrumentstoenhancetechnicaltalent.
6. Gain confidence in modellingof systems and algorithms for transient and steady-stateoperations,thermalstudy,etc.
7. Workondifferentsoftware/s(tools)tosimulate,analyzeandauthenticatetheoutputtointerpretan dconclude.

**Courseoutcome(CourseSkillSet)**

Attheendof thecoursethestudentwillbeableto:

| Sl.No. | Description | BloomsLevel |
|---|---|---|
| CO1 | Useefficientanalyticaltoolsforquantifyingthebehaviourofbasiccircuitsbyinspection. | L2,L3 |
| CO2 | Designhigh-performance,amplifiercircuitswiththetrade-offsbetweenspeed, precisionandpowerdissipation. | L3, L4 |
| CO3 | Designandstudythebehaviourofphase-locked-loopsfortheapplications. | L3,L4 |
| CO4 | Identifythecriticalparametersthataffecttheanalogandmixed-signalVLSIcircuits'performance | L3 |
| CO5 | Perform calculationsin the digital or discrete time domain,more sophisticateddataconverterstotranslatethedigitaldatatoandfrominherentlyanalogwor ld. | L5 |

**ProgramOutcomeofthiscourse**

| Sl.No. | Description | POs |
|---|---|---|
| 1. | Independentlycarryout research/investigationanddevelopmentworktosolvepracticalproblemsrelatedtoVLSIDesignan dembeddedsystems. | PO1 |
| 2. | Demonstrate a degree of mastery over the areas of VLSI Design and embedded systems. Themastery should be at a level higher than the requirements in the bachelor's in Electronics &CommunicationEngineering. | PO2 |
| 3. | Applyappropriatemethodologyandmodernengineering/ITtoolstomeettheinternationalstandar dsinthe area ofVLSIdesignandembeddedsystems. | PO3 |
| 4. | Acquire competency in areas of VLSI and Embedded Systems, IC Fabrication, Design, Testing,Verification and Integrate multiple sub-systems to develop System On Chip to optimize itsperformanceandexcelinindustrysectorsrelatedtoVLSI/ Embeddeddomain. | PO4 |
| 5. | Understandimpactofprofessionalengineeringsolutionsinsocietalandenvironmentalcontextsand | PO5 |

| VLSI Testing &Verification | | | |
|---|---|---|---|
| Course Code | MLVS202 | CIE Marks | 50 |
| Teaching Hours/Week(L:P:SDA) | 3:0:0 | SEE Marks | 50 |
| Total Hours of Pedagogy | 40Hoursof Teaching | Total Marks | 100 |
| Credits | 03 | Exam Hours | 03 |

**CourseLearningobjectives:**

- TostudyFaults indigitalcircuits.
- TolearnvariousalgorithmsfortestgenerationofCombinationalLogic Circuits.
- Tostudytheapproachtodealwiththetesting problemsatthechiplevel(BIST).
- ToknowaboutDesignVerificationConcepts,SimulatorArchitecturesandOperations.

**Module-1**

**Faultsindigitalcircuits:** FailuresandFaults,Modelingoffaults,TemporaryFaults.
**TestgenerationforCombinationalLogiccircuits:**FaultDiagnosisofdigitalcircuits,Testgeneration techniquesforcombinationalcircuits(One-DimensionalPathSensitization,BooleanDifference, D-Algorithm).

**RBT Levels:** L2, L3

**Module-2**

**Testgenerationfor CombinationalLogiccircuits:**Test generationtechniquesforcombinationalcircuits(PODEM,FAN, DelayFaultDetection),Detectionof multiplefaultsinCombinationallogiccircuits.
**Designoftestablesequentialcircuits:**ControllabilityandObservability,Ad-Hocdesignrulesforimproving testability,designofdiagnosablesequentialcircuits,thescan-pathtechniquefortestablesequentialcircuitdesign.

**RBT Levels:** L2, L3

**Module-3**

**Built-InSelfTest:** TestpatterngenerationforBIST,Outputresponse analysis,CircularBIST,BISTArchitectures.

**RBT Levels:** L2, L3

**Module-4**

**An Invitation to Design Verification:** What is design verification? The basic verification principle, Verificationmethodology, Simulation-based verification versus formal verification, Limitations of formal verification, A quickoverview of Verilog scheduling andexecutionsemantics.
**CodingforVerification:**Functionalcorrectness,Timingcorrectness.

**RBT Levels:** L2, L3

**Module-5**

**SimulatorArchitecturesandOperations:**Thecompilers,Thesimulators,Simulatortaxonomyandcomparison,Simulatoroperationsandapplications.

**RBT Levels:** L2, L3

## AssessmentDetails(bothCIEandSEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. Theminimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of themaximum marks of SEE.A student shall be deemed to have satisfied the academic requirements and earned thecredits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sumtotalof theCIE(ContinuousInternalEvaluation)andSEE(SemesterEndExamination)takentogether.

## ContinuousInternalEvaluation:

1. TwoUnitTests eachof**25Marks**
2. Twoassignmentseachof **25Marks**or**oneSkillDevelopmentActivityof 50marks** toattaintheCOs andPOs

Thesumof twotests, twoassignments/skillDevelopmentActivities, willbe**scaleddownto50marks**

**CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per theoutcomedefinedforthecourse.**

## Semester-EndExamination:

1. TheSEEquestionpaperwillbesetfor100marksandthe marksscoredwillbeproportionatelyreducedto50.
2. Thequestionpaperwillhavetenfullquestionscarrying equalmarks.
3. Eachfullquestionisfor20marks.Therewillbetwofullquestions(withamaximumoffoursub-questions)fromeachmodule.
4. Eachfullquestionwillhaveasub-questioncoveringallthetopicsunderamodule.
5. Thestudentswillhavetoanswerfivefullquestions, selecting onefullquestionfromeachmodule

**SuggestedLearningResources:**

**Books**


1) LalaParagK,"DigitalCircuitTestingandTestability",NewYork,AcademicPress1997.
2) AbramoviciM,BreuerMA,"DigitalSystemsTestingandTestableDesignandFriedmanAD",Wiley1994.
3) WilliamK.Lam,"HardwareDesignVerification:SimulationandFormalMethod-BasedApproaches",PrenticeHallPTR, 2005.
4) VishwaniDAgarwal,"EssentialofElectronicTestingforDigital,MemoryandMixedSignalCircuits",Springer2002


**WeblinksandVideoLectures(e-Resources):**

- https://www.youtube.com/watch?v=O5lyBoWR-PA&list=PLx98Qgh5zPjh6oWI73QfQHZAmAiyt8Wkf
- https://www.youtube.com/watch?v=Abld-fSxjNM&list=PLbMVogVj5nJTClnafWQ9FK2nt3cGG8kCF
- https://www.youtube.com/watch?v=MEaMm423t0w&list=PLZjlBaHNchvOFBWBAtAP9exwQgYpKqsO4&index=1

**SkillDevelopmentActivitiesSuggested**

**SkillDevelopmentActivitiesSuggested:**

1) Interactwithindustry(small,medium,andlarge).
2) Involveinresearch/testing/projectstounderstandtheirproblemsandhelpcreativeandinnovativemethodstosolvetheproblem.
3) Involveincase studiesandfieldvisits/fieldwork.
4) Accustomtotheuse ofstandards/codesetc.,tonarrowthe gapbetweenacademia andindustry.
5) Handleadvancedinstrumentstoenhancetechnicaltalent.
6) Gainconfidenceinmodellingof systemsandalgorithmsfortransientandsteady-state operations,thermalstudy,etc.
7) Workondifferentsoftware/s(tools) tosimulate,analyzeandauthenticatetheoutputtointerpretandconclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills,Statisticalanalysis,fiscalexpertise,etc.

Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learningand application skills of the study they have undertaken. The students with the help of the course teacher can take up relevanttechnical–activitieswhichwillenhance theirskill.The preparedreportshallbeevaluatedfor CIEmarks.

**Courseoutcome(CourseSkillSet)**

Attheendof thecoursethestudentwillbeableto:

| Sl.No. | Description | BloomsLevel |
|---|---|---|
| CO1 | Analyzetheneedforfaultmodeling andtesting ofdigitalcircuits | |
| | L3CO2 | |
| | Generatefaultlists fordigitalcircuits andcompressthetestsforefficiency | L2, |
| L3CO3 | Applyboundaryscantechniquetovalidatetheperformanceofdigitalcircuits | L3, |
| L4CO4 | Designbuilt-inself tests forcomplexdigitalcircuits | L3 |
| CO5 | ApplytheVerificationConceptstoDigitalCircuits. | L3 |

**ProgramOutcomeofthiscourse**

| Sl.No. | Description | POs |
|---|---|---|
| 1. | Independentlycarryoutresearch/investigationanddevelopmentworktosolvepracticalproblemsrelatedtoVLSIDesignandembeddedsystems. | PO1 |
| 2. | Demonstratea degree ofmasteryoverthe areasofVLSIDesignandembeddedsystems.Themasteryshouldbeata levelhigherthantherequirementsinthe bachelor'sinElectronics& CommunicationEngineering. | PO2 |
| 3. | Applyappropriatemethodologyandmodernengineering/ITtoolstomeettheinternationalstandards inthe area ofVLSIdesignandembeddedsystems. | PO3 |
| 4. | Acquire competency in areas of VLSI and Embedded Systems, IC Fabrication, Design, Testing,Verification and Integrate multiple sub-systems to develop System On Chip to optimize itsperformanceandexcelinindustrysectorsrelatedtoVLSI/ Embeddeddomain. | PO4 |
| 5. | Understandimpactofprofessionalengineeringsolutionsinsocietalandenvironmentalcontextsand demonstratethe knowledge forsustainable development. | PO5 |

| ARM Cortex-M3 and M4 Processors | | | |
|---|---|---|---|
| Course Code | MLVS203 | CIE Marks | 50 |
| Teaching Hours/Week(L:P:SDA) | 3:0:0 | SEE Marks | 50 |
| Total Hours of Pedagogy | 40hoursTheory | Total Marks | 100 |
| Credits | 03 | Exam Hours | 03 |

**CourseLearningObjectives:**

- TostudyARMCortex-M3/M4microcontrollers.
- Developassembly-levelandEmbeddedC-programsandinterfacewithotherexternaldevices.
- Toknow-how todevelopsoftwareforsystemsbasedonCortex-M3/M4processor.

**Module-1**

**IntroductiontoARMCortex-MProcessors**:Introduction,AdvantagesandApplicationstoCortex_-Mprocessors,Resources for using ARM_ processors and ARM Microcontrollers, Background and history of ARM.
**Introductionto Embedded Software Development:** Inside typical ARM_ microcontrollers, Development suites & boards,Softwaredevelopmentflow,Compilingapplications,Softwareflow,DatatypesinCprogramming,Inputs,outputs, andperipheralsaccessesandMicrocontrollerinterfaces.

**RBT Levels:** L2, L3

**Module-2**

**Introduction to Embedded Software Development:** The Cortex microcontroller software interface standard(**CMSIS)**
**TechnicalOverview:**GeneralinformationabouttheCortex-M3andCortex-M4processors,Featuresofthe Cortex_-M3andCortex-M4processors.

**RBT Levels:** L2, L3

**Module-3**

**Architecture:**Behaviour of the application program status register (APSR), Memory system, Exceptions andinterrupts,Systemcontrolblock(SCB),Debug, Resetandresetsequence.
**InstructionSet:**BackgroundtotheinstructionsetinARMCortexMprocessors,Comparisonoftheinstructionset inARMCortexMprocessors,Understanding theassemblylanguagesyntax, Useof a suffixininstructions, UAL.

**RBT Levels:** L2, L3

**Module-4**

**InstructionSet**:InstructionSet

**RBT Levels:** L2, L3

**Module-5**

**ExceptionsandInterrupts:**Overviewofexceptionsandinterrupts,Exceptiontypes,Overviewofinterruptmanagement, Definitionsofpriority,Vectortableandvectortablerelocation,Interruptinputsandpendingbehaviors, Exception sequence overview, Details of NVIC registers for interrupt control, Details of SCB registers forexceptionandinterruptcontrol,Detailsofspecialregistersforexceptionorinterruptmasking,Exampleprocedures insettingupinterrupts,Softwareinterrupts.

**RBT Levels:** L2, L3

## AssessmentDetails(bothCIEandSEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. Theminimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of themaximum marks of SEE.A student shall be deemed to have satisfied the academic requirements and earned thecredits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sumtotalof theCIE(ContinuousInternalEvaluation)andSEE(SemesterEndExamination)takentogether.

## ContinuousInternalEvaluation:

1. TwoUnitTests eachof**25Marks**
2. Twoassignmentseachof **25Marks**or**oneSkillDevelopmentActivityof50marks** toattaintheCOs andPOs

Thesumoftwotests,twoassignments/skillDevelopmentActivities,willbe**scaleddownto50marks**

**CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per theoutcomedefinedforthecourse.**

## Semester-EndExamination:

1. TheSEEquestionpaperwillbesetfor100marksandthemarksscoredwillbeproportionatelyreducedto50.
2. Thequestionpaperwillhavetenfullquestionscarrying equalmarks.
3. Eachfullquestionisfor20marks.Therewillbetwofullquestions(withamaximumoffoursub-questions)fromeachmodule.
4. Eachfullquestionwillhaveasub-questioncoveringallthetopicsunderamodule.
5. Thestudentswillhavetoanswerfivefullquestions, selecting onefullquestionfromeachmodule

**SuggestedLearningResources:**

**TextBooks**

1) J.Yiu,TheDefinitiveGuidetoARMCortex-M3andCortex-M4Processors,3rdEdition,NewnesPublication,2013.

**ReferenceBooks:**

2) S.Furber,ARMSystem-on-ChipArchitecture,2ndEdition,Addison-Wesley,2000.
3) A.Deshmukh,Microcontroller-Theory&Applications,Tata McGrawHill,2017.

**OtherReferences**:

1) Cortex-Mseries-ARMReferenceManual
2) Cortex-M3TechnicalReferenceManual(TRM)
3) STM32L152xxARMCortexM3MicrocontrollerReference Manual
4) ARMArchitectureReferenceManual–ARMDDI0100E
5) ARMv7-MArchitectureReferenceManual(ARMv7-MARM)

**WeblinksandVideoLectures(e-Resources):**

- **ARMArchitectureFundamentals–https://youtu.be/7LqPJGnBPMM**
- **https://www.youtube.com/watch?v=cP6NxivTY94&list=PLbMVogVj5nJRDS4w20GO7l4SepLhuAj9X&index=17**
- **https://www.youtube.com/watch?v=Kju5UMLC7hg**

https://nptel.ac.in/courses/108105057:byProf.R.MallandProf.A.Patra,IITKharagpur

**SkillDevelopmentActivitiesSuggested**

1) Interactwithindustry(small,medium,andlarge).
2) Involveinresearch/testing/projectstounderstandtheirproblemsandhelpcreativeandinnovativemethodstosolvetheproblem.
3) Involveincase studiesandfieldvisits/fieldwork.
4) Accustomtotheuse ofstandards/codesetc.,tonarrowthe gapbetweenacademia andindustry.
5) Handleadvancedinstrumentstoenhancetechnicaltalent.
6) Gainconfidenceinmodellingof systemsandalgorithmsfortransientandsteady-state operations,thermalstudy,etc.
7) Workondifferentsoftware/s(tools) tosimulate,analyzeandauthenticatetheoutputtointerpretandconclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills,Statisticalanalysis,fiscalexpertise,etc.
Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learningand application skills of the study they have undertaken. The students with the help of the course teacher can take up relevanttechnical–activitieswhichwillenhance theirskill.The preparedreportshallbeevaluatedfor CIEmarks.

**Courseoutcome(CourseSkillSet)**

Attheendof thecoursethestudentwillbeableto:

| Sl.No. | Description | BloomsLevel |
|---|---|---|
| CO1 | Describethearchitecture,modesofoperation,memoryorganization,interruptsofARMCortex-M3familyof microprocessors. | L1 |
| CO2 | DescribetheprogrammingandinterruptsofARMCortex-M3familyofmicroprocessors. | L1 |
| CO3 | DemonstrateperipheralinterfacingwithadvancedprogrammingofARMCortex-M3/M4microcontrollersforreal-timeapplications. | L2 |

**ProgramOutcomeofthiscourse**

| Sl.No. | Description | POs |
|---|---|---|
| 1. | Independentlycarryoutresearch/investigationanddevelopmentworktosolvepractical problemsrelatedtoVLSIDesignandembeddedsystems. | PO1 |
| 2. | Demonstrate adegreeofmasteryoverthe areas ofVLSI Design andembeddedsystems.Themasteryshouldbeatalevelhigherthantherequirementsinthebachelor'sinElectronics& | PO2CommunicationEngineering. |
| 3. | Applyappropriatemethodologyandmodernengineering/ITtoolstomeettheinternational standardsinthe area ofVLSIdesignandembeddedsystems. | PO3 |
| 4. | AcquirecompetencyinareasofVLSIandEmbeddedSystems,ICFabrication,Design,Testing,Verificationand dIntegratemultiplesub-systemstodevelopSystemOnChiptooptimizeits | PO4performanceandexcelinindustrysectorsrelatedtoVLSI/ Embeddeddomain. |
| 5. | Understandimpactofprofessionalengineeringsolutionsinsocietalandenvironmental contextsanddemonstrate theknowledge for sustainable development. | PO5 |

| Real Time Operating System | | | |
|---|---|---|---|
| Course Code | MLVS204 | CIE Marks | 50 |
| Teaching Hours/Week(L:P:SDA) | 3:0:0 | SEE Marks | 50 |
| Total Hours of Pedagogy | 40hoursTheory | Total Marks | 100 |
| Credits | 03 | Exam Hours | 03 |

**CourseLearningObjectives:**

1. Toexplaintheconceptofareal-timesystemandwhythesesystemsareusuallyimplementedasconcurrentprocesses
2. Todescribeadesignprocessforreal-timesystems.
3. Toexplaintheroleof a real-timeoperatingsystems.
4. TointroducedebuggingprocessarchitecturesRTOS.

**Module-1**

**Real-Time Systems and Resources**: Brief history of Real Time Systems, A brief history of Embedded Systems.SystemResources,ResourceAnalysis,Real-TimeServiceUtility,Schedulerconcepts,Real-TimeOS,Statetransitiondiagramandtables, ThreadSafeReentrantFunctions.(Text1:SelectedsectionsfromChap.1,2)

**RBT Levels:** L2, L3

**Module-2**

**ProcessingwithRealTimeScheduling**:SchedulerConcepts,PreemptiveFixedPrioritySchedulingPolicieswithtimingdiagramsandproblemsandissues,Feasibility,RateMonotonicleastupperbound,NecessaryandSufficientfeasibility,Deadline–Monotonic Policy,Dynamicprioritypolicies,AlternativetoRMpolicy.

**RBT Levels:** L2, L3

**Module-3**

**Memory and I/O**: Worst case execution time, Intermediate I/O, Shared Memory, ECC Memory, Flash file systems.Multi-resourceServices,Blocking,Deadlockandlivelock,Criticalsectionstoprotectsharedresources,Missed deadline,QoS,ReliabilityandAvailability,Similaritiesanddifferences,Reliablesoftware,Availablesoftware.

**RBT Levels:** L2, L3

**Module-4**

**FirmwareComponents**:The3firmwarecomponents,RTOSsystemsoftwaremechanisms,Softwareapplication components.DebuggingComponents,Exceptions,assert,Checkingreturncodes,Single-stepdebugging,Testaccessports, TracePorts.

**RBT Levels:** L2, L3

**Module-5**

**ProcessandThreads**:Processandthreadcreations,Programsrelatedtosemaphores,messagequeue,sharedBufferapplicationsinvolvingintertask/threadcommunication

**RBT Levels:** L2, L3

## AssessmentDetails(bothCIEandSEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. Theminimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of themaximum marks of SEE.A student shall be deemed to have satisfied the academic requirements and earned thecredits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sumtotalof theCIE(ContinuousInternalEvaluation)andSEE(SemesterEndExamination)takentogether.

## ContinuousInternalEvaluation:

1. TwoUnitTests eachof**25Marks**
2. Twoassignmentseachof **25Marks**or**oneSkillDevelopmentActivityof50marks** toattaintheCOs andPOs

Thesumoftwotests,twoassignments/skillDevelopmentActivities,willbe**scaleddownto50marks**
**CIEmethods/questionpaperisdesignedtoattainthedifferentlevelsofBloom'staxonomyaspertheoutcomedefinedforthecourse.**

## Semester-EndExamination:

1. TheSEEquestionpaperwillbesetfor100marksandthemarksscoredwillbeproportionatelyreducedto50.
2. Thequestionpaperwillhavetenfullquestionscarrying equalmarks.
3. Eachfullquestionisfor20marks.Therewillbetwofullquestions(withamaximumoffoursub-questions)fromeachmodule.
4. Eachfullquestionwillhaveasub-questioncoveringallthetopicsunderamodule.
5. Thestudentswillhavetoanswerfivefullquestions, selecting onefullquestionfromeachmodule

**SuggestedLearningResources:**

**Books**

TextBooks:1.SamSiewert,"Real-TimeEmbeddedSystemsandComponents",CengageLearningIndiaEdition,2007.
2.Dr.K.V.K.KPrasad,Embedded/RealTimeSystems,Concepts,DesignandProgramming,BlackBook,DreamTechPress,Newedition,2010.

ReferenceBooks:1.JamesWSLiu,"RealTime System",Pearsoneducation,2008.
2.Dream TechSoftwareTeam,"ProgrammingforEmbeddedSystems",JohnWiley,IndiaPvt.Ltd.,2008.

**WeblinksandVideoLectures(e-Resources):**

- https://www.youtube.com/watch?v=dHsHP9RrXBw&list=PLJ5C_6qdAvBH-JNRIlupFb44miyx9M8JD

**SkillDevelopmentActivitiesSuggested:**

1) Interactwithindustry(small,medium,andlarge).
2) Involveinresearch/testing/projectstounderstandtheirproblemsandhelpcreativeand innovativemethods tosolvetheproblem.
3) Involveincase studiesandfieldvisits/fieldwork.
4) Accustomtotheuse ofstandards/codesetc.,tonarrowthe gapbetweenacademia andindustry.
5) Handleadvancedinstrumentstoenhancetechnicaltalent.
6) Gainconfidenceinmodellingof systemsandalgorithmsfortransientandsteady-state operations,thermalstudy,etc.
7) Workondifferentsoftware/s(tools) tosimulate,analyzeandauthenticatetheoutputtointerpretandconclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills,Statisticalanalysis,fiscalexpertise,etc.
Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learningand application skills of the study they have undertaken. The students with the help of the course teacher can take up relevanttechnical–activitieswhichwillenhancetheir skill.The preparedreportshallbeevaluatedfor CIEmarks.

**Courseoutcome(CourseSkillSet)**

Attheendof thecoursethestudentwillbeableto:

| Sl.No. | Description | LEVELS |
|---|---|---|
| 1 | Developprogramsforrealtimeservices,firmwareandRTOS,usingthefundamentalsofRealTime EmbeddedSystem,realtimeserviceutilities,debuggingmethodologiesand optimizationtechniques. | L6 |
| 2 | Select the appropriate system resources (CPU, I/O, Memory,Cache,ECCMemory,Microcontroller/FPGA/ASICtoimprovethesystemperformance. | L1,L2 |
| 3 | Applyprioritybasedstaticanddynamicrealtimeschedulingtechniquesforthegiven specifications | L3 |
| 4 | Analyzedeadlockconditions,sharedmemoryproblem,criticalsectionproblem,misseddeadlines,availability,reliabilityandQoS. | L4 |
| 5 | Develop programsformulti-threadedapplicationsusingsuitabletechniquesanddata | L6 |

**ProgramOutcomeofthiscourse**

| Sl.No. | Description | POs |
|---|---|---|
| **1.** | Independentlycarryoutresearch/investigationanddevelopmentworktosolvepracticalproblemsrelatedtoVLSI Designandembeddedsystems. | PO1 |
| 2. | Demonstrate a degree of mastery over the areas of VLSI Design and embeddedsystems. The mastery should be at a level higher than the requirements in thebachelor'sinElectronics&CommunicationEngineering. | PO2 |
| 3. | Applyappropriatemethodologyandmodernengineering/ITtoolstomeettheinternationalstandardsintheareaofVLSI designandembeddedsystems. | PO3 |
| 4. | AcquirecompetencyinareasofVLSIandEmbeddedSystems,ICFabrication,Design,Testing, Verification and Integrate multiple sub-systems to develop System On Chipto optimize its performance and excel in industry sectors related to VLSI /Embeddeddomain. | PO4 |
| 5. | Understandimpactofprofessionalengineeringsolutionsinsocietaland environmental contexts and demonstrate the knowledge for sustainabledevelopment. | PO5 |

| Fin FETs and Other Multi-Gate Transistors | | | |
|---|---|---|---|
| Course Code | MLVS215A | CIE Marks | 50 |
| Teaching Hours/Week(L:P:SDA) | 3:0:0 | SEE Marks | 50 |
| Total Hours of Pedagogy | 40hoursTheory | Total Marks | 100 |
| Credits | 03 | Exam Hours | 03 |

**CourseLearningobjectives:**

- TolearntheevolutionofSOIMOStransistor.
- Tohaveaninsightintothinfilmformationtechniquesandadvancedgatestackdeposition.
- ToenablethestudentstoanalysephysicsbehindBSIM-CMG.
- Toanalysetheelectrostaticsof themulti-gateMOSsystem.
- Torealisetheinterrelationshipbetweenthemulti-gateFET deviceproperties anddigitalandanalogcircuits.

**Module-1**

**TheSOIMOSFET:**FromSingleGatetoMultiGate:AbriefhistoryofMultiple-GateMOSFETs,MultiGateMOSFETphysics.

**RBT Levels:** L2, L3

**Module-2**

**MultigateMOSFETTechnology:**Introduction,ActiveArea:Fins,GateStack

**RBT Levels:** L2, L3

**Module-3**

**BSIM-CMG:**ACompactModelforMult-GateTransistors:Introduction,FrameworkforMultiGateFETModeling,MultiGateModels, BSIM-CMG andBSIM-IMG, BSIM-CMG.

**RBT Levels:** L2, L3

**Module-4**

**PhysicsoftheMultiGateMOSsystem:**Deviceelectrostatics,DoublegateMOSsystem,Two-dimensionalconfinement

**RBT Levels:** L2, L3

**Module-5**

**Multi-GateMOSFETcircuitDesign:**Introduction,DigitalCircuitDesign,AnalogCircuitDesign

**RBT Levels:** L2, L3

## AssessmentDetails(bothCIEandSEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. Theminimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of themaximum marks of SEE.A student shall be deemed to have satisfied the academic requirements and earned thecredits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sumtotalof theCIE(ContinuousInternalEvaluation)andSEE(SemesterEndExamination)takentogether.

## ContinuousInternalEvaluation:

1. TwoUnitTests eachof**25Marks**
2. Twoassignmentseachof **25Marks**or**oneSkillDevelopmentActivityof50marks** toattaintheCOs andPOs

Thesumoftwotests,twoassignments/skillDevelopmentActivities,willbe **scaleddownto50marks**

**CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per theoutcomedefinedforthecourse.**

## Semester-EndExamination:

1. TheSEEquestionpaperwillbesetfor100marksandthemarksscoredwillbeproportionatelyreducedto50.
2. Thequestionpaperwillhavetenfullquestionscarrying equalmarks.
3. Eachfullquestionisfor20marks.Therewillbetwofullquestions(withamaximumoffoursub-questions)fromeachmodule.
4. Eachfullquestionwillhaveasub-questioncoveringallthetopics underamodule.
5. Thestudentswillhavetoanswerfivefullquestions, selecting onefullquestionfromeachmodule

| **Suggested Learning Resources:Books** |
| --- |

1) J.P.Colinge,:FinFETsandother Multi-GateTransistors,springer,Serieson IntegratedCircuitsandSystems.
2) SamarSaha,: FinFETDevicesforVLSICircuitsandSystems,CRCPress, FirstEdition,2020
3) WeihuaHan,ZhimingM.Wang,:TowardQuantumFinFET,Springer Cham,FirstEdition2021.
4) YogeshsinghChauhan,DarsenD,et.al,FinFETModelingforICSimulationandDesign:usingtheBSIM-CMGstandard,AcademicPress,2015.

**WeblinksandVideoLectures(e-Resources):**

1. http://www.ee.iitb.ac.in
2. http://onlinecourses.nptel.ac.in
3. http;//icmaskdesign.com
4. http;//link.springer.com

**SkillDevelopmentActivitiesSuggested**

1) Interactwithindustry(small,medium,andlarge).
2) Involveinresearch/testing/projectstounderstandtheirproblemsandhelpcreativeandinnovativemethodstosolvetheproblem.
3) Involveincase studiesandfieldvisits/fieldwork.
4) Accustomtotheuse ofstandards/codesetc.,tonarrowthe gapbetweenacademia andindustry.
5) Handleadvancedinstrumentstoenhancetechnicaltalent.
6) Gainconfidenceinmodellingof systemsandalgorithmsfortransientandsteady-state operations,thermalstudy,etc.
7) Workondifferentsoftware/s(tools) tosimulate,analyzeandauthenticatetheoutputtointerpretandconclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills,Statisticalanalysis,fiscalexpertise,etc.
Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learningand application skills of the study they have undertaken. The students with the help of the course teacher can take up relevanttechnical–activitieswhichwillenhance theirskill.The preparedreportshallbeevaluatedfor CIEmarks.

**Courseoutcome(CourseSkillSet)**

Attheendof thecoursethestudentwillbeableto:

| Sl.No. | Description | BloomsLevel |
|---|---|---|
| CO1 | ListouttheadvantagesandchallengesofMulti-gateFinFETs. | L1 |
| CO2 | Describethinfilmformationtechnique,gatestackdepositionandphysicsbeyond BSIMCMG | L2 |
| CO3 | AnalyseelectrostaticsofmultI-gateMOSsystemandcorelatemultigateFETdevice propertiesandelementarydigitalandanalogcircuits. | L4 |

**ProgramOutcomeofthiscourse**

| Sl.No. | Description | POs |
|---|---|---|
| 1. | Independentlycarryout research/investigationanddevelopmentworktosolvepracticalproblemsrelatedtoVLSIDesignandembeddedsystems. | PO1 |
| 2. | Demonstrate a degree of mastery over the areas of VLSI Design and embedded systems. Themastery should be at a level higher than the requirements in the bachelor's in Electronics &CommunicationEngineering. | PO2 |
| 3. | Applyappropriatemethodologyandmodernengineering/ITtoolstomeettheinternationalstandardsinthe area ofVLSIdesignandembeddedsystems. | PO3 |
| 4. | Acquire competency in areas of VLSI and Embedded Systems, IC Fabrication, Design, Testing,Verification and Integrate multiple sub-systems to develop System On Chip to optimize itsperformanceandexcelinindustrysectorsrelatedtoVLSI/ Embeddeddomain. | PO4 |
| 5. | Understandimpactofprofessionalengineeringsolutionsinsocietalandenvironmentalcontextsand demonstratethe knowledge forsustainable development. | PO5 |

| Hard ware Security | | | |
|---|---|---|---|
| Course Code | MLVS215B | CIE Marks | 50 |
| Teaching Hours/Week(L:P:SDA) | 3:0:0 | SEE Marks | 50 |
| Total Hours of Pedagogy | 40hoursTheory | Total Marks | 100 |
| Credits | 03 | Exam Hours | 03 |

**CourseLearningobjectives:**

- TounderstandthecurrentpracticeofSoCdesignandvalidationmethodology.
- TounderstandtheSecurityassetsandattackmodels.
- TolearnthedetectionofhardwareTrojans inIPs

**Module-1**

**SecurityandTrustVulnerabilitiesinThird-PartyIPs:**DesignandValidationofSoCs,SecurityandTrustVulnerabilitiesinThird-PartyIPs,TrustworthySoCDesignUsingUntrustedIps

**RBT Levels:** L2, L3

**Module-2**

**SecurityRuleCheck**:Introduction,SecurityAssetsandAttackModels,DSeRC:DesignSecurityRuleCheck,Development of DSeRCFramework

**RBT Levels:** L2, L3

**Module-3**

DigitalCircuitVulnerabilitiestoHardwareTrojans:Introduction,TheGate-LevelDesignVulnerabilityAnalysisFlow,TheLayout-LevelDesignVulnerabilityAnalysisFlow,TrojanAnalyses

**RBT Levels:** L2, L3

**Module-4**

CodeCoverageAnalysisforIPTrustVerification,HardwareTrojanStructure,RelatedWork,ACaseStudyfor IPTrustVerification,SimulationResults

**RBT Levels:** L2, L3

**Module-5**

SecurityBasedonPhysicalUnclonabilityandDisorder:Introduction,UniqueObjects,WeakPhysicalUnclonableFunctions, StrongPhysicalUnclonableFunctions, ControlledPhysicalUnclonableFunctions,

**RBT Levels:** L2, L3

## AssessmentDetails(bothCIEandSEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. Theminimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% ofthemaximummarksofSEE.Astudentshallbedeemedtohavesatisfiedtheacademicrequirementsandearnedthe credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) inthesumtotaloftheCIE(ContinuousInternalEvaluation)andSEE(SemesterEndExamination)takentogether.**Continuous Internal Evaluation:**

1. TwoUnitTests eachof**25Marks.**
2. Twoassignmentseachof **25Marks**or**oneSkillDevelopmentActivityof50marks** toattaintheCOs andPOs

Thesumoftwotests,twoassignments/skillDevelopmentActivities,willbe **scaleddownto50marks**

**CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per theoutcomedefinedforthecourse.**

## Semester-EndExamination:

1. The SEEquestionpaperwillbesetfor100marksandthemarksscoredwillbeproportionatelyreducedto50.
2. Thequestionpaperwillhavetenfullquestionscarrying equalmarks.
3. Eachfullquestionisfor20marks.Therewillbetwofullquestions(withamaximumoffoursub-questions)fromeachmodule.
4. Eachfullquestionwillhaveasub-questioncoveringallthetopics underamodule.
5. Thestudentswillhavetoanswerfivefullquestions, selecting onefullquestionfromeachmodule

**SuggestedLearningResources:**

**Books**

- HardwareIPSecurityandTrust,PrabhatMishra•SwarupBhunia•MarkTehranipoorEditors©SpringerInternationalPublishing AG 2017.
- Introduction toHardware SecurityandTrust,MohammadTehranipoor•CliffWangEditors,SpringerScience+BusinessMedia, LLC 2012.
- HARDWARE SECURITY Design, Threats, and Safeguards Debdeep Mukhopadhyay Rajat Subhra Chakraborty Indian Institute of Technology Kharagpur West Bengal, India.

**WeblinksandVideoLectures(e-Resources):**

https://archive.nptel.ac.in/courses/106/105/106105194/

**SkillDevelopmentActivitiesSuggested**

1) Interactwithindustry(small,medium,andlarge).
2) Involveinresearch/testing/projectstounderstandtheirproblemsandhelpcreativeandinnovativemethodstosolvetheproblem.
3) Involveincasestudiesandfieldvisits/ fieldwork.
4) Accustomtotheuseofstandards/codesetc.,tonarrowthegapbetweenacademiaandindustry.
5) Handleadvancedinstrumentstoenhancetechnicaltalent.
6) Gainconfidenceinmodellingofsystemsandalgorithmsfortransientandsteady-stateoperations,thermalstudy, etc.
7) Workondifferentsoftware/s(tools)tosimulate,analyzeandauthenticatetheoutputtointerpretanddconclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities,management skills, Statistical analysis, fiscal expertise, etc. Students and the course instructor/s to involveeither individually or in groups to interact together to enhance the learning and application skills of thestudytheyhaveundertaken. Thestudents withthehelpof thecourseteachercantakeuprelevanttechnical –activitieswhichwillenhancetheirskill. Thepreparedreportshallbeevaluatedfor CIEmarks.

**Courseoutcome(CourseSkillSet)**

Attheendof thecoursethestudentwillbeableto:

| Sl.No. | Description | BloomsLevel |
|---|---|---|
| CO1 | DescribethecurrentpracticeofSoCdesignandvalidationmethodologyand | L1 |
| | securityandtrustvulnerabilitiesinthird-partyIPs. Section. | |
| CO2 | Presenttherulesandmetricswhicharerequiredtoquantitativelyanalyze | |
| | vulnerabilitiesanddevelopmentDSeRC framework | L3 |
| CO3 | Analysethegate-levelvulnerabilityflow | L4 |
| CO4 | Understandthe detectionof hardwareTrojansin3PIPs L2CO5 | |
| | Realizing secureand reliableidentification, authentication, andintegrity checking ofnetworkedsmartobjects. | L3,L6 |

| ProgramOutcomeofthiscourse | | |
|---|---|---|
| **Sl.No.** | **Description** | **POs** |
| 1. | Independentlycarryoutresearch/investigationanddevelopmentworktosolvepracticalproblemsrelatedtoVLSI Designandembeddedsystems. | PO1 |
| 2. | Demonstrateadegree ofmasteryoverthe areasofVLSIDesignandembedded systems.Themasteryshouldbeatalevelhigherthantherequirementsinthebachelor'sinElectronics&CommunicationEngineering. | PO2 |
| 3. | Applyappropriatemethodologyandmodernengineering/ITtoolstomeettheinternationalstandardsintheareaof VLSIdesignandembeddedsystems. | PO3 |
| 4. | Acquire competency in areas of VLSI and Embedded Systems, IC Fabrication, Design,Testing,VerificationandIntegratemultiplesub-systemstodevelopSystemOnChiptooptimize its performance and excel in industry sectors related to VLSI / Embeddeddomain. | PO4 |
| 5. | Understandimpactofprofessionalengineeringsolutionsinsocietalandenvironmentalcontexts and demonstrate theknowledge for sustainable development. | PO5 |
| | | |

| Static Timing Analysis | | | |
|---|---|---|---|
| Course Code | MLVS215C | CIE Marks | 50 |
| Teaching Hours/Week(L:P:SDA) | 3:0:0 | SEE Marks | 50 |
| Total Hours of Pedagogy | 40hoursTheory | Total Marks | 100 |
| Credits | 03 | Exam Hours | 03 |

**CourseLearningobjectives:**

- TounderstandtheSTAEnvironmentandconcepts.
- Toknowstandardcelllibrarywithtiming modelanddelaymodel.
- Tostudydelaycalculationsandtiming verificationconceptsofflip-flops.

**Module-1**

Introduction: Nanometer Designs, What is Static Timing Analysis? Why Static Timing Analysis?, Crosstalk andNoise, Design Flow, CMOS Digital Designs, FPGA Designs, Asynchronous Designs, STA at Different Design Phases,LimitationsofStaticTimingAnalysis,PowerConsiderations,ReliabilityConsiderationsSTAConcepts:CMOSLogicDesign, Basic MOS Structure, CMOS Logic Gate, Standard Cells, Modeling of CMOS Cells, Switching Waveform,PropagationDelay,SlewofaWaveform,SkewbetweenSignals,TimingArcsandUnateness,Minand Max Timing
Paths,ClockDomains,OperatingConditions

**RBT Levels:** L2, L3

**Module-2**

StandardCellLibrary:PinCapacitance,TimingModeling,LinearTimingModel,Non-LinearDelayModel,Exampleof Non-Linear, Delay Model Lookup, Threshold Specifications and Slew Derating Timing Models - CombinationalCells,DelayandSlewModels,PositiveorNegativeUnate,GeneralCombinationalBlock,TimingModels-SequentialCells,SynchronousChecks:SetupandHold,ExampleofSetupandHoldChecks,NegativeValuesinSetupandHoldChecks,AsynchronousChecks,RecoveryandRemovalChecksPulseWidthChecks,ExampleofRecovery,Removaland Pulse Width Checks, Propagation Delay, State- Dependent Models XOR,XNOR and Sequential Cells, InterfaceTimingModelforaBlackBox,AdvancedTimingModeling,ReceiverPinCapacitance,SpecifyingCapacitanceatthePinLevel,SpecifyingCapacitanceattheTimingArcLevel,OutputCurrent,ModelsforCrosstalkNoiseAnalysis,DCCurrent, Output Voltage, Propagated Noise, Noise Models for Two-Stage Cells, Noise Models for Multi-stage andsequentialCells, OtherNoiseModels,PowerDissipationModeling, ActivePower

**RBT Levels:** L2, L3

**Module-3**

Interconnect Parasitics: RLC for Interconnect, Wireload Models, Interconnect Trees, Specifying Wire load Models,Representation of Extracted Parasitic, Detailed Standard Parasitic Format ,Reduced Standard Parasitic Format,StandardParasiticExchangeFormat,RepresentingCouplingCapacitances,HierarchicalMethodology,BlockReplicated in Layout, Reducing Parasitic for Critical Nets, Reducing Interconnect Resistance, Increasing WireSpacing, Parasitics for Correlated Nets. Delay Calculation: Overview, Delay Calculation Basics, Delay Calculationwith Interconnect, Pre-layout Timing, Post-layout Timing, Cell Delay using Effective Capacitance, InterconnectDelay, Elmore Delay, Higher Order Interconnect Delay Estimation, Full Chip Delay Calculation, Slew Merging,Different SlewThresholds,DifferentVoltage Domains,PathDelay Calculation,Combinational PathDelay,Pathto
a Flip-flop, InputtoFlip-flopPath,Flip-floptoFlip-flopPath,MultiplePaths, SlackCalculation.

**RBT Levels:** L2, L3

**Module-4**

Configuring the STA Environment: What is theSTA Environment? Specifying Clocks, Clock Uncertainty, ClockLatency, Generated Clocks, Example of Master Clock at Clock Gating Cell Output, Generated Clock using Edge andEdgeshiftOptions,GeneratedClockusingInvertOption,ClockLatencyforGeneratedClocks,TypicalClockGeneration Scenario, Constraining Input Paths, Constraining Output Paths, Example A, Example B, Example TimingPathGroups,ModelingofExternalAttributes,ModelingDriveStrengths,ModelingCapacitiveLoad,DesignRule Checks,VirtualClocks,

**RBT Levels:** L2, L3

**Module-5**

Timing Verification: Setup Timing Check, Flip-flop to Flip-flop Path, Input to Flip-flop Path, Input Path with ActualClock, Flip flop to Output Path, Input to Output Path, Frequency Histogram, Hold Timing Check, Flip-flop to FlipflopPath, Hold Slack Calculation, Input to Flip-flop Path, Flip-flop to Output Path, Flip-flop to Output Path with ActualClock, Input to Output Path, Multicycle Paths, Crossing Clock Domains, False Paths, Half- Cycle Paths, RemovalTimingCheck,RecoveryTimingCheck,TimingacrossClockDomains,SlowtoFastClockDomains,FasttoSlowClock
Domains, Half-cyclePath- Case1, Half-cyclePath-Case2,FasttoSlowClockDomain, SlowtoFastClockDomain

**RBT Levels:** L2, L3

## AssessmentDetails(bothCIEandSEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. Theminimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of themaximum marks of SEE.A student shall be deemed to have satisfied the academic requirements and earned thecredits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sumtotalof theCIE(ContinuousInternalEvaluation)andSEE(SemesterEndExamination)takentogether.

## ContinuousInternalEvaluation:

1. TwoUnitTests eachof**25Marks**
2. Twoassignmentseachof **25Marks**or**oneSkillDevelopmentActivityof50marks** toattaintheCOs andPOs

Thesumoftwotests,twoassignments/skillDevelopmentActivities,willbe **scaleddownto50marks**

**CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per theoutcomedefinedforthecourse.**

## Semester-EndExamination:

1. TheSEEquestionpaperwillbesetfor100marksandthemarksscoredwillbeproportionatelyreducedto50.
2. Thequestionpaperwillhavetenfullquestionscarrying equalmarks.
3. Eachfullquestionisfor20marks.Therewillbetwofullquestions(withamaximumoffoursub-questions)fromeachmodule.
4. Eachfullquestionwillhaveasub-questioncoveringallthetopicsunderamodule.
5. Thestudentswillhavetoanswerfivefullquestions, selecting onefullquestionfromeachmodule

**SuggestedLearningResources:**

**Books**

1. J.Bhasker,R Chadha,"StaticTimingAnalysis forNanometerDesigns:APracticalApproach",Springer2009ReferenceBooks

2. SridharGangadharan,SanjayChuriwala,"ConstrainingDesignsforSynthesisandTimingAnalysis– APracticalGuidetoSynopsisDesignConstraints(SDC)", Springer, 2013

3. NareshMaheshwariandSachinSapatnekar,"TimingAnalysisandOptimizationofSequentialCircuits",SpringerScience andBusinessMedia, 1999

**WeblinksandVideoLectures(e-Resources):**

- https://www.youtube.com/watch?v=KlUn2GjNOfY&list=PLYdInKVfi0Ka5c6kraib5qiCFhPWE9G6e
- https://www.youtube.com/watch?v=yYR8BzysTmM&list=PLYdInKVfi0Ka5c6kraib5qiCFhPWE9G6e&index=2

**SkillDevelopmentActivitiesSuggested**

1) Interactwithindustry(small,medium,andlarge).
2) Involveinresearch/testing/projectstounderstandtheirproblemsandhelpcreativeandinnovativemethodstosolvetheproblem.
3) Involveincasestudiesandfieldvisits/ fieldwork.
4) Accustomtotheuseofstandards/codesetc.,tonarrow thegapbetweenacademia andindustry.
5) Handleadvancedinstrumentstoenhancetechnicaltalent.
6) Gainconfidenceinmodellingofsystemsandalgorithmsfortransientandsteady-stateoperations,thermalstudy, etc.
7) Workondifferentsoftware/s(tools)tosimulate,analyzeandauthenticate theoutputtointerpretandconclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities,management skills, Statistical analysis, fiscal expertise, etc. Students and the course instructor/s to involve eitherindividuallyoringroupstointeracttogethertoenhancethelearningandapplicationskillsof thestudytheyhaveundertaken.Thestudentswiththehelpof thecourseteachercantakeuprelevanttechnical–activitieswhichwill
enhancetheirskill. ThepreparedreportshallbeevaluatedforCIEmarks.

**Courseoutcome(CourseSkillSet)**

Attheendof thecoursethestudentwillbeable to:

| Sl.No. | Description | BloomsLevel |
|---|---|---|
| CO1 | Evaluatethedelayofanygivendigitalcircuits | L5 |
| CO2 | Preparetheresourcestoperform thestatictiminganalysisusingEDAtool | L6 |
| CO3 | Preparetimingconstraints for thedesign basedon thespecification. | L6 |
| CO4 | Generatethetiminganalysis reportusingEDAtoolfordifferentchecks. | L6 |
| CO5 | Performverificationandanalysethegeneratedreporttoidentifycriticalissuesand bottleneck fortheviolation andsuggestthetechniques tomakethedesigntomeettiming | L3 |

**ProgramOutcomeofthiscourse**

| Sl.No. | Description | POs |
|---|---|---|
| 1. | Independentlycarryoutresearch/investigationanddevelopmentworktosolve practicalproblemsrelatedtoVLSI Designandembeddedsystems. | PO1 |
| 2. | Demonstrateadegree ofmasteryoverthe areasofVLSIDesignandembeddedsystems.Themasteryshouldbeatalevelhigherthantherequirements inthe bachelor'sinElectronics&CommunicationEngineering. | PO2 |
| 3. | Applyappropriatemethodologyandmodernengineering/ITtoolstomeetthe internationalstandardsinthearea of VLSI designandembeddedsystems. | PO3 |
| 4. | AcquirecompetencyinareasofVLSIandEmbeddedSystems,ICFabrication,Design,Testing,VerificationandIntegratemultiplesub-systemstodevelopSystemOnChipto optimizeitsperformanceandexcelinindustrysectorsrelatedtoVLSI/Embedded domain. | PO4 |
| 5. | Understandimpactofprofessionalengineeringsolutionsin societal andenvironmentalcontexts and demonstrate theknowledge for sustainable development. | PO5 |

| Embedded Linux System Design and Development Processing | | | |
|---|---|---|---|
| Course Code | MLVS215D | CIE Marks | 50 |
| Teaching Hours/Week(L:P:SDA) | 3:0:0 | SEE Marks | 50 |
| Total Hours of Pedagogy | 40hoursTheory | Total Marks | 100 |
| Credits | 03 | Exam Hours | 03 |

**CourseLearningobjectives:**

- TounderstandtheimportanceofEmbeddedLinuxinembeddedsystemdesign.
- ToGaintheknowledgeof BoardSupportPackage.
- ToAnalysethe memoryrequirementsfordesign.
- Tolearn theembeddeddriversandkernelmodules.
- TolearntheportingapplicationsfromtraditionalRTOS

**Module-1**

Introduction:HistoryofEmbeddedLinux,WhyEmbeddedLinux,EmbeddedLinuxVersusDesktopLinux,FrequentlyAskedQuestions,EmbeddedLinuxDistributions,PortingRoadmap.GettingStarted:ArchitectureofEmbeddedLinux,LinuxKernelArchitecture,UserSpace,LinuxStart-UpSequence,GNU CrossPlatformToolchain

**RBT Levels:** L2, L3

**Module-2**

BoardSupportPackage:InsertingBSPinKernelBuildProcedure,MemoryMap,InterruptManagement,ThePCI Subsystem,Timers, UART, PowerManagement

**RBT Levels:** L2, L3

**Module-3**

EmbeddedStorage:FlashMap,MTD—MemoryTechnologyDevice,MTDArchitecture,SampleMTDDriverforNORFlash,TheFlash-MappingDrivers,MTDBlockandCharacterDevices,MtdutilsPackage,EmbeddedFileSystems, OptimizingStorageSpace,Tuning Kernel Memory.

**RBT Levels:** L2, L3

**Module-4**

EmbeddedDrivers:Linux SerialDriver,EthernetDriver,I2CSubsystemonLinux,USBGadgets,WatchdogTimer,KernelModules

**RBT Levels:** L2, L3

**Module-5**

PortingApplications:ArchitecturalComparison,ApplicationPortingRoadmap,ProgrammingwithPthreads, Operating SystemPortingLayer(OSPL), KernelAPIDriver.

**RBT Levels:** L2, L3

## AssessmentDetails(bothCIEandSEE)

TheweightageofContinuousInternalEvaluation(CIE)is50%andforSemesterEndExam(SEE)is50%.Theminimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40%of the maximum marks of SEE.A student shall be deemed to have satisfied the academic requirements andearnedthecreditsallottedtoeachsubject/courseifthestudentsecuresnotlessthan50%(50marksoutof100)inthesumtotaloftheCIE(ContinuousInternalEvaluation)andSEE(SemesterEndExamination)takentogether.

## ContinuousInternalEvaluation:

1. TwoUnitTests eachof**25Marks**
2. Twoassignmentseachof **25Marks**or**oneSkillDevelopmentActivityof50marks** toattaintheCOs andPOs

Thesumoftwotests,twoassignments/skillDevelopmentActivities,willbe **scaleddownto50marks**
**CIEmethods/questionpaperisdesignedtoattainthedifferentlevelsofBloom'staxonomyaspertheoutcomedefinedforthecourse.**

## Semester-EndExamination:

1. TheSEEquestionpaperwillbesetfor100marksandthemarksscoredwillbeproportionatelyreducedto50.
2. Thequestionpaperwillhavetenfullquestionscarrying equalmarks.
3. Eachfullquestionisfor20marks.Therewillbetwofullquestions(withamaximumoffoursub-questions)fromeachmodule.
4. Eachfullquestionwillhaveasub-questioncoveringallthetopicsunderamodule.
5. Thestudentswillhavetoanswerfivefullquestions, selecting onefullquestionfromeachmodule

**SuggestedLearningResources:**

**Books**

1. P.Raghavan,AmolLad,SriramNeelakandan"EmbeddedLinuxSystemDesignAndDevelopment",AuerbachPublications,Taylor&FrancisGroup, 2006

2. KarimYaghmour,JonMasters,GiladBenYossef,andPhilippeGerum"BuildingEmbeddedLinuxSystems"O'Reillypublications,2ndedition

**WeblinksandVideoLectures(e-Resources):**

- https://www.youtube.com/watch?v=9vsu67uMcko

**SkillDevelopmentActivitiesSuggested**

1) Interactwithindustry(small,medium,andlarge).
2) Involveinresearch/testing/projectstounderstandtheirproblemsandhelpcreative andinnovativemethodstosolve the problem.
3) Involveincase studiesandfieldvisits/fieldwork.
4) Accustomtotheuse of standards/codesetc.,tonarrowthe gapbetweenacademia andindustry.
5) Handleadvancedinstrumentstoenhancetechnicaltalent.
6) Gainconfidenceinmodellingofsystemsandalgorithmsfortransientandsteady-stateoperations,thermalstudy,etc.
7) Workondifferentsoftware/s(tools)tosimulate,analyzeandauthenticatetheoutputtointerpretandconclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, managementskills, Statistical analysis, fiscal expertise, etc. Students and the course instructor/s to involve either individually orin groups to interact together to enhance the learning and application skills of the study they have undertaken. Thestudentswiththehelpof thecourseteachercantakeuprelevanttechnical–activitieswhichwillenhancetheirskill.
Thepreparedreportshallbeevaluatedfor CIEmarks.

**Courseoutcome(CourseSkillSet)**

Attheendof thecoursethestudentwillbeable to:

| Sl.No. | Description | Blooms Level |
|---|---|---|
| CO1 | Understand theembeddedLinuxdevelopmentenvironment | L1,L2 |
| CO2 | Understand andcreate LinuxBSPfora hardware platform | L1,L2 |
| CO3 | UnderstandtheLinuxmodelforembeddedstorageandwritedriversand applicationsforthesame | L1,L2 |
| CO4 | UnderstandvariousembeddedLinux driverssuchasserial,I2C,andso on | L1,L2 |
| CO5 | Portapplicationsto embeddedLinux fromatraditionalRTOS | L3 |

**ProgramOutcomeofthiscourse**

| Sl.No. | Description | POs |
|---|---|---|
| 1. | Independently carry outresearch/investigationand developmentworkto solvepractical problemsrelatedtoVLSIDesignandembeddedsystems. | PO1 |
| 2. | Demonstrateadegreeofmasteryovertheareasof VLSIDesignandembeddedsystems. Themasteryshouldbeatalevelhigherthantherequirementsinthebachelor'sin Electronics&CommunicationEngineering. | PO2 |
| 3. | Apply appropriate methodology and modern engineering/IT tools to meet the internationalstandardsinthearea ofVLSIdesignandembeddedsystems. | PO3 |
| 4. | AcquirecompetencyinareasofVLSIandEmbeddedSystems,ICFabrication,Design,Testing,Verificatio nandIntegratemultiplesub-systemstodevelopSystemOnChipto optimizeitsperformanceandexcelinindustrysectorsrelatedtoVLSI/Embeddeddomain. | PO4 |
| 5. | Understandimpactofprofessionalengineeringsolutionsinsocietalandenvironmental contextsanddemonstratethe knowledge forsustainable development. | PO5 |

| Reconfigurable Computing | | | |
|---|---|---|---|
| Course Code | MLVS216A | CIE Marks | 50 |
| Teaching Hours/Week(L:P:SDA) | 3:0:0 | SEE Marks | 50 |
| Total Hours of Pedagogy | 40hoursTheory | Total Marks | 100 |
| Credits | 03 | Exam Hours | 03 |

**CourseLearningobjectives:**

- Thiscoursewillenablestudentsto:
- TolearnthevariousReconfigurablesystems.
- TostudythedifferentLanguagesandCompilation.
- TounderstandtheImplementationof FPGA.
- TolearnPartialReconfigurationDesign
- TounderstandtheSignalProcessingApplications

**Module-1**

**Introduction**:History,ReconfigurablevsProcessorbasedsystem,RCArchitecture.
**ReconfigurableLogicDevices**:FieldProgrammable Gate Array,CoarseGrainedReconfigurableArrays.
**ReconfigurableComputing System:**ParallelProcessingonReconfigurableComputers,AsurveyofReconfigurableComputing System.

**RBT Levels:** L2, L3

**Module-2**

**LanguagesandCompilation**:DesignCycle,Languages,HDL,HighLevelCompilation,LowlevelDesignflow,Debugging ReconfigurableComputing Applications.

**RBT Levels:** L2, L3

**Module-3**

**Implementation**:Integration,FPGADesignflow,LogicSynthesis.
**HighLevelSynthesisforReconfigurableDevices**:Modelling,TemporalPartitioningAlgorithms.

**RBT Levels:** L2, L3

**Module-4**

**Partial Reconfiguration Design**: Partial Reconfiguration Design, Bitstream Manipulation with JBits, Themodular Design flow, The Early Access Design Flow, Creating Partially Reconfigurable Designs, PartialReconfigurationusing Hansel-C Designs, PlatformDesign.

**RBT Levels:** L2, L3

**Module-5**

**SignalProcessingApplications**:ReconfigurablecomputingforDSP,DSPapplicationbuildingblocks,Examples:Beamforming,SoftwareRadio,Imageandvideoprocessing,LocalNeighbourhoodfunctions, Convolution.**SystemonaProgrammableChip:**IntroductiontoSoPC,AdaptiveMultiprocessingonChip.

**RBT Levels:** L2, L3

## AssessmentDetails(bothCIEandSEE)

TheweightageofContinuousInternalEvaluation(CIE)is50%andforSemesterEndExam(SEE)is50%.Theminimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40%of the maximum marks of SEE.A student shall be deemed to have satisfied the academic requirements andearnedthecreditsallottedtoeachsubject/courseifthestudentsecuresnotlessthan50%(50marksoutof100)inthesumtotaloftheCIE(ContinuousInternalEvaluation)andSEE(SemesterEndExamination)takentogether.

## ContinuousInternalEvaluation:

1. TwoUnitTests eachof**25Marks**
2. Twoassignmentseachof **25Marks**or**oneSkillDevelopmentActivityof50marks** toattaintheCOs andPOs

Thesumoftwotests, twoassignments/skillDevelopmentActivities,willbe**scaleddownto50marks**

**CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as pertheoutcomedefinedforthecourse.**

## Semester-EndExamination:

1. TheSEEquestionpaperwillbesetfor100marksandthemarksscoredwillbeproportionatelyreducedto50.
2. Thequestionpaperwillhavetenfullquestionscarrying equalmarks.
3. Eachfullquestionisfor20marks.Therewillbetwofullquestions(withamaximumoffoursub-questions)fromeachmodule.
4. Eachfullquestionwillhaveasub-questioncoveringallthetopicsunderamodule.
5. Thestudentswillhavetoanswerfivefullquestions,selecting onefullquestionfromeachmodule

**SuggestedLearningResources:**

**Books**

1.Reconfigurable Computing:AcceleratingComputationwithField-Programmable Gate ArraysM.GokhaleandP. GrahamSpringer, ISBN:978-0-387-26105-82005

2.IntroductiontoReconfigurableComputing:Architectures,AlgorithmsandApplicationsC.BobdaSpringer,ISBN: 978-1-4020-6088-52007

**ReferenceBooks**

1. PracticalFPGAProgramminginC D. PellerinandS. ThibaultPrentice-Hall2005
2. FPGABasedSystemDesignW.Wolf Prentice-Hall2004
3. RapidSystemPrototypingwithFPGAs:AcceleratingtheDesignProcessR.CoferandB.HardingNewnes2005

**WeblinksandVideoLectures(e-Resources):**

- nptel.ac.in

**SkillDevelopmentActivitiesSuggested**

1) Interactwithindustry(small,medium,andlarge).
2) Involveinresearch/testing/projectstounderstandtheirproblemsandhelpcreativeandinnovativemethodstosolvetheproblem.
3) Involveincasestudiesandfieldvisits/ fieldwork.
4) Accustomtotheuseofstandards/codesetc.,tonarrowthegapbetweenacademiaandindustry.
5) Handleadvancedinstrumentstoenhancetechnicaltalent.
6) Gainconfidenceinmodellingofsystemsandalgorithmsfortransientandsteady-stateoperations,thermalstudy, etc.
7) Workondifferentsoftware/s(tools)tosimulate,analyzeandauthenticatetheoutputtointerpretandconclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities,management skills, Statistical analysis, fiscal expertise, etc. Students and the course instructor/s toinvolveeitherindividuallyoringroupstointeracttogethertoenhancethelearningandapplicationskillsof the study they have undertaken. The students with the help of the course teacher can take up relevanttechnical–activitieswhichwillenhancetheirskill. Thepreparedreportshallbeevaluatedfor CIEmarks.

**Courseoutcome(CourseSkillSet)**

Attheendof thecoursethestudentwillbeableto:

| Sl.No. | Description | Bloo msLe vel |
|---|---|---|
| CO1 | Understandthefundamentalprinciplesandpracticesinreconfigurablearchitecture | L2 |
| CO2 | Simulateandsynthesizethereconfigurablecomputing architectures. | L5 |
| CO3 | UnderstandtheFPGAdesignprinciples, andlogic synthesis | L2 |
| CO4 | Integratehardwareandsoftwaretechnologiesforreconfigurationcomputingfocusing onpartialreconfigurationdesign. | L3 |
| CO5 | Designdigitalsystemsforavarietyofapplicationsonsignalprocessingandsystemon chipconfigurations | L6 |

| Program Sl.No. | Outcomeofthiscourse Description | POs |
|---|---|---|
| 1. | Independentlycarryoutresearch/investigationanddevelopmentworktosolvepractical problemsrelatedtoVLSIDesignandembeddedsystems. | PO1 |
| 2. | Demonstrate adegreeofmasteryoverthe areas ofVLSI Design andembeddedsystems.Themasteryshouldbeatalevelhigherthantherequirementsinthebachelor'sin Electronics& CommunicationEngineering. | PO2 |
| 3. | Applyappropriatemethodologyandmodernengineering/ITtoolstomeettheinternational standardsinthe area ofVLSIdesignandembeddedsystems. | PO3 |
| 4. | AcquirecompetencyinareasofVLSIandEmbeddedSystems,ICFabrication,Design,Testing,Verificationand dIntegratemultiplesub-systemstodevelopSystemOnChiptooptimizeits performanceandexcelinindustrysectorsrelatedtoVLSI/ Embeddeddomain. | PO4 |
| 5. | Understandimpactofprofessionalengineeringsolutionsinsocietalandenvironmental contextsanddemonstrate theknowledge for sustainabledevelopment. | PO5 |

| Long Term Reliability of VLSI Systems | | | |
|---|---|---|---|
| Course Code | MLVS216B | CIE Marks | 50 |
| Teaching Hours/Week(L:P:SDA) | 3:0:0 | SEE Marks | 50 |
| Total Hours of Pedagogy | 40 hours Theory | Total Marks | 100 |
| Credits | 03 | Exam Hours | 03 |

**CourseLearningobjectives:**

- ToUnderstandtheVariousConceptsRelatedto ElectromigrationReliability.
- TostudytheFastEMStressEvolutionAnalysis.
- TostudytheEMAssessmentforPowerGridNetworks.
- TounderstandtheTransistorAging EffectsandReliability.
- TolearntheAging EffectsinSequentialElements.

**Module-1**

**ElectromigrationReliability**:WhyElectromigrationReliability?,Whysystem-levelEMReliabilityManagement? Physics- based EM Modeling, Electromigration Fundamentals, Stress based EM Modelingandstressdiffusionequations,ModelingfortransientEMeffectsandInitialstressconditions,postvoidingstressandvoidvolumeevolution,compactphysicsbasedEMmodelforasinglewire,otherrelevantEM modelsandanalysismethods.

**RBT Levels:** L2, L3

**Module-2**

**FastEMStressEvolutionAnalysis:**Introduction,TheLTIordinary differentialequations forEMstressevolution,ThepresentedKrylovfastEMstressanalysis,Numericalresultsanddiscussions.

**RBT Levels:** L2, L3

**Module-3**

**EMAssessmentforPowerGridNetworks**:Newpowergridreliabilityanalysismethod,cross-layouttemperatureandthermalstresscharacterization,impactofacross-layouttemperatureandthermalstress onEM.

**RBT Levels:** L2, L3

**Module-4**

**Transistor Aging Effects andReliability:**Introduction, Transistor reliability in advanced technologynodes,TransistorAging,BTI-BiasTemperatureInstability,HCI–HotCarrierInjection,CouplingmodelsforBTIandHCIdegradations,RTN–RandomTelegraphNoise,TDDB–TimeDependentDielectricBreakdown.

**RBT Levels:** L2, L3

**Module-5**

**AgingEffectsinSequentialElements:**Introduction,Background:flipfloptiminganalysis,processvariationmodel, voltagedroopmodel, Robustnessanalysis, reliability-awareflip-flopdesign.

**RBT Levels:** L2, L3

## AssessmentDetails(bothCIEandSEE)

TheweightageofContinuousInternalEvaluation(CIE)is50%andforSemesterEndExam(SEE)is50%.Theminimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40%of the maximum marks of SEE.A student shall be deemed to have satisfied the academic requirements andearnedthecreditsallottedtoeachsubject/courseifthestudentsecuresnotlessthan50%(50marksoutof100)inthesumtotaloftheCIE(ContinuousInternalEvaluation)andSEE(SemesterEndExamination)takentogether.

## ContinuousInternalEvaluation:

1. TwoUnitTests eachof**25Marks**
2. Twoassignmentseachof **25Marks**or**oneSkillDevelopmentActivityof50marks** toattaintheCOs andPOs

Thesumoftwotests,twoassignments/skillDevelopmentActivities,willbe **scaleddownto50marks**

**CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as pertheoutcomedefinedforthecourse.**

## Semester-EndExamination:

1. TheSEEquestionpaperwillbesetfor100marksandthemarksscoredwillbeproportionatelyreducedto50.
2. Thequestionpaperwillhavetenfullquestionscarrying equalmarks.
3. Eachfullquestionisfor20marks.Therewillbetwofullquestions(withamaximumoffoursub-questions)fromeachmodule.
4. Eachfullquestionwillhaveasub-questioncoveringallthetopicsunderamodule.
5. Thestudentswillhavetoanswerfivefullquestions,selecting onefullquestionfromeachmodule

**SuggestedLearningResources:**

**Books**

1.Long-TermReliabilityofNanometerVLSISystemsSheldonX.D.Tan,MehdiBaradaranTahoori,TaeyoungKim,SamanKiamehr,ZeyuSpringerInternationalPublishing1stEdition,2019ISBN:978-3-030-26171-9

**ReferenceBooks:**

1. ReliabilityWearoutMechanismsinAdvancedCMOSTechnologiesAlvinWayneStrong,Rolf-PeterVollertsen, Timothy D. Sullivan, Ernest Y. Wu, Giuseppe La Rosa, Jordi Sune Wiley, Copyright © theInstituteof ElectricalandElectronicsEngineers, Inc.2009PrintISBN:9780471731726
2. Hot-carrierReliabilityofMOSVLSICircuitsYusufLeblebici,SMKangSpringerScience&BusinessMedia1stEdition, 1993

Fundamentals of ElectromigrationAware Integrated Circuit Design Matthias Thiele, Jens Lienig SpringerInternationalPublishing 2018

**WeblinksandVideoLectures(e-Resources):**

nptel.ac.in

**SkillDevelopmentActivitiesSuggested**

1) Interactwithindustry(small,medium,andlarge).
2) Involveinresearch/testing/projectstounderstandtheirproblemsandhelpcreativeandinnovativemethodstosolvetheproblem.
3) Involveincasestudiesandfieldvisits/ fieldwork.
4) Accustomtotheuseofstandards/codesetc.,tonarrowthegapbetweenacademiaandindustry.
5) Handleadvancedinstrumentstoenhancetechnicaltalent.
6) Gainconfidenceinmodellingofsystemsandalgorithmsfortransientandsteady-stateoperations,thermalstudy, etc.
7) Workondifferentsoftware/s(tools)tosimulate,analyzeandauthenticatetheoutputtointerpretandconclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities,management skills, Statistical analysis, fiscal expertise, etc. Students and the course instructor/s toinvolveeitherindividuallyoringroupstointeracttogethertoenhancethelearningandapplicationskillsof the study they have undertaken. The students with the help of the course teacher can take up relevanttechnical–activitieswhichwillenhancetheirskill. Thepreparedreportshallbeevaluatedfor CIEmarks.

**Courseoutcome(CourseSkillSet)**

Attheendof thecoursethestudentwillbeableto:

| Sl.No. | Description | Blooms Level |
|---|---|---|
| CO1 | Comprehend the recent research in the area of interconnect and device reliability. | L2 |
| CO2 | Understandthephysics-basedEMmodeling. | L2 |
| CO3 | UnderstandtheunderlyingphenomenaofBTI,HCI,TDDBleadingtodevice-levelreliabilitydegradation. | L2 |
| CO4 | Relate to considerations at the circuit-level with both combinational and sequentialelements. | L4 |

**ProgramOutcomeofthiscourse**

| Sl.No. | Description | POs |
|---|---|---|
| 1. | Independentlycarryoutresearch/investigationanddevelopmentworktosolve practicalproblemsrelatedtoVLSI Designandembeddedsystems. | PO1 |
| 2. | Demonstrateadegree ofmasteryoverthe areasofVLSIDesignandembeddedsystems.Themasteryshouldbeatalevelhigherthantherequirementsinthe | PO2 |
| 3. | bachelor'sinElectronics&CommunicationEngineering. Applyappropriatemethodologyandmodernengineering/ITtoolstomeetthe internationalstandardsinthearea of VLSI designandembeddedsystems. | PO3 |
| 4. | AcquirecompetencyinareasofVLSIandEmbeddedSystems,ICFabrication,Design, Testing,VerificationandIntegratemultiplesub-systemstodevelopSystemOnChipto optimizeitsperformanceandexcelinindustrysectorsrelatedtoVLSI/Embedded domain. | PO4 |
| 5. | Understandimpactofprofessionalengineeringsolutionsin societal andenvironmentalcontexts and demonstrate theknowledge for sustainable | PO5 |

| Low Power VLSI Design | | | |
|---|---|---|---|
| Course Code | MLVS216C | CIE Marks | 50 |
| Teaching Hours/Week(L:P:SDA) | 3:0:0 | SEE Marks | 50 |
| Total Hours of Pedagogy | 40hoursTheory | Total Marks | 100 |
| Credits | 03 | Exam Hours | 03 |

**CourseLearningobjectives:**

- TostudyState-of-theartapproachesof powerestimationandreduction.
- Tounderstandpowerdissipationatvariouslevelsof design

**Module-1**

**Introduction:**Needforlow powerVLSIchips,charging anddischarging capacitance,shortcircuitcurrent in CMOS leakage current, static current, basic principles of low power design, low power figure of merits.Simulationpoweranalysis:SPICEcircuitsimulation, MonteCarlosimulation.

**RBT Levels:** L2, L3

**Module-2**

**Circuit:**Transistorandgatesizing,equivalentpinordering,networkrestructuringandreorganization,speciallatchesandflipflops, lowpowerdigitalcelllibrary, adjustabledevicethresholdvoltage.

**RBT Levels:** L2, L3

**Module-3**

**Logic:** Gatereorganization,signalgating,logicencoding,statemachineencoding,pre-computationlogic.LowpowerClockDistribution:Powerdissipationinclockdistribution,singledriverVsdistributedbuffers.

**RBT Levels:** L2, L3

**Module-4**

**Low power Architecture & Systems:** Power & performance management, switching activity reduction, flowgraphtransformation.Lowpowermemorydesign:Introduction,sourcesandreductionsofpowerdissipationinmemorysubsystem.

**RBT Levels:** L2, L3

**Module-5**

**Algorithm&ArchitecturalLevelMethodologies:**Introduction,designflow,Algorithmiclevelanalysis&optimization,Architecturallevelestimation&synthesis.AdvancedTechniques:Adiabaticcomputation, Asynchronouscircuits.

**RBT Levels:** L2, L3

## AssessmentDetails(bothCIEandSEE)

TheweightageofContinuousInternalEvaluation(CIE)is50%andforSemesterEndExam(SEE)is50%.Theminimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40%of the maximum marks of SEE.A student shall be deemed to have satisfied the academic requirements andearnedthecreditsallottedtoeachsubject/courseifthestudentsecuresnotlessthan50%(50marksoutof100)inthesumtotaloftheCIE(ContinuousInternalEvaluation)andSEE(SemesterEndExamination)takentogether.

## ContinuousInternalEvaluation:

1. TwoUnitTests eachof**25Marks**
2. Twoassignmentseachof **25Marks**or**oneSkillDevelopmentActivityof50marks** toattaintheCOs andPOs

Thesumoftwotests,twoassignments/skillDevelopmentActivities,willbe **scaleddownto50marks**
**CIEmethods/questionpaperisdesignedtoattainthedifferentlevelsofBloom'staxonomyaspertheoutcomedefinedforthecourse.**

## Semester-EndExamination:

1. TheSEEquestionpaperwillbesetfor100marksandthemarksscoredwillbeproportionatelyreducedto50.
2. Thequestionpaperwillhavetenfullquestionscarrying equalmarks.
3. Eachfullquestionisfor20marks.Therewillbetwofullquestions(withamaximumoffoursub-questions)fromeachmodule.
4. Eachfullquestionwillhaveasub-questioncoveringallthetopicsunderamodule.
5. Thestudentswillhavetoanswerfivefullquestions, selecting onefullquestionfromeachmodule

**SuggestedLearningResources:**

**Books**

1) GaryK.Yeap,"PracticalLowPowerDigitalVLSIDesign",KluwerAcademic,1998.
2) JanM.Rabaey,MassoudPedram,"LowPowerDesignMethodologies",KluwerAcademic,2010.
3) KaushikRoy, SharatPrasad,"Low-PowerCMOSVLSICircuitDesign"Wiley, 2000
4) A.P.ChandrasekaranandR.W.Broadersen, "LowpowerdigitalCMOSdesign", KluwerAcademic,1995
.5)ABellamour andMIElmasri,"LowpowerVLSI CMOScircuitdesign",KluwerAcademic,1995.

**WeblinksandVideoLectures(e-Resources):**

1. https://archive.nptel.ac.in/courses/106/105/106105034/
2. https://www.youtube.com/watch?v=TFOO1JAll2Y
3. https://www.youtube.com/watch?v=ORtlxpW_LMU

**SkillDevelopmentActivitiesSuggested**

1) Interactwithindustry(small,medium,andlarge).
2) Involveinresearch/testing/projectstounderstandtheirproblemsandhelpcreativeandinnovativemethodstosolvetheproblem.
3) Involveincasestudiesandfieldvisits/ fieldwork.
4) Accustomtotheuseofstandards/codesetc.,tonarrowthegapbetweenacademiaandindustry.
5) Handleadvancedinstrumentstoenhancetechnicaltalent.
6) Gainconfidenceinmodellingofsystemsandalgorithmsfortransientandsteady-stateoperations,thermalstudy, etc.
7) Workondifferentsoftware/s(tools)tosimulate,analyzeandauthenticatetheoutputtointerpretandconclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities,management skills, Statistical analysis, fiscal expertise, etc. Students and the course instructor/s toinvolveeitherindividuallyoringroupstointeracttogethertoenhancethelearningandapplicationskillsof the study they have undertaken. The students with the help of the course teacher can take up relevanttechnical–activitieswhichwillenhancetheirskill. Thepreparedreportshallbeevaluatedfor CIEmarks.

**Courseoutcome(CourseSkillSet)**

Attheendof thecoursethestudentwillbeableto:

| Sl.No. | Description | Bloo msLe vel |
|---|---|---|
| CO1 | Identifythesources ofpowerdissipationinCMOS circuits. | L1,L2 |
| CO2 | Performpoweranalysisusing simulation-basedapproachesandprobabilisticanalysis | L2, |
| L3CO3 | Use optimization and trade-off techniques that involve power dissipation of digital circuits | |
| L2, L3CO4 L2,L3 | Makethepowerdesignarealitybymakingpowerdimensionanintegralpartofthedesign process | |
| CO5 | Usepracticallowpowerdesigntechniquesandtheiranalysisatvariouslevelsofdesign L3, L4abstractionandanalysehowthesearebeingcapturedinthelatestdesignautomationenvironments. | |

**ProgramOutcomeofthiscourse**

| Sl.No. | Description | POs |
|---|---|---|
| 1. | Independentlycarryoutresearch/investigationanddevelopmentworktosolvepractical problemsrelatedtoVLSI Design andembeddedsystems. | PO1 |
| 2. | Demonstrateadegree ofmasteryoverthe areasofVLSIDesignandembedded systems.Themasteryshouldbeatalevelhigherthantherequirementsinthebachelor'sinElectronics&CommunicationEngineering. | PO2 |
| 3. | Applyappropriatemethodologyandmodernengineering/ITtoolstomeettheinternationalstandardsintheareaof VLSIdesignandembeddedsystems. | PO3 |
| 4. | Acquire competency in areas of VLSI and Embedded Systems, IC Fabrication, Design,Testing,VerificationandIntegratemultiplesub-systemstodevelopSystemOnChiptooptimize its performance and excel in industry sectors related to VLSI / Embeddeddomain. | PO4 |
| 5. | Understandimpactofprofessionalengineeringsolutionsinsocietalandenvironmentalcontexts and demonstrate theknowledge for sustainable development. | PO5 |

| RISC V | | | |
|---|---|---|---|
| Course Code | MLVS216D | CIE Marks | 50 |
| Teaching Hours/Week(L:P:SDA) | 3:0:0 | SEE Marks | 50 |
| Total Hours of Pedagogy | 40 hours Theory | Total Marks | 100 |
| Credits | 03 | Exam Hours | 03 |

**CourseLearningobjectives:**

- TostudythebasicsofRISCVarchitecture.
- TounderstandtheRISC-VImplementation
- TocreatethedatapathinRISC-V.

**Module-1**

**Instructions:**Introduction ,Operations of the Computer, Operands of the Computer Hardware,SignedandUnsignedNumbers,RepresentingInstructionsintheComputer,Logical Operations,InstructionsforMakingDecisions,SupportingProceduresinComputerHardware,CommunicatingwithPeople,RISC-VAddressingforWideImmediateandAddresses.

**RBT Levels:** L2, L3

**Module-2**

**Instructionscontinued:**ParallelismandInstructions:Synchronization,TranslatingandStartingaProgram, A C Sort Example to Put it All Together, Real Stuff: The Rest of the RISC-V Instruction Set**Arithmetic for Computers:** Addition and Subtraction, Multiplication,Multiply in RISC-V ,Division DivideinRISC-V,Floating-PointInstructionsinRISC-V.

**RBT Levels:** L2, L3

**Module-3**

**TheProcessor:**A Basic RISC-V Implementation, An Overview of the Implementation, LogicDesign Conventions, Building a Datapath, A Simple Implementation Scheme, Overview of Pipelining.

**RBT Levels:** L2, L3

**Module-4**

**TheProcessorcontinued**:PipelinedDatapathandControl,DataHazards:ForwardingversusStalling,ControlHazards.HowExceptionsareHandledintheRISC-VArchitecture,Instruction-LevelParallelismandMatrixMultiply, **LargeandFast:**ExploitingMemoryHierarchy,MemoryTechnologies.

**RBT Levels:** L2, L3

**Module-5**

**Large and Fast:** Exploiting Memory Hierarchy continued: The Basics of Caches, Virtual Machines, VirtualMemory,Placing a Page and Finding It Again,Page Faults,Virtual Memory for Large Virtual Addresses,MakingAddressTranslationFast:theTLB,TheIntrinsityFastMATHTLB,IntegratingVirtualMemory, TLBs,andCaches.

**RBT Levels:** L2, L3

## AssessmentDetails(bothCIEandSEE)

TheweightageofContinuousInternalEvaluation(CIE)is50%andforSemesterEndExam(SEE)is50%.Theminimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40%of the maximum marks of SEE.A student shall be deemed to have satisfied the academic requirements andearnedthecreditsallottedtoeachsubject/courseifthestudentsecuresnotlessthan50%(50marksoutof100)inthesumtotaloftheCIE(ContinuousInternalEvaluation)andSEE(SemesterEndExamination)takentogether.

## ContinuousInternalEvaluation:

1. TwoUnitTests eachof**25Marks**
2. Twoassignmentseachof **25Marks**or**oneSkillDevelopmentActivityof50marks** toattaintheCOs andPOs

Thesumoftwotests,twoassignments/skillDevelopmentActivities,willbe **scaleddownto50marks CIEmethods/questionpaperisdesignedtoattainthedifferentlevelsofBloom'staxonomyaspertheoutcomedefinedforthecourse.**

## Semester-EndExamination:

1. TheSEEquestionpaperwillbesetfor100marksandthemarksscoredwillbeproportionatelyreducedto50.
2. Thequestionpaperwillhavetenfullquestionscarrying equalmarks.
3. Eachfullquestionisfor20marks.Therewillbetwofullquestions(withamaximumoffoursub-questions)fromeachmodule.
4. Eachfullquestionwillhaveasub-questioncoveringallthetopicsunderamodule.
5. Thestudentswillhavetoanswerfivefullquestions, selecting onefullquestionfromeachmodule

**SuggestedLearningResources:**

**Books:**

1.ComputerOrganizationandDesign:TheHardware/SoftwareInterface:RISC-VEdition,byDavidA.Patterson,JohnL. Hennessy,Elsevier.

2. DigitalDesignandComputerArchitecture,RISC-VEditionbyDavidHarris,SarahL.Harris.2021MorganKaufmanPublication.

3. GuidetoComputerProcessorArchitecture,ARISCVapproachbyGoossensBernard,SpringerInternationalPublishingAG

**WeblinksandVideoLectures(e-Resources):**

- https://www.youtube.com/watch?v=TVvMPh_P2is&list=PLgzAvj2cYr3qGvecT_PSnKzl5SxECZmI3&index=2,
- https://www.youtube.com/watch?v=BVvDHhG0RoA&list=PL5AmAh9QoSK7Fwk9vOJu-3VqBng_HjGFc

**SkillDevelopmentActivitiesSuggested**

1) Interactwithindustry(small,medium,andlarge).
2) Involveinresearch/testing/projectstounderstandtheirproblemsandhelpcreativeandinnovativemethodstosolvetheproblem.
3) Involveincasestudiesandfieldvisits/ fieldwork.
4) Accustomtotheuseofstandards/codesetc.,tonarrowthegapbetweenacademiaandindustry.
5) Handleadvancedinstrumentstoenhancetechnicaltalent.
6) Gainconfidenceinmodellingofsystemsandalgorithmsfortransientandsteady-stateoperations,thermalstudy, etc.
7) Workondifferentsoftware/s(tools)tosimulate,analyzeandauthenticatetheoutputtointerpretandconclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities,management skills, Statistical analysis, fiscal expertise, etc. Students and the course instructor/s toinvolveeitherindividuallyoringroupstointeracttogethertoenhancethelearningandapplicationskills

**Courseoutcome(CourseSkillSet)**

Attheendof thecoursethestudentwillbeableto:

| Sl.No. | Description | Blooms Level |
|---|---|---|
| CO1 | DescribeRISC-Vinstructionsandthelanguageof thecomputer. | L2 |
| CO2 | Constructadatapathandlearning moreaboutfloating-pointarithmetic | L6 |
| CO3 | UnderstandDataHazardsandhowExceptionsareHandledintheRISC-V Architecture | L2 |
| CO4 | Understandthememorymappingtechniques | L2 |

**ProgramOutcomeofthiscourse**

| Sl.No. | Description | POs |
|---|---|---|
| 1. | Independentlycarryoutresearch/investigationanddevelopmentworktosolve practicalproblemsrelatedtoVLSI Designandembeddedsystems. | PO1 |
| 2. | Demonstrateadegree ofmasteryovertheareasofVLSIDesignandembeddedsystems.Themasteryshouldbeatalevelhigherthantherequirementsinthe | PO2 |
| 3. | bachelor'sinElectronics&CommunicationEngineering. Applyappropriatemethodologyandmodernengineering/ITtoolstomeetthe internationalstandardsinthearea of VLSI designandembeddedsystems. | PO3 |
| 4. | AcquirecompetencyinareasofVLSIandEmbeddedSystems,ICFabrication,Design, Testing,VerificationandIntegratemultiplesub-systemstodevelopSystemOnChipto optimizeitsperformanceandexcelinindustrysectorsrelatedtoVLSI/Embedded domain. | PO4 |
| 5. | Understandimpactofprofessionalengineeringsolutionsin societal andenvironmentalcontexts and demonstrate theknowledge for sustainable development. | PO5 |

| VLSI Design and Embedded Systems Lab | | | |
|---|---|---|---|
| Course Code | **MLVSL207** | CIE Marks | 50 |
| Teaching Hours/Week(L:T:P:S) | 0:0:4 | SEE Marks | 50 |
| Credits | 02 | Exam Hours | 03 |

| **Sl.NO** | **Experiments** |
|---|---|
| **PartA:** FPGADIGITALDESIGNVLSIFrontEndDesignprograms: Programmingcanbedoneusinganycompiler.DownloadtheprogramsonFPGA/CPLDboardsandusepatterngenerator (32 channelsandlogicanalyzer)/Chipscopepro apartfrom verificationbysimulation | |
| 1 | WriteVerilogcodeforthedesignof8-biti. CarryRippleAdderii.CarryLookAhead adder iii.CarrySkip Adder |
| 2 | WriteVerilogCode for8-biti.ArrayMultiplication(SignedandUnsigned)ii.Booth Multiplication(Radix-4) |
| 3 | WriteVerilogcodefor4/8-biti.MagnitudeComparatorii.LFSRiii.ParityGenerator |
| 4 | Develop a Verilog model for a thermostat that has two 8-bit unsigned binary inputsrepresenting the target temperature and the actual temperature in degrees Fahrenheit(˚F). Assume that both temperatures are above freezing (32˚F). The detector has twooutputs: one to turn a heater on when the actual temperature is more than 5˚F belowtarget,andonetoturnacooleronwhentheactualtemperatureismorethan5˚Fabove target |
| 5 | DevelopaVerilogmodelofthe7-segmentdecoder,exerciseatestbench,synthesizeand dotheinitialtimingverificationwithgatelevelsimulation. |
| 6 | DesignaMealyandMooreSequenceDetectorusingVerilogtodetectSequence.Eg11101 (withand withoutoverlap)anysequencecanbespecified. |
| **PartB:** ARMCortexM3Programs- ProgrammingtobedoneusingsuitableCADtoolanddownloadtheprogramontoaM3evaluationboard . | |
| 7 | WriteanAssemblylanguageprogramtocalculatethesumanddisplaytheresultfortheadditionoffirsttennumbers.SUM =10+9+8+.+1 |
| 8 | WriteaEmbedded Cprogramtooutputthe“HelloWorld”messageusingUART |
| 9 | WriteaEmbedded Cprogram i. to operateabuzzer ,ii. tocontrolsteppermotorusing CortexM3 |
| 10 | WriteaEmbedded Cprogram to generate PWM (Using the Internal PWM module of ARM controller)and vary its duty cycle. |
| 11 | WriteaEmbedded Cprogram for interfacing a DAC and generate (Triangular and Square) waveforms. |
| 12 | WriteanAssemblylanguageprogramtostoredatainRAM |

**Courseoutcomes(CourseSkillSet):**

Attheend ofthecoursethestudentwill beableto:

1. UnderstandthefeaturesofCADtoolinVLSIdesign.
2. Designandverifythebehaviorofdigitalcircuitsusingdigitalflow
3. Verifythedesignusing alogicanalyzer
4. Analysephysicaldesign

5. Develop Assembly language programs and C language programs for different applicationsusing ARM-CortexM3Kit and KeiluVision-4tool.

**AssessmentDetails(bothCIEandSEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam(SEE)is50%.TheminimumpassingmarkfortheCIEis50%ofthemaximummarks.Astudentsh allbedeemedtohavesatisfiedtheacademicrequirementsandearnedthecreditsallottedtoeach course. The student has to secure not less than 40% of maximum marks in the semester-end examination(SEE). In total of CIE and SEE student has to secure 50% maximum marks ofthecourse.

**ContinuousInternalEvaluation(CIE):**

CIEmarksfor thepractical courseis **50 Marks**.

Thesplit-upofCIEmarksforrecord/ journal andtestareintheratio**60:40**.

- Each experiment to be evaluated for conduction with an observation sheet and recordwrite-up. Rubrics for the evaluation of the journal/write-up for hardware/softwareexperimentsdesignedbythefacultywhoishandlingthelaboratorysessi onandismadeknowntostudentsatthebeginningofthepracticalsession.
- Recordshouldcontainallthespecifiedexperimentsinthesyllabusandeachexperimentwrite-upwillbeevaluated for10marks.
- **Total marks scored by the students are scaled down to 30 marks** (60% of maximummarks).
- Weightagetobegivenfor neatnessand submissionofrecord/write-upontime.
- Department shall conduct 01 tests for 100 marks, test shall be conducted after the 14$^{th}$weekofthesemester.
- Intest,testwrite-up,conductionofexperiment,acceptableresult,andproceduralknowledgewillcarrya weightageof60%andtherest40%forviva-voce.
- Thesuitablerubricscanbedesignedto evaluateeachstudent'sperformanceandlearningability.
- **Thetestmarks isscaleddownto20 marks**(40%ofthemaximummarks).

TheSumof**scaled-down**marksscoredinthereportwrite-up/journalandmarksoftestisthetotal CIE marksscored bythestudent.

**SemesterEndEvaluation(SEE):**

SEEmarksforthepractical courseis50 Marks.

SEEshallbeconductedjointlybythetwoexaminersofthesameinstitute,examinersareappointedbyt heUniversity.

Alllaboratoryexperimentsaretobeincludedforpracticalexamination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answerscript to be strictly adhered to by the examiners.**OR** based on the course requirementevaluationrubricsshallbedecidedjointlybyexaminers.

Studentscanpick onequestion(experiment)fromthe questionslotpreparedby theinternal /externalexaminersjointly.

Evaluationoftestwrite-up/conductionprocedureandresult/vivawillbeconductedjointlybyexaminers.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedureandresultin-60%,Viva-voce20%ofmaximummarks.SEEforpracticalshallbeevaluatedfor100 marks and scored marks shall be scaled down to 50 marks (however, based on coursetype,rubricsshallbedecided bytheexaminers)

Changeofexperimentisallowedonlyonceand10%Marksallottedto theprocedureparttobemadezero.

ThedurationofSEEis03 hours

**SuggestedLearningResources:**

**Referencebook:**PeterJ.AshendenDigitalDesign(Verilog):AnEmbeddedSystemsApproachUsing Verilog1stEdition,KindleEdition