| Applied Linear Algebra and Random Processes | | | |
|---|---|---|---|
| Course Code | **1MEC101** | Scheme | 2026 |
| Type of Course | **Professional Core course** | Semester | 1 |
| Teaching Hours/Week (L:T:P) | 42:0:0 | CIE Marks | 50 |
| Total Hours of Pedagogy per semester L /T/P/SL&TW: | 42:00:00:45:03 | SEE Marks | 50 |
| Credits | **3** | Total Marks | 100 |
| Examination type (SEE) | Theory | Exam Hours | 3 |

**Course outcome (Course Skill Set)**

CO1: Apply linear algebra concepts to solve engineering problems involving matrices and vector spaces.

CO2: Analyze eigenvalues, matrix decompositions, and orthogonal transformations for engineering applications.

CO3: Apply probability theory and random variable models to analyze uncertainty in engineering systems.

CO4: Evaluate random processes and stochastic models for communication and signal processing applications.

**At the end of the course, the student will be able to:**

**Module-1**

**Linear Algebra Fundamentals**: Review of vectors and matrices, Matrix operations and properties, Rank, determinant, and trace, Systems of linear equations, Gaussian elimination, LU decomposition, Vector spaces and subspaces, Linear independence and basis and Dimension of vector spaces.

**Number of Hours:08**

**Module-2**

**Eigenvalues and Eigenvectors**: Eigenvalues and eigenvectors, Characteristic polynomial, Diagonalization of matrices, Similarity transformations, Cayley-Hamilton theorem, Positive definite matrices, Singular Value Decomposition (SVD) and Applications in engineering systems.

**Number of Hours: 09**

**Module-3**

**Orthogonality and Matrix Factorization:** Inner product spaces, Orthogonality and orthonormality, Gram-Schmidt orthogonalization, QR decomposition, Least squares approximation, Projection matrices, Applications in communications and machine learning.

**Number of Hours: 09**

**Module-4**

**Probability Theory and Random Variables:** Probability axioms, Conditional probability, Bayes' theorem, Random variables, Probability density function (PDF), Cumulative distribution function (CDF), Joint and marginal distributions and Expectation, variance, and moments

**Number of Hours: 08**

**Module-5**

**Random Processes:** Classification of random processes, Stationary and ergodic processes **,** Correlation and covariance functions, Power Spectral Density (PSD) **,** Gaussian random processes White noise processes, Markov processes and Applications in communication systems

**Number of Hours: 08**

**Suggested Learning Resources: (Text Book/ Reference Book/ Manuals):**

[1] D. C. Lay, S. R. Lay, and J. J. McDonald, *Linear Algebra and Its Applications*, 5th ed. Boston, MA, USA: Pearson, 2016, ISBN: 978-0-321-98238-4.

[2] P. Z. Peebles, Jr., *Probability, Random Variables, and Random Signal Principles*, 4th ed. New York, NY, USA: McGraw-Hill, 2001, ISBN: 978-0-07-047428-4.

[3] G. R. Grimmett and D. R. Stirzaker, *Probability and Random Processes*, 3rd ed. Oxford, U.K.: Oxford University Press, 2001, ISBN: 978-0-19-857222-0.

**Web links and Video Lectures (e-Resources):**

1. https://www.youtube.com/playlist?list=PLE7DDD91010BC51F8
2. https://www.youtube.com/playlist?list=PL221E2BBF13BECF6C
3. https://www.youtube.com/results?search_query=NPTEL+Probability+and+Random+Variables

**Teaching-Learning Process (Innovative Delivery Methods):**

The following are sample strategies that educators may adopt to enhance the effectiveness of the teaching-learning process and facilitate the achievement of course outcomes.

1. MATLAB/Python (NumPy, SciPy) demonstrations for matrix computations, probability distributions, and random process simulations.
2. Case studies on applications of linear algebra and random processes in AI, machine learning, communication, signal processing, and data analytics.
3. Flipped classroom through pre-class videos and reading materials followed by in-class discussions.

**Assessment Structure:**

The assessment in each course is divided equally between Continuous Internal Evaluation (CIE) and the Semester End Examination (SEE), with each carrying 50% weightage.

- To qualify and become eligible to appear for SEE, in the **CIE**, a student must score at least **40% of 50 marks**, i.e., **20 marks**.
- To pass the **SEE**, a student must score at least **35% of 50 marks**, i.e., **18 marks**.
- Notwithstanding the above, a student is considered to have **passed the course,** provided the combined total of **CIE and SEE** is at least **40 out of 100 marks**.

**Continuous Comprehensive Assessments (CCA)+ Internal Assessment Test (IA) = Continuous Internal Evaluation CIE [25+25=50 marks]**

A minimum of **two Internal Assessment Tests (IA)** shall be conducted, carrying a total of **25 marks**.

In addition, **Continuous Comprehensive Assessment (CCA)** shall be conducted for a total of **25 marks**.

It is recommended to include **a maximum of two learning activities** as part of the CCA to foster the **holistic development of students**. These activities shall be:

| Sl. No. | Name of the Learning activity | Maximum Marks |
|---|---|---|
| 1. | Random Process Simulations | 10 |
| 2. | AI based case study implementation | 15 |

**Suggested Learning Activities may include (but are not limited to):**

- Course Project
- Case Study Presentation
- Programming Assignment
- Tool/Software Exploration
- Literature Review
- Open Book Test (preferably at RBL4 and RBL5 levels)
- GATE-based Aptitude Test
- Assignment (at RBL3, RBL4, or RBL5 levels)

**Suggested Innovative Delivery Methods may include (but are not limited to):**

- Flipped Classroom
- Problem-Based Learning (PBL)
- Case-Based Teaching
- Simulation and Virtual Labs
- Partial Delivery of course by Industry expert/ industrial visits
- ICT-Enabled Teaching

| **Term Work (TW) and Self Learning (SL) components in Number of Hours per semester** | | |
|---|---|---|
| Term work (includes assignments, seminars, micro projects, industrial visits, any other student activities etc.) | | |
| **Sl. No.** | **Term Work (TW) Activity** | **Number of Hours / Semester** |
| 1. | Matrix Applications in Engineering | 01 |
| 2. | Analyze a real-world engineering problem involving SVD, least squares, or Markov processes and present the findings. | 03 |
| SL: Self Learning, MOOCs, spoken tutorials, online educational resources etc. | | |
| **Sl. No.** | **Self-Learning (SL) Activity** | **Number of Hours / Semester** |
| 1. | Computational Tool-Based Assignment | 20 |
| 2. | MOOC courses | 20 |
| 3. | Explore and present applications of linear algebra in machine learning, image processing, robotics, or communication systems. Draft a research article review | 05 |

| | Superior | Good | Fair | Needs Improvement | Unacceptable |
|---|---|---|---|---|---|
| **Performance Indicator- 1 (CO/PO Mapping)** | **H** | **M** | **H** | | |
| **Performance Indicator-2 (CO/PO Mapping)** | **L** | **L** | **L** | | |
| **Performance Indicator- 3 (CO/PO Mapping)** | **M** | **M** | **M** | | |

| AI for Electronics Engineers | | | |
|---|---|---|---|
| Course Code | **1MEC102** | Scheme | 2026 |
| Type of Course | **Professional Core Course** | Semester | 1 |
| Teaching Hours/Week (L:T:P) | 42:0 :0 | CIE Marks | 50 |
| Total Hours of Pedagogy per semester L /T/P/SL&TW: | 42:00:00:45:03 | SEE Marks | 50 |
| Credits | **3** | Total Marks | 100 |
| Examination type (SEE) | Theory | Exam Hours | 3 |

**Course outcome (Course Skill Set):**

**CO1:** Apply machine learning techniques for preprocessing, modeling, and analyzing engineering datasets.

**CO2:** Analyze and evaluate learning algorithms for electronics engineering applications.

**CO3:** Design AI integrated models for signal processing, communication, vision, and embedded AI applications.

**CO4:** Develop intelligent solutions for real-world electronics systems using modern AI frameworks and deployment platforms.

**At the end of the course, the student will be able to:**

**Module-1**

**AI Ecosystem and Intelligent Computing:** Introduction to foundation-model-based AI, AI paradigms: Symbolic AI, Statistical AI, Cognitive AI, Hybrid AI, and Intelligent Agent architectures, along with the complete AI development lifecycle, Fundamental neural network architectures: Perceptron, Artificial Neural Networks (ANN), Convolutional Neural Networks (CNN), Recurrent Neural Networks (RNN), Long Short-Term Memory (LSTM), Gated Recurrent Units (GRU), Autoencoders, Generative Adversarial Networks (GANs), Diffusion Models, and Transformer architectures.

**Number of Hours:08**

**Module-2**

**Generative AI, Foundation Models, and Large Language Models :** principles of generative modeling, prompt engineering, prompt chaining, AI agents, Retrieval-Augmented Generation (RAG), tool calling, and AI workflow orchestration. The architecture and capabilities of modern LLMs including GPT, Llama, Claude, Gemini, Gemma, Phi, and Falcon, will be examined. The module further introduces Vision Language Models (VLMs), multimodal AI systems, image generation models, speech models, video generation models, and code generation models

**Number of Hours: 09**

**Module-3**

**Deep Learning and Modern AI Architectures:** Deep Neural Networks (DNNs), Residual Networks (ResNet), EfficientNet, Vision Transformers (ViTs), attention mechanisms, encoder-only, decoder-only, and encoder-decoder Transformer architectures. Modern scalable architectures such as Mixture of Experts (MoE), sparse neural networks, graph neural networks, diffusion networks

**Number of Hours: 09**

**Module-4**

**Edge Intelligence, TinyML, and Embedded AI:** Edge AI architectures, TinyML principles, embedded machine learning pipelines, model compression, quantization, pruning, knowledge distillation, and inference optimization techniques, Hardware acceleration using GPUs, TPUs, NPUs, FPGAs, ASIC-based AI accelerators, and neuromorphic processors.

**Number of Hours: 08**

**Module-5**

**Agentic AI and Future Intelligent Electronic Systems:** concepts of Agentic AI, autonomous decision-making, reasoning systems, planning algorithms, multi-agent systems, collaborative AI, and AI orchestration frameworks. Emerging technologies such as Explainable AI (XAI), Responsible AI, Green AI, Federated Learning, Swarm Intelligence, Embodied AI, Physical AI, and AI governance **Number of Hours: 08**

**Suggested Learning Resources: (Text Book/ Reference Book/ Manuals):**


1. Aurélien Géron, *Hands-On Machine Learning with Scikit-Learn, Keras & TensorFlow: Concepts, Tools, and Techniques to Build Intelligent Systems*, 3rd Edition, O'Reilly Media, 2023.
2. Christopher M. Bishop and Hugh Bishop, *Deep Learning: Foundations and Concepts*, Springer, 2024.
3. Ian Goodfellow, Yoshua Bengio, and Aaron Courville, *Deep Learning*, MIT Press, 2016.
4. Simon Haykin, *Neural Networks and Learning Machines*, 3rd Edition, Pearson Education, 2009.


**Web links and Video Lectures (e-Resources):**

1. DeepLearning.AI (Andrew Ng) – Machine Learning & Deep Learning DeepLearning.AI YouTube Channel
2. StatQuest with Josh Starmer – Statistics and Machine Learning Concepts StatQuest YouTube Channel
3. 3Blue1Brown – Linear Algebra, Neural Networks, and Mathematical Foundations of ML 3Blue1Brown YouTube Channel
4. NPTEL (IIT Madras/IIT Kharagpur/IIT Delhi) – Machine Learning and Deep Learning Courses NPTEL YouTube Channel

**Teaching-Learning Process (Innovative Delivery Methods):**

The following are sample strategies that educators may adopt to enhance the effectiveness of the teaching-learning process and facilitate the achievement of course outcomes.

1. Hands-on programming sessions using Python, Scikit-learn, TensorFlow, and PyTorch.
2. Laboratory demonstrations using Jupyter Notebook, Google Colab, and MATLAB.
3. Case studies on AI applications in communication systems, VLSI, embedded systems, IoT, and signal processing.
4. Mini-projects involving sensor data analytics, predictive maintenance, and intelligent electronic systems.

**Assessment Structure:**

The assessment in each course is divided equally between Continuous Internal Evaluation (CIE) and the Semester End Examination (SEE), with each carrying 50% weightage.

- To qualify and become eligible to appear for SEE, in the **CIE**, a student must score at least **40% of 50 marks**, i.e., **20 marks**.
- To pass the **SEE**, a student must score at least **35% of 50 marks**, i.e., **18 marks**.
- Notwithstanding the above, a student is considered to have **passed the course,** provided the combined total of **CIE and SEE** is at least **40 out of 100 marks**.

| | Superior | Good | Fair | Needs Improvement | Unacceptable |
|---|---|---|---|---|---|
| **Performance Indicator- 1 (CO/PO Mapping)** | **H** | **M** | **M** | | |
| **Performance Indicator-2 (CO/PO Mapping)** | **M** | **L** | **L** | | |
| **Performance Indicator-3 (CO/PO Mapping)** | **L** | **H** | **H** | | |

**Continuous Comprehensive Assessments (CCA)+ Internal Assessment Test (IA) = Continuous Internal Evaluation CIE [25+25=50 marks]**

A minimum of **two Internal Assessment Tests(IA)** shall be conducted, carrying a total of **25 marks**.

In addition, **Continuous Comprehensive Assessment (CCA)** shall be conducted for a total of **25 marks**.

It is recommended to include **a maximum of two learning activities** as part of the CCA to foster the **holistic development of students**. These activities shall be:

| Sl. No. | Name of the Learning activity | Maximum Marks |
|---|---|---|
| 1. | Problem-Based Learning (PBL) using engineering datasets and industrial problem statements. | 25 |

**Suggested Learning Activities may include (but are not limited to):**

- Course Project
- Case Study Presentation
- Programming Assignment
- Tool/Software Exploration
- Literature Review
- Open Book Test (preferably at RBL4 and RBL5 levels)
- GATE-based Aptitude Test
- Assignment (at RBL3, RBL4, or RBL5 levels)

**Suggested Innovative Delivery Methods may include (but are not limited to):**

- Flipped Classroom
- Problem-Based Learning (PBL)
- Case-Based Teaching
- Simulation and Virtual Labs
- Partial Delivery of course by Industry expert/ industrial visits
- ICT-Enabled Teaching
- Role Play

| Term Work (TW) and Self Learning (SL) components in Number of Hours per semester | | |
|---|---|---|
| Term work (includes assignments, seminars, micro projects, industrial visits, any other student activities etc.) | | |
| **Sl. No.** | **Term Work (TW) Activity** | **Number of Hours / Semester** |
| 1. | Design, implement, and evaluate a machine learning model for an electronics engineering problem using Python/TensorFlow/Scikit-learn. | 03 |
| SL: Self Learning, MOOCs, spoken tutorials, online educational resources etc. | | |
| **Sl. No.** | **Self-Learning (SL) Activity** | **Number of Hours / Semester** |
| 2. | AI-enabled learning using GitHub Copilot, ChatGPT, and other code assistants for model development and debugging. | 20 |
| 3. | Collaborative learning through team-based algorithm implementation and peer presentations. | 25 |

| Computational Methods for Electronic System Design | | | |
|---|---|---|---|
| Course Code | **1MEC103** | Scheme | 2026 |
| Type of Course | **Professional Core Course** | Semester | 1 |
| Teaching Hours/Week (L:T:P) | 42:0 :0 | CIE Marks | 50 |
| Total Hours of Pedagogy per semester L /T/P/SL&TW: | 42: 00 :00:45:03 | SEE Marks | 50 |
| Credits | **3** | Total Marks | 100 |
| Examination type (SEE) | Theory | Exam Hours | 3 |

**Course outcome (Course Skill Set)**

CO1: Apply numerical and optimization techniques to solve computational problems in electronic system design.

CO2: Analyze electronic systems using mathematical modeling, simulation, and computational algorithms.

CO 3: Design computational solutions for signal processing, communication, VLSI, and embedded system applications.

CO 4: Evaluate the performance and accuracy of computational models using modern software tools for electronic system design.

**At the end of the course, the student will be able to:**

**Module-1**

**Mathematical Foundations and Numerical Computing:** Numerical errors, floating-point arithmetic, conditioning and stability of algorithms, numerical differentiation and integration, root-finding techniques (Bisection, Newton-Raphson, Secant methods), systems of linear equations, matrix operations, eigenvalue problems, interpolation methods, and curve fitting. Applications in circuit analysis and electronic system modelling.

**Number of Hours:09**

**Module-2**

**Computational Modelling of Electronic Circuits and Systems:** Nodal and mesh analysis using matrix methods, state-space representation of electronic systems, transient and steady-state analysis, numerical solutions of ordinary differential equations (Euler, Runge-Kutta methods), nonlinear circuit analysis, and simulation methodologies. Electronic Design Automation (EDA) tools and SPICE-based simulation concepts are introduced with practical examples

**Number of Hours: 09**

**Module-3**

**Optimization Techniques for Electronic System Design:** Unconstrained and constrained optimization, gradient-based optimization methods, linear programming, nonlinear programming, convex optimization fundamentals, heuristic optimization techniques such as Genetic Algorithms (GA), Particle Swarm Optimization (PSO), Simulated Annealing (SA), and multi-objective optimization.

**Number of Hours: 08**

| Module-4 |
| --- |
| **Computational Signal Processing and Data-Driven Design:** Discrete-time signal processing algorithms, Fast Fourier Transform (FFT), wavelet transforms, adaptive filtering, statistical signal analysis, machine learning-assisted signal processing, feature extraction, dimensionality reduction, and computational techniques for sensor data analytics. Applications in communication systems,biomedical electronics, radar systems, and IoT platforms. **Number of Hours: 08** |
| **Module-5** |
| **Advanced Computational Techniques and Emerging Trends:** High-performance computing for electronics, parallel and distributed computing, GPU acceleration, hardware-software co-design, FPGA-based acceleration, AI-assisted electronic design automation (EDA), Reinforcement learning for adaptive systems, and computational approaches for 6G communication networks and smart electronic systems. **Number of Hours: 08** |
| **Suggested Learning Resources: (Text Book/ Reference Book/ Manuals):**<br>[1] S. C. Chapra and R. P. Canale, *Numerical Methods for Engineers*, 8th ed. New York, NY, USA: McGraw-Hill Education, 2021.<br>[2] A. Gilat and V. Subramaniam, *Numerical Methods for Engineers and Scientists: An Introduction with Applications Using MATLAB*, 4th ed. Hoboken, NJ, USA: Wiley, 2018.<br>[3] S. S. Rao, *Engineering Optimization: Theory and Practice*, 5th ed. Hoboken, NJ, USA: Wiley, 2019.<br>[4] . Wen-mei W. Hwu, David B. Kirk and Izzat El Hajj, *Programming Massively Parallel Processors: A Hands-on Approach*, 5th Edition, Morgan Kaufmann–Elsevier, 2026.<br>[5] **.** Sabih H. Gerez, *Algorithms for VLSI Design Automation*, John Wiley & Sons, 1999, ISBN: 978-0-471-98489-4. |
| **Web links and Video Lectures (e-Resources): .**<br>1. MIT OpenCourseWare – Numerical Methods for Engineers https://www.youtube.com/@mitocw<br>2. MATLAB Official – MathWorks (Numerical Computing, Optimization, Signal Processing, Simulink) https://www.youtube.com/@MATLAB<br>3. NPTEL – Numerical Methods, Scientific Computing, Optimization, MATLAB Programming https://www.youtube.com/@nptelhrd<br>4. Steve Brunton – Scientific Computing, Linear Algebra, Numerical Methods, Optimization, Machine Learning for Engineers https://www.youtube.com/@Eigensteve |

**Teaching-Learning Process (Innovative Delivery Methods):**

The following are sample strategies that educators may adopt to enhance the effectiveness of the teaching-learning process and facilitate the achievement of course outcomes.

1. Applications include filter design, antenna optimization, power minimization, resource allocation, and communication system parameter tuning.
2. Develop and compare computational algorithms for solving an electronics engineering problem such as circuit simulation, optimization, or signal processing.

**Assessment Structure:**

The assessment in each course is divided equally between Continuous Internal Evaluation (CIE) and the Semester End Examination (SEE), with each carrying 50% weightage.

- To qualify and become eligible to appear for SEE, in the **CIE**, a student must score at least **40% of 50 marks**, i.e., **20 marks**.
- To pass the **SEE**, a student must score at least **35% of 50 marks**, i.e., **18 marks**.
- Notwithstanding the above, a student is considered to have **passed the course,** provided the combined total of **CIE and SEE** is at least **40 out of 100 marks**.

**Continuous Comprehensive Assessments (CCA)+ Internal Assessment Test (IA) = Continuous Internal Evaluation CIE [25+25=50 marks]**

A minimum of **two Internal Assessment Tests(IA)** shall be conducted, carrying a total of **25 marks**.

In addition, **Continuous Comprehensive Assessment (CCA)** shall be conducted for a total of **25 marks**.

It is recommended to include **a maximum of two learning activities** as part of the CCA to foster the **holistic development of students**. These activities shall be:

| Sl. No. | Name of the Learning activity | Maximum Marks |
|---|---|---|
| 3. | **Simulation-Based Case Study:** Collaboratively model and simulate an electronic system using MATLAB, Python, or | 25 |

| | Superior | Good | Fair | Needs Improvement | Unacceptable |
|---|---|---|---|---|---|
| **Performance Indicator- 1 (CO/PO Mapping)** | **H** | **L** | **M** | | |
| **Performance Indicator-2 (CO/PO Mapping)** | **M** | **M** | **L** | | |
| **Performance Indicator-3 (CO/PO Mapping)** | **L** | **L** | **M** | | |

**Suggested Learning Activities may include (but are not limited to):**

- Course Project
- Case Study Presentation
- Programming Assignment
- Tool/Software Exploration
- Literature Review
- Open Book Test (preferably at RBL4 and RBL5 levels)
- GATE-based Aptitude Test
- Assignment (at RBL3, RBL4, or RBL5 levels)
- Any other relevant and innovative academic activity
- Use of MOOCs and Online Platforms

**Suggested Innovative Delivery Methods may include (but are not limited to):**

- Flipped Classroom
- Problem-Based Learning (PBL)
- Case-Based Teaching
- Simulation and Virtual Labs
- Partial Delivery of course by Industry expert/ industrial visits
- ICT-Enabled Teaching
- Role Play

| Term Work (TW) and Self Learning (SL) components in Number of Hours per semester | | |
|---|---|---|
| Term work (includes assignments, seminars, micro projects, industrial visits, any other student activities etc.) | | |
| **Sl. No.** | **Term Work (TW) Activity** | **Number of Hours / Semester** |
| 1. | **Algorithm Development Challenge:** Design, implement, and benchmark numerical or optimization algorithms for an engineering application, presenting the computational efficiency and accuracy. | 03 |
| SL: Self Learning, MOOCs, spoken tutorials, online educational resources etc. | | |
| **Sl. No.** | **Self-Learning (SL) Activity** | **Number of Hours / Semester** |
| 4. | **Computational Design Project:** Develop and compare computational algorithms for solving an electronics engineering problem such as circuit simulation, optimization, or signal processing. | 20 |
| 5. | Implement selected computational algorithms using **MATLAB or Python** and document their performance on engineering datasets. | 20 |
| 6. | **Research Paper Review:** Analyze and present a recent IEEE paper on computational methods applied to VLSI, embedded systems, communication, or electronic system design. | 05 |

| | | | | |
|---|---|---|---|---|
| | **ADVANCED EMBEDDED SYSTEMS** | | | |
| | Course Code | **1MEC104A** | Scheme | 2026 |
| | Type of course | **Integrated Professional Core Course** | Semester | I |
| | Teaching Hours/Week (L:T:P) | 3:0:1 | CIE Marks | 50 |
| | Total Hours of Pedagogy L:T:P:SL:TW | 42:10:00:35:03 | SEE Marks | 50 |
| | Credits | **04** | Total Marks | 100 |
| | Type of Examination (IPCC): | Theory- CIE +SEE, and Lab- CIE only. | Exam Hours | 03 |

**Course outcome (Course Skill Set):**

At the end of the course, the student will be able to:

**CO1:** Analyse embedded-system requirements and select appropriate hardware components based on performance, power, memory, cost and application constraints.

**CO2:** Apply RTOS concepts, including task management, scheduling, multitasking, synchronization and inter-task communication, to develop real-time embedded applications.

**CO3:** Develop embedded applications using ARM Cortex-M3 and RISC-V architectures by utilizing their processor features, instruction sets and peripheral capabilities.

**CO4:** Design, program and evaluate embedded-system solutions for different end-use applications using suitable programming techniques and development tools.

**Module-1**

**Embedded System:** Embedded v/s General Computing System, classification, application and purpose of ES. Core of an Embedded System, Memory, Sensors, Actuators, LED, Optocoupler, Communication Interface, Reset circuits, RTC (Real Time Clock), Watchdog Timer (WDT) , Characteristics and Quality Attributes of Embedded Systems, Automotive- Domain specific examples of Embedded systems. **Number of Hours:9**

**Module-2**

**Hardware Software Co-Design:** Fundamental issues in hardware software co-design, computational models, introduction to unified modelling language (UML),

**Real-Time Operating System (RTOS) based Embedded System Design:** Operating system basics, types of operating systems, tasks, processes and threads, multiprocessing and multitasking, task scheduling

**Number of Hours:9**

| | |
|---|---|
| | **Module-3** |
| | **ARM - 32 bit Microcontroller:** Thumb-2 technology and applications of ARM, Architecture of ARM Cortex M3, Various Units in the architecture, General Purpose Registers, Special Registers, exceptions, interrupts, stack operation, reset sequence.<br><br>**Number of Hours:8** |
| | **Module-4** |
| | **Instruction Sets:** Assembly basics, Instruction list and description, useful instructions, Memory Systems, Memory maps, Cortex M3 implementation overview, pipeline and bus interface, Exceptions, Nested Vector interrupt controller design, Sys Tick Timer, Cortex- M3 Programming using assembly and C language, CMSIS. **Number of Hours:8** |
| | **Module-5** |
| | **Introduction to RISC - V**: Operations of the Computer Hardware, Operands of the Computer Hardware, Signed and Unsigned Numbers, Representing Instructions in the Computer, Logical Operations, Instructions for Making Decisions, RISC-V Addressing for Wide Immediate and Addresses, Parallelism and Instructions: Synchronization. **Number of Hours:8** |
| | **PRACTICAL COMPONENTS OF IPCC** |
| | **FIXED SET OF EXPERIMENTS:**<br>1. Develop and test programs:<br>(a) To create child process and display it's ID.<br>(b) child process function using switch structure.<br>2. Develop and test the program for a multi-threaded application, where communication is through shared memory for the conversion of lowercase text to uppercase text.<br>3. Develop program for inter-thread communication using a message queue. Data is to be input from the keyboard for the chosen application.<br>4. Create 'n' number of child threads. Each thread prints the message "I'm in thread number …" and sleeps for 50 ms and then quits. The main thread waits for complete execution of all the child threads and then quits. Compile and execute in Linux. |

5. Implement the multi-thread application satisfying the following:
   (a) child threads are created with normal priority.
   (b) Thread 1 receives and prints its priority and sleeps for 50ms and then quits.
   (c) Thread 2 prints the priority of the thread 1 and rises its priority to above normal and retrieves the new priority of thread 1, prints it and then quits.
   (d) The main thread waits for the child thread to complete its job and quits.
6. Write ALP to find the square of a number (1 to 10) using look-up table.
7. Write an ALP to arrange a series of 32 bit numbers in ascending/descending order.
8. Write an ALP to count the number of ones and zeros in two consecutive memory locations.
9. Interface a simple Switch and display its status through Relay, Buzzer and LED, DAC. (Study Expt.)
10. Implement a clock capable of displaying (and being set to the correct time). Include an alarm facility which can be set by the user and will 'go off' at the correct time.

**Suggested Learning Resources: (Text Book/ Reference Book/**

**Manuals): Text books:**

1. 'Introduction to embedded systems', K. V.Shibu, TMH education Pvt.Ltd., 2009.
2. 'The Definitive Guide to the ARM Cortex-M3', Joseph Yiu, Newnes,(Elsevier), 2ndedn, 2010.
3. 'Computer Organization and Design RISC-V Edition', David A. Patterson, John L. Hennessy, Morgan Kaufmann, ISBN: 9780128122761.

**Reference books / Manuals:**

1. Embedded systems - A contemporary design tool', James K.Peckol, JohnWiley, 2008.

**Web links and Video Lectures (e-Resources):**

1. https://onlinecourses.nptel.ac.in/e-learning/preview/noc20_ee98
2. https://onlinecourses.nptel.ac.in/e-learning/preview/noc22_cs93

**Teaching-Learning Process (Innovative Delivery Methods):**

The following are sample strategies that educators may adopt to enhance the effectiveness of the teaching-learning process and facilitate the achievement of course outcomes.

1. Project-Based Learning through real-time embedded system design projects.
2. Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc. and then deploy them on actual hardware platforms such as ARM Cortex-M, Arduino, or ESP32 boards.

**Assessment Structure:**

The assessment for each course is equally divided between Continuous Internal Evaluation (CIE) and the Semester End Examination (SEE), with each component carrying **50% weightage** (i.e., 50 marks each).

The CIE Theory component will be **25 marks** and CIE Practical component will be **25 marks**.

The CIE Theory component consists of IA tests for 25 marks. The CIE Practical component for continuous assessments will be for 15 marks through rubrics and for lab tests will be for 10 marks.

- To qualify and become eligible to appear for SEE, in the **CIE theory component**, a student must score at least **40% of 25 marks**, i.e., **10 marks**.
- To qualify and become eligible to appear for SEE, in the **CIE Practical component**, a student must secure **a minimum of 40% of 25 marks**, i.e., **10 marks**.
- To pass the **SEE**, a student must secure **a minimum of 35% of 50 marks**, i.e., **18 marks**.
- A student is deemed to have **successfully completed the course** if the **combined total of CIE and SEE is at least 40 out of 100 marks**.

**CIE Practical component:**

The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report using a defined set of rubrics. Each experiment report can be evaluated for 30 marks. The summation of all the experiments marks to be scaled down to 15 marks.

The laboratory test (duration 03 hours) at the end of the last week of the semester /after completion of all the experiments (whichever is early) shall be conducted for 50 marks and scaled down to 10 marks. For laboratory test, the student is required to conduct one experiment.

| Rubrics for Learning Activity (Based on the nature of learning activity, design the rubrics for each activity): | | | | | |
|---|---|---|---|---|---|
| | **Superior** | **Good** | **Fair** | **Needs Improvement** | **Unacceptable** |
| **Performance Indicator-1 (CO/PO Mapping)** | **H** | **M** | **H** | | |
| **Performance Indicator-2 (CO/PO Mapping)** | **M** | **H** | **L** | | |
| **Performance Indicator-3 (CO/PO Mapping)** | **M** | **M** | **M** | | |

| Performance Indicators | Excellent | Very Good | Good | Satisfactory |
|---|---|---|---|---|
| Fundamental Knowledge (4) (PO1) | The student has well depth knowledge of the topics related to the course (4) | Student has good knowledge of some of the topics related to course (3) | Student is capable of narrating the answer but not capable to show in depth knowledge (2) | Student has not understood the concepts clearly (1) |
| Design Of Experiment (5) (PO2 & PO3) | Student is capable of discussing more than one design for his/her problem statement and capable of proving the best suitable design with proper reason (5) | Student is capable of discussing few designs for his/her problem statement but not capable of selecting best (4) | Student is capable of discussing single design with its merits and de-merits (3) | Student is capable of explaining the design (1-2) |
| Implementation (8) (PO3 & PO8) | Student is capable of implementing the design with best suitable algorithm considering optimal solution. (7-8) | Student is capable of implementing the design with best suitable algorithm and should be capable of explaining it (5-6) | Student is capable of implementing the design with proper explanation. (3-4) | Student is capable of implementing the design. (1-2) |
| Result &Analysis (5) (PO4) | Student is able to run the program on various cases and compare the result with proper analysis. (5) | Student will be able to run the program for all the cases. (4) | Student will be able to run the code for few cases and analyze the output (3) | Student will be able to run the program but not able to analyze the output (1-2) |
| Demonstration (8) (PO9) | The lab record is well-organized, with clear sections (e.g., Introduction, Method, Results, Conclusion). Transitions between sections are smooth. (7-8) | The lab record is organized, with clear sections, but some sections are not well-defined. (5-6) | The lab record lacks clear organization or structure. Some sections are unclear or incomplete. (3-4) | The lab record is poorly organized, with missing or unclear sections. (1-2) |

**Suggested Learning Activities may include (but are not limited to):**

- Course Project
- Case Study Presentation
- Programming Assignment
- Tool/Software Exploration
- Literature Review
- Open Book Test (preferably at RBL4 and RBL5 levels)
- GATE-based Aptitude Test
- Assignment (at RBL3, RBL4, or RBL5 levels)
- Use of MOOCs and Online Platforms

<table>
<tr><th colspan="3">Term Work (TW) and Self Learning (SL) components in<br>Number of hours per semester</th></tr>
<tr><td colspan="3">Term work (includes assignments, seminars, micro projects, industrial visits, any other student activities etc.)</td></tr>
<tr><td>Sl. No.</td><td>Term Work (TW) Activity</td><td>Number of Hours / Semester</td></tr>
<tr><td>1.</td><td>- Problem-Based Learning (PBL)<br>- Case-Based Teaching</td><td>03+06</td></tr>
<tr><td colspan="3">SL: Self Learning, MOOCs, spoken tutorials, online educational resources etc.</td></tr>
<tr><td>Sl. No.</td><td>Self-Learning (SL) Activity</td><td>Number of Hours / Semester</td></tr>
<tr><td>1.</td><td>Study at least three RTOS platforms such as:<br>● FreeRTOS<br>● Zephyr RTOS<br>● VxWorks<br>● QNX<br>● RTLinux<br>● ThreadX (Azure RTOS)</td><td>25</td></tr>
<tr><td>2.</td><td>Investigate RTOS applications in various domains:<br>● Automotive systems (ADAS, ECU)<br>● Aerospace and Defense<br>● Industrial Automation & Robotics<br>● Medical Devices<br>● Consumer Electronics<br>● IoT and Smart Devices</td><td>20</td></tr>
</table>

## Continuous Internal Evaluation (CIE)

### (i) Theory component

The CIE marks of 25 shall be earmarked for two tests.

The first test shall be conducted after completing two modules of the syllabus and the second one after completing the rest three modules.

Each test shall be conducted for 25 marks. The average of the two tests scaled down to 25 marks shall constitute the test marks for a maximum of 25 marks.

### (ii) Laboratory component

Out of 25 marks, 15 marks shall be assigned for assessment as per the rubrics listed in the course syllabus.

The remaining 10 marks shall be based on the practical test conducted by two Internal examiners appointed by the HoD. The allotment of marks shall be as per the rubrics defined for regular class work and practical test as indicated in the Table – ICs/IPCCs 1.

(i) To qualify and become eligible to appear for the SEE of the IC/IPCC, a student shall secure at least 40 % of 25 marks, i.e., 10 marks, in the CIE theory component, and at least 40 % of 25 marks, i.e., 10 marks in the CIE Practical component.

**Table – ICs/IPCCs 1 Distribution of marks**

| Component | Description | Marks |
|---|---|---|
| **Allotment of marks for regular class work** | | |
| Ability in Conducting Experiments | Initiative, skill, safety practices, teamwork, and independent handling of equipment during regular lab sessions. | 5 marks |
| Laboratory Record / Journal | Regular and neat maintenance of lab record, accuracy of results, and timely submission. | 10 marks |
| | **Subtotal** | **15** |
| **Allotment of marks for CIE practical test** | | |
| Laboratory Test / Experiment Performance | Ability to set up apparatus, follow procedure, take observations, and obtain correct results in the test experiment. | 5 marks |
| Viva-Voce | Understanding of theory, concepts, and experimental procedure; ability to explain results and answer related questions. | 5 marks |
| | **Subtotal** | **10** |
| | **Total** | **25** |

## Passing requirement in SEE

For a pass in the Semester End Examination (SEE), a student shall secure a minimum of 35 marks out of 100.

For the declaration of a pass grade, the sum of the Continuous Internal Evaluation (CIE) marks (out of 50) marks and the SEE marks scaled down to 50 shall be greater than or equal to 40 marks.

If the total (CIE + SEE) is less than 40 marks, the student shall be awarded the grade ‘F’ (Fail).

| INDUSTRIAL AUTOMATION & PROCESS CONTROL | | | |
|---|---|---|---|
| Course Code | **1MEC104B** | Scheme | 2026 |
| Type of course | **Integrated Professional Core Course** | Semester | I |
| Teaching Hours/Week (L:T:P) | 3:0:1 | CIE Marks | 50 |
| Total Hours of Pedagogy L:T:P:SL:TW | 42:10 :00:35:03 | SEE Marks | 50 |
| Credits | **04** | Total Marks | 100 |
| Type of Examination (IPCC): | Theory- CIE +SEE, and Lab- CIE only. | Exam Hours | 03 |

**Course Learning objectives:** This course will enable students to:

CO1: Apply industrial automation principles, sensors, actuators, PLCs, and SCADA systems for process automation.
CO2: Analyze dynamic process behavior and design suitable control strategies for industrial applications.
CO3: Design and implement industrial automation solutions using PLC, HMI, DCS, and industrial communication protocols.
CO4: Evaluate the performance, reliability, and efficiency of automated process control systems using simulation and modern engineering tools.

| **Module-1** |
|---|
| **Industrial Automation Systems and Instrumentation :** Evolution of Industrial Automation and Industry 4.0, Process industries and manufacturing automation, Industrial Automation Architecture (ISA-95), Sensors, Smart Sensors and Industrial Transmitters, Signal Conditioning and Data Acquisition Systems, Actuators: Pneumatic, Hydraulic and Electric Actuators, Industrial Control Valves and Final Control Elements, Industrial Standards and Safety (IEC, ISA) **Number of Hours: 09** |
| **Module-2** |
| **Process Dynamics and Advanced Process Control:** Mathematical Modelling of Industrial Processes, Dynamic Characteristics of First and Higher Order Systems, PID Controller Design and Tuning Techniques, Cascade, Ratio, Feedforward and Override Control, Model Predictive Control (MPC), Adaptive and Robust Control, Process Performance Evaluation and Control Loop Optimization **Number of Hours: 08** |
| **Module-3** |
| **PLC, DCS and Industrial Communication:** PLC Architecture and its Programming Languages, Ladder Logic, Function Block Diagram and Sequential Function Chart, Distributed Control Systems (DCS), SCADA Architecture and Human Machine Interface (HMI), Industrial Communication Protocols: Modbus, Profibus, Profinet, EtherNet/IP, OPC UA, CAN and Industrial Ethernet, Remote Monitoring and Data Acquisition **Number of Hours: 08** |

**Module-4**

**Smart Factory Technologies:** Industrial Internet of Things (IIoT), Cyber-Physical Systems (CPS), Edge Computing and Cloud-based Automation, MQTT and OPC UA Integration, Digital Twin for Process Industries, Industrial Data Analytics, AI and Machine Learning for Process Monitoring, Predictive Maintenance and Condition Monitoring Cybersecurity for Industrial Control Systems

**Number of Hours: 09**

**Module-5**

**Intelligent Automation and Industrial Applications:** Robotics and Collaborative Robots (Cobots), Vision-Based Inspection Systems, Variable Frequency Drives (VFDs) and Motion Control, CNC and Flexible Manufacturing Systems, Manufacturing Execution Systems (MES), Enterprise Integration (ERP–MES–SCADA), Industrial Case Studies: Chemical Plants, Oil & Gas, Power Plants, Semiconductor Manufacturing, Smart Manufacturing.

**Number of Hours: 08**

**List of Experiments:**

1. Develop PLC programs using Ladder Logic for basic logic operations, timers, counters, and latching circuits using OpenPLC.
2. Design and implement sequential control of an industrial process using Ladder Diagram and Function Block Diagram (FBD).
3. Interface OpenPLC with Arduino/ESP32 for digital input and output monitoring and control.
4. Implement PID-based process control for temperature, level, or flow using analog input/output modules.
5. Develop a SCADA-based Human Machine Interface (HMI) for real-time monitoring and control using OpenPLC and ScadaBR/OpenSCADA.
6. Configure and implement Modbus TCP/RTU communication between OpenPLC and industrial devices.
7. Develop an MQTT-based Industrial IoT application for remote monitoring and control using Node-RED and OpenPLC.
8. Simulate an industrial automation process (tank filling, conveyor, traffic signal, or bottle filling) using OpenPLC integrated with Factory I/O or OpenModelica.
9. Perform industrial data acquisition, visualization, and predictive maintenance analysis using Python and sensor data collected from OpenPLC.
10. Design and implement an Industry 4.0 mini project integrating PLC, SCADA, IIoT, industrial communication protocols, and cloud-based monitoring.

**Suggested Learning Resources:**

**Text Books:**

[1] B. G. Lipták, *Instrument Engineers' Handbook: Process Control and Optimization*, 5th ed. Boca Raton, FL, USA: CRC Press, 2019.

[2] C. D. Johnson, *Process Control Instrumentation Technology*, 8th ed. Upper Saddle River, NJ, USA: Pearson, 2014.

[3] F. G. Shinskey, *Process Control Systems: Application, Design, and Tuning*, 4th ed. New York, NY, USA: McGraw-Hill Education, 1996.

[4] W. Bolton, *Programmable Logic Controllers*, 7th ed. Oxford, U.K.: Newnes (Elsevier), 2021.

| **Skill Development Activities Suggested:** | 40 hours per Semester | Total Marks | 20 |
|---|---|---|---|
| 1) Interact with industry (small, medium, and large).<br>2) Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.<br>3) Involve in case studies and field visits/ fieldwork.<br>4) Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.<br>5) Handle advanced instruments to enhance technical talent.<br>6) Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.<br>7) Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude. | | | |

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous Internal Evaluation:**

1. Two Unit Tests each of **25 Marks**
2. Two assignments each of **25 Marks** or **one Skill Development Activity of 50 marks** to attain the COs and POs

The sum of two tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

**CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester-End Examination:**

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.

Each full question will have a sub-question covering all the topics under a module.

| SYSTEMVERILOG | | | |
|---|---|---|---|
| Course Code | **1MEC104C** | Scheme | 2026 |
| Type of the course | **Integrated Professional Core Courses** | CIE Marks | 50 |
| Teaching Hours/Week (L:P:SDA) | 3:0:1 | SEE Marks | 50 |
| Total Hours of Pedagogy | 42:0:25:50:03 | Total Marks | 100 |
| Credits | 04 | Exam Hours | 03 |

**Course Learning objectives:** This course will enable students to:

CO1: Apply SystemVerilog language constructs to model and verify digital designs using reusable testbenches.

CO2: Develop interface-based, assertion-enabled and layered verification environments for digital systems.

CO3: Construct object-oriented and constrained-random testbenches using classes, randomization and inter-process communication.

CO4: Design coverage-driven verification solutions and evaluate verification completeness using functional and cross-coverage metrics.

**Module-1**

**Verification Guidelines:** The Verification Process, Basic Test Bench Functionality, Directed Testing, Methodology Basics, Constrained Random Stimulus, Randomization, Functional Coverage, Test Bench Components, Layered Test Bench.

**Data Types**: Built-In Data Types, Fixed and Dynamic Arrays, Queues, Associative Arrays, Linked Lists, Array Methods, Choosing A Storage Type, Creating New Types with typedef, Creating User Defined Structures, Type Conversion, Enumerated Types, Constants and Strings, Expression Width.

**No. of Hours:08**

**Module-2**

**Procedural Statements and Routines**: Procedural Statements, Tasks, Functions and Void Functions, Task and Function Overview, Routine Arguments, Returning from a Routine, Local Data Storage, Time Values.

**Connecting the Test Bench and Design**: Separating the Test Bench and Design, The Interface Construct, Stimulus Timing, Interface Driving and Sampling, System Verilog Assertions.

**No. of Hours:09**

**Module-3**

**Basic OOPs:** Introduction, define a class, OOP(Object Oriented Programming) terminology, Creating new objects, Object de-allocation, Using objects, Static variables vs. Global variables, Class methods, Defining methods outside of the class, Scoping rules, Using one class inside another, Understanding dynamic objects, Copying objects, Public vs. private, Straying off course, building a test bench.

**Randomization:** Introduction, What to randomize?, Randomization in System Verilog, Random number functions, Common randomization problems, Random Number Generators.

**No. of Hours:08**

**Module-4**

**Threads and Inter Process Communication**: Working with Threads, Disabling Threads, Inter Process Communication, Events, Semaphores, Mailboxes, Building A Test Bench with Threads and Inter Process Communication, AI driven thread monitoring and optimization

**No. of Hours:08**

**Module-5**

**Functional Coverage:** Coverage Types, Functional Coverage Strategies, Simple Functional Coverage Example, Anatomy of Cover Group, Triggering a cover group, Data Sampling, Cross Coverage, Generic Cover Groups, Coverage Options, Analyzing Coverage Data, Measuring Coverage Statistics During Simulation.

**No. of Hours:09**

**Laboratory Component**

- Model and simulate SystemVerilog scalar, packed/unpacked, enumerated and structure data types.
- Implement dynamic arrays, queues and associative arrays; demonstrate array methods and storage selection.
- Develop reusable tasks/functions and a self-checking testbench for a combinational and sequential DUT.
- Create an interface with modports/clocking blocks and connect a testbench to a counter, FIFO or UART DUT.
- Write immediate and concurrent assertions to verify reset, handshake, FIFO and protocol properties.
- Develop classes demonstrating inheritance, polymorphism, composition, shallow/deep copy and virtual methods.
- Create constrained-random transactions using rand/randc, constraint blocks, inline constraints and callbacks.
- Implement generator-driver-monitor-scoreboard communication using threads, events, mailboxes and semaphores.
- Develop covergroups with value, transition and cross coverage; identify and close coverage holes.
- Mini project: build a layered, constrained-random, assertion- and coverage-enabled verification environment for an ALU, FIFO, UART, SPI or APB peripheral.

Suggested tools: Questa/ModelSim, Synopsys VCS, Cadence Xcelium, Vivado Simulator, Verilator or an equivalent simulator; Git may be used for version control.

**Suggested Learning Resources (Text Books / Reference Books / Manuals)**

**Text books:**

- Chris Spear and Greg Tumbush, SystemVerilog for Verification: A Guide to Learning the Testbench Language Features, 3rd Edition, Springer, 2012.
- Stuart Sutherland, Simon Davidmann and Peter Flake, SystemVerilog for Design: A Guide to Using SystemVerilog for Hardware Design and Modeling, 2nd Edition, Springer, 2006.
- Janick Bergeron, Writing Testbenches Using SystemVerilog, 2nd Edition, Springer, 2006.

**Reference standards/manuals:**

- IEEE Std 1800, SystemVerilog—Unified Hardware Design, Specification, and Verification Language.

**Web Links and Video Lectures (e-Resources)**

- https://nptel.ac.in/
- https://www.accellera.org/
- https://standards.ieee.org/standard/1800-2023.html
- https://verificationacademy.com/
- https://www.edaplayground.com/
- https://www.verilator.org/

**Assessment Details (both CIE and SEE)**

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The sum of two tests, two assignments/skill Development Activities, will be **scaled down to 50 marks CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester-End Examination:**

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.

**Suggested Learning Resources:**

**Books**

1. Chris Spear, "System Verilog for Verification – A guide to learning the Test bench language features", Springer Publications Second Edition, 2010.
2. Stuart Sutherland, Simon Davidmann, Peter Flake, "System Verilog for Design- A guide to using system Verilog for Hardware design and modelling", Springer Publications Second Edition, 2006.

**Skill Development Activities Suggested:**

1) Interact with industry (small, medium, and large).
2) Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3) Involve in case studies and field visits/ fieldwork.
4) Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5) Handle advanced instruments to enhance technical talent.
6) Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7) Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc.
Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical –activities which will enhance their skill. The prepared report shall be

| Sl. No. | Description | Blooms Level |
|---|---|---|
| CO1 | Apply the System Verilog concepts to verify the design. | L3 |
| CO2 | Apply constrained random tests benches using System Verilog. | L3 |
| CO3 | Illustrate the concepts of OOP terminology. | L3 |
| CO4 | Appreciate Functional Coverage. | L3, L4 |

| | | | | |
|---|---|---|---|---|
| | **ASIC Design** | | | |
| | Course Code | **1MEC105A** | Scheme | 2026 |
| | Type of Course | **Professional Elective Course - I** | Semester | I |
| | Teaching Hours/Week (L:T:P) | 3:0 :0 | CIE Marks | 50 |
| | Total Hours of Pedagogy per semester L /T/P/SL&TW: | 40:0: 0:45:03 | SEE Marks | 50 |
| | Credits | **3** | Total Marks | 100 |
| | Examination type (SEE) | Theory | Exam Hours | 3 |
| | **Course outcome (Course Skill Set)**<br>At the end of the course, the student will be able to:<br>CO1: To learn ASIC methodologies and programmable logic cells to implement a function on IC.<br>CO2: To Analyse back-end physical design flow, including partitioning, floor-planning, placement, and routing.<br>CO3: To Gain sufficient theoretical knowledge for carrying out FPGA and ASIC designs.<br>CO4: To develop a low powered ASIC model for real time applications. | | | |
| | **Module-1** | | | |
| | **Introduction to ASICs:** Full custom, Semi-custom and Programmable ASICs, ASIC Design flow, ASIC cell libraries.<br>**CMOS Logic:** Data path Logic Cells: Data Path Elements, Adders: Carry skip, Carry bypass, Carry save, Carryselect, Conditional sum, Multiplier (Booth encoding), Data path Operators, I/O cells, Cell Compilers. **Number of Hours: 8** | | | |
| | **Module-2** | | | |
| | **ASIC Library Design:** Logical effort: Predicting Delay, Logical area and logical efficiency, Logical paths, Multi stage cells, Optimum delay and number of stages, library cell design.<br>**Programmable ASIC Logic Cells:** MUX as Boolean function generators, Acted ACT: ACT 1, ACT 2 and ACT 3 Logic Modules, Xilinx LCA: XC3000 CLB, Altera FLEX and MAX, Programmable ASIC I/O Cells: Xilinx and Altera I/O Block.<br>**Number of Hours: 9** | | | |
| | **Module-3** | | | |
| | **Low-level design entry:** Schematic entry: Hierarchical design, The cell library, Names, Schematic Icons & Symbols, Nets, Schematic Entry for ASICs, Connections, vectored instances & buses, Edit in place, attributes, Netlist screener.<br>**ASIC Construction:** Physical Design, CAD Tools System partitioning, Estimating ASIC size. Partitioning: Goals and objectives, Constructive Partitioning, Iterative Partitioning Improvement, KL, FM and Look Ahead algorithms.<br>**Number of Hours: 9** | | | |
| | **Module-4** | | | |
| | **Floor planning and placement:** Goals and objectives, Measurement of delay in Floor planning, Floor planning tools, Channel definition, I/O and Power planning and Clock planning. | | | |

| | |
|---|---|
| | **Placement:** Goals and Objectives, Min-cut Placement algorithm, Iterative Placement Improvement, Time driven placement methods, Physical Design Flow.<br>**Number of Hours: 8** |
| | **Module-5** |
| | **Routing:** Global Routing: Goals and objectives, Global Routing Methods, Global routing between blocks, Back-annotation. Detailed Routing: Goals and objectives, Measurement of Channel Density, Left-Edge Algorithm, Area-Routing Algorithms, Multilevel routing, Timing –Driven detailed routing, Final routing steps, Special Routing, Circuit extraction and DRC. **Number of Hours: 8** |

**Suggested Learning Resources: (Text Book/ Reference Book/ Manuals):**

**Text books:**

1. Michael John Sebastian Smith, "Application - Specific Integrated Circuits", Addison-Wesley Professional, 2005
2. Neil H.E. Weste, David Harris, and Ayan Banerjee, "CMOS VLSI Design: A Circuits and Systems Perspective", Addison Wesley/ Pearson education 3rd edition, 2011
3. Vikram Arkalgud Chandrasetty, "VLSI Design: A Practical Guide for FPGA and ASIC Implementations" Springer, ISBN: 978-1-4614-1119-2. 2011
4. Rakesh Chadha, Bhasker J, "An ASIC Low Power Primer", Springer, ISBN: 978-14614-4270-7.

**Reference books:**

5. Peter J. Ashenden Digital Design (Verilog): An Embedded Systems Approach Using Verilog,1st Edition, Kindle Edition

**Web links and Video Lectures (e-Resources):**

1. https://www.youtube.com/watch?v=oZSv68esbgI
2. https://www.youtube.com/watch?v=4cPkr1VHu7Q
3. https://nptel.ac.in/courses/106105161

**Teaching-Learning Process (Innovative Delivery Methods):**

The following are sample strategies that educators may adopt to enhance the effectiveness of the teaching-learning process and facilitate the achievement of course outcomes.

1. Flipped Classroom
2. Problem-Based Learning (PBL)
3. Case-Based Teaching
4. Simulation and Virtual Labs
5. ICT-Enabled Teaching

**Assessment Structure:**

The assessment in each course is divided equally between Continuous Internal Evaluation (CIE) and the Semester End Examination (SEE), with each carrying 50% weightage.

- To qualify and become eligible to appear for SEE, in the **CIE**, a student must score at least **40% of 50 marks**, i.e., **20 marks**.
- To pass the **SEE**, a student must score at least **35% of 50 marks**, i.e., **18 marks**.

- Notwithstanding the above, a student is considered to have **passed the course,** provided the combined total of **CIE and SEE** is at least **40 out of 100 marks**.

**Continuous Comprehensive Assessments (CCA)+ Internal Assessment Test (IA) = Continuous Internal Evaluation CIE [25+25=50 marks]**

A minimum of **two Internal Assessment Tests(IA)** shall be conducted, carrying a total of **25 marks**.

In addition, **Continuous Comprehensive Assessment (CCA)** shall be conducted for a total of **25 marks**.

It is recommended to include **a maximum of two learning activities** as part of the CCA to foster the **holistic development of students**. These activities shall be:

| Sl. No. | Name of the Learning activity | Maximum Marks |
|---|---|---|
| 1. | RTL Coding & Simulation,Synthesis & Timing Closure,Physical Design. | 15 |
| 2. | Design for Test (DFT) Implementation, Verification & Testbench,Technical Report: Communicating hardware trade-offs, | 10 |

**Instruction for Learning activity 1**

1. The course instructor shall guide students to conduct an extensive literature survey on recent trends in low-power design for mobile and embedded applications and select a suitable emerging trend for detailed study.
2. Based on the selected trend, students shall carry out a comprehensive case study, focusing on its concepts, design methodologies, implementation techniques, advantages, challenges, and real-world applications.
3. Students shall prepare and submit a detailed technical report and deliver a presentation summarizing the findings of their case study.
4. The course instructor shall evaluate student performance based on the quality of the literature survey, depth of analysis in the case study, report preparation, presentation skills, and adherence to the prescribed evaluation rubrics

**Instruction for Learning activity 2**

1. The course instructor shall provide students with a basic Verilog design (e.g., 4-bit counter, ALU, etc.) and instruct them to simulate the design and measure its power consumption using suitable EDA tools.
2. Students shall apply at least two low-power design techniques and re-simulate the design to evaluate and compare the power savings achieved.
3. Students shall prepare a brief report highlighting the power analysis results, techniques implemented, associated trade-offs, and any impact on performance or area.
4. The course instructor shall facilitate a group discussion on the effectiveness of various low-power techniques for different design scenarios..

**Rubrics for Learning Activity 1**

| Performance Indicator | Superior | Good | Fair | Needs Improvement | Unacceptable |
|---|---|---|---|---|---|
| PI 1: Literature Survey & Trend Identification (10 Marks) (CO1/PO1,PO2,PO12) | Extensive review of recent, high-quality literature; trend selected with strong technical justification. | Good review of relevant literature; trend selection well justified. | Adequate review with reasonable justification. | Limited literature reviewed; weak justification. | Very few sources reviewed; trend selection unsupported. |
| PI2: Analysis of Low-Power Techniques (10 Marks) (CO2/PO2,PO4) | Demonstrates comprehensive understanding with critical analysis and insights. | Demonstrates strong understanding with good analysis. | Demonstrates satisfactory understanding of concepts. | Basic understanding with limited analysis. | Poor understanding and inadequate analysis. |
| PI3: Design Methodologies, Challenges and Applications (10 Marks) (CO3/PO3,PO4) | Thorough evaluation of methodologies, advantages, challenges, and applications with supporting evidence. | Good evaluation covering most aspects. | Adequate discussion with some relevant examples. | Limited discussion and weak connections. | Incomplete or inaccurate evaluation. |
| PI4: Technical Report (10 Marks) (CO1-CO5/PO9,PO10,PO12) | Professionally organized, technically sound, well-referenced, and error-free. | Well-structured report with minor errors. | Acceptable structure and documentation. | Report lacks clarity and contains several errors. | Poorly organized and incomplete report. |

| | | | | | |
|---|---|---|---|---|---|
| PI5: Presentation and Q&A (10 Marks) (CO1-CO5/PO9,PO10,PO12) | Excellent delivery, effective visuals, confident responses to all questions. | Very good presentation and responses to most questions. | Good presentation with satisfactory responses. | Fair presentation; difficulty answering questions. | Poor presentation and unable to answer questions adequately. |

**Suggested Learning Activities may include (but are not limited to):**

- Course Project
- Case Study Presentation
- Programming Assignment
- Tool/Software Exploration
- Literature Review
- Open Book Test (preferably at RBL4 and RBL5 levels)

| Performance Indicator | Superior | Good | Fair | Needs Improvement | Unacceptable |
|---|---|---|---|---|---|
| PI1: Simulation and Power Measurement (10 Marks) (CO1,CO5/PO1,PO5) | Correct simulation, accurate power measurement, and complete verification of results. | Minor errors in setup; power analysis largely correct. | Simulation completed with acceptable results. | Partial simulation or incomplete power analysis. | Unable to simulate or obtain meaningful results. |
| PI2: Implementation of Low-Power Techniques (10 Marks) (CO3,CO4/PO3,PO5) | Successfully implements two or more suitable techniques with proper justification. | Implements two techniques with minor issues. | Implements at least one technique effectively and another partially. | Limited implementation with significant errors. | No meaningful implementation of low-power techniques. |

| | | | | | |
|---|---|---|---|---|---|
| PI3: Analysis of Power Savings and Trade-offs (10 Marks) (CO2,CO5/PO2,PO4) | Comprehensive comparison of power, area, and performance impacts with clear conclusions. | Good analysis with relevant comparisons. | Adequate analysis of power reduction results. | Limited interpretation of results. | Inaccurate or missing analysis. |
| PI4: Technical Report (10 Marks) (CO5/PO10) | Well-structured, technically sound, complete results, figures, and discussions. | Good report with minor deficiencies. | Satisfactory documentation and presentation of results. | Incomplete or poorly organized report. | Very poor or missing report. |
| PI5: Group Discussion and Communication (10 Marks) (CO2,CO3/PO9,PO10) | Actively contributes, demonstrates strong technical understanding, and answers questions confidently. | Good participation with sound technical inputs. | Participates adequately with basic understanding. | Limited participation and weak responses. | No participation or inability to explain work. |

**Suggested Innovative Delivery Methods may include (but are not limited to):**

- Flipped Classroom
- Problem-Based Learning (PBL)
- Case-Based Teaching
- Simulation and Virtual Labs
- Partial Delivery of course by Industry expert/ industrial visits
- ICT-Enabled Teaching

| | | | |
|---|---|---|---|
| | **Term Work (TW) and Self Learning (SL) components in Number of Hours per semester** | | |
| | Term work (includes assignments, seminars, micro projects, industrial visits, any other student activities etc.) | | |
| | **Sl. No.** | **Term Work (TW) Activity** | **Number of Hours / Semester** |
| | 1. | **Semicustom vs. Full-Custom Cell Layout Comparison:** *Drawing a clean schematic vs. stick diagrams, analyzing propagation delays using Logical Effort.* | **3 Hours** |
| | 2. | **Pre-Layout Size Estimation & Partitioning Lab:** *Manually applying the Kernighan-Lin (KL) algorithm on a 10-node netlist graph* | **3 Hours** |
| | 3. | **Floorplanning & Pad Ring IO Constraints Workshop:** *Defining power/ground rings, macro placement, and configuring I/O cell bonding pads* | **3 Hours** |
| | 4. | **Design Rule Checking (DRC) & Layout vs. Schematic (LVS):***Running extraction tools to spot electromigration issues, antenna effects, and geometric violations* | **3 Hours** |
| | SL: Self Learning, MOOCs, spoken tutorials, online educational resources etc. | | |
| | **Sl. No.** | **Self-Learning (SL) Activity** | **Number of Hours / Semester** |
| | 1. | **Advanced Datapath Components** *Deep dive into Booth-recoded Wallace Tree multipliers and high-performance I/O cell structures* : **NPTEL / Swayam**: *Digital VLSI Design* lectures or IEEE Solid-State Circuits Society tutorials | **4 Hours** |
| | 2. | **Commercial Hardware Architectures** *Analyzing how modern AMD/Xilinx UltraScale+ CLBs or Intel Agilex ALMs handle complex logic functions:* Official Xilinx/Altera reference manuals detailing hardware macro architectures. | **4 Hours** |
| | 3. | **Graph Theory in Physical Design Automation** *Understanding hypergraphs, simulated annealing for layout optimization, and timing-driven placement math* :**Coursera / edX**: *VLSI CAD: Logic to Layout* | **4 Hours** |

| | | | |
|---|---|---|---|
| | | (University of Illinois) or open-source courses on EDA algorithms | |
| | 4. | **Open-Source Toolchains Exploration** *Getting familiar with open EDA flows like OpenLane, Yosys, and SkyWater 130nm PDKs* :**GitHub Repositories / OpenRoad Project**: Hands-on exploration of end-to-end open-source silicon design paths | **4 Hours** |
| | 5. | **Deep Sub-Micron (DSM) Realities** *Studying modern physical limitations like crosstalk, interconnect parasitics, and 3D IC/FinFET routing* : **Industry Tech Journals**: Seminar topics pulled from recent IEEE ISSCC or DAC conference papers | **4 Hours** |

## Continuous Internal Evaluation (CIE)

1. The CIE marks shall be decided based on internal tests and other outcome-based activities. The continuous internal evaluation shall be carried out by the teacher handling the course.
2. Out of 50 marks earmarked for CIE, 25 marks shall be assigned for internal tests. The first test shall be conducted after completing two modules of the syllabus and the second one after completing the remaining three modules.
3. The remaining 25 marks shall be assigned for Continuous Course Assessment (CCA), conducted as per the rubrics listed in the assessment section of the respective syllabus.
4. A student shall obtain a minimum of 40% marks or 20 out of 50 marks allotted to CIE to become eligible to appear for the SEE.

## Passing requirement in SEE

1. For a pass in the Semester End Examination (SEE), a student shall secure a minimum of 35 marks out of 100.
2. For the declaration of a pass grade, the sum of the Continuous Internal Evaluation (CIE) marks (out of 50) marks and the SEE marks scaled down to 50 shall be greater than or equal to 40 marks.
3. If the total (CIE + SEE) is less than 40 marks, the student shall be awarded the grade ‘F’ (Fail).

| ADVANCED COMPUTER NETWORKS | | | |
|---|---|---|---|
| Course Code | **1MEC105B** | Scheme | 2026 |
| Type of course | **Professional Elective Course- I** | Semester | I |
| Teaching Hours/Week (L:T:P) | 3:0:0 | CIE Marks | 50 |
| Total Hours of Pedagogy L:T:P:SL:TW | 42:00 :00:45:03 | SEE Marks | 50 |
| Credits | **03** | Total Marks | 100 |
| Type of Examination (IPCC): | Theory- CIE +SEE, and Lab- CIE only. | Exam Hours | 03 |

**Course outcome (Course Skill Set)**

At the end of the course, the student will be able to:

1. Explore advanced concepts of next generation networks.
2. Analyze TCP/IP variants, network Algorithm's, Protocols and their functionalities.
3. Comprehend features of SDN and its application to next generation systems.
4. Develop different protocols used at application layer.

**Module-1**

**Foundation:** Building a Network, Requirements, Perspectives, Scalable Connectivity, -Cost Effective Resource sharing, Internet, Protocol, Network Edge, Network Core, Access Networks and Physical Media, Delay and Loss in Packet-Switched Networks, Protocol Layers and Their Service Models, Internet Backbones, NAPs, and ISPs. Network models, OSI, TCP/IP Protocol layering, Performance, Bandwidth and Latency, Delay X Bandwidth Product, Stop-and-Wait, Sliding Window. **Number of Hours:8**

**Module-2**

**Internetworking I:** Switching and Bridging, Datagram's, Virtual Circuit Switching, Source Routing, Bridges and LAN Switches, Basic Internetworking (IP), Internetwork, Global Addresses, Datagram Forwarding in IP, Subnetting and classless addressing, Address Translation (ARP) Host Configuration (DHCP), Error Reporting(ICMP), Virtual Networks and Tunnels. **Number of Hours:9**

**Module-3**

**Internetworking- II:** Network as a Graph, Distance Vector (RIP), Link State (OSPF), Metrics, The Global Internet, Routing Areas, Routing among Autonomous systems (BGP), IP Version 6(IPv6), Mobility and Mobile IP. **End-to-End Protocols:** Simple Demultiplexer (UDP), Reliable Byte Stream (TCP), End-to-End Issues, Segment Format, Connecting Establishment and Termination

**Number of Hours:9**

| Module-4 |
|---|
| **Modern day Networking**: Network Impasse, Network Ossification, Network Softwarization – Introduction, Network Virtualization, Network Function Virtualization (NFV)- Architecture and Concepts, Separation of control plane and data plane, Software Defined Networking (SDN). **Number of Hours:8** |
| **Module-5** |
| **Congestion Control and Resource Allocation:** Congestion-Avoidance Mechanisms, DEC bit, Random Early Detection (RED), Source-Based Congestion Avoidance. The Domain Name System (DNS), Electronic Mail (SMTP, POP, IMAP, MIME), World Wide Web (HTTP), Network Management (SNMP) **Number of Hours:8** |

**Suggested Learning Activities may include (but are not limited to):**

- Course Project
- Case Study Presentation
- Programming Assignment
- Tool/Software Exploration
- Literature Review
- Open Book Test (preferably at RBL4 and RBL5 levels)
- GATE-based Aptitude Test
- Assignment (at RBL3, RBL4, or RBL5 levels)
- Use of MOOCs and Online Platforms

| **Term Work (TW) and Self Learning (SL) components in**<br>**Number of hours per semester** | | |
|---|---|---|
| Term work (includes assignments, seminars, micro projects, industrial visits, any other student activities etc.) | | |
| **Sl. No.** | **Term Work (TW) Activity** | **Number of Hours / Semester** |
| 1. | Flipped Classroom<br>Problem-Based Learning (PBL)<br>Case-Based Teaching | 11 |
| SL: Self Learning, MOOCs, spoken tutorials, online educational resources etc. | | |
| **Sl. No.** | **Self-Learning (SL) Activity** | **Number of Hours / Semester** |
| 1. | Modelling Software Defined Networks | 03 |
| 2. | Architecting the WiFi 6/7 RAN, Adaptive Schedulaing | 03 |

**Continuous Internal Evaluation (CIE)**

**(i)Theory component**

The CIE marks of 25 shall be earmarked for two tests.

The first test shall be conducted after completing two modules of the syllabus and the second one after completing the rest three modules.

Each test shall be conducted for 25 marks. The average of the two tests scaled down to 25 marks shall constitute the test marks for a maximum of 25 marks.

**(ii) Laboratory component**

Out of 25 marks, 15 marks shall be assigned for assessment as per the rubrics listed in the course syllabus.

The remaining 10 marks shall be based on the practical test conducted by two Internal examiners appointed by the HoD. The allotment of marks shall be as per the rubrics defined for regular class work and practical test as indicated in the Table – ICs/IPCCs 1.

(i) To qualify and become eligible to appear for the SEE of the IC/IPCC, a student shall secure at least 40 % of 25 marks, i.e., 10 marks, in the CIE theory component, and at least 40 % of 25 marks, i.e., 10 marks in the CIE Practical component.

**Table – ICs/IPCCs 1 Distribution of marks**

| Component | Description | Marks |
|---|---|---|
| **Allotment of marks for regular class work** | | |
| Ability in Conducting Experiments | Initiative, skill, safety practices, teamwork, and independent handling of equipment during regular lab sessions. | 5 marks |
| Laboratory Record / Journal | Regular and neat maintenance of lab record, accuracy of results, and timely submission. | 10 marks |
| | **Subtotal** | **15** |
| **Allotment of marks for CIE practical test** | | |
| Laboratory Test / Experiment Performance | Ability to set up apparatus, follow procedure, take observations, and obtain correct results in the test experiment. | 5 marks |
| Viva-Voce | Understanding of theory, concepts, and experimental procedure; ability to explain results and answer related questions. | 5 marks |
| | **Subtotal** | **10** |
| | **Total** | **25** |

## Passing requirement in SEE

For a pass in the Semester End Examination (SEE), a student shall secure a minimum of 35 marks out of 100.

For the declaration of a pass grade, the sum of the Continuous Internal Evaluation (CIE) marks (out of 50) marks and the SEE marks scaled down to 50 shall be greater than or equal to 40 marks.

If the total (CIE + SEE) is less than 40 marks, the student shall be awarded the grade ‘F’ (Fail).

| | | | | |
|---|---|---|---|---|
| | **Wearable Health Monitoring System** | | | |
| | Course Code | 1MEC105C | Scheme | 2026 |
| | Type of Course | I | Semester | I |
| | Teaching Hours/Week (L:T:P) | 3: 0 : 0 | CIE Marks | 50 |
| | Total Hours of Pedagogy per semester L /T/P/SL&TW: | 42:0:0:45:03 | SEE Marks | 50 |
| | Credits | **3** | Total Marks | 100 |
| | Examination type (SEE) | Theory | Exam Hours | 3 |

**Course outcome (Course Skill Set)**

After successful completion of this course, students will be able to:

**CO1:** Explain the fundamentals of wearable and wireless healthcare systems, movement disorders, and the role of deep brain stimulation in the treatment of Parkinson's disease and essential tremor.

**CO2:** Analyze the design, operation, and clinical applications of deep brain stimulation systems, including device components, implantation procedures, programming, and associated risks.

**CO3:** Evaluate wearable sensing technologies, wireless communication systems, and machine learning techniques for monitoring, assessment, and management of movement disorders and other healthcare conditions.

**CO4:** Apply concepts of wearable healthcare technologies in telehealth, home care, wellness monitoring, remote patient monitoring (RPM), and digital healthcare delivery.

**Module-1**

**Wearable and Wireless Systems for Movement Disorder Evaluation and Deep Brain Stimulation Systems:** Movement Disorders: Parkinson's Disease and Essential Tremor—A General Perspective, Traditional Ordinal Strategies for Establishing the Severity and Status of Movement Disorders Such as Parkinson's Disease and Essential Tremor, Deep Brain Stimulation for the Treatment of Movement Disorder Regarding Parkinson's Disease and Essential Tremor with Device Characterization, Surgical Procedure for Deep Brain Stimulation Implantation and Operative Phase with Postoperative Risks, Preliminary Wearable and Locally Wireless Systems for Quantification of Parkinson's Disease and Essential Tremor Characteristics, Wearable and Wireless Systems with Internet Connectivity for Quantification of Parkinson's Disease and Essential Tremor Characteristics, Role of Machine Learning for Classification of Movement Disorder and Deep Brain Stimulation Status, Assessment of Machine Learning Classification Strategies for the Differentiation of Deep Brain Stimulation "On" and "Off" Status for Parkinson's Disease Using a Smartphone as a Wearable and Wireless Inertial Sensor for Quantified Feedback, New Perspectives for Network Centric Therapy for the Treatment of Parkinson's Disease and Essential Tremor.

| | |
|---|---|
| | Clinical Assessment of Parkinson's Disease, Clinical Assessment of Essential Tremor, Wearable and Wireless Systems for the Quantification of Movement Disorder Tremor, Extrapolation to Network Centric Therapy. **Number of Hours: 9** |
| | **Module-2** |
| | **Deep Brain Stimulation for the Treatment of Movement Disorder Regarding Parkinson's Disease and Essential Tremor with Device Characterization**:Introduction, The Foundations of Deep Brain Stimulation, Long-Term Efficacy and the Quest to Define the Mechanisms of Deep Brain Stimulation, Benefit and Risk Consideration of Deep Brain Stimulation, Target Selection for Deep Brain Stimulation, Essential Tremor, Parkinson's Disease, Deep Brain Stimulation System Device Description, Electrode Leads and the Implantable Pulse Generator, Battery, Electrical Signal, Deep Brain Stimulation System Programmer, Attaining the Optimal Parameter Configuration for Deep Brain Stimulation an Issue with Tuning, Future Perspectives for Deep Brain Stimulation.<br><br>**Surgical Procedure for Deep Brain Stimulation Implantation and Operative Phase with Postoperative Risks:** General Surgical Perspective and Considerations for the Application of Deep Brain Stimulation, Deep Brain Stimulation Operative Risks and Complications, Postoperative Risk Regarding Energy Interaction, Adverse Neurological and Neuropsychological Effects for Deep Brain Stimulation, Operative Technique Advocated by Allegheny General Hospital, Applied Deep Brain Stimulation Programming from Allegheny General Hospital.<br>**Number of Hours: 9** |
| | **Module-3** |
| | **Adaptive Deep Brain Stimulation:**Introduction, Foundational Technology for Adaptive Deep Brain Stimulation, Optimization Incorporating Wearable Inertial Sensor Systems, Optimization Incorporating Electrode Recordings.<br><br>**Advanced Concepts:**Introduction, Metaverse for Healthcare, Smartwatch, Flexible Electronics, Neuromorphic Artificial Intelligence, Electromagnetic Interference for Deep Brain Stimulation, Discovery and Clarification of Biomarkers, Improved Ethics for Implementing Deep Brain Stimulation.<br><br>**Number of Hours: 8** |
| | **Module-4** |
| | **Current and Future Uses of Wearable Devices:** A Diabetic's Story of Wearable Technology: A Spider Bites—Now You're a Type 1 Diabetic,The Adoption of Wearables,The Future of Wearables,Home Care and Wellness,Telehealth,Remote Patient Monitoring (RPM), RPM Data to Enable Improved Patient Care (Who Uses RPM Data?).<br><br>**COMPONENTS OF WEARABLE DEVICES:** Physiological Sensors, Wireless Communication,Batteries and Other Power Sources, Cybersecurity **Number of Hours: 8** |

| | Module-5 |
|---|---|
| | **SUCCESSFUL APPLICATIONS:** Voice Technology and Wearables: Remote Patient Monitoring, Connected Device for Improved Adherence,COVID-19 Wellness Monitoring Turns to Health Monitoring, Conclusion.<br><br>**STANDARDS AND REGULATORY:** Regulatory and Emerging Standards, Payment Strategies and Codes, Medical-Grade Interoperability.<br><br>**Number of Hours: 8** |

**Suggested Learning Resources: (Text Book/ Reference Book/ Manuals):**

**Text books:**

**1.** Wearable and Wireless Systems for Healthcare II Movement Disorder Evaluation and Deep Brain Stimulation Systems Second Edition Robert LeMoyneTimothy MastroianniDonald WhitingNestor Tomycz

**2.** Closing the Care Gap with Wearable Devices A Preface itors 1 Current and Uses of Wearable Innovating Healthcare with Wearable Patient Monitoring Routledge Taylor & Francis Group A PRODUCTIVITY PRESS BOOK Michael W Davis, Michael J Kirwan, Walter N. Maclay Harry P. Pappas

**Reference books / Manuals:**

**1.** U-Healthcare Monitoring Systems Design and Application, Volume one AP, Volume Editors: Nilanjan Dey, Amira S. Ashour, Simon James Fong and Surekha Borra.

**2.** Wearable and Nearable Biosensors and Systems for Healthcare, Edited by Marco Di Rienzo and Ramakrishna Mukkamala Printed Edition of the Special Issue Published in Sensors

**Web links and Video Lectures (e-Resources):**

1. https://www.youtube.com/watch?v=wV_wDURdGqc

2. http://www.digimat.in/nptel/courses/video/102108344/L34.html

**Teaching-Learning Process (Innovative Delivery Methods):**
The following are sample strategies that educators may adopt to enhance the effectiveness of the teaching-learning process and facilitate the achievement of course outcomes.

1. Interactive Lectures and Multimedia Presentations
2. Case-Based Learning
3. Problem-Based Learning (PBL)
4. Demonstrations and Virtual Labs
5. Flipped Classroom Approach
6. Mini Projects and Design Activities
7. Seminars and Student Presentations
8. Industry Expert Lectures and Webinars
9. Collaborative Learning and Group Discussions

10. Continuous Assessment Using Digital Learning Tools
11. Research Article Review and Discussion
12. Project-Based Learning
13. Simulation-Based Learning
14. Peer Learning Activities
15. Outcome-Based Assignments and Tutorials

**Assessment Structure:**
The assessment in each course is divided equally between Continuous Internal Evaluation (CIE) and the Semester End Examination (SEE), with each carrying 50% weightage.

- To qualify and become eligible to appear for SEE, in the **CIE**, a student must score at least **40% of 50 marks**, i.e., **20 marks**.
- To pass the **SEE**, a student must score at least **35% of 50 marks**, i.e., **18 marks**.
- Notwithstanding the above, a student is considered to have **passed the course,** provided the combined total of **CIE and SEE** is at least **40 out of 100 marks**.

**Continuous Comprehensive Assessments (CCA)+ Internal Assessment Test (IA) = Continuous Internal Evaluation CIE [25+25=50 marks]**
A minimum of **two Internal Assessment Tests(IA)** shall be conducted, carrying a total of **25 marks**.
In addition, **Continuous Comprehensive Assessment (CCA)** shall be conducted for a total of **25 marks**.
It is recommended to include **a maximum of two learning activities** as part of the CCA to foster the **holistic development of students**. These activities shall be:

| Sl. No. | Name of the Learning activity | Maximum Marks |
|---|---|---|
| 1 | Seminar Presentation on Wearable Healthcare Systems, Deep Brain Stimulation, or Emerging Healthcare Technologies | 15 Marks |
| 2 | Mini Project / Case Study Analysis on Movement Disorder Monitoring, Remote Patient Monitoring, or Wearable Device Applications | 10 Marks |

**Rubrics for Learning Activity (Based on the nature of learning activity, design the rubrics for each activity):**

| Performance Indicator (CO/PO Mapping) | Superior (5) | Good (4) | Fair (3) | Needs Improvement (2) | Unacceptable (1) |
|---|---|---|---|---|---|
| Technical Understanding (CO1, PO1) | Demonstrates comprehensive understanding of the topic | Good understanding with minor gaps | Adequate understanding | Limited understanding | Poor understanding |
| Content Organization & Presentation (CO2, PO10) | Well-structured, clear, and professional presentation | Mostly organized and clear | Moderately organized | Poor organization | Disorganized presentation |
| Analysis of Current Technologies (CO3, PO2) | Excellent analysis and critical evaluation | Good analysis | Basic analysis | Limited analysis | No meaningful analysis |
| Communication & Response to Questions (CO2, PO10) | Answers all questions confidently and accurately | Answers most questions correctly | Answers some questions | Difficulty answering questions | Unable to answer questions |

**Suggested Learning Activities may include (but are not limited to):**

- Course Project
- Case Study Presentation
- Programming Assignment
- Tool/Software Exploration
- Literature Review
- Open Book Test (preferably at RBL4 and RBL5 levels)
- GATE-based Aptitude Test
- Assignment (at RBL3, RBL4, or RBL5 levels)
- Any other relevant and innovative academic activity
- Use of MOOCs and Online Platforms

**Suggested Innovative Delivery Methods may include (but are not limited to):**

- Flipped Classroom
- Problem-Based Learning (PBL)
- Case-Based Teaching
- Simulation and Virtual Labs
- Partial Delivery of course by Industry expert/ industrial visits
- ICT-Enabled Teaching
- Role Play

| Sl. No. | Term Work (TW) Activity | Number of Hours / Semester |
|---|---|---|
| 1 | Assignment on Wearable Healthcare Systems, Parkinson's Disease, and Deep Brain Stimulation | 5 Hours |
| 2 | Seminar Presentation on Emerging Trends in Wearable Devices and Remote Patient Monitoring | 8 Hours |
| 3 | Mini Project / Case Study Analysis on Movement Disorder Monitoring or Healthcare IoT Applications | 12 Hours |
| 4 | Self-Learning and Review of Research Articles, E-Resources, and Technical Reports Related to the Course | 5 Hours |

| Sl. No. | Self-Learning (SL) Activity | Number of Hours / Semester |
|---|---|---|
| 1 | Completion of Online Courses/MOOCs on Wearable Healthcare Systems, IoT, or Machine Learning in Healthcare | 5 Hours |
| 2 | Study of Video Lectures and E-Resources on Parkinson's Disease, Essential Tremor, and Deep Brain Stimulation | 5 Hours |
| 3 | Review and Summary of Research Articles on Adaptive DBS, Remote Patient Monitoring, and Emerging Wearable Technologies | 4 Hours |
| 4 | Self-Study of Standards, Regulatory Guidelines, and Healthcare Interoperability Frameworks (FDA, HL7, IEEE, ISO) | 4 Hours |

## Continuous Internal Evaluation (CIE)

1. The CIE marks shall be decided based on internal tests and other outcome-based activities. The continuous internal evaluation shall be carried out by the teacher handling the course.
2. Out of 50 marks earmarked for CIE, 25 marks shall be assigned for internal tests. The first test shall be conducted after completing two modules of the syllabus and the second one after completing the remaining three modules.
3. The remaining 25 marks shall be assigned for Continuous Course Assessment (CCA), conducted as per the rubrics listed in the assessment section of the respective syllabus.
4. A student shall obtain a minimum of 40% marks or 20 out of 50 marks allotted to CIE to become eligible to appear for the SEE.

## Passing requirement in SEE

1. For a pass in the Semester End Examination (SEE), a student shall secure a minimum of 35 marks out of 100.

2. For the declaration of a pass grade, the sum of the Continuous Internal Evaluation (CIE) marks (out of 50) marks and the SEE marks scaled down to 50 shall be greater than or equal to 40 marks.
3. If the total (CIE + SEE) is less than 40 marks, the student shall be awarded the grade ‘F’ (Fail).

| ELECTRONIC POWER CONVERTERS | | | |
|---|---|---|---|
| Course Code | **1MEC105D** | Scheme | 2026 |
| Type of Course | **Professional Elective Course- I** | Semester | 1 |
| Teaching Hours/Week (L:T:P) | 42:0:0 | CIE Marks | 50 |
| Total Hours of Pedagogy per semester L /T/P/SL&TW: | 42:00:00:45:03 | SEE Marks | 50 |
| Credits | **3** | Total Marks | 100 |
| Examination type (SEE) | Theory | Exam Hours | 3 |

**Course outcome (Course Skill Set)**

**At the end of the course, the student will be able to:**

**1:** Analyze the switching characteristics, losses and protection requirements of power semiconductor devices.

**2:** Analyze and design AC–DC, DC–DC, DC–AC and AC–AC power converter circuits.

**3:** Apply modulation and control techniques to improve converter performance and power quality.

**4:** Evaluate and select suitable converter topologies for renewable energy, electric vehicle and industrial applications.

**Module-1**

**Characteristics and switching behaviour of power diodes:** SCRs, MOSFETs, IGBTs and IGCTs; comparison of silicon, silicon carbide and gallium nitride devices; static and dynamic characteristics; conduction and switching losses; safe operating area; device selection; series and parallel operation; gate-drive circuits; isolation techniques; snubber circuits; protection against overcurrent, overvoltage and thermal stress; heat sinks and thermal design; introduction to power converter classification and performance indices**.**

**Number of Hours:08**

**Module-2**

**AC DC Converters:** Single-phase and three-phase uncontrolled rectifiers; semi-controlled and fully controlled converters; effect of source inductance and overlap angle; converter operation with R, RL and RLE loads; dual converters; performance parameters; input power factor and harmonic distortion; pulse-width-modulated rectifiers; active front-end converters; single-phase and three-phase AC voltage controllers; integral cycle control; cycloconverters; matrix converters; applications in heating, lighting and speed-control systems.

**Number of Hours: 09**

**Module-3**

**DC-DC Converters:** Principles of switch-mode DC–DC conversion; analysis and design of buck, boost, buck–boost, Ćuk, SEPIC and Zeta converters; continuous and discontinuous conduction modes; converter ripple analysis; selection of inductors, capacitors and semiconductor devices; isolated converters—flyback, forward, push-pull, half-bridge and full-bridge converters; transformer design considerations; current-mode and voltage-mode control; small-signal modelling; closed-loop control; interleaved and bidirectional converters; applications in battery charging and electric vehicles.

**Number of Hours: 09**

**Module-4**

**DC- AC converters and Modulation techniques:** Single-phase and three-phase voltage-source inverters; current-source inverters; square-wave, quasi-square-wave and pulse-width modulation techniques; sinusoidal PWM, space-vector PWM and selective harmonic elimination; inverter output-voltage control; harmonic analysis; dead-time effects; multilevel inverter topologies—diode-clamped, flying-capacitor and cascaded H-bridge converters; modulation and capacitor-voltage balancing; grid-connected inverters; synchronization and current-control techniques; L, LC and LCL filter design.

**Number of Hours: 08**

**Module-5**

**Resonant Converters and Emerging Applications**: Principles of soft switching, zero-voltage switching and zero-current switching, resonant-switch, series-resonant, parallel-resonant and LLC resonant converters; soft-switched PWM converters; high-frequency converter design; electromagnetic interference and electromagnetic compatibility considerations; converters for solar photovoltaic and wind-energy systems; maximum power-point tracking; battery energy-storage interfaces; electric-vehicle traction and charging converters; solid-state transformers; HVDC and FACTS converter applications; wide-bandgap-device-based high-frequency converters; efficiency and reliability evaluation.

**Number of Hours: 08**

**Suggested Learning Resources: (Text Book/ Reference Book/ Manuals):**

**[1]** M. H. Rashid, *Power Electronics: Devices, Circuits, and Applications*, 4th ed. Harlow, U.K.: Pearson, 2014.

[2] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics: Converters, Applications, and Design*, 3rd ed. Hoboken, NJ, USA: Wiley, 2003.

[3] R. W. Erickson and D. Maksimović, *Fundamentals of Power Electronics*, 3rd ed. Cham, Switzerland: Springer, 2020.

[4] D. W. Hart, *Power Electronics*. New York, NY, USA: McGraw-Hill, 2011.

**Assessment Structure:**

The assessment in each course is divided equally between Continuous Internal Evaluation (CIE) and the Semester End Examination (SEE), with each carrying 50% weightage.

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**Continuous Comprehensive Assessments (CCA)+ Internal Assessment Test (IA) = Continuous Internal Evaluation CIE [25+25=50 marks]**

A minimum of **two Internal Assessment Tests (IA)** shall be conducted, carrying a total of **25 marks**.

In addition, **Continuous Comprehensive Assessment (CCA)** shall be conducted for a total of **25 marks**.

It is recommended to include **a maximum of two learning activities** as part of the CCA to foster the **holistic development of students**. These activities shall be:

**Rubrics for Learning Activity (Based on the nature of learning activity, design the rubrics for each activity):**

| | Superior | Good | Fair | Needs Improvement | Unacceptable |
|---|---|---|---|---|---|
| **Performance Indicator- 1 (CO/PO Mapping)** | **H** | **M** | **H** | | |
| **Performance Indicator-2 (CO/PO Mapping)** | **L** | **L** | **L** | | |
| **Performance Indicator- 3 (CO/PO Mapping)** | **M** | **M** | **M** | | |

**Term Work (TW) and Self Learning (SL) components in Number of Hours per semester**

Term work (includes assignments, seminars, micro projects, industrial visits, any other student activities etc.)

| Sl. No. | Term Work (TW) Activity | Number of Hours / Semester |
|---|---|---|
| 1. | Flipped Classroom<br>Problem-Based Learning (PBL)<br>Case-Based Teaching | 11 |

SL: Self Learning, MOOCs, spoken tutorials, online educational resources etc.

| Sl. No. | Self-Learning (SL) Activity | Number of Hours / Semester |
|---|---|---|
| 1. | GATE-based Aptitude Test | 20 |
| 2. | Case Study Presentation | 20 |
| 3. | Assignment (at RBL3, RBL4, or RBL5 levels) | 05 |

| LOW POWER VLSI DESIGN | | | |
|---|---|---|---|
| Course Code | **1MEC106A** | Scheme | 2026 |
| Type of Course | **Professional Elective Courses- II** | Semester | I |
| Teaching Hours/Week (L:T:P) | 3:0 :0 | CIE Marks | 50 |
| Total Hours of Pedagogy per semester L /T/P/SL&TW: | 42:0:0:45:03 | SEE Marks | 50 |
| Credits | **3** | Total Marks | 100 |
| Examination type (SEE) | Theory | Exam Hours | 3 |

**Course outcome (Course Skill Set)**

At the end of the course, the student will be able to:

CO1: Identify and illustrate the sources of power dissipation, also formulate and compute the dissipated power at different abstract levels of the circuits.

CO2: Analyse the given circuits for the impact of transistor sizing, gate sizing, equivalent pin ordering, network restructuring, and special latches and flip-flops in power consumption reduction.

CO3: Apply circuit-level and logic-level design strategies such as transistor sizing, gate sizing, signal gating, logic encoding, and low-power cell design to minimize power consumption.

CO4: Design and optimize low-power digital cells using techniques such as adjustable device threshold voltage, gate reorganization, signal gating, and logic encoding.

**Module-1**

**Introduction:** Need for low power VLSI chips, charging and discharging capacitance, short circuit current in CMOS leakage current, static current, basic principles of low power design, low power figure of merits. Simulation power analysis: SPICE circuit simulation, Monte Carlo simulation.

Number of Hours: **9 Hours**

**Module-2**

**Circuit:** Transistor and gate sizing, equivalent pin ordering, network restructuring and reorganization, special latches and flip flops, low power digital cell library, adjustable device threshold voltage.

Number of Hours: **8 Hours**

**Module-3**

**Logic:** Gate reorganization, signal gating, logic encoding, state machine encoding, precomputation logic.

**Low power Clock Distribution**: Power dissipation in clock distribution, single driver versus distributed buffers.

Number of Hours: **9 Hours**

**Module-4**

**Low power Architecture and Systems**: Power and performance management, switching activity reduction, flow graph transformation.

**Low power memory design**: Introduction, sources and reductions of power dissipation in memory subsystem.

Number of Hours: **8 Hours**

**Module-5**

**Algorithm and Architectural Level Methodologies**: Introduction, design flow, Algorithmic level analysis and optimization, Architectural level estimation and synthesis. **Advanced Techniques**: Adiabatic computation, Asynchronous circuits.

Number of Hours: **8 Hours**

**Suggested Learning Resources: (Text Book/ Reference Book/ Manuals):**

**Text books:**

1. Practical Low Power Digital VLSI Design, Gary K.Yeap, 1998, ISBN 978-1-4613 7778-8, ISBN 978-1 4615-6065-4, (eBook) DOI 10.1007/978-1-4615 6065-4.
2. Low Power Design Methodologies, Jan M. Rabaey University Califomia and Massoud Pedram University of Southem Califomia, 2010, ISBN 978-1-46 13 5975-3, ISBN 978-1 4615-2307-9, (eBook) DOI 10.1007/978-1-4615 2307-9.

**Reference books:**

1. Low-Power CMOS VLSI Circuit Design, Kaushik Roy and Sharat Prasad, John Wiley, 2000. ISBN 13 9788126520237
2. Low-Voltage Low-Power Subsystems, K.-S. Yeo and K. Roy, McGraw Hill, 2004.
3. Dynamic Power Management Design Techniques and CAD Tools, L. Benini and G. De Micheli, Springer, 1998.
4. Leakage in Nanometer CMOS Technologies, S. G. Narendra and A. Chandrakasan, Springer, 2005.

**Web links and Video Lectures (e-Resources):**

1. https://www.youtube.com/watch?v=TFOO1JAll2Y
2. https://www.youtube.com/watch?v=ORtlxpW_LMU
3. https://www.youtube.com/watch?v=_A7fUR2Itsc
4. https://www.youtube.com/watch?v=t-PyfAI-fX4
5. https://www.youtube.com/watch?v=dZM5jmw_xLE
6. VLSI with SPICE Code Virtual lab https://vlsis-iiith.vlabs.ac.in/
7. Power Management in VLSI https://www.geeksforgeeks.org/electronics-engineering/power-management-in-vlsi/
8. https://www.geeksforgeeks.org/computer-organization-architecture/difference-between-sram-and-dram/

**Teaching-Learning Process (Innovative Delivery Methods):**

The following are sample strategies that educators may adopt to enhance the effectiveness of the teaching-learning process and facilitate the achievement of course outcomes.

1. Flipped Classroom
2. Problem-Based Learning (PBL)
3. Case-Based Teaching
4. Simulation and Virtual Labs
5. ICT-Enabled Teaching

**Assessment Structure:**

The assessment in each course is divided equally between Continuous Internal Evaluation (CIE) and the Semester End Examination (SEE), with each carrying 50% weightage.

- To qualify and become eligible to appear for SEE, in the **CIE**, a student must score at least **40% of 50 marks**, i.e., **20 marks**.
- To pass the **SEE**, a student must score at least **35% of 50 marks**, i.e., **18 marks**.

- Notwithstanding the above, a student is considered to have **passed the course,** provided the combined total of **CIE and SEE** is at least **40 out of 100 marks**.

**Continuous Comprehensive Assessments (CCA)+ Internal Assessment Test (IA) = Continuous Internal Evaluation CIE [25+25=50 marks]**

A minimum of **two Internal Assessment Tests(IA)** shall be conducted, carrying a total of **25 marks**.

In addition, **Continuous Comprehensive Assessment (CCA)** shall be conducted for a total of **25 marks**.

It is recommended to include **a maximum of two learning activities** as part of the CCA to foster the **holistic development of students**.

These activities shall be:

| Sl. No. | Name of the Learning activity | Maximum Marks |
|---|---|---|
| 1. | Case studies Recent trends in low-power design for mobile and embedded application. | 20 |
| 2. | Design & Optimize: Low-Power Digital Circuit Challenge | 20 |

**Instruction for Learning activity 1**

1. The course instructor shall guide students to conduct an extensive literature survey on recent trends in low-power design for mobile and embedded applications and select a suitable emerging trend for detailed study.
2. Based on the selected trend, students shall carry out a comprehensive case study, focusing on its concepts, design methodologies, implementation techniques, advantages, challenges, and real-world applications.
3. Students shall prepare and submit a detailed technical report and deliver a presentation summarizing the findings of their case study.
4. The course instructor shall evaluate student performance based on the quality of the literature survey, depth of analysis in the case study, report preparation, presentation skills, and adherence to the prescribed evaluation rubrics

**Instruction for Learning activity 2**

1. The course instructor shall provide students with a basic Verilog design (e.g., 4-bit counter, ALU, etc.) and instruct them to simulate the design and measure its power consumption using suitable EDA tools.
2. Students shall apply at least two low-power design techniques and re-simulate the design to evaluate and compare the power savings achieved.

| Performance Indicator | Superior | Good | Fair | Needs Improvement | Unacceptable |
|---|---|---|---|---|---|
| PI 1: Literature Survey & Trend Identification (10 Marks) (CO1/PO1,PO 2,PO12) | Extensive review of recent, high-quality literature; trend selected with strong technical justification. | Good review of relevant literature; trend selection well justified. | Adequat e review with reasonab le justificati on. | Limited literature reviewed; weak justification. | Very few sources reviewed; trend selection unsupported. |
| PI2: Analysis of Low-Power Techniques (10 Marks) (CO2/PO2,PO 4) | Demonstrat es comprehens ive understandi ng with critical analysis and insights. | Demonstrates strong understandin g with good analysis. | Demonst rates satisfacto ry understa nding of concepts. | Basic understanding with limited analysis. | Poor understanding and inadequate analysis. |
| PI3: Design Methodologies , Challenges and Applications (10 Marks) (CO3/PO3,PO 4) | Thorough evaluation of methodologi es, advantages, challenges, and applications with supporting | Good evaluation covering most aspects. | Adequat e discussio n with some relevant examples . | Limited discussion and weak connections. | Incomplete or inaccurate evaluation. |
| **Performance Indicator** | **Superior** | **Good** | **Fair** | **Needs Improvement** | **Unacceptable** |
| PI1: Simulation and Power Measurement (10 Marks) (CO1,CO5/PO1 ,PO5) | Correct simulation, accurate power measuremen t, and complete verification of results. | Minor errors in setup; power analysis largely correct. | Simulati on complet ed with acceptab le results. | Partial simulation or incomplete power analysis. | Unable to simulate or obtain meaningful results. |
| PI2: Implementation | Successfully implements | Implements two | Impleme nts at | Limited implementation | No meaningful implementation |

| | | | | | |
|---|---|---|---|---|---|
| of Low-Power Techniques (10 Marks) (CO3,CO4/PO3 ,PO5) | two or more suitable techniques with proper justification. | techniques with minor issues. | least one techniqu e effective ly and another partially. | with significant errors. | of low-power techniques. |
| PI3: Analysis of Power Savings and Trade-offs (10 Marks) (CO2,CO5/PO2 ,PO4) | Comprehens ive comparison of power, area, and performance impacts with clear conclusions. | Good analysis with relevant comparisons. | Adequat e analysis of power reductio n results. | Limited interpretation of results. | Inaccurate or missing analysis. |
| PI4: Technical Report (10 Marks) (CO5/PO10) | Well-structured, technically sound, complete results, figures, and discussions. | Good report with minor deficiencies. | Satisfact ory docume ntation and presenta tion of results. | Incomplete or poorly organized report. | Very poor or missing report. |
| PI5: Group Discussion and Communication (10 Marks) (CO2,CO3/PO9 ,PO10) | Actively contributes, demonstrate s strong technical understandi ng, and answers questions confidently. | Good participation with sound technical inputs. | Participa tes adequate ly with basic understa nding. | Limited participation and weak responses. | No participation or inability to explain work. |

**Suggested Learning Activities may include (but are not limited to):**

- Course Project
- Case Study Presentation
- Programming Assignment
- Tool/Software Exploration
- Literature Review
- Open Book Test (preferably at RBL4 and RBL5 levels)
- GATE-based Aptitude Test
- Assignment (at RBL3, RBL4, or RBL5 levels)
- Any other relevant and innovative academic activity
- Use of MOOCs and Online Platforms

**Term Work (TW) and Self Learning (SL) components in Number of Hours per semester**

Term work (includes assignments, seminars, micro projects, industrial visits, any other student activities etc.)

| Sl. No. | Term Work (TW) Activity | Number of Hours / Semester |
|---|---|---|
| 1. | Problem-Based Learning (PBL) | 03 |
| 2. | Case-Based Teaching | 06 |

SL: Self Learning, MOOCs, spoken tutorials, online educational resources etc.

| Sl. No. | Self-Learning (SL) Activity | Number of Hours / Semester |
|---|---|---|
| 1. | Discrete Transistor Modeling and Analysis, Gate-Level Logic Simulation, Architecture-Level Analysis, and Data Correlation Analysis in DSP Systems using simulation tools and mathematical methods. | 4 |
| 2. | Special latches and flip-flops, low-power digital cell library. | 4 |
| 3. | Gate reorganization, signal gating, logic and state machine encoding, and pre-computation logic. | 4 |
| 4. | Sources of Power Dissipation in DRAM and SRAM, Low Power DRAM Circuits and Low Power SRAM Circuits to enhance energy efficiency in memory systems. | 4 |
| 5. | Pass Transistor Logic Synthesis, Basics of Pass Transistor Logic, Boolean Decision Diagram and Pass Transistor Logic, Pass Transistor Logic Synthesis System. | 4 |

**Continuous Internal Evaluation (CIE)**

1. The CIE marks shall be decided based on internal tests and other outcome-based activities. The continuous internal evaluation shall be carried out by the teacher handling the course.
2. Out of 50 marks earmarked for CIE, 25 marks shall be assigned for internal tests. The first test shall be conducted after completing two modules of the syllabus and the second one after completing the remaining three modules.
3. The remaining 25 marks shall be assigned for Continuous Course Assessment (CCA), conducted as per the rubrics listed in the assessment section of the respective syllabus.
4. A student shall obtain a minimum of 40% marks or 20 out of 50 marks allotted to CIE to become eligible to appear for the SEE.

**Passing requirement in SEE**

1. For a pass in the Semester End Examination (SEE), a student shall secure a minimum of 35 marks out of 100.
2. For the declaration of a pass grade, the sum of the Continuous Internal Evaluation (CIE) marks (out of 50) marks and the SEE marks scaled down to 50 shall be greater than or equal to 40 marks.
3. If the total (CIE + SEE) is less than 40 marks, the student shall be awarded the grade ‘F’ (Fail).

| | | | | |
|---|---|---|---|---|
| | **Advanced Wireless Communication Systems** | | | |
| | Course Code | **1MEC106B** | Scheme | 2026 |
| | Type of Course | **Professional Elective Courses- II** | Semester | 1 |
| | Teaching Hours/Week (L:T:P) | 42:0:0 | CIE Marks | 50 |
| | Total Hours of Pedagogy per semester<br>L /T/P/SL&TW: | 42:0 :0:45:03 | SEE Marks | 50 |
| | Credits | **3** | Total Marks | 100 |
| | Examination type (SEE) | Theory | Exam Hours | 3 |

**Course outcome (Course Skill Set)**

**At the end of the course, the student will be able to:**

CO1: Analyze advanced wireless channels, waveforms and link-performance metrics for contemporary communication systems.

CO2: Evaluate 5G NR/5G-Advanced architectures, physical-layer procedures, massive-MIMO techniques and radio-resource-management strategies.

CO3: Design and assess advanced WLAN, IoT and Open RAN solutions using standards-based architectures and performance criteria.

CO4: Apply AI/ML methods to channel estimation, signal detection, beam management and wireless resource allocation, and examine emerging 6G/ISAC technologies.

CO5: Investigate non-terrestrial, secure and future wireless networks through simulation, experimentation and research-oriented system studies.

**Module-1**

**Advanced Wireless Channel and Physical Layer**

**Evolution and design context:** 4G, 5G, 5G-Advanced and 6G; IMT-2020/IMT-2030; eMBB, URLLC, mMTC, throughput-latency-reliability-energy-spectral-efficiency trade-offs.

**Channel modelling:** Large-/small-scale fading; frequenc/time-selective channels; spatial correlation; MIMO, UMa, UMi and high-frequency propagation; ray tracing and geometry-based stochastic models.

**Waveforms and performance:** OFDM, CP-OFDM, PAPR reduction, link adaptation; BER/BLER, SINR, signal outage, spectral/energy efficiency, link budget and CSI acquisition/feedback.

Number of Hours:10

**Module-2**

**Adavnced MIMO**

**Advanced MIMO and RRM:** Massive MIMO, beamforming, precoding, codebooks, beam management, MU-MIMO and coordinated transmission; scheduling, proportional-fair and QoS-aware scheduling, HARQ, link adaptation and dynamic spectrum allocation.

**5G-Advanced:** AI/ML-assisted RAN, CSI feedback and beam management; MIMO evolution, RedCap, positioning, sidelink, UAV/UAM communication and time-sensitive communication.

Number of Hours:08

| | |
|---|---|
| | **Module-3** |
| | **Advanced WLAN, IoT and Open RAN**<br>**Wi-Fi 6/6E/7:** IEEE 802.11ax, OFDMA, MU-MIMO, BSS colouring, TWT and 6-GHz operation; IEEE 802.11be, 320-MHz channels, 4096-QAM, MLO, Multi-RU, preamble puncturing and low-latency Wi-Fi.<br>**Advanced IoT:** NB-IoT, LTE-M, 5G RedCap, industrial IoT, URLLC, TSN integration, wireless sensor networks, energy-efficient communication and edge intelligence.<br>Number of Hours: 08 |
| | **Module-4** |
| | **AI-Native Wireless and Emerging 6G**<br>**Machine learning for wireless:** Supervised channel estimation; deep-learning signal detection; CNN/RNN/Transformer applications; reinforcement, multi-agent and federated learning;<br>**AI-native RAN:** AI-assisted scheduling,intelligent handover, traffic prediction, energy-aware RAN, distributed intelligence and AI model lifecycle.<br>Number of Hours: 08 |
| | **Module-5** |
| | **Non-Terrestrial, Secure and Future Wireless Networks**<br>**Non-terrestrial networks:** NTN architecture; LEO/MEO/GEO; 3GPP NTN; satellite-UE links, Doppler compensation, timing advance, beam hopping, satellite handover, direct-to-device and NTN-IoT.<br>**Wireless security:** Physical-layer security; jamming, spoofing and eavesdropping; zero-trust wireless networks.<br>Number of Hours: 08 |

**Laboratory Component**

- 5G NR resource grid and numerology
- OFDM/OTFS waveform comparison
- Massive-MIMO beamforming
- 5G NR scheduler
- AI-based channel estimation
- RL-based wireless scheduling
- Federated learning for wireless optimization

Tools: MATLAB, Python, NumPy, SciPy, Matplotlib, PyTorch/TensorFlow; MATLAB 5G Toolbox, ns-3, Simu5G, OMNeT++/INET; GNU Radio/USRP; OpenAirInterface, srsRAN; Linux, Wireshark, Docker and Git/GitHub.

**Suggested Learning Resources: (Text Book/ Reference Book/ Manuals):**

**Text books:**

1. Erik Dahlman, Stefan Parkvall and Johan Sköld, *5G/5G-Advanced: The New Generation Wireless Access Technology*, 3rd Edition, Academic Press–Elsevier, 2023.
2. Afif Osseiran, José F. Monserrat and Patrick Marsch (Editors), *5G Mobile and Wireless Communications Technology*, Cambridge University Press, 2016.
3. Le Liang, Shi Jin, Hao Ye and Geoffrey Ye Li, *Wireless Communications and Machine Learning*, Cambridge University Press, 2025.

**Reference books / Manuals:**

1. 'Digital Communications: Fundamentals and Applications: Fundamentals & Applications', Bernard Sklar, Pearson Education, ISBN:9788131720929, 2nd edition, 2009
2. 'Digital Communications Systems', Simon Haykin, Wiley, ISBN:9788126542314, 1st edition, 2014

**Web links and Video Lectures (e-Resources):**

- https://www.3gpp.org/
- https://www.itu.int/itu-r/en/
- https://www.ieee802.org/11/
- https://www.o-ran.org/
- https://www.nsnam.org/
- https://www.srslte.com/ (srsRAN)

**Teaching-Learning Process (Innovative Delivery Methods):**

The following are sample strategies that educators may adopt to enhance the effectiveness of the teaching-learning process and facilitate the achievement of course outcomes.

- Interactive lectures supported by standards extracts and multimedia demonstrations
- Simulation-based learning and virtual laboratories
- Problem-based and case-based learning using 5G/Wi-Fi/O-RAN scenarios
- Flipped classroom and guided research-paper discussions
- Programming assignments using MATLAB/Python/ns-3

**Continuous Comprehensive Assessments (CCA)+ Internal Assessment Test (IA) = Continuous Internal Evaluation CIE [25+25=50 marks]**

A minimum of **two Internal Assessment Tests(IA)** shall be conducted, carrying a total of **25 marks**.

In addition, **Continuous Comprehensive Assessment (CCA)** shall be conducted for a total of **25 marks**.

It is recommended to include **a maximum of two learning activities** as part of the CCA to foster the **holistic development of students**.

These activities shall be:

| Sl. No. | Name of the Learning activity | Maximum Marks |
|---|---|---|
| 1. | Simulation-based learning and virtual laboratories | 20 |
| 2. | Programming assignments using MATLAB/Python/ns-3 | 20 |

**Rubrics for Learning Activity (Based on the nature of learning activity, design the rubrics for each activity):**

| | Superior | Good | Fair | Needs Improvement | Unacceptable |
|---|---|---|---|---|---|
| **Performance Indicator- 1 (CO/PO Mapping)** | | | | | |
| **Performance Indicator-2 (CO/PO Mapping)** | | | | | |
| **…** | | | | | |
| **Performance Indicator-n (CO/PO Mapping)** | | | | | |

**Suggested Learning Activities may include (but are not limited to):**

Students will autonomously engage in simulation-based exercises to enhance their conceptual understanding.

1. To design and simulate QPSK modulation and demodulation using simulation tool.
2. To simulate QPSK with Rayleigh fading and AWGN
3. To simulate Simulation of signal constellation M-ary QAM with AWGN fading
4. To simulate LMS algorithm
5. Generation Gold Sequence and verify its properties

Simulation of QPSK modulation and demodulation 5 Simulation of signal constellation QPSK with Rayleigh fading and AWGN 6 Simulation of signal constellation M-ary QAM with AWGN fading 7 To simulate the communication link 8 To simulate Zero Forcing algorithm 9 To simulate LMS algorithm

- Course Project
- Case Study Presentation
- Programming Assignment
- Tool/Software Exploration
- Literature Review
- Open Book Test (preferably at RBL4 and RBL5 levels)
- GATE-based Aptitude Test

- Assignment (at RBL3, RBL4, or RBL5 levels)
- Any other relevant and innovative academic activity
- Use of MOOCs and Online Platform.

**Term Work (TW) and Self Learning (SL) components in Number of Hours per semester**

Term work (includes assignments, seminars, micro projects, industrial visits, any other student activities etc.)

| Sl. No. | Term Work (TW) Activity | Number of Hours / Semester |
|---|---|---|
| 1. | Role Play | 03 |
| 2. | Case-Based Teaching | 06 |

SL: Self Learning, MOOCs, spoken tutorials, online educational resources etc.

| Sl. No. | Self-Learning (SL) Activity | Number of Hours / Semester |
|---|---|---|
| 1. | 1. To design and simulate QPSK modulation and demodulation using simulation tool<br>2. To simulate QPSK with Rayleigh fading and AWGN.<br>3. To simulate Simulation of signal constellation M-ary QAM with AWGN fading | 20 |

**Continuous Internal Evaluation (CIE)**

1. The CIE marks shall be decided based on internal tests and other outcome-based activities. The continuous internal evaluation shall be carried out by the teacher handling the course.
2. Out of 50 marks earmarked for CIE, 25 marks shall be assigned for internal tests. The first test shall be conducted after completing two modules of the syllabus and the second one after completing the remaining three modules.
3. The remaining 25 marks shall be assigned for Continuous Course Assessment (CCA), conducted as per the rubrics listed in the assessment section of the respective syllabus.
4. A student shall obtain a minimum of 40% marks or 20 out of 50 marks allotted to CIE to become eligible to appear for the SEE.

**Passing requirement in SEE**

1. For a pass in the Semester End Examination (SEE), a student shall secure a minimum of 35 marks out of 100.
2. For the declaration of a pass grade, the sum of the Continuous Internal Evaluation (CIE) marks (out of 50) marks and the SEE marks scaled down to 50 shall be greater than or equal to 40 marks.
3. If the total (CIE + SEE) is less than 40 marks, the student shall be awarded the grade ‘F’ (Fail).

| MEDICAL IMAGE PROCESSING AND AI DIAGNOSIS | | | |
|---|---|---|---|
| Course Code | **1MEC106C** | Scheme | 2026 |
| Type of Course | Professional Elective Courses - II | Semester | 1 |
| Teaching Hours/Week (L:T:P) | **3 : 0 : 0** | CIE Marks | **50** |
| Total Hours of Pedagogy per semester L /T/P/SL&TW: | 42 : 0 : 0 : 45 : 09 | SEE Marks | **50** |
| Credits | **3** | Total Marks | **100** |
| Examination type (SEE) | Theory | Exam Hours | 3 |

**Course outcome (Course Skill Set)**

*At the end of the course, the student will be able to:*

- CO1: Explain medical image-formation principles, modality characteristics, image quality, DICOM data and clinical imaging workflows.
- CO2: Apply enhancement, restoration, segmentation, feature extraction and registration techniques to medical images.
- CO3: Develop and evaluate machine-learning and radiomics pipelines for computer-aided detection and diagnosis.
- CO4: Design deep-learning models for medical image classification, detection and segmentation, with explainability and uncertainty assessment.

## Module-1

**Medical Imaging Foundations and Digital Image Representation**

**Imaging ecosystem:** Role of medical imaging in screening, diagnosis and treatment planning; anatomical, functional and molecular imaging; clinical questions and engineering workflow.

**Digital medical images:** Sampling and quantization, pixels/voxels, intensity distributions, colour and multidimensional images, image-quality measures (SNR, CNR, MSE, PSNR, SSIM); DICOM metadata, PACS, anonymization and basic visualization.

**Number of Hours: 09**

## Module-2

**Medical Image Enhancement, Segmentation and Registration**

**Pre-processing and enhancement:** Intensity normalization, windowing, histogram methods, spatial and frequency-domain filtering, denoising, sharpening, bias-field correction and artefact reduction.

**Segmentation and morphology:** Thresholding, region growing, edge-based methods, clustering, watershed, active contours/level sets, graph cuts; binary morphology, connected components and quantitative region analysis.

**Number of Hours: 09**

## Module-3

**Machine Learning, Radiomics and Computer-Aided Diagnosis**

**Feature engineering:** Shape, first-order statistics, texture features (GLCM/GLRLM), local descriptors, dimensionality reduction and feature selection; reproducibility and harmonization in radiomics.

**Learning methods:** Supervised/unsupervised learning; logistic regression, k-NN, SVM, decision trees, random forests, clustering and ensemble methods; imbalanced data and data leakage.

**Number of Hours: 08**

## Module-4

**Deep Learning for Medical Image Analysis**

**Architectures:** CNN fundamentals, transfer learning and fine-tuning; 2D/2.5D/3D CNNs; U-Net and variants; object-detection models; attention mechanisms and vision transformers.

**Training pipeline:** Annotation formats, patch/slice/volume sampling, augmentation, loss functions (cross-entropy, Dice, focal), optimization, regularization, hyperparameter tuning and experiment tracking.

**Number of Hours: 08**

## Module-5

**AI-Assisted Diagnosis, Clinical Translation and Responsible Deployment**

**Diagnostic applications:** Case studies in chest X-ray/CT, brain MRI, retinal imaging, mammography, ultrasound and digital pathology; lesion detection, organ/tumour segmentation, disease classification, triage and prognosis.

**Clinical translation:** Workflow integration and decision-support interfaces; prospective versus retrospective evaluation; bias and fairness, privacy, cybersecurity, explainability, documentation, lifecycle monitoring, regulatory and ethical considerations. AI output as decision support—not autonomous clinical judgment.

**Number of Hours: 08**

**Practice / Simulation Component**

- Read, anonymize and visualize DICOM images; apply CT windowing and inspect metadata.
- Enhance and denoise an X-ray, MRI or ultrasound image and compare PSNR/SSIM.
- Segment an anatomical structure using thresholding, morphology and active-contour methods.
- Perform rigid/affine registration and evaluate alignment using similarity measures.
- Extract radiomic features and train a classical classifier with leakage-safe validation.
- Fine-tune a pretrained CNN for medical image classification and report ROC-AUC and calibration.
- Implement U-Net-based segmentation and evaluate Dice score and IoU.
- Generate Grad-CAM explanations, analyse failure cases and prepare a model card.

Suggested tools: Python, Jupyter, NumPy, pandas, Matplotlib, OpenCV, scikit-image, scikit-learn, PyTorch/TensorFlow, MATLAB/Image Processing Toolbox

**Suggested Learning Resources (Text Books / Reference Books / Manuals)**

**Text books:**


- Rafael C. Gonzalez and Richard E. Woods, Digital Image Processing, 4th Edition, Pearson, 2022.
- Atam P. Dhawan, Medical Image Analysis, 2nd Edition, Wiley-IEEE Press, 2011.
- Le Lu, Yefeng Zheng, Gustavo Carneiro and Lin Yang (Editors), Deep Learning and Convolutional Neural Networks for Medical Image Computing, Springer, 2017.


**Reference books / manuals:**


- Gobert Lee and Hiroshi Fujita (Editors), Deep Learning in Medical Image Analysis: Challenges and Applications, Springer, 2020.

- The DICOM Standard, NEMA; MONAI documentation; 3D Slicer documentation; relevant peer-reviewed IEEE, MICCAI and medical-imaging literature.

**Web Links and Video Lectures (e-Resources)**

- https://www.dicomstandard.org/
- https://monai.io/
- https://www.slicer.org/
- https://www.cancerimagingarchive.net/
- https://physionet.org/
- https://www.kaggle.com/medmnist
- https://opencv.org/
- https://scikit-image.org/

**Teaching-Learning Process (Innovative Delivery Methods)**

*The following strategies may be adopted to facilitate achievement of the course outcomes:*

- Modality-based interactive lectures using anonymized clinical images
- Demonstrations with DICOM viewers, 3D Slicer and Python notebooks
- Case-based learning centred on diagnostic questions and model failure analysis
- Flipped classroom and guided review of medical-AI research papers
- Simulation-based learning for enhancement, segmentation, registration and AI diagnosis
- Dataset annotation, reproducible experiments and collaborative code review
- Clinician/radiologist interaction or expert webinar where feasible
- Ethics, bias, explainability and regulatory case discussions

**Continuous Comprehensive Assessments (CCA) + Internal Assessment Test (IA) = CIE [25 + 25 = 50 marks]**

A minimum of two Internal Assessment Tests shall carry a total of 25 marks. Continuous Comprehensive Assessment shall carry 25 marks. A maximum of two learning activities is recommended.

**Recommended CCA activities:**

- Medical-image processing/AI programming assignment with reproducible results and technical report.
- Clinical case study, research-paper review or mini project with diagnostic-performance and ethical-risk analysis.

**Rubrics for Learning Activity (Based on the nature of learning activity, design the rubrics for each activity):**

| | Superior | Good | Fair | Needs Improvement | Unacceptable |
|---|---|---|---|---|---|
| **Technical implementation (CO2, CO3, CO4)** | Correct, reproducible pipeline with justified choices | Mostly correct pipeline with minor gaps | Functional basic implementation | Partly functional; substantial guidance needed | Incorrect or non-functional implementation |
| **Diagnostic evaluation (CO3, CO4)** | Rigorous validation; appropriate metrics and uncertainty analysis | Appropriate validation and metrics with minor omissions | Basic metrics and acceptable interpretation | Weak validation or incomplete metric analysis | No valid evaluation or misleading claims |
| **Clinical interpretation and responsible AI (CO1, CO5)** | Insightful clinical linkage; limitations, bias and safety clearly addressed | Good clinical interpretation with most risks addressed | Adequate interpretation and basic risk awareness | Limited clinical context or risk analysis | Unsafe/unsubstantiated interpretation |
| **Communication and reproducibility (CO3, CO5)** | Clear report, traceable results, organized code and complete model card | Well-organized report/code with minor documentation gaps | Understandable report with basic reproducibility | Poor organization or incomplete documentation | Disorganized submission; results not reproducible |

**Suggested Learning Activities may include (but are not limited to):**

- DICOM exploration and anonymization exercise
- Image enhancement and quantitative quality comparison
- Segmentation and registration programming assignment
- Radiomics-based disease-classification case study
- CNN transfer-learning experiment
- U-Net segmentation mini project
- Explainability, bias and failure-case audit
- Research-paper presentation or clinical workflow mapping

| | Term Work (TW) and Self Learning (SL) components |
|---|---|
| | Term work includes assignments, seminars, mini projects, clinical case studies, tool demonstrations and other student activities. |

| | Sl. No. | Term Work (TW) Activity | Hours / Semester |
|---|---|---|---|
| | 1 | Clinical case-study presentation and diagnostic workflow analysis | 03 |
| | 2 | Medical-image processing and AI mini project with demonstration | 06 |
| | SL: Self Learning through MOOCs, tutorials, research literature, public datasets and online educational resources. | | |
| | **Sl. No.** | **Self-Learning (SL) Activity** | **Hours / Semester** |
| | 1 | • Complete guided tutorials on DICOM, MONAI or 3D Slicer.<br>• Study two peer-reviewed medical-AI papers and reproduce one experiment using a public dataset.<br>• Prepare a model card covering performance, limitations, bias, privacy and intended clinical use. | 45 |

**Continuous Internal Evaluation (CIE)**

1. The CIE marks shall be decided based on internal tests and other outcome-based activities. The continuous internal evaluation shall be carried out by the teacher handling the course.
2. Out of 50 marks earmarked for CIE, 25 marks shall be assigned for internal tests. The first test shall be conducted after completing two modules of the syllabus and the second one after completing the remaining three modules.
3. The remaining 25 marks shall be assigned for Continuous Course Assessment (CCA), conducted as per the rubrics listed in the assessment section of the respective syllabus.
4. A student shall obtain a minimum of 40% marks or 20 out of 50 marks allotted to CIE to become eligible to appear for the SEE.

**Passing requirement in SEE**

1. For a pass in the Semester End Examination (SEE), a student shall secure a minimum of 35 marks out of 100.
2. For the declaration of a pass grade, the sum of the Continuous Internal Evaluation (CIE) marks (out of 50) marks and the SEE marks scaled down to 50 shall be greater than or equal to 40 marks.
3. If the total (CIE + SEE) is less than 40 marks, the student shall be awarded the grade ‘F’ (Fail).

| SOFTWARE DEFINED VEHICLE | | | |
|---|---|---|---|
| **Course Code** | 1MEC106D | **Semester** | I |
| **Teaching Hours/Week (L:T:P:S)** | 3:0:0:0 | **CIE Marks** | 50 |
| **Total Hours of Pedagogy** | 42:0:0:45:03 | **SEE Marks** | 50 |
| **Credits** | 03 | **Total Marks** | 100 |
| **Examination type (SEE)** | Theory | **Exam Hours** | 3 Hours |

**Course Outcome (Course Skill Set)**

**At the end of the course, the student will be able to:**

1. Explain the concept of Software Defined Vehicle, E/E architecture evolution, high-compute platforms, zonal controllers and vehicle operating system requirements.
2. Analyse service-oriented communication and in-vehicle networking protocols such as Automotive Ethernet, SOME/IP, DDS, Protobuf and vehicle APIs.
3. Interpret AUTOSAR Classic and Adaptive Platform architecture and apply Adaptive AUTOSAR middleware concepts for SDV software realization.
4. Evaluate virtualization, hypervisors, containers, cloud-native development, OTA update mechanisms and CI/CD workflows for automotive systems.
5. Assess functional safety, cybersecurity, validation, diagnostics and lifecycle management issues in SDV-based automotive platforms.

**MODULE 1**

**Introduction to Software Defined Vehicles and E/E Architecture Evolution:** Software Defined Vehicle fundamentals; need for SDV; vehicle software evolution; smartphone-on-wheels concept; digital-first vehicle lifecycle; cross-domain applications and data fusion; E/E architecture evolution; distributed ECU architecture; high-compute platforms; traditional software architecture vs SDV software architecture.

**Number of Hrs: 8**

**MODULE 2**

**Service-Oriented Communication and Automotive Networking for SDV:** In-vehicle networking evolution; CAN, LIN, MOST, FlexRay and Automotive Ethernet; Automotive Ethernet channels and PHY overview; IP, VLAN, switching/routing; QoS, AVB and TSN; middleware and SOME/IP; Service Discovery; Vehicle APIs; DDS and Protocol Buffers.

**Number of Hrs: 8**

**MODULE 3**

**AUTOSAR Platforms and SDV Middleware:** AUTOSAR overview and evolution; AUTOSAR Classic Platform; AUTOSAR Adaptive Platform; Classic reference architecture; Adaptive reference architecture; AUTOSAR methodology and meta-model; ECU middleware; Communication Management; Execution Management; Update and Configuration Management; Linux/QEMU-based platform realization concepts.

**Number of Hrs: 10**

**MODULE 4**

**Virtualization, OTA, Containers and Cloud-Native SDV Development:** Virtualization in on-board automotive systems; hypervisor concept and types; mixed-criticality consolidation; containerization; on-board vs off board deployment; cloud-native development; open-source development; OTA updates; vehicle app store; value stream management; shift-left and shift-north engineering; CI/CD and software factory concepts.

**Number of Hrs: 10**

**MODULE 5**

**Safety, Cybersecurity, Validation and Lifecycle Management of SDV:** Functional safety and ISO 26262 lifecycle; ASIL concept; safety in Vehicle SOA; cybersecurity engineering and ISO/SAE 21434; threat and risk analysis; network security; validation and testing; SIL/MIL/HIL; architecture evaluation; metrics; diagnostics; lifecycle management and post-deployment monitoring.

**Number of Hrs: 08**

**Suggested Learning Resources: (Text Book/ Reference Book/ Manuals):**

**Text Books:**

1. Dirk Slama, Achim Nonnenmacher and Thomas Irawan, The Software-Defined Vehicle, O'Reilly Media, 2023, ISBN: 978-1098157814.

2. Miroslaw Staron, Automotive Software Architectures: An Introduction, 2nd Edition, Springer Cham, 2021, ISBN: 978-3-030-65939-4.
3. Kirsten Matheus and Thomas Königseder, Automotive Ethernet, 3rd Edition, Cambridge University Press, 2021, ISBN: 978-1108841955.

**Reference Books:**

1. AUTOSAR, SOME/IP Protocol Specification, AUTOSAR Foundation Standard, latest available release.
2. AUTOSAR, Adaptive Platform Specifications: Communication Management, Execution Management, Update and Configuration Management, State Management and Persistency, latest available release.
3. ISO 26262, Road vehicles - Functional safety, International Organization for Standardization, latest edition.
4. ISO/SAE 21434:2021, Road vehicles - Cybersecurity engineering.
5. Thomas D. Nadeau and Ken Gray, Software Defined Networking, O'Reilly Media, 2013.
6. James Larminie and John Lowry, Electric Vehicle Technology Explained, 2nd Edition, Wiley, 2012.

**Web links and Video Lectures (e-Resources):**

1. Official AUTOSAR documentation portal: https://www.autosar.org/standards
2. Eclipse Software Defined Vehicle resources: https://sdv.eclipse.org/
3. NPTEL / SWAYAM courses related to Automotive Electronics, Embedded Systems, IoT, Cloud Computing and Cybersecurity may be used as supplementary resources.
4. digital.auto / SDV guide resources for practical SDV architecture discussion: https://www.digital.auto/

**Course Objectives:**

- Understand the fundamentals of Software Defined Vehicle (SDV), vehicle software evolution, and the transition from hardware-centric to software-centric automotive platforms.
- Analyse the evolution of automotive E/E architectures from distributed ECUs to domain, centralized and zonal architectures using high-compute platforms.
- Apply the principles of service-oriented architecture and communication protocols such as Automotive Ethernet, SOME/IP, DDS and Protobuf for SDV applications.
- Understand AUTOSAR Classic and Adaptive Platforms, Adaptive AUTOSAR middleware, communication management, life cycle management and update/configuration management.
- Evaluate virtualization, hypervisors, containers, cloud-native development, OTA updates and CI/CD pipelines in SDV software realization.
- Discuss functional safety, cybersecurity, validation, diagnostics and lifecycle management requirements for SDV-based automotive systems.

**Teaching-Learning Process (General Instructions):**

These are sample strategies; which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecture method may be supplemented with case studies from automotive OEMs, Tier-1 suppliers and open SDV initiatives.
2. Demonstrate architecture diagrams of distributed, domain, centralized and zonal vehicle architectures using classroom discussion.
3. Show videos/animations on Automotive Ethernet, SOA, SOME/IP, Adaptive AUTOSAR, OTA updates and virtualization in automotive systems.
4. Use simulation-based learning with Linux, QEMU, Docker/container examples or open-source middleware demonstrations wherever feasible.
5. Encourage group learning through mini case studies on vehicle feature migration from ECU-based design to service-oriented SDV design.
6. Ask HOTS questions on safety-security trade-offs, mixed-criticality consolidation, cloud connectivity and lifecycle software updates.
7. Assign students to prepare a service catalogue, architecture sketch, software deployment model and validation plan for one SDV use case.
8. Conduct seminars on standards and ecosystems such as AUTOSAR, ISO 26262, ISO/SAE 21434, Eclipse SDV.

**Assessment Structure:**

The assessment in each course is divided equally between Continuous Internal Evaluation (CIE) and the Semester End Examination (SEE), with each carrying 50% weightage.

- To qualify and become eligible to appear for SEE, in the CIE, a student must score at least 40% of 50 marks, i.e., 20 marks.
- To pass the SEE, a student must score at least 35% of 50 marks, i.e., 18 marks.

- Notwithstanding the above, a student is considered to have passed the course, provided the combined total of CIE and SEE is at least 40 out of 100 marks.

**Continuous Comprehensive Assessments (CCA)+ Internal Assessment Test (IA) = Continuous Internal Evaluation CIE [25+25=50 marks]**

- A minimum of two Internal Assessment Tests(IA) shall be conducted, carrying a total of 25 marks.
- In addition, Continuous Comprehensive Assessment (CCA) shall be conducted for a total of 25 marks.
- It is recommended to include a maximum of two learning activities as part of the CCA to foster the holistic development of students. These activities shall be:

| Sl. No. | Name of the Learning Activity | Maximum Marks |
|---|---|---|
| 1. | **Activity 1: SDV Case Study Presentation and Literature Review**<br>Select one SDV use case such as smart HVAC, vehicle health monitoring, battery health monitoring, OTA update, predictive maintenance, infotainment personalization or fleet telematics. Compare legacy ECU-based design with SDV-based design, include E/E architecture, service-oriented view, protocols/standards, safety and cybersecurity points. Deliverables: 8-12 slide PPT, 2-3 page technical note and viva. | **10** |
| 2. | **Activity 2: SDV Mini Design / Tool Exploration Project**<br>Design and demonstrate a small SDV concept in a team of 2-3. Include architecture sketch, service catalogue, interface definition, protocol choice such as SOME/IP, DDS, MQTT or REST, Adaptive AUTOSAR-style service mapping, Linux/QEMU/Docker/container illustration, OTA workflow and validation plan. Deliverables: design document, tool screenshots/demo and viva. | **15** |

**Rubrics for Learning Activity (Based on the nature of learning activity, design the rubrics for each activity):**
**Rubrics for Learning Activity 1: SDV Case Study Presentation and Literature Review (10 Marks):**

| Performance Indicator (CO/PO Mapping) | Superior (2M) | Good (1.5M) | Fair (1M) | Needs Improvement(0.5M) | Unacceptable (0M) |
|---|---|---|---|---|---|
| PI-1: SDV problem understanding and relevance CO1, CO2 / PO1, PO2 Max: 2 marks | Clearly defines the use case, need for SDV and vehicle-level relevance with strong technical clarity. | Defines the use case and SDV relevance with minor gaps. | Basic use case description; SDV relevance is partially explained. | Weak problem statement; limited SDV linkage. | No clear problem definition or SDV relevance. |
| PI-2: Architecture analysis CO1, CO2 / PO2, PO3 Max: 2 marks | Accurately compares legacy, domain, centralized and zonal architecture with clear diagrams. | Good architecture comparison with adequate diagrams. | Basic comparison, but diagram/detail is limited. | Architecture explanation is incomplete or incorrect in parts. | No valid architecture analysis. |
| PI-3: Protocols, middleware and standards usage CO2, CO3 / PO3, PO5 Max: 2 marks | Correctly uses relevant protocols/standards such as Ethernet, SOME/IP, DDS, AUTOSAR and OTA concepts. | Uses relevant protocols/standards with minor inaccuracies. | Mentions protocols but lacks technical depth. | Very limited standards/protocol discussion. | No relevant protocol/standard reference. |
| PI-4: Critical analysis of safety, cybersecurity and lifecycle issues CO4, CO5 / PO3, PO6 Max: 2 marks | Excellent analysis of safety, cybersecurity, update, validation and lifecycle implications. | Good analysis with most key issues included. | Basic analysis of a few issues. | Superficial or generic discussion. | No critical analysis. |
| PI-5: Presentation, documentation and viva CO2, CO5 / PO5, PO6 Max: 2 marks | Professional slides, correct citations, confident viva and clear technical communication. | Good presentation and satisfactory viva. | Average presentation; answers basic questions only. | Poor presentation quality or weak viva. | No proper submission/presentation. |

**Rubrics for Learning Activity 2: SDV Mini Design / Tool Exploration Project (15 Marks):**

| Performance Indicator (CO/PO Mapping) | Superior(3M) | Good (2M) | Fair (1.5M) | Needs Improvement (1M) | Unacceptable (0M) |
|---|---|---|---|---|---|
| PI-1: Use-case definition and service catalogue CO1, CO2 / PO2, PO3 Max: 3 marks | Excellent use-case scope, actors, signals/data, service list, inputs/outputs and expected SDV value. | Good definition with most service elements included. | Basic definition; service catalogue partially complete | Weak definition; unclear service view. | No meaningful use-case/service catalogue. |
| PI-2: Architecture and middleware/protocol design CO2, CO3 / PO3, PO5 Max: 3 marks | Correct architecture diagram, middleware mapping and suitable protocol selection with justification. | Good architecture and protocol choice with minor gaps. | Basic architecture; protocol choice not fully justified. | Incomplete architecture or incorrect mapping. | No valid architecture/protocol design |

| | | | | | |
|---|---|---|---|---|---|
| PI-3: Tool/software exploration or demonstration CO3, CO4 / PO4, PO5 Max: 3 marks | Working demonstration/simulation or strong tool exploration using Linux, Docker, QEMU, pub-sub, API or equivalent. | Good tool exploration with screenshots and partial demo. | Limited demo; mostly conceptual screenshots. | Very weak or unclear tool work. | No tool/software exploration |
| PI-4: Safety, cybersecurity, validation and OTA workflow CO4, CO5 / PO3, PO6 Max: 3 marks | Comprehensive validation plan with safety hazards, cybersecurity risks, update workflow and test strategy. | Good plan covering most issues. | Basic plan, missing some important issues. | Superficial plan with limited technical relevance. | No safety/security/validation consideration. |
| PI-5: Report, documentation, teamwork and viva CO4, CO5 / PO5, PO6 Max: 3 marks | Well-structured report with diagrams, references, traceability, individual contribution and confident viva. | Good report and satisfactory viva. | Average report; limited technical explanation | Poor documentation or weak viva. | No acceptable report/viva |

**Suggested Learning Activities may include (but are not limited to):**

| Learning Activity Type | SDV-specific activity content for M.Tech students |
|---|---|
| **Course Project** | Design a small SDV feature using service-oriented architecture, prepare service catalogue, interface map, deployment view and validation plan. |
| **Case Study Presentation** | Compare SDV strategies of OEM/Tier-1/open-source ecosystem such as centralized compute, zonal architecture, vehicle OS, OTA and data-driven services. |
| **Programming / Tool Assignment** | Demonstrate a simple publisher-subscriber/service communication using SOME/IP concept, DDS/MQTT/REST API, Docker container, Linux/QEMU or equivalent open-source tools. |
| **Tool/Software Exploration** | Explore Adaptive AUTOSAR concepts, Eclipse SDV resources, digital.auto playground, Docker containers, QEMU, Wireshark traces or automotive Ethernet examples. |
| **Literature Review** | Review recent SDV, AUTOSAR Adaptive, automotive Ethernet, OTA, cybersecurity or vehicle cloud papers/whitepapers and summarize the technical findings. |
| **Open Book Test** | Conduct RBL4/RBL5 open-book questions on architecture trade-offs, service decomposition, safety-security conflicts and virtualization choices. |
| **Assignment** | Prepare E/E architecture diagram, SOME/IP message flow, AUTOSAR service mapping, OTA update workflow and ISO 26262/ISO 21434 analysis for a selected feature. |
| **MOOCs and Online Platforms** | Use NPTEL/SWAYAM/industry webinars on automotive electronics, embedded systems, cloud computing, cybersecurity and SDV-related online resources. |

**Suggested Innovative Delivery Methods may include (but are not limited to):**

| Method | Implementation in Software Defined Vehicle course |
|---|---|
| **Flipped Classroom** | Students read assigned textbook sections on SDV, AUTOSAR Adaptive, Ethernet/SOME-IP and virtualization before class; class time is used for problem discussion and architecture drawing. |
| **Problem-Based Learning (PBL)** | A vehicle feature such as smart HVAC or diagnostics is given as a problem; students identify services, data flows, middleware, safety and cybersecurity needs. |
| **Case-Based Teaching** | Use real SDV industry cases such as zonal architecture, vehicle OS, OTA update failure, cybersecurity incident or feature-on-demand model. |
| **Simulation and Virtual Labs** | Use Linux, Docker, QEMU, Wireshark, DDS/MQTT tools, digital.auto or equivalent software platforms for demonstration. |
| **Industry Expert / Industrial Visit** | Invite automotive embedded systems/SDV/AUTOSAR/EV software industry experts for one technical session or arrange virtual industry interaction. |

| | |
|---|---|
| **ICT-Enabled Teaching** | Use architecture animations, protocol flow diagrams, online SDV resources, GitHub repositories and recorded demonstrations. |
| **Role Play** | Students act as OEM architect, Tier-1 supplier, cloud engineer, cybersecurity engineer and safety engineer to debate SDV design decisions. |

**Term Work (TW) and Self Learning (SL) Components in Number of Hours per Semester:**

| Sl. No. | Term Work (TW) Activity | Number of Hours / Semester |
|---|---|---|
| **1.** | Analytical assignment on SDV fundamentals and E/E architecture evolution: distributed ECU, domain centralized, centralized and zonal architecture comparison for a selected vehicle feature. | **4** |
| **2.** | Protocol and middleware assignment: prepare message/service flow for Automotive Ethernet, SOME/IP/DDS/Protobuf and relate it to service-oriented vehicle functions. | **4** |
| **3.** | AUTOSAR reading and mapping exercise: Classic vs Adaptive AUTOSAR, ara::com communication, execution/lifecycle management and update/configuration management. | **4** |
| **4.** | Mini project design work: service catalogue, interface specification, deployment view, OTA update workflow, validation checklist and safety/security impact analysis. | **6** |
| **5.** | Seminar / industrial case study discussion on SDV platform, vehicle OS, virtualization, containers, cloud-native development or connected vehicle services. | **2** |
| **Total** | **Total suggested Term Work hours** | **20** |
| **Sl. No.** | **Self-Learning (SL) Activity** | **Number of Hours / Semester** |
| **1.** | Textbook reading notes from selected chapters of The Software-Defined Vehicle, Automotive Software Architectures and Automotive Ethernet. | **5** |
| **2.** | Self-study using AUTOSAR official documentation, Eclipse SDV resources, digital.auto resources and NPTEL/SWAYAM videos related to automotive electronics, embedded systems and cloud/cybersecurity. | **5** |
| **3.** | Hands-on exploration of open-source or freely available tools: Linux basics, Docker/container demo, QEMU overview, Wireshark trace observation, DDS/MQTT/publisher-subscriber sample or digital.auto API exploration. | **5** |
| **4.** | Reading and review of one recent research paper/industry whitepaper on SDV, Adaptive AUTOSAR, vehicle OS, OTA update, cybersecurity, virtualization or automotive Ethernet. | **3** |
| **5.** | Preparation of SDV concept map, short question bank and final revision notes linking modules, COs and applications. | **2** |
| **Total** | **Total suggested Self-Learning hours** | **20** |

**CCA Activity - Module and Course Outcome Mapping:**

| CCA Activity | Modules Covered | Major Learning Evidence | Mapped COs | Marks |
|---|---|---|---|---|
| **Activity 1: Case Study Presentation and Literature Review** | Module 1: SDV fundamentals; Module 2: SOA/communication; Module 5: safety, cybersecurity and lifecycle | Presentation, technical note, architecture comparison, literature/standards references and viva | CO1, CO2, CO5 | 10 |
| **Activity 2: Mini Design / Tool Exploration Project** | Module 2: protocols; Module 3: AUTOSAR/middleware; Module 4: virtualization/containers/cloud; Module 5: validation and OTA | Design document, service catalogue, interface flow, tool demo/screenshots, validation plan and viva | CO2, CO3, CO4, CO5 | 15 |

| Python for Electronic System Design | | | |
|---|---|---|---|
| Course Code | **1MECL107A** | Scheme | 2026 |
| Type of course | **Professional Core Course Lab- I** | Semester | I |
| Teaching Hours/Week (L:T:P) | 0:0:1 | CIE Marks | 50 |
| Total Hours of Pedagogy L:T:P:SL:TW | 0:0:0:28:0 | SEE Marks | 50 |
| Credits | **01** | Total Marks | 100 |
| Type of Examination (PCCL): | Theory- CIE +SEE, and Lab- CIE only. | Exam Hours | 03 |

**List of Experiments**

1. Develop Python programs for matrix operations, numerical computation, and scientific visualization using NumPy and Matplotlib.
2. Implement signal generation, convolution, correlation, and Fourier Transform using SciPy.
3. Develop Python applications for digital filter design and frequency response analysis.
4. Interface sensors with Raspberry Pi/ESP32 and acquire real-time data using Python.
5. Design a GUI-based electronic instrument using Tkinter or PyQt for measurement and visualization.
6. Develop serial communication applications between Python and embedded hardware (UART, I²C, SPI).
7. Implement image acquisition and basic computer vision techniques using OpenCV for electronic inspection.
8. Perform electronic measurement data acquisition and analysis using Python and NI-VISA/PyVISA.
9. Develop machine learning models for electronic system fault classification using Scikit-Learn.
10. Design and implement a mini project integrating Python with embedded hardware for intelligent electronic system development.

| Electronics & Communication | | | |
|---|---|---|---|
| Course Code | **1MECL107B** | Scheme | 2026 |
| Type of course | **Professional Core Course Lab- I** | Semester | I |
| Teaching Hours/Week (L:T:P) | 0:0:1 | CIE Marks | 50 |
| Total Hours of Pedagogy L:T:P:SL:TW | 0:0:0:28:0 | SEE Marks | 50 |
| Credits | **01** | Total Marks | 100 |
| Type of Examination (PCCL): | Theory- CIE +SEE, and Lab- CIE only. | Exam Hours | 03 |

**List of Experiments**

1. Design and characterize analog amplifier circuits using simulation and hardware implementation.
2. Analyze frequency response and stability of active filter circuits.
3. Design RF communication circuits and evaluate performance using simulation tools.
4. Implement digital communication techniques including ASK, FSK, PSK, and QAM modulation.
5. Perform error control coding and decoding using MATLAB/Python.
6. Design and analyze antenna radiation characteristics using simulation software.
7. Implement software-defined radio (SDR) communication using GNU Radio.
8. Evaluate wireless communication performance under noisy and fading channels.
9. Interface communication modules (BLE, LoRa, Wi-Fi, ZigBee) for wireless data transmission.
10. Design and demonstrate an integrated communication system as a mini project.

| Digital IC Design | | | |
|---|---|---|---|
| Course Code | **1MECL107C** | Scheme | 2026 |
| Type of course | **Professional Core Course Lab- I** | Semester | I |
| Teaching Hours/Week (L:T:P) | 0:0:1 | CIE Marks | 50 |
| Total Hours of Pedagogy L:T:P:SL:TW | 0:0:0:28:0 | SEE Marks | 50 |
| Credits | **01** | Total Marks | 100 |
| Type of Examination (PCCL): | Theory- CIE +SEE, and Lab- CIE only. | Exam Hours | 03 |

**List of Experiments**

1. Design CMOS inverter, NAND and NOR gates using Cadence Virtuoso or an open-source EDA tool. Analyse DC transfer characteristics, noise margins, propagation delay, power dissipation and process-voltage-temperature variations.
2. Design and simulate complex static CMOS, transmission-gate and pass-transistor logic circuits. Compare transistor count, delay, power and signal integrity.
3. Model multiplexers, encoders, decoders, comparators and code converters using structural, dataflow and behavioural Verilog/SystemVerilog. Develop self-checking testbenches for functional verification.
4. Design registers, shift registers, synchronous/asynchronous counters and Moore/Mealy finite-state machines. Verify reset behaviour, state transitions and illegal-state recovery.
5. Implement ripple-carry, carry-look-ahead and carry-select adders. Compare area, delay and power through synthesis and timing reports.
6. Develop array, Booth and Wallace-tree multipliers and a configurable ALU. Evaluate architectural trade-offs in latency, throughput, area and power.
7. Develop reusable parameterized RTL modules and pipeline a computation-intensive datapath. Verify functional equivalence and quantify the improvement in maximum operating frequency.
8. Synthesize a Verilog/SystemVerilog design using Xilinx Vivado, Intel Quartus, Yosys or a commercial synthesis tool. Define clocks and I/O constraints and analyse resource utilization, timing and inferred hardware.
9. Perform setup and hold analysis, identify critical paths and evaluate clock uncertainty, input/output delays and timing exceptions. Apply pipelining, logic restructuring and constraint refinement to achieve timing closure.
10. Implement an RTL design on an FPGA, including synthesis, placement, routing and bitstream generation. Validate the hardware using switches, LEDs, UART or on-chip logic analysers such as ILA/SignalTap.

| Advanced Signal Processing | | | |
|---|---|---|---|
| Course Code | **1MECL107D** | Scheme | 2026 |
| Type of course | **Professional Core Course Lab- I** | Semester | I |
| Teaching Hours/Week (L:T:P) | 0:0:1 | CIE Marks | 50 |
| Total Hours of Pedagogy L:T:P:SL:TW | 0:0:0:28:0 | SEE Marks | 50 |
| Credits | **01** | Total Marks | 100 |
| Type of Examination (PCCL): | Theory- CIE +SEE, and Lab- CIE only. | Exam Hours | 03 |

**List of Experiments**

1. Generate and analyze discrete-time signals using MATLAB/Python.
2. Design FIR filters using windowing and optimization techniques.
3. Design IIR filters using Butterworth, Chebyshev, and Elliptic approximations.
4. Implement adaptive filtering using LMS and RLS algorithms.
5. Perform spectral estimation using FFT, periodogram, and Welch methods.
6. Implement wavelet transform for signal denoising and feature extraction.
7. Develop speech processing algorithms for enhancement and recognition.
8. Perform image enhancement and restoration using digital signal processing techniques.
9. Implement real-time DSP applications using MATLAB/Python and DSP hardware.
10. Design and evaluate a signal processing application for biomedical, communication, or radar systems as a mini project.