**SCHEME OF TEACHING AND EXAMINATION**
**M.Tech in DIGITAL ELECTRONICS / ELECTRONICS**

**(Common to M.Tech in Digital Electronics and M.Tech in Electronics)**

**I SEMESTER**

| Sl. No | Subject Code | Title | Teaching Hours /Week | | Examination | | | | Credit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Theory | Practical/Field Work/ Assignment | Duration | I.A. Marks | Theory/ Practical Marks | Total Marks | |
| 1 | 16ELD11 | Advanced Engineering Mathematics | 4 | - | 3 | 20 | 80 | 100 | 4 |
| 2 | 16EVE12 | Digital VLSI Design | 4 | - | 3 | 20 | 80 | 100 | 4 |
| 3 | 16EVE13 | Advanced Embedded System | 4 | - | 3 | 20 | 80 | 100 | 4 |
| 4 | 16ELD14 | Digital Circuit and Logic Design | 4 | - | 3 | 20 | 80 | 100 | 4 |
| 5 | 16EXX15X | Elective-1 | 3 | - | 3 | 20 | 80 | 100 | 3 |
| 6 | 16ELDL16 | Digital Electronics Lab -1 | | 3 | 3 | 20 | 80 | 100 | 2 |
| 7 | 16ELD17 | Seminar on advanced topics from refereed journals | - | 3 | - | 100 | - | 100 | 1 |
| **TOTAL** | | | **19** | **6** | **18** | **220** | **480** | **700** | **22** |
| | | | | | | | | | |

| **Elective-1** | |
|---|---|
| 16EVE151 | Digital System Design using Verilog |
| 16EVE152 | Nanoelectronics |
| 16EVE153 | ASIC Design |
| 16ELD154 | Advanced Computer Architecture |

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**II SEMESTER**

| Sl. No | Subject Code | Title | Teaching Hours /Week | | Examination | | | | Credit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Theory | Practical/Field Work/ Assignment | Duration | I.A. Marks | Theory/ Practical Marks | Total Marks | |
| 1 | 16ECS21 | Advanced DSP | 4 | - | 3 | 20 | 80 | 100 | 4 |
| 2 | 16ECS22 | Error Control Coding | 4 | - | 3 | 20 | 80 | 100 | 4 |
| 3 | 16EVE23 | Advances in VLSI Design | 4 | - | 3 | 20 | 80 | 100 | 4 |
| 4 | 16EVE24 | Real Time Operating System | 4 | - | 3 | 20 | 80 | 100 | 4 |
| 5 | 16EXX25X | Elective –2 | 3 | - | 3 | 20 | 80 | 100 | 3 |
| 6 | 16ELDL26 | Digital Electronics Lab - 2 | | 3 | 3 | 20 | 80 | 100 | 2 |
| 7 | 16ELD27 | Seminar on Advanced topics from refereed journals | - | 3 | - | 100 | - | 100 | 1 |
| **TOTAL** | | | **19** | **6** | **18** | **220** | **480** | **700** | **22** |

| **Elective-2** | |
|---|---|
| 16ELD251 | Automotive Electronics |
| 16ECS252 | Multimedia Over Communication Links |
| 16ELD253 | Micro Electro Mechanical Systems |
| 16ECS254 | Cryptography and Network Security |

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**III SEMESTER: Internship**

| Sl. No | Subject Code | Title | Teaching Hours /Week | | Examination | | | | Credit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Theory | Practical/Field Work/ Assignment | Duration | I.A. Marks | Theory/ Practical Marks | Total Marks | |
| 1 | 16ELD31 | Seminar / Presentation on Internship (After 8 weeks from the date of commencement) | - | - | - | 25 | - | 25 | 20 |
| 2 | 16ELD32 | Report on Internship | - | - | - | 25 | - | 50 | |
| 3 | 16ELD33 | Evaluation and Viva-Voce of Internship | - | - | - | - | 50 | 50 | |
| 4 | 16ELD34 | Evaluation of Project phase -1 | - | - | - | 50 | - | 25 | 1 |
| **TOTAL** | | | **-** | **-** | **-** | **100** | **50** | **150** | **21** |

**M.Tech in DIGITAL ELECTRONICS / ELECTRONICS**

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**IV SEMESTER**

| Sl. No | Subject Code | Title | Teaching Hours /Week | | Examination | | | | Credit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Theory | Practical/Field Work/ Assignment | Duration | I.A. Marks | Theory/ Practical Marks | Total Marks | |
| 1 | 16ELD41 | Synthesis and optimization of Digital Circuits | 4 | - | 3 | 20 | 80 | 100 | 4 |
| 2 | 16EXX42X | Elective-3 | 3 | - | 3 | 20 | 80 | 100 | 3 |
| 3 | 16ELD43 | Evaluation of Project phase -2 | - | - | - | 50 | - | 50 | 3 |
| 4 | 16ELD44 | Evaluation of Project and Viva-Voce | - | - | - | - | 100+100 | 200 | 10 |
| **TOTAL** | | | **-** | **-** | **6** | **90** | **360** | **450** | **20** |

| **Elective-3** | |
|---|---|
| 16EVE421 | CMOS RF Circuit Design |
| 16ECS422 | Advances in Image Processing |
| 16ECS423 | Communication System Design using DSP Algorithms |
| 16ELD424 | Reconfigurable Computing |

**Note:**

**1. Project Phase-1:** 6-week duration shall be carried out between 2nd and 3rd Semester vacation. Candidates in consultation with the guide shall carry out literature survey/ visit industries to finalize the topic of Project.

**2. Project Phase-2:** 16-week duration during 4th semester**.** Evaluation shall be done by the committee constituted comprising of HoD as Chairman, Guide and Senior faculty of the department.

**3**. **Project Evaluation**: Evaluation shall be taken up at the end of 4th semester. Project work evaluation and Viva-Voce examination shall be conducted .

a. Internal Examiner shall carry out the evaluation for 100 marks.

b. External Examiner shall carry out the evaluation for 100 marks.

c .The average of marks allotted by the internal and external examiner shall be the final marks of the project evaluation.

d. Viva-Voce examination of Project work shall be conducted jointly by Internal and External examiner for 100 marks.

# M.Tech – DE & E - FIRST SEMESTER SYLLABUS

| **ADVANCED ENGINEERING MATHEMATICS**<br>[As per Choice Based Credit System (CBCS) scheme]<br>SEMESTER – I | | | |
|---|---|---|---|
| Subject Code | 16ELD11 | IA Marks | 20 |
| Number of Lecture Hours/Week | 04 | Exam Marks | 80 |
| Total Number of Lecture Hours | 50 (10 Hours per Module) | Exam Hours | 03 |
| CREDITS – 04 | | | |

**Course objectives**: This course will enable students to:

- Acquaint with principles of linear algebra, calculus of variations, probability theory and random process.
- Apply the knowledge of linear algebra, calculus of variations, probability theory and random process in the applications of electronics and communication engineering sciences.

| **Modules** | **Revised Bloom's Taxonomy (RBT) Level** |
|---|---|
| **Module -1** | |
| **Linear Algebra-I**<br>Introduction to vector spaces and sub-spaces, definitions, illustrative examples and simple problems. Linearly independent and dependent vectors-definition and problems. Basis vectors, dimension of a vector space. Linear transformations- definition, properties and problems. Rank-Nullity theorem(without proof). Matrix form of linear transformations-Illustrative examples.**(Text 1 & Ref. 1)** | **L1,L2** |
| **Module -2** | |
| **Linear Algebra-II**<br>Computation of Eigen values and Eigen vectors of real symmetric matrices-Given's method. Orthogonal vectors and orthogonal bases. Gram-Schmidt orthogonalization process. QR decomposition, singular value decomposition, least square approximations.**(Text 1 & Ref. 1)** | **L1,L2** |
| **Module -3** | |
| **Calculus of Variations**<br>Concept of functional-Eulers equation. functional dependent on first and higher order derivatives, functional on several dependent variables. Isoperimetric problems-variation problems with moving boundaries.**(Text 2 & Ref. 2)** | **L1,L2** |
| **Module -4** | |

| | |
|---|---|
| **Probability Theory**<br>Review of basic probability theory. Definitions of random variables and probability distributions, probability mass and density functions, expectation, moments, central moments, characteristic functions, probability generating and moment generating functions-illustrations. Binomial, Poisson, Exponential, Gaussian and Rayleigh distributions-examples.**(Text 3 & Ref. 3)** | **L1,L2** |
| **Module -5** | |
| **Joint probability distributions**<br>Definition and properties of CDF, PDF, PMF, conditional distributions. Expectation, covariance and correlation. Independent random variables. Statement of central limit theorem-Illustrative examples.<br>Random process- Classification, stationary and ergodic random process. Auto correlation function-properties, Gaussian random process.**(Text 3 & Ref. 3)** | **L1,L2** |

**Course Outcomes:** After studying this course, students will be able to:

- Understand vector spaces, basis, linear transformations and the process of obtaining matrix of linear transformations arising in magnification and rotation of images.
- Apply the techniques of QR and singular value decomposition for data compression, least square approximation in solving inconsistent linear systems.
- Utilize the concepts of functionals and their variations in the applications of communication systems, decision theory, synthesis and optimization of digital circuits.
- Learn the idea of random variables (discrete/continuous) and probability distributions in analyzing the probability models arising in control systems and system communications.
- Apply the idea of joint probability distributions and the role of parameter-dependent random variables in random process.

**Question paper pattern:**

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

**Text Books**:


1. David C.Lay, Steven R.Lay and J.J.McDonald: Linear Algebra and its Applications, 5th Edition, Pearson Education Ltd., 2015.
2. E. Kreyszig, "Advanced Engineering Mathematics", 10th edition, Wiley, 2015.
3. Scott L.Miller, Donald G. Childers: "Probability and Random Process with application to Signal Processing", Elsevier Academic Press, 2nd Edition,2013.


**Reference books:**


1. Richard Bronson: "Schaum's Outlines of Theory and Problems of Matrix Operations", McGraw-Hill, 1988.
2. Elsgolts, L.:"Differential Equations and Calculus of Variations", MIR Publications, 3rd Edition, 1977.
3. T.Veerarajan: "Probability, Statistics and Random Process",3rd Edition, Tata McGraw Hill Co.,2008.


**Web links:**

1. http://nptel.ac.in/courses.php?disciplineId=111
2. http://www.class-central.com/subject/math(MOOCs)
3. http://ocw.mit.edu/courses/mathematics/
4. www.wolfram.com

**DIGITAL VLSI DESIGN**

[As per Choice Based Credit System (CBCS) scheme]

| | | | |
|---|---|---|---|
| Subject Code | 16EVE12 | IA Marks | 20 |
| Number | 04 | Exam Marks | 80 |
| Total Number of | 50 (10 Hours per Module) | Exam Hours | 03 |

CREDITS – 04

**Course objectives:** This course will enable students to:

- Explain VLSI Design Methodologies
- Learn Static and Dynamic operation principles, analysis and design of inverter circuit.
- Infer state of the art Semiconductors Memory circuits.
- Outline the comprehensive coverage of Methodologies and Design practice that are used to reduce the Power Dissipation of large scale digital circuits.
- Illustrate VLSI and ASIC design.

| **Modules** | **Revised Bloom's Taxonomy (RBT) Level** |
|---|---|
| **Module -1** | |
| **MOS Transistor**: The Metal Oxide Semiconductor (MOS) Structure, The MOS System under External Bias, Structure and Operation of MOS Transistor, MOSFET Current-Voltage Characteristics, MOSFET Scaling and Small-Geometry Effects.<br>**MOS Inverters-Static Characteristics**: Introduction, Resistive-Load Inverter, Inverters with n_Type MOSFET Load. | **L1, L2** |
| **Module -2** | |
| **MOS Inverters-Static Characteristics**: CMOS Inverter.<br><br>**MOS Inverters**: Switching Characteristics and Interconnect Effects: Introduction, Delay-Time Definition, Calculation of Delay Times, Inverter Design with Delay Constraints, Estimation of Interconnect Parasitics, Calculation of Interconnect Delay, Switching Power Dissipation of CMOS Inverters. | **L2, L3** |
| **Module -3** | |

| | |
|---|---|
| **Semiconductor Memories:** Introduction, Dynamic Random Access Memory (DRAM), Static Random Access Memory (SRAM), Nonvolatile Memory, Flash Memory, Ferroelectric Random Access Memory (FRAM). | **L1, L2, L3** |
| **Module -4** | |
| **Dynamic Logic Circuits**: Introduction, Basic Principles of Pass Transistor Circuits, Voltage Bootstrapping, Synchronous Dynamic Circuit Techniques, Dynamic CMOS Circuit Techniques, High Performance Dynamic CMOS Circuits.<br>**BiCMOS Logic Circuits**: Introduction, Bipolar Junction Transistor (BJT): Structure and Operation, Dynamic Behavior of BJTs, Basic BiCMOS Circuits: Static Behavior, Switching Delay in BiCMOS Logic Circuits, BiCMOS Applications. | **L1,L2, L3** |
| **Module -5** | |
| **Chip Input and Output (I/O) Circuits**: Introduction, ESD Protection, Input Circuits, Output Circuits and L(di/dt) Noise, On-Chip Clock Generation and Distribution, Latch-Up and Its Prevention.<br>**Design for Manufacturability**: Introduction, Process Variations, Basic Concepts and Definitions, Design of Experiments and Performance Modeling. | **L2, L3** |

**Course outcomes:**

After studying this course, students will be able to:

1. Analyse issues of On-chip interconnect Modelling and Interconnect delay calculation.
2. Analyse the Switching Characteristics in Digital Integrated Circuits.
3. Use the Dynamic Logic circuits in state-of-the-art VLSI chips.
4. Study critical issues such as ESD protection, Clock distribution, Clock buffering, and Latch phenomenon
5. Use Bipolar and Bi-CMOS circuits in very high speed design.

**Question Paper Pattern**

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

**Text Book**:

Sung Mo Kang & Yosuf Leblebici, “CMOS Digital Integrated Circuits: Analysis and Design”, Tata McGraw-Hill, Third Edition.

**Reference Books**:


1. Neil Weste and K. Eshragian, “Principles of CMOS VLSI Design: A System Perspective”, Second Edition, Pearson Education (Asia) Pvt. Ltd. 2000.
2. Wayne, Wolf, “Modern VLSI Design: System on Silicon” Prentice Hall PTR/Pearson Education, Second Edition, 1998.
3. Douglas A Pucknell & Kamran Eshragian , “Basic VLSI Design” PHI 3rd Edition (original Edition – 1994).

**ADVANCED EMBEDDED SYSTEM**

[As per Choice Based Credit System (CBCS) scheme]

SEMESTER – I

| | | | |
|---|---|---|---|
| Subject Code | 16EVE13 | IA Marks | 20 |
| Number of Lecture Hours/Week | 04 | Exam Marks | 80 |
| Total Number of Lecture Hours | 50 (10 Hours per Module) | Exam Hours | 03 |

CREDITS – 04

**Course objectives:** This course will enable students to:

- Understand the basic hardware components and their selection method based on the characteristics and attributes of an embedded system.
- Describe the hardware software co-design and firmware design approaches
- Explain the architectural features of ARM CORTEX M3, a 32 bit microcontroller including memory map, interrupts and exceptions.
- Program ARM CORTEX M3 using the various instructions, for different applications.

| **Modules** | **Revised Bloom's Taxonomy (RBT) Level** |
|---|---|
| **Module -1** | |
| **Embedded System**: Embedded vs General computing system, classification, application and purpose of ES. Core of an Embedded System, Memory, Sensors, Actuators, LED, Opto coupler, Communication Interface, Reset circuits, RTC, WDT, Characteristics and Quality Attributes of Embedded Systems (Text 1: Selected Topics from Ch -1, 2, 3). | **L1, L2, L3** |
| **Module -2** | |
| Hardware Software Co-Design, embedded firmware design approaches, computational models, embedded firmware development languages, Integration and testing of Embedded Hardware and firmware, Components in embedded system development environment (IDE), Files generated during compilation, simulators, emulators and debugging (Text 1: Selected Topics From Ch-7, 9, 12, 13). | **L1, L2, L3** |
| **Module -3** | |
| **ARM-32 bit Microcontroller**: Thumb-2 technology and applications of ARM, Architecture of ARM Cortex M3, Various Units in the architecture, General Purpose Registers, Special Registers, exceptions, interrupts, stack operation, reset sequence (Text 2: Ch 1, 2, 3) | **L1, L2, L3** |

| | |
|---|---|
| **Module -4** | |
| **Instruction Sets**: Assembly basics, Instruction list and description, useful instructions, Memory Systems, Memory maps, Cortex M3 implementation overview, pipeline and bus interface (Text 2: Ch-4, 5, 6) | **L1, L2, L3** |
| **Module -5** | |
| Exceptions, Nested Vector interrupt controller design, Systick Timer, Cortex-M3 Programming using assembly and C language, CMSIS (Text 2: Ch-7, 8, 10) | **L1, L2, L3** |

**Course Outcomes:** After studying this course, students will be able to:

- Understand the basic hardware components and their selection method based on the characteristics and attributes of an embedded system.
- Explain the hardware software co-design and firmware design approaches.
- Acquire the knowledge of the architectural features of ARM CORTEX M3, a 32 bit microcontroller including memory map, interrupts and exceptions.
- Apply the knowledge gained for Programming ARM CORTEX M3 for different applications.

**Question paper pattern:**

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

**Text Books:**

1. K. V. Shibu, "Introduction to embedded systems", TMH education Pvt. Ltd. 2009.
2. Joseph Yiu, “The Definitive Guide to the ARM Cortex-M3”, 2nd edn, Newnes, (Elsevier), 2010.

**Reference Book:**

James K. Peckol, "Embedded systems- A contemporary design tool", John Wiley, 2008.

**DIGITAL CIRCUITS AND LOGIC DESIGN**

[As per Choice Based Credit System (CBCS) scheme]

SEMESTER – I

| | | | |
|---|---|---|---|
| Subject Code | 16ELD14 | IA Marks | 20 |
| Number of Lecture | 04 | Exam Marks | 80 |
| Total Number of Lecture Hours | 50 (10 Hours per Module) | Exam Hours | 03 |

CREDITS – 04

**Course objectives:** This course will enable students to:

- Understand the concepts of sequential machines
- Design Sequential Machines/Circuits
- Analyze the faults in the design of circuits
- Apply fault detection experiments to sequential circuits

| **Modules** | **Revised Bloom's Taxonomy (RBT) Level** |
|---|---|
| **Module -1** | |
| Threshold Logic: Introductory Concepts, Synthesis of Threshold Networks, Capabilities, Minimization, and Transformation of Sequential Machines: The Finite- State Model, Further Definitions, Capabilities. | **L1, L2,L3** |
| **Module -2** | |
| Fault Detection by Path Sensitizing, Detection of Multiple Faults, Failure-Tolerant Design, Quadded Logic, Reliable Design and Fault Diagnosis Hazards: Fault Detection in Combinational Circuits. | **L1, L2, L3,L4** |
| **Module -3** | |
| Fault-Location Experiments, Boolean Differences, Limitations of Finite – State Machines, State Equivalence and Machine Minimization, Simplification of Incompletely Specified Machines. | **L1, L2, L3,L4** |
| **Module -4** | |
| Structure of Sequential Machines: Introductory Example, State Assignments Using Partitions, The Lattice of closed Partitions, Reductions of the Output Dependency, Input Independence and Autonomous Clocks, Covers and Generation of closed Partitions by state splitting, Information Flow in Sequential Machines, ELD ecompositions, Synthesis of Multiple Machines. | **L1, L2, L3,L4** |
| **Module -5** | |

| | |
|---|---|
| State Identifications and Fault-Detection Experiments: Homing Experiments, Distinguishing Experiments, Machine Identification, Fault Detection Experiments, Design of Diagnosable Machines, Second Algorithm for the Design of Fault Detection Experiments, Fault-Detection. | **L1, L2, L3,L4** |

**Course outcomes:** At the end of the course, the students will be able to:

- Understand the concepts of sequential machines
- Design Sequential Machines/Circuits
- Analyze the faults in the design of circuits
- Apply fault detection experiments to sequential circuits

**Question paper pattern**:

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

**Text Book:**

Zvi Kohavi, "Switching and Finite Automata Theory", 2nd Edition, TMH.

**Reference Books:**


1. Charles Roth Jr., "Digital Circuits and logic Design", 7thedn, Cengage Learning, 2014.
2. Parag K Lala, "Fault Tolerant And Fault Testable Hardware Design", Prentice Hall Inc. 1985.
3. E. V. Krishnamurthy, "Introductory Theory of Computer", Macmillan Press Ltd, 1983
4. Mishra & Chandrasekaran, "Theory of computer science – Automata, Languages and Computation", 2nd Edition, PHI, 2004.

| **DIGITAL SYSTEM DESIGN USING VERILOG**<br>[As per Choice Based Credit System (CBCS) scheme] | | | |
|---|---|---|---|
| Subject Code | 16EVE151 | IA Marks | 20 |
| Number of Lecture Hours/Week | 03 | Exam Marks | 80 |
| Total Number of Lecture Hours | 40 (08 Hours per Module) | Exam Hours | 03 |
| CREDITS – 03 | | | |

**Course objectives:** This course will enable students to:

- Understand the concepts of Verilog Language
- Design the digital systems as an activity in a larger systems design context.
- Study the design and operation of semiconductor memories frequently used in application specific digital system.
- Inspect how effectively IC's are embedded in package and assembled in PCB's for different application
- Design and diagnosis of processors and I/O controllers they can be used in embedded systems

| **Modules** | **Revised Bloom's Taxonomy (RBT) [illegible]** |
|---|---|
| **Module -1** | |
| **Introduction and Methodology**: Digital Systems and Embedded Systems, Binary representation and Circuit Elements, Real-World Circuits, Models, Design Methodology. | **L1, L2** |
| **Module -2** | |
| **Number Basics**: Unsigned and Signed Integers, Fixed and Floating-point Numbers.<br>**Sequential Basics**: Storage elements, Counters, Sequential Data paths and Control, Clocked Synchronous Timing Methodology. | **L1, L2** |
| **Module -3** | |
| **Memories**: Concepts, Memory Types, Error Detection and Correction.<br>**Implementation Fabrics**: ICs, PLDs, Packaging and Circuit Boards, Interconnection and Signal Integrity. | **L1, L2** |
| **Module -4** | |
| **Processor Basics**: Embedded Computer Organization, Instruction and Data, Interfacing with memory.<br>**I/O interfacing**: I/O devices, I/O controllers, Parallel Buses, Serial Transmission, I/O software. | **L2, L3** |
| **Module -5** | |

| | |
|---|---|
| **Accelerators**: Concepts, case study, Verification of accelerators.<br>**Design Methodology**: Design flow, Design optimization, Design for test. | **L2, L3** |

**Course outcomes:** After studying this course, students will be able to:

- Design embedded systems, using small microcontrollers, larger CPUs/DSPs, or hard or soft processor cores.
- Design construct the combinational circuits using discrete gates and programmable logic devices.
- Describe Verilog model for sequential circuits and test pattern generation
- Explore the different types of semiconductor memories and their usage for specific chip design
- Synthesis different types of processor and I/O controllers that are used in embedded system design

**Question paper pattern:**

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

**Text Book:**

Peter J. Ashenden, "Digital Design: An Embedded Systems Approach Using VERILOG", Elesvier, 2010.

**Reference Book:**

Verilog HDL: A Guide to Digital Design and Synthesis, Second Edition by Samir Palnitkar.

| **NANOELECTRONICS**<br>[As per Choice Based Credit System (CBCS) scheme] | | | |
|---|---|---|---|
| Subject Code | 16EVE152 | IA Marks | 20 |
| Number of Lecture Hours/Week | 03 | Exam Marks | 80 |
| Total Number of Lecture Hours | 40 (08 Hours per Module) | Exam Hours | 03 |
| CREDITS – 03 | | | |

**Course objectives:** This course will enable students to:

- Enhance basic engineering science and technological knowledge of nanoelect ronics.
- Explain basics of top-down and bottom-up fabrication process, devices and systems.
- Describe technologies involved in modern day electronic devices.
- Appreciate the complexities in scaling down the electronic devices in the future.

| **Modules** | **Revised Bloom's Taxonomy (RBT) Level** |
|---|---|
| **Module -1** | |
| **Introduction:** Overview of nanoscience and engineering. Development milestones in microfabrication and electronic industry. Moores' law and continued miniaturization, Classification of Nanostructures, Electronic properties of atoms and solids: Isolated atom, Bonding between atoms, Giant molecular solids, Free electron models and energy bands, crystalline solids, Periodicity of crystal lattices, Electronic conduction, effects of nanometer length scale, Fabrication methods: Top down processes, Bottom up processes methods for templating the growth of nanomaterials, ordering of nanosystems (Text 1). | **L1, L2** |
| **Module -2** | |
| **Characterization:** Classification, Microscopic techniques, Field ion microscopy, scanning probe techniques, diffraction techniques: bulk and surface diffraction techniques (Text1). | **L1,L2,L3** |
| **Module -3** | |

| | |
|---|---|
| **Characterization:** spectroscopy techniques: photon, radiofrequency, electron, surface analysis and dept profiling: electron, mass, Ion beam, Reflectrometry, Techniques for property measurement: mechanical, electron, magnetic, thermal properties.<br>**Inorganic semiconductor nanostructures:** overview of semiconductor physics. Quantum confinement in semiconductor nanostructures: quantum wells, quantum wires, quantum dots, super-lattices, band offsets, electronic density of states (Text1). | **L1-L3** |
| **Module -4** | |
| **Fabrication techniques:** requirements of ideal semiconductor, epitaxial growth of quantum wells, lithography and etching, cleaved-edge over growth, growth of vicinal substrates, strain induced dots and wires, electrostatically induced dots and wires, Quantum well width fluctuations, thermally annealed quantum wells, semiconductor nanocrystals, collidal quantum dots, self-assembly techniques.<br>**Physical processes:** modulation doping, quantum hall effect, resonant tunneling, charging effects, ballistic carrier transport, Inter band absorption, intraband absorption, Light emission processes, phonon bottleneck, quantum confined stark effect, nonlinear effects, coherence and dephasing, characterization of semiconductor nanostructures: optical electrical and structural (Text1). | **L1-L3** |
| **Module -5** | |
| **Methods of measuring properties:** atomic, crystollography, microscopy, spectroscopy (Text 2).<br><br>**Applications**: Injection lasers, quantum cascade lasers, single-photon sources, biological tagging, optical memories, coulomb blockade devices, photonic structures, QWIP's, NEMS, MEMS (Text 1). | **L1-L3** |

**Course outcomes:** After studying this course, students will be able to:

- Know the principles behind Nanoscience engineering and Nanoelectronics.
- Apply the knowledge to prepare and characterize nanomaterials.
- Know the effect of particles size on mechanical, thermal, optical and electrical properties of nanomaterials.
- Design the process flow required to fabricate state of the art transistor technol ogy.
- Analyze the requirements for new materials and device structure in the future technologies.

**Question paper pattern:**

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

**Text Books:**

1. Ed Robert Kelsall, Ian Hamley, Mark Geoghegan, “Nanoscale Science and Technology”, John Wiley, 2007.
2. Charles P Poole, Jr, Frank J Owens, “Introduction to Nanotechnology”, John Wiley, Copyright 2006, Reprint 2011.

**Reference Book:**

Ed William A Goddard III, Donald W Brenner, Sergey E. Lyshevski, Gerald J Iafrate, “Hand Book of Nanoscience Engineering and Technology”, CRC press, 2003.

**ASIC DESIGN**

[As per Choice Based Credit System (CBCS) scheme]

SEMESTER – I

| | | | |
|---|---|---|---|
| Subject Code | 16EVE153 | IA Marks | 20 |
| Number of Lecture Hours/Week | 03 | Exam Marks | 80 |
| Total Number of Lecture Hours | 40 | Exam Hours | 03 |

CREDITS – 03

**Course objectives:** This course will enable students to:

- Explain ASIC methodologies and programmable logic cells to implement a function on IC.
- Analyse back-end physical design flow, including partitioning, floor-planning, placement, and routing.
- Gain sufficient theoretical knowledge for carrying out FPGA and ASIC designs.
- Design CAD algorithms and explain how these concepts interact in ASIC design.

| **Modules** | **Revised Bloom's Taxonomy (RBT)Level** |
|---|---|
| **Module -1** | |
| **Introduction to ASICs**, Full custom, Semi-custom and Programmable ASICs, ASIC Design flow, ASIC cell libraries.<br>**CMOS Logic:** Datapath Logic Cells**:** Data Path Elements, Adders: Carry skip, Carry bypass, Carry save, Carry select, Conditional sum, Multiplier (Booth encoding), Data path Operators, I/O cells. | **L1,L2** |
| **Module -2** | |
| **ASIC Library Design:** Logical effort: Predicting Delay, Logical area and logical efficiency, Logical paths, Multi stage cells, Optimum delay and number of stages.<br>**Programmable ASIC Logic Cells:**<br>MUX as Boolean function generators, Actel ACT: ACT 1, ACT 2 and ACT 3 Logic Modules, Xilinx LCA: XC3000 CLB, Altera FLEX and MAX. | **L1-L3** |
| **Module -3** | |
| **Programmable ASIC I/O Cells:** Xilinx and Altera I/O Block.<br>**Low-level design entry:** Schematic entry: Hierarchical design, Netlist screener.<br>**ASIC Construction:** Physical Design, CAD Tools.<br>**Partitioning:** Goals and objectives, Constructive Partitioning, Iterative Partitioning Improvement, KL, FM and Look Ahead algorithms. | **L1-L4** |
| **Module -4** | |
| **Floor planning and placement:** Goals and objectives, Floor planning tools, Channel definition, I/O and Power planning and Clock planning.<br>Placement**:** Goals and Objectives, Min-cut Placement algorithm, Iterative Placement Improvement, Physical Design Flow. | **L1-L3** |

**Module -5**

| | |
|---|---|
| **Routing:** Global Routing: Goals and objectives, Global Routing Methods, Back-annotation. Detailed Routing: Goals and objectives, Measurement of Channel Density, Left-Edge and Area-Routing Algorithms.<br>Special Routing, Circuit extraction and DRC. | **L1-L3** |

**Course outcomes:**

After studying this course, students will be able to:

- Describe the concepts of ASIC design methodology, data path elements, logical effort and FPGA architectures.
- Analyze the design of FPGAs and ASICs suitable for specific tasks, perform design entry and explain the physical design flow.
- Design data path elements for ASIC cell libraries and compute optimum path delay.
- Create floor plan including partition and routing with the use of CAD algorithms.

**Question paper pattern:**

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

**Text Book:**

Michael John Sebastian Smith, "Application - Specific Integrated Circuits" Addison-Wesley Professional; 2005.

**Reference Books:**


1. Neil H.E. Weste, David Harris, and Ayan Banerjee, "CMOS VLSI Design: A Circuits and Systems Perspective", 3rd edition, Addison Wesley/ Pearson education, 2011.
2. Vikram Arkalgud Chandrasetty, "VLSI Design: A Practical Guide for FPGA and ASIC Implementations", Springer, 2011, ISBN: 978-1-4614-1119-2.
3. Rakesh Chadha**,** BhaskerJ., "An ASIC Low Power Primer", Springer, ISBN: 978-1-4614-4270-7.

**ADVANCED COMPUTER ARCHITECTURE**

[As per Choice Based Credit System (CBCS) scheme]

SEMESTER – I

| | | | |
|---|---|---|---|
| Subject Code | 16ELD154 | IA Marks | 20 |
| Number of Lecture Hours/Week | 03 | Exam Marks | 80 |
| Total Number of Lecture Hours | 40 | Exam Hours | 03 |

CREDITS – 03

**Course objectives:** This course will enable students to:

- Understand the basic concepts for parallel processing
- Analyze program partitioning and flow mechanisms
- Apply pipelining concept for the performance evaluation
- Learn the advanced processor architectures for suitable applications

| Modules | Revised Bloom's Taxonomy (RBT) Level |
|---|---|
| **Module -1** | |
| **Parallel Computer Models**: Classification of parallel computers, Multiprocessors and multicomputers, Multivector and SIMD computers. Program and Network Properties, Conditions of parallelism, Data and resource Dependences, Hardware and software parallelism. **(Text 1)** | **L2, L3, L4** |
| **Module -2** | |
| Program partitioning and scheduling, Grain Size and latency, Program flow mechanisms, Control flow versus data flow, Data flow Architecture, Demand driven mechanisms, Comparisons of flow mechanisms, Principles of Scalable Performance, Performance Metrics and Measures, Parallel Processing Applications, Speedup Performance Laws, Scalability Analysis and Approaches. **(Text 1)** | **L2, L3, L4** |
| **Module -3** | |
| **Advanced Processors**: Advanced processor technology, Instruction-set Architectures, CISC Scalar Processors, RISC Scalar Processors, Superscalar Processors, VLIW Architectures, Pipelining, Linear pipeline processor, nonlinear pipeline processor, Instruction pipeline design. **(Text 1)** | **L1, L2, L3** |
| **Module -4** | |
| Mechanisms for instruction pipelining, Dynamic instruction scheduling, Branch Handling techniques, branch prediction, Arithmetic Pipeline Design, Computer arithmetic principles, Static Arithmetic pipeline, Multifunctional arithmetic pipelines. **(Text 1)** | **L2, L3, L4** |
| **Module -5** | |

| | |
|---|---|
| Multithread and Dataflow Architecture: Principles of Multithreading, Scalable and Multithreaded Architecture, Dataflow Architecture, Symmetric shared memory architecture, distributed shared memory architecture. **(Text 1 & 2)** | **L1, L2, L3** |

**Course outcomes:** At the end of this course, the students will be able to:

- Understand the basic concepts for parallel processing
- Analyze program partitioning and flow mechanisms
- Apply pipelining concept for the performance evaluation
- Learn the advanced processor architectures for suitable applications

**Question paper pattern:**

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

**Text Books:**


1. Kai Hwang, "Advanced computer architecture", TMH. 2007.
2. Kai Hwang and Zu, "Scalable Parallel Computers Architecture", MGH, 2008.


**Reference Books:**


1. M.J. Flynn, "Computer Architecture, Pipelined and Parallel Processor Design", Narosa Publishing, 2002.
2. D.A.Patterson, J.L.Hennessy, "Computer Architecture: A quantitative approach", Morgan Kauffmann feb,2002.

**DIGITAL ELECTRONICS LAB -1**

[As per Choice Based Credit System (CBCS) scheme]

SEMESTER – I

| | | | |
|---|---|---|---|
| Laboratory Code | 16ELDL16 | IA Marks | 20 |
| Number of Lecture Hours/Week | 01Hr Tutorial (Instructions) + 02 Hours Laboratory | Exam Marks | 80 |
| | | Exam Hours | 03 |

CREDITS – 02

**Course objectives:** This laboratory course enables students to get practical experience on the

- Design tool such as Cadence OrCAD/ OrCAD Lite /EDA tool
- Design of analog and digital circuits using the simulation tool
- FPGA Design and testing for digital circuits
- Verilog programming and design of digital circuits
- Design, verification and performance testing

| **Laboratory Experiments** | **Revised Bloom's Taxonomy (RBT) Level** |
|---|---|
| **1.Using Cadence OrCAD or OrCAD Lite or any EDA Tool, design and verify the following:**<br><br>a) 3½ Digit Digital Voltmeter<br>b) Monolithic function Generator<br>c) Regulated Power supplies<br>d) Batch counter using TTL ICs.<br>e) DAC and ADC<br>f) P, PI, PID and ON/OFF Controllers<br>g) Programmable Timers<br>h) Filters and Resonance Circuits | **L2,L3,L4** |

| | |
|---|---|
| **2. Develop Verilog Program for design and testing the following digital circuits (for 4/8 bits) using FPGA/CPLD. Use logic analyzer/Chipscope for the verification of results.**<br><br>**(Note:** Programming can be done using any complier. Down load the programs on FPGA/CPLD boards and performance testing may be done using pattern generator (32 channels and logic analyzer )/Chipscope pro. Implementing the above designs on Xilinx/Altera/Cypress/equivalent based FPGA/CPLD kits.)<br><br>a. Carry skip and carry look ahead adder<br>b. BCD adder and subtractor<br>c. Array Multiplication (signed and unsigned)<br>d. Booth multiplication (radix-4)<br>e. Magnitude comparator<br>f. LFSR<br>g. Parity generator<br>h. Universal Shift Register<br>i. Sequence generation (11101 say) using Mealy/Moore FSM | **L2, L3, L4** |

**Course outcomes:** On the completion of this laboratory course, the students will be able to:

- Design an analog and digital systems using Cadence OrCAD, OrCAD Lite or any EDA tool.
- Develop Verilog Programs for Digital Circuit design simulation.
- Design and implement digital systems on FPGA/CPLD
- Testing and validation of digital systems using Logic analyzer/Chipscope

**Conduct of Practical Examination:**

1. All laboratory experiments are to be included for practical examination.
2. For examination, two questions using different tool to be set.
3. Students are allowed to pick one experiment from the lot.
4. Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.
5. Change of experiment is allowed only once and Marks allotted to the procedure part to be made zero.

# M.Tech – DE & E - SECOND SEMESTER SYLLABUS

| **Advanced DSP**<br>[As per Choice Based credit System (CBCS) Scheme<br>SEMESTER – II | | | |
|---|---|---|---|
| Subject Code | 16ECS21 | IA Marks | 20 |
| Number of Lecture Hours/Week | 04 | Exam marks | 80 |
| Total Number of Lecture Hours | 50<br>(10 Hours per Module) | Exam Hours | 03 |
| CREDITS – 04 | | | |

**Course objectives:** This course will enable students to:

- Understand Multirate digital signal processing principles and its applications.
- Estimate the various spectral components present in the received signal using different spectral estimation methods such as Parametric and Nonparametric.
- Design and implement an optimum adaptive filter using LMS and RLS algorithms.
- Understand the concepts and mathematical representations of Wavelet transforms.

| **Modules** | **RBT Level** |
|---|---|
| **Module 1** | |
| **Multirate Digital Signal Processing:** Introduction, decimation by a factor 'D', Interpolation by a factor 'I', sampling rate conversion by a factor 'I/D', Implementation of sampling rate conversion, Multistage implementation of sampling rate conversion, Applications of multirate signal processing, Digital filter banks, two channel quadrature mirror filter banks, M-channel QMF bank. (Text 1) | L1,L2,L3 |
| **Module 2** | |
| **Linear prediction and Optimum Linear Filters:** Random signals, Correlation Functions and Power Spectra, Innovations Representation of a Stationary Random Process. Forward and Backward Linear Prediction. Solution of the Normal Equations The Levinson-Durbin Algorithm. Properties of the Linear Prediction-Error Filters. (Text 1) | L1,L2,L3 |
| **Module 3** | |
| **Adaptive filters: Applications of adaptive filters**- Adaptive channel equalization,, Adaptive noise cancellation, Linear Predictive coding of Speech Signals, Adaptive direct form FIR filters-The LMS algorithm, Properties of LMS algorithm.<br>**Adaptive direct form filters-** RLS algorithm. (Text 1) | L1,L2,L3 |
| **Module 4** | |
| **Power Spectrum Estimation:** Non parametric Methods for Power Spectrum Estimation - Bartlett Method, Welch Method, Blackman and Tukey Methods.<br>**Parametric Methods for Power Spectrum Estimation:**<br>Relationship between the auto correlation and the model | |

| | |
|---|---|
| parameters, Yule and Walker methods for the AR Model Parameters, Burg Method for the AR Model parameters, Unconstrained least-squares method for the AR Model parameters, Sequential estimation methods for the AR Model parameters, ARMA Model for Power Spectrum Estimation. (Text 1) | L1,L2,L3 |
| **Module 5** | |
| **WAVELET TRANSFORMS:**T he Age of Wavelets, The origin of Wavelets, Wavelets and other reality transforms, History of wavelets, Wavelets of the future.<br>**Continuous Wavelet and Short Time Fourier Transform:** Wavelet Transform, Mathematical preliminaries, Properties of wavelets.<br>**Discrete Wavelet Transform**: Haar scaling functions, Haar wavelet function, Daubechies Wavelets. (Chapters 1, 3 & 4 of Text 2) | L1,L2,L3 |

**Course Outcomes:** After studying this course, students will be able to:

- Design adaptive filters for a given application
- Design multirate DSP Systems
- Implement adaptive signal processing algorithm
- Design active networks
- Understand important advanced signal processing techniques, including multi-rate processing and time-frequency analysis techniques

**Question paper pattern:**

The question paper will have ten questions.

- Each full question consists of 16marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.
- The Students will have to answer 5 full questions, selecting one full question from each module.

**Text Books:**


1. "Digital Signal Processing, Principles, Algorithms and Applications", John G.Proakis, Dimitris G.Manolakis, Fourth edition, Pearson-2007.
2. Insight into Wavelets- from Theory to Practice", K.P Soman, Ramachandran, Resmi- PHI Third Edition-2010.


**Reference Books:**


1. "Modern Digital signal processing", Robert. O. Cristi, Cengage Publishers, India, 2003.
2. "Digital signal processing: A Practitioner's approach", E.C. Ifeachor, and B. W. Jarvis, , Second Edition, Pearson Education, India, 2002, Reprint.
3. "Wavelet Transforms, Introduction to Theory and applications", Raghuveer. M. Rao, Ajit S.Bopardikar, Pearson Education, Asia, 2000.

**Error Control Coding**

[As per Choice Based Credit System (CBCS) Scheme]

SEMESTER – II

| | | | |
|---|---|---|---|
| Subject Code | 16ECS22 | IA Marks | 20 |
| Number of Lecture Hours/Week | 04 | Exam marks | 80 |
| Total Number of Lecture Hours | 50 (10 Hours per Module) | Exam Hours | 03 |

CREDITS – 04

**Course objectives:** This course will enable students to:

- Explain the Entropy, information rate and capacity for the Discrete memoryless channel.
- Apply modern algebra and probability theory for the coding.
- Compare Block codes such as Linear Block Codes, Cyclic codes etc and Convolutional codes.
- Detect and correct errors for different data communication and storage systems.
- Implement different Block code encoders and decoders.
- Analyse and implement convolutional encoders and decoders.
- Analyse and apply soft and hard Viterbi algorithm for decoding of convolutional codes.

| **Modules** | **RBT Level** |
|---|---|
| **Module 1** | |
| **Information theory:** Introduction, Entropy, Source coding theorem, discrete memoryless channel, Mutual Information, Channel Capacity Channel coding theorem.(Chap. 5 of Text 1)<br>**Introduction to algebra**: Groups, Fields, binary field arithmetic, Construction of Galois Fields GF ($2^m$) and its properties, (Only statements of theorems without proof) Computation using Galois filed GF ($2^m$) arithmetic, Vector spaces and Matrices. (Chap. 2 of Text 2) | L1,L2,L3 |
| **Module 2** | |
| **Linear block codes**: Generator and parity check matrices, Encoding circuits, Syndrome and error detection, Minimum distance considerations, Error detecting and error correcting capabilities, Standard array and syndrome decoding, Single Parity Check Codes(SPC),Repetition codes, Self dual codes, Hamming codes, Reed-Muller codes. Product codes and Interleaved codes. (Chap. 3 of Text 2) | L1,L2,L3 |
| **Module 3** | |
| **Cyclic codes:** Introduction, Generator and parity check polynomials, Encoding of cyclic codes, Syndrome computing and error detection, Decoding of cyclic codes, Error trapping Decoding, Cyclic hamming codes, Shortened cyclic codes.(Chap. 4 of Text2) | L1,L2,L3 |
| **Module 4** | |
| **BCH codes:** Binary primitive BCH codes, Decoding procedures, Implementation of Galois field arithmetic, Implementation of error correction. (Chap. 6 of Text 2)<br>**Reed -Solomon codes.** (Chap. 7 of Text 2) | |

| | |
|---|---|
| **Majority Logic decodable codes**: One -step majority logic decoding, One-step majority logic decodable codes, Two-step majority logic, decoding, Multiple-step majority logic. (Chap. 8 of Text 2) | L1,L2,L3 |
| **Module 5** | |
| **Convolution codes:** Convolutional Encoding, Convolutional Encoder Representation, Formulation of the Convolutional Decoding Problem, Properties of Convolutional Codes: Distance property of convolutional codes, Systematic and Nonsystematic Convolutional Codes, Performance Bounds for Convolutional Codes, Coding Gain. Other Convolutional Decoding Algorithms: Sequential Decoding, Feedback Decoding.(Chap. 7 of Text 3) | L1,L2,L3 |

**Course Outcomes:** After studying this course, students will be able to:

- Analyse a discrete memoryless channel, given the source and transition probabilities.
- Apply the concept of modern linear algebra for the error control coding technique.
- Implement efficient LBC, Cyclic codes etc encoder and decoders.
- Apply decoding algorithms for efficient decoding of Block codes and Convolutional codes.

**Question paper pattern:**

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

**Text Books:**


1. Simon Haykin, ”Digital Communication systems”, First edition, Wiley India Private. Ltd, 2014. ISBN 978-81-265-4231-4
2. Shu Lin and Daniel J. Costello. Jr, "Error control coding", Pearson, Prentice Hall, 2nd edition, 2004.
3. Bernard Sklar, ”Digital Communications - Fundamentals and Applications”, 2nd Edition Pearson Education (Asia) Ptv. Ltd, 2001.


**Reference Books:**


1. Blahut. R. E, "Theory and practice of error control codes", Addison Wesley, 1984.
2. 2. Salvatore Gravano, “Introduction to Error control coding”, Oxford university press, 2007.

**Advances in VLSI Design**

[As per Choice Based credit System (CBCS) Scheme

SEMESTER – II

| | | | |
|---|---|---|---|
| Subject Code | 16EVE23 | IA Marks | 20 |
| Number of Lecture Hours/Week | 04 | Exam marks | 80 |
| Total Number of Lecture Hours | 50 (10 Hours per Module) | Exam Hours | 03 |

CREDITS – 04

**Course Objectives:** This course will enable the students to:

- Learn circuit-oriented approach towards digital design
- Illustrate the impact of interconnect wiring on the functionality and performance of a digital gate.
- Infer different approaches to digital timing and clocking circuits
- Understand the impact of clock skew on the behaviour of digital synchronous circuits
- Explain the role of peripheral circuitry such as the decoders, sense amplifiers, drivers and control circuitry in the design of reliable and fast memories

| **Modules** | **RBT Level** |
|---|---|
| **Module 1** | |
| **Implementation Strategies For Digital ICS:** Introduction, From Custom to Semicustom and Structured Array Design Approaches, Custom Circuit Design, Cell-Based Design Methodology, Standard Cell, Compiled Cells, Macrocells, Megacells and Intellectual Property, Semi-Custom Design Flow, Array-Based Implementation Approaches, Pre-diffused (or Mask-Programmable) Arrays, Pre-wired Arrays, Perspective-The Implementation Platform of the Future. | L1,L2,L3 |
| **Module 2** | |
| **Coping With Interconnect:** Introduction, Capacitive Parasitics, Capacitance and Reliability-Cross Talk, Capacitance and Performance in CMOS, Resistive Parasitics, Resistance and Reliability-Ohmic Voltage Drop, Electromigration, Resistance and Performance-RC Delay, Inductive Parasitics, Inductance and Reliability-Voltage Drop, Inductance and Performance-Transmission Line Effects, Advanced Interconnect Techniques, Reduced-Swing Circuits, Current-Mode Transmission Techniques, Perspective: Networks-on-a-Chip. | L1,L2,L3 |
| **Module 3** | |
| **Timing Issues In Digital Circuits:** Introduction, Timing Classification of Digital Systems, Synchronous Interconnect, Mesochronous interconnect, Plesiochronous Interconnect, Asynchronous Interconnect, Synchronous Design — An In-depth Perspective, Synchronous Timing Basics, Sources of Skew and Jitter, Clock-Distribution Techniques, Latch-Based Clocking, Self-Timed Circuit Design, Self-Timed Logic - An Asynchronous Technique, Completion-Signal Generation, Self-Timed Signaling, Practical Examples of Self-Timed Logic, Synchronizers and Arbiters, | L1,L2,L3 |

| | |
|---|---|
| Synchronizers-Concept and Implementation, Arbiters, Clock Synthesis and Synchronization Using a Phase-Locked Loop, Basic Concept, Building Blocks of a PLL. | |
| **Module 4** | |
| **Designing Memory and Array Structures:** Introduction, Memory Classification, Memory Architectures and Building Blocks, The Memory Core, Read-Only Memories, Nonvolatile Read-Write Memories, Read-Write Memories (RAM), Contents-Addressable or Associative Memory (CAM), Memory Peripheral Circuitry, The Address Decoders, Sense Amplifiers, Voltage References, Drivers/Buffers, Timing and Control. | L1,L2,L3 |
| **Module 5** | |
| **Designing Memory and Array Structures:** Memory Reliability and Yield, Signal-to-Noise Ratio, Memory yield, Power Dissipation in Memories, Sources of Power Dissipation in Memories, Partitioning of the memory, Addressing the Active Power Dissipation, Data-retention dissipation, Case Studies in Memory Design: The Programmable Logic Array (PLA), A 4 Mbit SRAM, A 1 Gbit NAND Flash Memory, Perspective: Semiconductor Memory Trends and Evolutions. | L1,L2,L3 |

**Course Outcomes:** After studying this course, students will be able to:

- Apply design automation for complex circuits using the different implementation methodology like custom versus semi-custom, hardwired versus fixed, regular array versus ad-hoc.
- Use the approaches to minimize the impact of interconnect parasitics on performance, power dissipation and circuit reliability
- Impose the ordering of the switching events to meet the desired timing constraints using synchronous, clocked approach.
- Infer the reliability of the memory.

**Question paper pattern:**

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

**Text Book**:

Jan M Rabey, Anantha Chandrakasan, Borivoje Nikolic, “Digital Integrated Circuits-A Design Perspective”, PHI, 2nd Edition.

**Reference Books**:


1. M. Smith, “ Application Specific Integrated circuits”, Addison Wesley, 1997
2. H. Veendrick, “ MOS IC’s: From Basics to ASICs, Wiley-VCH, 1992.
3. Anantha P. Chandrakasan , Robert W. Brodersen, “Low Power Digital CMOS Design”, Kluwer Academic Publisher, 1995.

| **Real Time Operating System**<br>[As per Choice Based credit System (CBCS) Scheme<br>SEMESTER – II | | | |
|---|---|---|---|
| Subject Code | 16EVE24 | IA Marks | 20 |
| Number of Lecture Hours/Week | 04 | Exam marks | 80 |
| Total Number of Lecture Hours | 50<br>(10 Hours per Module) | Exam Hours | 03 |
| CREDITS – 04 | | | |

**Course Objectives:** This course will enable the students to:

- Introduce the fundamental concepts of Real Time Operating Systems and the real time embedded system
- Apply concepts relating to operating systems such as Scheduling techniques, Thread Safe Reentrant Functions, Dynamic priority policies.
- Describe concepts related to Multi resource services like blocking, Deadlock, live lock & soft real-time services.
- Discuss Memory management concepts, Embedded system components, Debugging components and file system components.
- Study programs for multithreaded applications using suitable data structures.

| **Modules** | **RBT Level** |
|---|---|
| **Module 1** | |
| **Real-Time Systems and Resources:** Brief history of Real Time Systems, A brief history of Embedded Systems. System Resources, Resource Analysis, Real-Time Service Utility, Scheduler concepts, Real-Time OS, State transition diagram and tables, Thread Safe Reentrant Functions. (Text 1: Selected sections from Chap. 1, 2) | L1,L2,L3 |
| **Module 2** | |
| **Processing with Real Time Scheduling:** Scheduler Concepts, Preemptive Fixed Priority Scheduling Policies with timing diagrams and problems and issues, Feasibility, Rate Monotonic least upper bound, Necessary and Sufficient feasibility, Deadline –Monotonic Policy, Dynamic priority policies, Alternative to RM policy. (Text 1: Chap. 2,3,7) | L1,L2,L3 |
| **Module 3** | |
| **Memory and I/O**: Worst case execution time, Intermediate I/O, Shared Memory, ECC Memory, Flash file systems. Multi-resource Services, Blocking, Deadlock and live lock, Critical sections to protect shared resources, Missed deadline, QoS, Reliability and Availability, Similarities and differences, Reliable software, Available software.<br>(Text 1: Selected topics from Chap. 4,5,6,7,11) | L1,L2,L3 |
| **Module 4** | |
| **Firmware Components:** The 3 firmware components, RTOS system software mechanisms, Software application components. Debugging Components, Exceptions, assert, Checking return codes, Single-step debugging, kernel scheduler traces, Test access ports, Trace | L1,L2,L3 |

| | |
|---|---|
| Ports, External test equipment. (Text 1: Selected topics from Chap. 8,9) | |
| **Module 5** | |
| **Process and Threads**: Process and thread creations, Simple Programs, Programs related to semaphores, message queue, shared buffer applications involving inter task/thread communication using multiple threads. (Text 2: Chap. 11) | L1,L2,L3 |

**Course Outcomes:** After studying this course, students will be able to:

- Develop programs for real time services, firmware and RTOS, using the fundamentals of Real Time Embedded System, real time service utilities, debugging methodologies and optimization techniques.
- Select the appropriate system resources (CPU, I/O, Memory, Cache, ECC Memory, Microcontroller/FPGA/ASIC to improve the system performance.
- Apply priority based static and dynamic real time scheduling techniques for the given specifications.
- Analyse deadlock conditions, shared memory problem, critical section problem, missed deadlines, availability, reliability and QoS.
- Develop programs for multithreaded applications using suitable techniques and data structure

**Question paper pattern:**

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

**Text Books**:


1. Sam Siewert, "Real-Time Embedded Systems and Components", Cengage Learning India Edition, 2007.
2. Dr. K.V.K.K Prasad, Embedded/Real Time Systems, Concepts, Design and Programming, Black Book, DreamTech Press, New edition, 2010.


**Reference Books**:


1. James W S Liu, "Real Time System", Pearson education, 2008.
2. DreamTech Software Team, "Programming for Embedded Systems", John Wiley, India Pvt. Ltd., 2008.

**Automotive Electronics**

[As per Choice Based credit System (CBCS) Scheme

SEMESTER – II

| | | | |
|---|---|---|---|
| Subject Code | 16ELD251 | IA Marks | 20 |
| Number of Lecture Hours/Week | 03 | Exam marks | 80 |
| Total Number of Lecture Hours | 40 (8 Hours per Module) | Exam Hours | 03 |

CREDITS – 03

**Course Objectives:** This course will enable students to:

- Understand the complete dynamics of automotive electronics
- Design and implement the electronics that attributes the smartness to the automobiles by way of unprecedented safety, add-on features, and comforts.

| **Modules** | **RBT Level** |
|---|---|
| **Module 1** | |
| **Automotive Fundamentals, the Systems Approach to Control and Instrumentation**: Use Of Electronics In The Automobile, Antilock Brake Systems, (ABS), Electronic steering control, Power steering, Traction control, Electronically controlled suspension. (Chap.1 and 2 of Text) | L1,L2 |
| **Module 2** | |
| **Automotive instrumentation Control:** Sampling, Measurement and signal conversion of various parameters. (Chap. 4 of Text) | L1,L2, L3 |
| **Module 3** | |
| **The basics of Electronic Engine control:** Integrated body: Climate controls, Motivation for Electronic Engine Control, Concept of An Electronic Engine Control System, Definition of General Terms, Definition of Engine Performance Terms, Electronic fuel control system, Engine control sequence, Electronic Ignition, Sensors and Actuators, Applications of sensors and actuators, air flow rate sensor, Indirect measurement of mass air flow, Engine crankshaft angular position sensor, Automotive engine control actuators, Digital engine control, Engine speed sensor, Timing sensor for ignition and fuel delivery, Electronic ignition control systems, Safety systems, Interior safety, Lighting, Entertainment systems. (Chap. 5 and 6 of Text) | L1,L2,L3 |
| **Module 4** | |

| | |
|---|---|
| **Vehicle Motion Control and Automotive diagnostics:** Cruise control system, Digital cruise control, Timing light, Engine analyzer, On-board and off-board diagnostics, Expert systems. Stepper motor-based actuator, Cruise control electronics, Vacuum - antilock braking system, Electronic suspension ystem Electronic steering control, Computer-based instrumentation system, Sampling and Input\output signal conversion, Fuel quantity measurement, Coolant temperature measurement, Oil pressure measurement, Vehicle speed measurement, Display devices, Trip-Information-Computer, Occupant protection systems. (Chap. 8 and 10 of Text) | L1,L2, L3 |
| **Module 5** | |
| **Future automotive electronic systems:**<br>Alternative Fuel Engines, Collision Wide Range Air/Fuel Sensor, Alternative Engine, Low Tire Pressure Warning System, Collision avoidance Radar Warning Systems, Low Tire Pressure Warning System, Radio Navigation, Advance Driver information System. Alternative-Fuel Engines , Transmission Control , Collision Avoidance Radar Warning System, Low Tire Pressure Warning System, Speech Synthesis Multiplexing in Automobiles, Control Signal Multiplexing, Navigation Sensors, Radio Navigation, Sign post Navigation , Dead Reckoning Navigation Future Technology, Voice Recognition Cell Phone Dialing Advanced Driver information System, Automatic Driving Control. (Chap. 11 of Text) | L1, L2, L3 |
| **Course Outcomes:** After studying this course, students will be able to:<br>• Implement various control requirements in the automotive system.<br>• Comprehend dashboard electronics and engine system electronics.<br>• Identify various physical parameters that are to be sensed and monitored for maintaining the stability of the vehicle under dynamic conditions.<br>• Understand and implement the controls and actuator system pertaining to the comfort and safety of commuters.<br>• Design sensor network for mechanical fault diagnostics in an automotive vehicle. | |
| **Question paper pattern:**<br>• The question paper will have 10 full questions carrying equal marks.<br>• Each full question consists of 16 marks with a maximum of four sub questions.<br>• There will be 2 full questions from each module covering all the topics of the module<br>• The students will have to answer 5 full questions, selecting one full question from each module. | |
| **Text Book**:<br>William B. Ribbens , "Understanding Automotive Electronics", SAMS/Elsevier publishing, 6th Edition, 1997.<br><br>**Reference Book**:<br>Robert Bosch Gmbh, "Automotive Electrics and Automotive Electronics-Systems and Components, Networking and Hybrid Drive", Springer Vieweg, 5th Edition, 2007. | |

**Multimedia over Communication Links**

[As per Choice Based credit System (CBCS) Scheme

SEMESTER – II

| | | | |
|---|---|---|---|
| Subject Code | 16ECS252 | IA Marks | 20 |
| Number of Lecture Hours/Week | 03 | Exam marks | 80 |
| Total Number of Lecture Hours | 40 (8 Hours per Module) | Exam Hours | 03 |

CREDITS – 03

**Course Objectives:** This course will enable students to:

- Gain fundamental knowledge in understanding the basics of different multimedia networks, applications, media types like text and image.
- Analyse media types like audio and video and gain knowledge on multimedia systems.
- Analyse Audio compression techniques required to compress Audio.
- Analyse compression techniques required to compress video.
- Gain fundamental knowledge about the Multimedia Communications in different Networks.

| **Modules** | **RBT Level** |
|---|---|
| **Module 1** | |
| **Multimedia Communications**: Introduction, Multimedia information representation, multimedia networks, multimedia applications, Application and networking terminology. (Chap. 1 of Text1)<br>**Information Representation**: Introduction, Text, Images. (Chap. 2- Sections 2.2 and 2.3 of Text 1) | L1, L2, L3 |
| **Module 2** | |
| **Information Representation**: Audio and Video. (Chap. 2 - Sections 2.4 and 2.5 of Text 1)<br>**Distributed multimedia systems**: Introduction, main Features of a DMS, Resource management of DMS, Networking, Multimedia operating systems. (Chap. 4 - Sections 4.1 to 4.5 of Text 2) | L1, L2, L3 |
| **Module 3** | |
| **Multimedia Processing in Communication:** Introduction, Perceptual coding of digital Audio signals, Transform Audio Coders, Audio Sub band Coders. (Chap. 3 - Sections 3.1, 3.2, 3.6, 3.7 of Text 2) | L1, L2, L3 |
| **Module 4** | |
| **Multimedia Communication Standards:** Introduction, MPEG approach to multimedia standardization, MPEG-1, MPEG-2, Overview of MPEG-4. (Chap. 5 - Sections 5.1 to 5.4 and 5.5.1 of Text 2) | L1, L2, L3 |
| **Module 5** | |
| **Multimedia Communication Across Networks:** Packet audio/video in the network environment, Video transport across generic networks, Multimedia Transport across ATM Networks. (Chap. 6 - Sections 6.1, 6.2, 6.3 of Text 2) | L1, L2, L3 |

**Course Outcomes:** After studying this course, students will be able to:

- Understand basics of different multimedia networks, applications.
- Analyse media types like audio and video to represent in digital form.
- Understand different compression techniques to compress audio.
- Understand different compression techniques to compress audio video.
- Describe the basics of Multimedia Communication Across Networks

**Question paper pattern:**

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

**Text Books**:

1. Fred Halsall, "Multimedia Communications", Pearson education, 2001, ISBN -9788131709948.
2. K. R. Rao, Zoran S. Bojkovic, Dragorad A. Milovanovic, "Multimedia Communication Systems", Pearson education, 2004. ISBN - 9788120321458.

**Reference Book**:

Raif steinmetz, Klara Nahrstedt, "Multimedia: Computing, Communications and Applications", Pearson education, 2002, ISBN -9788177584417.

| **Micro Electro Mechanical Systems**<br>[As per Choice Based credit System (CBCS) Scheme]<br>SEMESTER – II | | | |
|---|---|---|---|
| Subject Code | 16ELD253 | IA Marks | 20 |
| Number of Lecture Hours/Week | 03 | Exam marks | 80 |
| Total Number of Lecture Hours | 40<br>(8 Hours per Module) | Exam Hours | 03 |
| CREDITS – 03 | | | |

**Course Objectives:** This course will enable students to:

- Understand overview of microsystems, their fabrication and application areas.
- Working principles of several MEMS devices.
- Develop mathematical and analytical models of MEMS devices
- Know methods to fabricate MEMS devices
  Various application areas where MEMS devices can be used.

| **Modules** | **RBT Level** |
|---|---|
| **Module 1** | |
| **Overview of MEMS and Microsystems:** MEMS and Microsystem, Typical MEMS and Microsystems Products, Evolution of Microfabrication, Microsystems and Microelectronics, Multidisciplinary Nature of Microsystems, Miniaturization. Applications and Markets. | L1, L2 |
| **Module 2** | |
| **Working Principles of Microsystems:**<br>Introduction, Microsensors, Microactuation, MEMS with Microactuators, Microaccelerometers, Microfluidics.<br>Engineering Science for Microsystems Design and Fabrication.<br>Introduction, Atomic Structure of Matters, Ions and Ionization, Molecular Theory of Matter and Inter-molecular Forces, Doping of Semiconductors, The Diffusion Process, Plasma Physics, Electrochemistry. | L1, L2 |
| **Module 3** | |
| **Engineering Mechanics for Microsystems Design:**<br>Introduction, Static Bending of Thin Plates, Mechanical Vibration, Thermomechanics, Fracture Mechanics, Thin Film Mechanics, Overview on Finite Element Stress Analysis. | L1,L2,L3 |
| **Module 4** | |
| **Scaling Laws in Miniaturization:**<br>Introduction, Scaling in Geometry, Scaling in Rigid-Body Dynamics, Scaling in Electrostatic Forces, Scaling of Electromagnetic Forces, Scaling in Electricity, Scaling in Fluid Mechanics, Scaling in Heat Transfer. | L1,L2, L3 |
| **Module 5** | |
| **Overview of Micromanufacturing:**<br>Introduction, Bulk Micromanufacturing, Surface Micromachining, The LIGA Process, Summary on Micromanufacturing. | L1,L2, L3 |

| | |
|---|---|
| **Microsystem Design:**<br>Introduction, Design Considerations, Process Design, Mechanical Design, Using Finite Element Method. | |

**Course Outcomes:** After studying this course, students will be able to:

- Appreciate the technologies related to Micro Electro Mechanical Systems.
- Understand design and fabrication processes involved with MEMS devices.
- Analyse the MEMS devices and develop suitable mathematical models
- Know various application areas for MEMS device

**Question paper pattern:**

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

**Text Book**:

1. Tai-Ran Hsu, MEMS and Micro systems: Design, Manufacture and Nanoscale Engineering, 2nd Ed, Wiley.

**Reference Books:**

1. Hans H. Gatzen, Volker Saile, Jurg Leuthold, Micro and Nano Fabrication: Tools and Processes, Springer, 2015.
2. Dilip Kumar Bhattacharya, Brajesh Kumar Kaushik, Micro Electromechanical Systems (MEMS), Cenage Learning.

| **Cryptography and Network Security**<br>[As per Choice Based credit System (CBCS) Scheme<br>SEMESTER – II | | | |
|---|---|---|---|
| Subject Code | 16ECS254 | IA Marks | 20 |
| Number of Lecture Hours/Week | 03 | Exam marks | 80 |
| Total Number of Lecture Hours | 40<br>(8 Hours per Module) | Exam Hours | 03 |
| CREDITS – 03 | | | |

**Course Objectives:** This course will enable students to:

- Understand the basics of symmetric key and public key cryptography.
- Understand some basic mathematical concepts and pseudorandom number generators required for cryptography.
- Authenticate and protect the encrypted data.
- Enrich knowledge about Email, IP and Web security.

| **Modules** | **RBT Level** |
|---|---|
| **Module 1** | |
| **Foundations:** Terminology, Steganography, substitution ciphers and transpositions ciphers, Simple XOR, One-Time Pads, Computer Algorithms (Text 2: Chapter 1: Section 1.1 to 1.6)<br>**SYMMETRIC CIPHERS:** Traditional Block Cipher structure, Data encryption standard (DES), The AES Cipher. (Text 1: Chapter 2: Section2.1, 2.2, Chapter 4) | L1,L2,L3 |
| **Module 2** | |
| Introduction to modular arithmetic, Prime Numbers, Fermat's and Euler's theorem, primality testing, Chinese Remainder theorem, discrete logarithm. (Text 1: Chapter 7: Section 1, 2, 3, 4, 5)<br>Principles of Public-Key Cryptosystems, The RSA algorithm, Diffie - Hellman Key Exchange, Elliptic Curve Arithmetic, Elliptic Curve Cryptography (Text 1: Chapter 8, Chapter 9: Section 9.1, 9.3, 9.4) | L1, L2, L3 |
| **Module 3** | |
| **Pseudo-Random-Sequence Generators and Stream Ciphers:** Linear Congruential Generators, Linear Feedback Shift Registers, Design and analysis of stream ciphers, Stream ciphers using LFSRs, A5, Hughes XPD/KPD, Nanoteq, Rambutan, Additive generators, Gifford, Algorithm M, PKZIP (Text 2: Chapter 16) | L1, L2, L3 |
| **Module 4** | |
| **One-Way Hash Functions:** Background, Snefru, N-Hash, MD4, MD5, Secure Hash Algorithm [SHA],One way hash functions using symmetric block algorithms, Using public key algorithms, Choosing a one-way hash functions, Message Authentication Codes. Digital Signature Algorithm, Discrete Logarithm Signature Scheme (Text 2: Chapter 18: Section 18.1 to 18.5, 18.7, 18.11 to 18.14 and Chapter 20: Section 20.1, 20.4) | L1, L2, L3 |
| **Module 5** | |
| **E-mail Security:** Pretty Good Privacy-S/MIME (Text 1: Chapter 17: Section 17.1, 17.2).<br>**IP Security:** IP Security Overview, IP Security Policy, Encapsulation | L1, L2, L3 |

| | |
|---|---|
| Security Payload (ESP),Combining security Associations. (Text 1: Chapter 18: Section 18.1 to 18.4).<br>**Web Security:** Web Security Considerations, SSL(Text 1: Chapter 15: Section 15.1, 15.2). | |

**Course Outcomes:** After studying this course, students will be able to:

- Use basic cryptographic algorithms to encrypt the data.
- Generate some pseudorandom numbers required for cryptographic applications.
- Provide authentication and protection for encrypted data.

**Question paper pattern:**

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

**Text Books**:


1. William Stallings , "Cryptography and Network Security Principles and Practice", Pearson Education Inc., 6th Edition, 2014, ISBN: 978-93-325-1877-3
2. Bruce Schneier, "Applied Cryptography Protocols, Algorithms, and Source code in C", Wiley Publications, 2nd Edition, ISBN: 9971-51-348-X


**Reference Books**:


1. Cryptography and Network Security, Behrouz A. Forouzan, TMH, 2007.
2. Cryptography and Network Security, Atul Kahate, TMH, 2003.

**Digital Electronics Lab -2**

[As per Choice Based Credit System (CBCS) scheme]

SEMESTER – II

| | | | |
|---|---|---|---|
| Laboratory Code | 16ELDL26 | IA Marks | 20 |
| Number of Lecture Hours/Week | 01Hr Tutorial (Instructions) + 02 Hours Laboratory | Exam Marks | 80 |
| | | Exam Hours | 03 |

CREDITS – 02

**Course objectives:** This laboratory course enables students to

1. Design and simulate digital electronic circuits using graphical programming tool LabVIEW.
2. Create user friendly interfaces using LabVIEW and analyze the input and output data for various digital circuits.
3. Use of assembly level programming for different applications using ARM-CORTEX M3 Kit and Keil uVision-4 tool.
4. Practice the different concepts and applications of C programming environment with ARM CORTEX M3.

| **Laboratory Experiments** | **Revised Bloom's Taxonomy (RBT) Level** |
|---|---|
| **PART-A: Graphical Programming using LabVIEW**<br>a) Design of 4 bit Adders (CLA, CSA, CMA, Parallel adders)<br>b) Design of Binary Subtractors<br>c) Design of Encoder (8X3), Decoder(3X8)<br>d) Design of Multiplexer (8X1), and Demultiplexer (1X8)<br>e) Design of code converters & Comparator<br>f) Design of FF (SR, D, T, JK, and Master Slave with delays)<br>g) Design of registers using latches and flip-flops<br>h) Design of 8 bit Shift registers<br>i) Design of Asynchronous & Synchronous Counters | L3 |

| | |
|---|---|
| **PART-B: ARM-CORTEX M3**<br>**[Programming to be done using Keil uVision 4 and download the program on to a M3 evaluation board such as NXP LPC1768 or ATMEL ATSAM3U]**<br>a) Write an Assembly language program to calculate 10+9+8+.....+1<br>b) Write a Assembly language program to link Multiple object files and link them together.<br>c) Write a Assembly language program to store data in RAM.<br>d) Write a C program to Output the "Hello World" message using UART.<br>e) Write a C program to Design a Stopwatch using interrupts.<br>f) Write an Exception vector table in C<br>g) Write an Assembly Language Program for locking a Mutex.<br>h) Write a SVC handler in C. Use the wrapper code to extract the correct stack frame starting location. The C handler can then use this to extract the stacked PC location and the stacked register values. | L3 |

**Course outcomes:** On the completion of this laboratory course, the students will be able to:

- Design and simulate the digital circuits using graphical programming tool LabVIEW.
- Build user friendly interfaces to interact with the digital circuits and to observe the outputs.
- Develop assembly programs for different applications using ARM Cortex M3 and Keil uVision-4 tool.
- Develop C Programs for different applications using ARM-Cortex M3 and Keil uVision-4 tool.

**Conduct of Practical Examination:**

1. All laboratory experiments are to be included for practical examination.
2. For examination, one question each to be set from PART-A and PART-B.
3. Students are allowed to pick one experiment from the lot.
4. Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.
5. Change of experiment is allowed only once and Marks allotted to the procedure part will be made zero.

# M.Tech – DE & E - FOURTH SEMESTER SYLLABUS

| **Synthesis and Optimization of Digital Circuits**<br>[As per Choice Based credit System (CBCS) Scheme<br>SEMESTER – IV | | | |
|---|---|---|---|
| Subject Code | 16ELD41 | IA Marks | 20 |
| Number of Lecture Hours/Week | 04 | Exam marks | 80 |
| Total Number of Lecture Hours | 50<br>(10 Hours per Module) | Exam Hours | 03 |
| CREDITS – 04 | | | |

**Course Objectives:** This course will enable students to:

- Understand the need for optimization and dimensions of optimization for digital circuits.
- Understand basic optimization techniques used in circuits design
- Understand advanced tools and techniques in digital systems design including Hardware Modeling and Compilation Techniques.
- Explain details of Logic-Level synthesis and optimization techniques for combinational and sequential circuits.
- Explain the concept of scheduling and resource binding for optimization.

| **Modules** | **RBT Level** |
|---|---|
| **Module 1** | |
| **Introduction to Synthesis and optimization**: Design of Microelectronics circuits, Computer aided Synthesis and Optimization.<br>**Hardware Modeling**: HDLs for Synthesis, Abstract models, Compilation and Behavioral Optimization.<br>(Text1: Topics from Chap. 1,3) | L1, L2, L3 |
| **Module 2** | |
| **Graph theory for CAD for VLSI**: Graphs, Combinatorial Optimization, Graph Optimization problems and Algorithms, Boolean Algebra and Applications.<br>**Architectural Synthesis and Optimization:** Fundamental Architectural Synthesis problems, Area and Performance Estimation, Strategies for Architectural Optimization, Datapath Synthesis, Control Path Synthesis.(Text1: Topics From Chap. 2,4) | L1, L2, L3 |
| **Module 3** | |
| **Two level Combinational Logic Optimization**: Introduction, Logic Optimizations, Operations on Two level Logic Covers, Algorithms for Logic Minimization, Symbolic Minimization and Encoding Problems.<br>**Multiple Level Combinational Logic Optimization**: Introduction, Models and Transformations for Combinational Networks, The Algebraic Model, The Boolean Model. (Text1: Chap. 7, 8) | L1, L2, L3 |
| **Module 4** | |
| **Sequential Logic Optimization:**<br>Introduction, Sequential Logic Optimization using State based Models, Sequential Logic Optimization using Network Models, | L1, L2, L3 |

| | |
|---|---|
| Implicit FSM Traversal Methods, Testability concerns for Synchronous Circuits. (Text 1: Chap. 9) | |
| **Module 5** | |
| **Scheduling Algorithms**: Introduction, A Model for Scheduling problems, Scheduling with Resource Constraints, Scheduling without Resource Constraints, Scheduling Algorithms for Extended Sequencing Models, Scheduling Pipelined Circuits.<br>**Resource Sharing and Binding:** Sharing and Binding for Resource dominated circuits, Sharing and Binding for General Circuits, Concurrent Binding and Scheduling, Resource sharing and Binding for Non – Scheduled Sequencing Graphs.<br>(Text1: Chap. 5,6) | L1, L2, L3 |

**Course Outcomes:** After studying this course, students will be able to:

- Understand the process of synthesis and optimization in a top down approach for digital circuits models using HDLs.
- Understand the terminologies of graph theory and its algorithms to optimize a Boolean equation.
- Apply different two level and multilevel optimization algorithms for combinational circuits
- Apply the different sequential circuit optimization methods using state models and network models.
- Apply different scheduling algorithms with resource binding and without resource binding for pipelined sequential circuits and extended sequencing models.

**Question paper pattern:**

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

**Text Book:**

Giovanni De Micheli, "Synthesis and Optimization of Digital Circuits", Tata McGraw-Hill, 2003.

**Reference Book:**

Edwars M.D., Automatic Logic synthesis Techniques for Digital Systems, Macmillan New Electronic Series, 1992.

**CMOS RF Circuit Design**

[As per Choice Based credit System (CBCS) Scheme
SEMESTER – IV

| | | | |
|---|---|---|---|
| Subject Code | 16EVE421 | IA Marks | 20 |
| Number of Lecture Hours/Week | 03 | Exam marks | 80 |
| Total Number of Lecture Hours | 40 (8 Hours per Module) | Exam Hours | 03 |

CREDITS – 03

**Course Objectives:** This course will enable students to:

- Learn basic concepts in RF and microwave design emphasizing the effects of nonlinearity and noise.
- Appreciate communication system, multiple access and wireless standards necessary for RF circuit design.
- Deal with transceiver architecture, various receiver and transmitter designs, their merits and demerits.
- Understand the design of RF building blocks such as Low Noise Amplifiers and Mixers.

| **Modules** | **RBT Level** |
|---|---|
| **Module 1** | |
| **Introduction to RF Design and Wireless Technology:**<br>**Basic concepts in RF design(I):** General considerations, Effects of Nonlinearity, Noise, Sensitivity and dynamic range. | L1,L2,L3 |
| **Module 2** | |
| **Basic concepts in RF design (II**): Passive impedance transformation, scattering parameters, analysis of nonlinear dynamic systems | L1,L2,L3 |
| **Module 3** | |
| **Communication Concepts:** General concepts, analog modulation, digital modulation, spectral re-growth, Mobile RF communications, Multiple access techniques, Wireless standards | L1,L2,L3 |
| **Module 4** | |
| **Transceiver Architecture(I):** General considerations, Receiver architecture. | L1,L2,L3 |
| **Module 5** | |
| **Transceiver Architecture(II):** Transmitter architectures<br>**Low Noise Amplifiers:** LNA topologies: common-source stage with inductive load, common-source stage with resistive feedback.<br>**Mixers:** General considerations, passive down conversion mixers. | L1,L2,L3 |

**Course Outcomes:** After studying this course, students will be able to:

- Analyse the effect of nonlinearity and noise in RF and microwave design.
- Exemplify the approaches taken in actual RF products.

- Minimize the number of off-chip components required to design mixers and Low-Noise Amplifiers.
- Explain various receivers and transmitter topologies with their merits and drawbacks.
- Demonstrate how the system requirements define the parameters of the circuits and how the performance of each circuit impacts that of the overall transceiver.

**Question paper pattern:**

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

**Text Book**:

B. Razavi, "**RF Microelectronics**", PHI, second edition.

**Reference Books**:


1. R. Jacob Baker, H.W. Li, D.E. Boyce "**CMOS Circuit Design, layout and Simulation**", PHI 1998.
2. Thomas H. Lee "**Design of CMOS RF Integrated Circuits**" Cambridge University press 1998.
3. Y.P. Tsividis, "**Mixed Analog and Digital Devices and Technology**", TMH 1996

**Advances in Image Processing**

[As per Choice Based credit System (CBCS) Scheme

SEMESTER – IV

| | | | |
|---|---|---|---|
| Subject Code | 16ECS422 | IA Marks | 20 |
| Number of Lecture Hours/Week | 03 | Exam marks | 80 |
| Total Number of Lecture Hours | 40 (8 Hours per Module) | Exam Hours | 03 |

CREDITS – 03

**Course Objectives:** This course will enable students to:

- Acquire fundamental knowledge in understanding the representation of the digital image and its properties
- Equip with some pre-processing techniques required to enhance the image for further analysis purpose.
- Select the region of interest in the image using segmentation techniques.
- Represent the image based on its shape and edge information.
- Describe the objects present in the image based on its properties and structure.

| **Modules** | **RBT Level** |
|---|---|
| **Module 1** | |
| **The image, its representations and properties:** Image representations a few concepts, Image digitization, Digital image properties, Color images. | L1 |
| **Module 2** | |
| **Image Pre-processing:** Pixel brightness transformations, geometric transformations, local pre-processing. | L1, L2 |
| **Module 3** | |
| **Segmentation:** Thresholding; Edge-based segmentation – Edge image thresholding, Edge relaxation, Border tracing, Hough transforms; Region – based segmentation – Region merging, Region splitting, Splitting and merging, Watershed segmentation, Region growing post-processing. | L1, L2, L3 |
| **Module 4** | |
| **Shape representation and description:** Region identification; Contour-based shape representation and description – Chain codes, Simple geometric border representation, Fourier transforms of boundaries, Boundary description using segment sequences, B-spline representation; Region-based shape representation and description – Simple scalar region descriptors, Moments, Convex hull. | L1, L2, L3 |
| **Module 5** | |
| **Mathematical Morphology:** Basic morphological concepts, Four morphological principles, Binary dilation and erosion, Skeletons and object marking, Morphological segmentations and watersheds. | L1, L2, L3 |

**Course Outcomes:** After studying this course, students will be able to:

- Understand the representation of the digital image and its properties

- Apply pre-processing techniques required to enhance the image for its further analysis.
- Use segmentation techniques to select the region of interest in the image for analysis
- Represent the image based on its shape and edge information.
- Describe the objects present in the image based on its properties and structure.
- Use morphological operations to simplify images, and quantify and preserve the main shape characteristics of the objects.

**Question paper pattern:**

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

**Text Book**:

Milan Sonka, Vaclav Hlavac, Roger Boyle, "Image Processing, Analysis, and Machine Vision", Cengage Learning, 2013, ISBN: 978-81-315-1883-0

**Reference Books**:

1. Geoff Doughertry, Digital Image Processing for Medical Applications, Cambridge university Press, 2010
2. S.Jayaraman, S Esakkirajan, T.Veerakumar, Digital Image Processing, Tata McGraw Hill, 2011

**Communication System Design using DSP Algorithms**

[As per Choice Based credit System (CBCS) Scheme

SEMESTER – IV

| | | | | |
|---|---|---|---|---|
| Subject Code | 16ECS423 | IA Marks | | 20 |
| Number of Lecture Hours/Week | 03 | Exam marks | | 80 |
| Total Number of Lecture Hours | 40 (8 Hours per Module) | Exam Hours | | 03 |

CREDITS – 03

**Course Objectives:** This course will enable students to:

- Understand communication systems, including algorithms that are particularly suited to DSP implementation.
- Understand Software and hardware tools, as well as FIR and IIR digital filters and the FFT.
- Discuss modulators and demodulators for classical analog modulation methods such as amplitude modulation (AM), double-sideband suppressed-carrier amplitude modulation (DSBSC-AM), single sideband modulation (SSB), and frequency modulation (FM).
- Explore digital communication methods leading to the implementation of a telephone-line modem.

| Modules | RBT Level |
|---|---|
| **Module 1** | |
| **Introduction to the course**: Digital filters, Discrete time convolution and frequency responses, FIR filters - Using circular buffers to implement FIR filters in C and using DSP hardware, Interfacing C and assembly functions, Linear assembly code and the assembly optimizer. IIR filters - realization and implementation, FFT and power spectrum estimation: DTFT window function, DFT and IDFT, FFT, Using FFT to implement power spectrum. | L1,L2 |
| **Module 2** | |
| **Analog modulation scheme:** Amplitude Modulation - Theory, generation and demodulation of AM, Spectrum of AM signal. Envelope detection and square law detection. Hilbert transform and complex envelope, DSP implementation of amplitude modulation and demodulation.<br>**DSBSC:** Theory generation of DSBSC, Demodulation, and demodulation using coherent detection and Costas loop. Implementation of DSBSC using DSP hardware.<br>**SSB:** Theory, SSB modulators, Coherent demodulator, Frequency translation, Implementation using DSP hardware. (Text 1, 2) | L1,L2 |
| **Module 3** | |
| **Frequency modulation:** Theory, Single tone FM, Narrow band FM, FM bandwidth, FM demodulation, Discrimination and PLL methods, Implementation using DSP hardware.<br>**Digital Modulation scheme:** PRBS, and data scramblers: Generation of PRBS, Self -synchronizing data scramblers, Implementation of PRBS and data scramblers. RS-232C protocol and BER tester: The | L1,L2 |

| | |
|---|---|
| protocol, error rate for binary signaling on the Gaussian noise channels, Three bit error rate tester and implementation. | |
| **Module 4** | |
| **PAM and QAM:** PAM theory, baseband pulse shaping and ISI, Implementation of transmit filter and interpolation filter bank. Simulation and theoretical exercises for PAM, Hardware exercises for PAM.<br>**QAM fundamentals:** Basic QAM transmitter, 2 constellation examples, QAM structures using passband shaping filters, Ideal QAM demodulation, QAM experiment. QAM receivers-Clock recovery and other frontend sub-systems. Equalizers and carrier recovery systems. | L1, L2,L3 |
| **Module 5** | |
| Experiment for QAM receiver frontend. Adaptive equalizer, Phase splitting, Fractionally spaced equalizer. Decision directed carrier tracking, Blind equalization, Complex cross coupled equalizer and carrier tracking experiment.<br>Echo cancellation for full duplex modems: Multicarrier modulation, ADSL architecture, Components of simplified ADSL transmitter, A simplified ADSL receiver, Implementing simple ADSL Transmitter and Receiver. | L1, L2,L3 |

**Course outcomes:** After studying this course, students will be able to:

- Implement DSP algorithms on TI DSP processors
- Implement FIR, IIR digital filtering and FFT methods
- Implement modulators and demodulators for AM,DSBSC-AM,SSB and FM
- Design digital communication methods leading to the implementation of a line communication system.

**Question paper pattern:**

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

**Text Book:**

1. Tretter, Steven A., "**Communication System Design Using DSP Algorithms With Laboratory Experiments for the TMS320C6713™ DSK",** Springer USA*, 2008.*

**Reference Books:**

1. Robert. O. Cristi, "**Modern Digital signal processing",** Cengage Publishers, India, 2003.
2. S. K. Mitra, "**Digital signal processing: A computer based approach",** 3rd edition, TMH, India, 2007.
3. E.C. Ifeachor, and B. W. Jarvis, "**Digital signal processing: A Practitioner's approach",** Second Edition, Pearson Education, India, 2002,
4. Proakis, and Manolakis, "**Digital signal processing**", 3rd edition, Prentice Hall, 1996.

**Reconfigurable Computing**

[As per Choice Based credit System (CBCS) Scheme

SEMESTER – IV

| | | | |
|---|---|---|---|
| Subject Code | 16ELD424 | IA Marks | 20 |
| Number of Lecture Hours/Week | 03 | Exam marks | 80 |
| Total Number of Lecture Hours | 40 (8 Hours per Module) | Exam Hours | 03 |

CREDITS – 03

**Course Objectives:** The aim of this course is to enable the students to

- Acquire fundamental knowledge and understanding of principles and practice in reconfigurable architecture.
- Understand the FPGA design principles, and logic synthesis.
- Integrate hardware and software technologies for reconfiguration computing focusing on partial reconfiguration design.
- Focus on different domains of applications on reconfigurable computing.

| **Modules** | **RBT Level** |
|---|---|
| **Module 1** | |
| **Introduction:** History, Reconfigurable Vs Processor based system, RC Architecture. **Reconfigurable Logic Devices**: Field Programmable Gate Array, Coarse Grained Reconfigurable Arrays. **Reconfigurable Computing System**: Parallel Processing on Reconfigurable Computers, A survey of Reconfigurable Computing System. (Text 1) | LI, L2 |
| **Module 2** | |
| **Languages and Compilation:** Design Cycle, Languages, HDL, High Level Compilation, Low level Design flow, Debugging Reconfigurable Computing Applications. (Text 1) | L1,L2 |
| **Module 3** | |
| **Implementation:** Integration, FPGA Design flow, Logic Synthesis. **High Level Synthesis for Reconfigurable Devices:** Modelling, Temporal Partitioning Algorithms. (Text 2) | L1, L2, L3 |
| **Module 4** | |
| **Partial Reconfiguration Design:** Partial Reconfiguration Design, Bitstream Manipulation with JBits, The modular Design flow, The Early Access Design Flow, Creating Partially Reconfigurable Designs, Partial Reconfiguration using Hansel-C Designs, Platform Design. (Text 2) | L1,L2 |
| **Module 5** | |
| **Signal Processing Applications:** Reconfigurable computing for DSP, DSP application building blocks, Examples: Beamforming, Software Radio, Image and video processing, Local Neighbourhood functions, Convolution. (Text 1)<br>**System on a Programmable Chip:** Introduction to SoPC, Adaptive Multiprocessing on Chip. (Text 2) | L1, L2,L3 |

**Course Outcomes::**After studying this course, students will be able to:

- Synthesize the reconfigurable computing architectures.
- Use the reconfigurable architectures for the design of a digital system.
- Design of digital systems for a variety of applications on signal processing

and system on chip configurations.

**Question paper pattern:**

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

**Text Books**:


1. M. Gokhale and P. Graham, "Reconfigurable Computing: Accelerating Computation with Field-Programmable Gate Arrays", Springer, 2005.
2. C. Bobda, "Introduction to Reconfigurable Computing: Architectures, Algorithms and Applications", Springer, 2007.


**Reference Books**:


1. D. Pellerin and S. Thibault, "Practical FPGA Programming in C", Prentice-Hall, 2005.
2. W. Wolf, "FPGA Based System Design", Prentice-Hall, 2004.
3. R. Cofer and B. Harding, "Rapid System Prototyping with FPGAs: Accelerating the Design Process", Newnes, 2005.