VISVESVARAYA TECHNOLOGICAL UNIVERSITY BELAGAVI

Scheme of Teaching and Examination and Syllabus M.Tech Microelectronics and Control Systems (EMS)

Eligibility: Bachelor's degree in Engineering or Technology in

(a)Electrical and Electronics Engineering (b) Electronics and Communication Engineering

(c) AMIE in appropriate branch

(i) GATE: EE, EC

(Effective from Academic year 2016-17)

I SEMESTER

	Teaching Hours /Week			Examination					
Sl. No	Course Code	Title	Theory	Practical/ Field work/ Assignment	Duration in hours	I.A. Marks	Theory/ Practical Marks	Total Marks	Credits
1	16EEE11	Applied Mathematics	04		03	20	80	100	4
2	16EMS12	Analysis of Linear Systems	04		03	20	80	100	4
3	16EMS13	VLSI Design	04		03	20	80	100	4
4	16EMS14	Embedded Systems	04		03	20	80	100	4
5	16EMS15X	Elective -1	03		03	20	80	100	3
6	16EMSL16	Microelectronics and Control Laboratory - I	-	3	03	20	80	100	2
7	16EMS17	Seminar	-	3	-	100	-	100	1
	T	OTAL	19	06	18	220	480	700	22

Number of credits completed at the end of I semester: 22

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Course Code under 16EMS15X	Title
16EMS151	Nonlinear Systems
16EMS152	Process Control and Instrumentation
16EMS153	Control Systems for HVAC
16EMS154	Nanotechnology for Microelectronics and Optoelectronics

II SEMESTER

			Teaching Hours /Week		Examination				
Sl. No	Course Code	Title	Theory	Practical/ Field work/ Assignment	Duration in hours	I.A. Marks	Theory/ Practical Marks	Total Marks	Credits
1	16EMS21	Industrial Control Technology - 1	04		03	20	80	100	4
2	16EMS22	Optimal Control Theory	04		03	20	80	100	4
3	16EMS23	High Speed VLSI Design	04		03	20	80	100	4
4	16EMS24	CAD Tools For VLSI Design	04		03	20	80	100	4
5	16EMS25X	Elective - 2	03		03	20	80	100	3
6	16EMSL26	Microelectronics and Control Laboratory - II	-	3	03	20	80	100	2
7	16EMS27	Seminar	1	3	-	100	-	100	1
TOTAL		19	06	18	220	480	700	22	

Number of credits completed at the end of II semester: 22+22=44

	4.	4
H)	ective	, - I

Course Code under 16EMS25X	Title
16EMS251	Low Power VLSI Design
16EMS252	Robust Control Theory
16EMS253	Digital System Design with VHDL
16EMS254	Real Time Approach to Process Control

Note: Project Phase-1: 6-week duration shall be carried out between 2nd and 3rd Semester vacation. Candidates in consultation with the guide shall carry out literature survey/ visit industries to finalize the topic of Project.

III SEMESTER

			Teaching l	Hours /Week	Examination				
Sl. No	Course Code	Title	Theory	Practical/ Field work/ Assignment	Duration in hours	I.A. Marks	Theory/ Practical Marks	Total Marks	Credits
1	16EMS31	Seminar / Presentation on Internship (After 8 weeks from the date of commencement)				25		25	20
2	16EMS32	Report on Internship				25	-	25	
3	16EMS33	Evaluation and Viva- Voce of Internship			1	1	75	75	
4	16EMS34	Evaluation of Project phase -1				50		50	1
	TOTAL					100	75	175	21

Number of credits completed at the end of III semester: 22+22+21=65

Note:

Internship of 16 weeks shall be carried out during III semester.

Major part of the Project work shall also be carried out during the III semester in consultation with the Guide/s.

IV SEMESTER

		Teaching Hours /Week		Examination					
Sl. No	Course Code	Title	Theory	Practical/ Field work/ Assignment	Duration in hours	I.A. Marks	Theory/ Practical Marks	Total Marks	Credits
1	16EMS41	Industrial Control Technology - 2	04		03	20	80	100	4
2	16EMS42X	Elective - 3	03		03	20	80	100	3
3	16EMS43	Evaluation of Project phase - 2				50	-	50	3
4	16EMS44	Evaluation of Project and Viva-Voce			03	-1	100 + 100	200	10
	•	TOTAL	07		09	90	360	450	20

Number of credits completed at the end of IV semester: 22+22+21+20=85

Elective -1				
Course Code under 16EMS42X Title				
16EMS421	Industrial Control - Software and Routines			
16EMS422	Digital System Design with FPGA			
16EMS423	Microelectronic Fabrication			
16EMS424	Reset Control Systems			

Note: 1. Project Phase-1: 6-week duration shall be carried out between 2nd and 3rd Semester vacation. Candidates in consultation with the guide shall carry out literature survey/ visit industries to finalize the topic of Project.

- **2. Project Phase-2:** 16-week duration during 4th semester. Evaluation shall be done by the committee comprising of HoD as Chairman, Guide and Senior faculty of the department.
- **3. Project Evaluation**: Evaluation shall be taken up at the end of 4th semester. Project work evaluation and Viva-Voce examination shall conducted

4. Project evaluation:

- a. Internal Examiner shall carry out the evaluation for 100 marks.
- b. External Examiner shall carry out the evaluation for 100 marks.
- c .The average of marks allotted by the internal and external examiner shall be the final marks of the project evaluation.
- d. Viva-Voce examination of Project work shall be conducted jointly by Internal and External examiner for 100 marks.

M.TECH MICROELECTRONICS AND CONTROL SYSTEMS (EMS) CHOICE BASED CREDIT SYSTEM (CBCS) **SEMESTER - I APPLIED MATHAMATICS (Core Course)** Course Code 16EEE11 IA Marks 20 Number of Lecture Hours/Week 04 Exam Hours 03 Total Number of Lecture Hours 50 Exam Marks 80 Credits - 04

Course objectives:

• The objectives of this course is to acquaint the students with principles of advanced mathematics through linear algebra, transform methods for differential equations, calculus of variations and linear and non-linear programming, that serve as an essential tool for applications of electrical engineering sciences. ■

Module-1		Teaching Hours		
	ods: Solution of algebraic and transcendental equations- iterative methods legree equation – Muller method(no derivation), Chebyshev method. Fixed	10		
	ethod (first order), acceleration of convergence- Δ^2 - Aitken's method. near equations – Newton-Raphson method. Complex roots by Bairstow's			
Revised Bloom's L ₂ – Understanding, L ₃ – Applying Taxonomy Level				
Module-2				
equations, parabo Crank-Nicolson n	on of Partial Differential Equations: Classification of second order lic equations-solution of one dimensional heat equation, explicit method, nethod. Hyperbolic equations- solution of one dimensional wave equation and Laplace equation by explicit method.	10		
Revised Bloom's Taxonomy Level L ₃ – Applying				
Module-3				
Linear Algebra: Vector spaces, linear dependent, independence, basis and dimension, elementary properties, examples. Linear Transformations: Definition, properties, range and null space, rank and nullity, algebra of linear transformations-invertible, singular and non-singular transformations, representation of transformations by matrices. ■				
Revised Bloom's Taxonomy Level	L_1 – Remembering, L_2 – Understanding			
Module-4				
System of linear algebraic equations and Eigen value problems: Iterative methods - Gauss-Seidal method, SOR method, Eigen value problems – Gerschgorian circle theorem, Eigen values and Eigen vectors of real symmetric matrices -Jacobi method. Interpolation: Hermite interpolation, spline interpolation, numerical solution of differential equations – Numerov method. ■				
Revised Bloom's Taxonomy Level	L ₃ – Applying			

M.TECH MICROELECTRONICS AND CONTROL SYSTEMS (EMS)					
16EEE11 APPLIED MATHAMATICS (Core Course) (continued)					
CHOICE BASED CREDIT SYSTEM (CBCS)					
Module-5	Teaching				
	Hours				
Optimization : Linear programming- formulation of the problem, general linear	10				
programming problem, simplex method, artificial variable technique, Big M-method.					
Graph Theory: Basic terminologies, types of graphs, sub graphs, graphs isomorphism,					
connected graphs-walks, paths, circuits, connected and disconnected graphs, operations on					
graphs, Eulerian paths and circuits, Hamiltonian paths and circuits, applications to electrical					

Course outcomes:

Taxonomy Level

circuits. ■

Revised Bloom's

At the end of the course the student will be able to:

 L_3 – Applying, L_4 – Analysing.

- 1. Employ numerical techniques in order to achieve more accurate values in the computation of roots of algebraic and non-linear equations.
- 2. Utilize analytical and numerical schemes to solve partial differential equations applicable to engineering problems.
- 3. Understand vector spaces, basis, linear transformations and the process of obtaining matrix of linear transformations arising in magnification and rotation of images.
- 4. Apply standard iterative methods to compute Eigen values and solve ordinary differential equations.
- 5. Employ linear and non-linear programming techniques in simulation of network systems and optimization of electrical circuits.

Graduate Attributes (As per NBA):

Critical Thinking, Problem Solving, Research Skill, Usage of Modern Tools.

Question paper pattern:

- The question paper will have ten questions.
- Each full question is for 16 marks.
- There will be 2 full questions (with a maximum of four sub questions in one full question) from each module.
- Each full question with sub questions will cover the contents under a module.
- Students will have to answer 5 full questions, selecting one full question from each module. ■

Text/Reference Books

1	Linear Algebra and its Applications	David C.Lay et al	Pearson	5th Edition,2015
2	Numerical methods in Engineering and Science (with C, C++ & MATLAB)	B.S.Grewal	Khanna Publishers	2014
3	Graph Theory with Applications to Engineering and Computer Science	Narsingh Deo	PHI	2012
4	Numerical Methods for Scientific and Engineering Computation	M. K. Jain et al	New Age International	9 th Edition, 2014
5	Higher Engineering Mathematics	B.S. Grewal	Khanna Publishers	43 rd Edition,2015
6	Linear Algebra	K.Hoffman et al	PHI	2011

- Web links: 1. http://nptel.ac.in/courses.php?disciplineId=111
 - 2. http://www.class-central.com/Course/math(MOOCs)
 - 3.www.wolfram.com

M.TECH MICROELECTRONICS AND CONTROL SYSTEMS (EMS) **CHOICE BASED CREDIT SYSTEM (CBCS) SEMESTER - I ANALYSIS OF LINEAR SYSTEMS (Core Course)** Course Code 16EMS12 IA Marks 20 Number of Lecture Hours/Week Exam Hours 03 04 Total Number of Lecture Hours 50 Exam Marks 80 Credits - 04 **Course objectives:** To model Continuous and Discrete time system in state space To solve the continuous and discrete time system state space models. To assess the controllability and observability of state space models in the continuous and discrete time Understand the concepts of state feedback techniques. ■

• Understand the concep	ts of state feedback techniques.	
Module-1		Teaching Hours
consistency conditions, State sp variables. Eigen values, Eigen v	n of Continuous Time Systems: Introduction, concepts of state, ace representation using physical variables, phase variables, canonical vectors, state equations for dynamic systems, Non-uniqueness of state grams for continuous time state models. ■	10
Taxonomy Level	mbering, L_2 – Understanding, L_3 – Applying, L_4 – Analyzing.	
Module-2		
and quantization error, Data acq transfer function, State space re for discrete time state models. ■	of Discrete Time Systems: Digital control system, quantizing quisition and conversion, Impulse sampling and data hold, pulse presentation of discrete time systems, State diagrams - state diagrams mbering, L ₂ – Understanding, L ₃ – Applying, L ₄ – Analyzing.	10
Module-3		
time state equations, Solution of of matrix exponential, series eva Cayley- Hamilton technique, Ex	S: Introduction, Existence and Uniqueness of solution to continuous f Linear time invariant continuous time state equations — Evaluation aluation, Evaluation using symmetry transformation, Evaluation using valuation using Inverse Laplace transformation. Solution of Discrete rm approach, Pulse transfer function matrix, Discretization of ations.	10
$\begin{tabular}{ll} \textbf{Revised Bloom's} \\ \textbf{Taxonomy Level} \end{tabular} & L_1-\text{Reme} \\ \end{tabular}$	mbering, L_2 – Understanding, L_3 – Applying, L_4 – Analyzing.	
Module-4		
Controllability, General Concep Systems – Time Invariant Case, Case, Controllability and Obser Controllability and Observability and Observability due to Sampl	ability of Systems: Introduction, General Concept of of Observability, Controllability Tests For Continuous Time Observability Tests For Continuous Time Systems – Time Invariant vability of Discrete Time Systems – Time Invariant Case y of State Model in Jordan Canonical Form. Loss of Controllability ing. ■ mbering, L₂ – Understanding, L₃ – Applying, L₄ – Analyzing.	10
Module-5		
Output Systems, Effect of State i	Controllable and Observable Companion Forms – Single Input /Single feedback on Controllability and Observability, Pole Placement by State ms, Stabilizability, Full Oder Observer, Reduced Order Observer,	10
	mbering, L_2 – Understanding, L_3 – Applying, L_4 – Analysing.	

M.TECH MICROELECTRONICS AND CONTROL SYSTEMS (EMS) 16EMS12 ANALYSIS OF LINEAR SYSTEMS (Core Course) (continued) CHOICE BASED CREDIT SYSTEM (CBCS)

Course outcomes:

At the end of the course the student will be able to:

- Provide a state variable models for Continuous and discrete time systems.
- Solve the State equations to provide a solution and analyze them in both continuous and discrete time domains.
- Assess the controllability and observability of state space models developed.
- Apply the concepts of state feedback techniques in controlling the systems.

Graduate Attributes (As per NBA):

Engineering Knowledge, Problem Analysis, Design / development of solutions, Ethics.

Question paper pattern:

- The question paper will have ten questions.
- Each full question is for 16 marks.
- There will be 2 full questions (with a maximum of four sub questions in one full question) from each module.
- Each full question with sub questions will cover the contents under a module.
- Students will have to answer 5 full questions, selecting one full question from each module.

Text/Reference Books

1	Modern Control System Theory	M Gopal	New Age International	2012 Reprint
2	Discrete Time Control Systems	Ogata K	PHI	2 nd Edition, 2016

M.TECH MICROELECTRONICS AND CONTROL SYSTEMS (EMS) CHOICE BASED CREDIT SYSTEM (CBCS)					
	SEMESTER	- I			
VLSI DESIGN (Core Course)					
Course Code	Course Code 16EMS13 IA Marks 20				
Number of Lecture Hours/Week	Number of Lecture Hours/Week 04 Exam Hours 03				
Total Number of Lecture Hours 50 Exam Marks 80					
	Credits - 04	1			

- To study in detail the basic processing details and the characteristics of MOS transistors.
- To discuss techniques to optimize combinational circuits for lower delay, alternate CMOS logic configurations or circuit families.
- To discuss sequential circuits and designing of bot static and dynamic sequential circuits.
- To design and analyze CMOS power and differential amplifiers.
- To Design and analyze the current mirrors as both bias elements and signal processing components and CMOS Op Amps. ■

CMOS OF	o Amps. ■	
Module-1		Teaching Hours
MOS Transistor T	Theory: MOS Transistors, CMOS Fabrication and Layout, Long – Channel I-V	10
	V Characteristics, Non-ideal I-V Effects, DC Transfer Characteristics, Pitfalls and	
Fallacies.		
CMOS Processing	Technology: Introduction, CMOS Technologies, Layout Design Rules, CMOS	
Process Enhanceme		
Revised Bloom's	L_1 – Remembering, L_2 – Understanding.	
Taxonomy Level	. 6, 2	
Module-2		
Combinational Ci	rcuit Design: Introduction, Circuit Families, Circuit Pitfalls, More Circuit	10
Families, Silicon-o	n-Insulator Circuit Design, Subthreshold Design, Pitfalls and Fallacies, Historical	
Perspective. ■		
Revised Bloom's	L_1 – Remembering, L_2 – Understanding, L_3 – Applying, L_4 – Analysing.	
Taxonomy Level	L ₁ = Remembering, L ₂ = Onderstanding, L ₃ = Applying, L ₄ = Analysing.	
Module-3		
	Design: Introduction, Sequencing Static Circuits, Circuit Design of Latches and	10
	equencing Element Methodology, Sequencing Dynamic Circuits, Synchronizers,	10
Wave Pipelining, Pitfalls and Fallacies, Case study ■		
Revised Bloom's	L_1 – Remembering, L_2 – Understanding, L_3 – Applying, L_4 – Analysing.	
Taxonomy Level		
Module-4		
	lifiers: Basic Concepts, Common – Source Stage, Source Follower, Common –	10
	le Stage, Choice of Device Models.	
	ifiers: Single – Ended and Differential Operations, Basic Differential Pair,	
Common – Mode F	Response, Differential Pair with MOS Loads, Gilbert Cell. ■	
Revised Bloom's	L_1 – Remembering, L_2 – Understanding, L_3 – Applying, L_4 – Analysing.	
Taxonomy Level		
Module-5		•
Passive and Active	e Current Mirrors: Basic Current Mirrors, Cascode Current Mirrors, Active	10
Current Mirrors.	,	
	lifiers: General Considerations, One – Stage Op Amps, Two – Stage Op Amps,	
	mparison, Common – Mode Feedback, Input Range Limitations, Slew Rate, Power	
	Noise in Op Amps. ■	
Revised Bloom's	L_1 - Remembering, L_2 - Understanding, L_3 - Applying, L_4 - Analysing.	
Taxonomy Level		
<u>-</u>	1	1

M.TECH MICROELECTRONICS AND CONTROL SYSTEMS (EMS) 16EMS13 VLSI DESIGN (Core Course) (continued) CHOICE BASED CREDIT SYSTEM (CBCS)

Course outcomes:

At the end of the course the student will be able to:

- Explain in detail the basic processing details and the characteristics of MOS transistors.
- Optimize combinational circuits for lower delay, discuss alternate CMOS circuit families.
- Design both static and dynamic sequential circuits.
- Design and analyze CMOS power and differential amplifiers.
- Design and analyze the current mirrors as both bias elements and signal processing components and CMOS Op Amps.

Graduate Attributes (As per NBA):

Engineering Knowledge, Problem Analysis, Design / development of solutions.

Question paper pattern:

- The question paper will have ten questions.
- Each full question is for 16 marks.
- There will be 2 full questions (with a maximum of four sub questions in one full question) from each module.
- Each full question with sub questions will cover the contents under a module.
- Students will have to answer 5 full questions, selecting one full question from each module. ■

Text/Reference Books

1	CMOS VLSI Design: A Circuits and Systems Perspective	Neil H. E. Weste, David Money Harris	Pearson	4 th Edition, 2015
2	Design of Analog CMOS Integrated Circuits	Behzad Razavi	Mc Graw Hill	31st Reprint, 2015

M.TECH MICROELECTRONICS AND CONTROL SYSTEMS (EMS) CHOICE BASED CREDIT SYSTEM (CBCS) SEMESTER - I					
EMBEDDED SYSTEMS (Core Course)					
Course Code	Course Code 16EMS14 IA Marks 20				
Number of Lecture Hours/Week	Number of Lecture Hours/Week 04 Exam Hours 03				
Total Number of Lecture Hours 50 Exam Marks 80					
·	Credits - 04	1			

- To impart knowledge of embedded systems with suitable examples, explanation of process, classification of embedded systems.
- To explain the processor architecture, memory organization, communication with processor and interrupt services.
- To explain the program modeling concepts, inter-process communication and synchronization of processes. ■

processes. ■		
Module-1		Teaching Hours
Embedded Hardwa Embedded Systems Complex Systems System Design, De	Imbedded Systems: Embedded Systems, Processor Embedded into a System, re Units and Devices in a System, Embedded Software in a System, Examples of Embedded Systems − on −chip (Soc) and Use of VLSI Circuit Design Technology, Design and Processors, Design of Process in Embedded System, Formulation of esign Process and Design Examples, Classification of Embedded Systems, Skill pedded System Designer. ■	10
Revised Bloom's Taxonomy Level	L_1 – Remembering, L_2 – Understanding.	
Module-2		
Introduction to Adv	eture and Memory Organisation: 8051 Architecture, Real world Interfacing, ranced Architecture, Processor and Memory Organization, Instruction Level mance Metrics, Memory − Types, Memory − Maps and Addresses, Processor Selection. ■ L ₁ − Remembering, L ₂ − Understanding.	10
Taxonomy Level		
Module-3		T
Communication De Wireless Devices, T Embedded Systems PCI –X and Advand Device Drivers and	d Interrupts Service Mechanisms: Programmed – I/O Busy – wait Approach ervice Mechanism, ISR Concept, Interrupt Sources, Interrupt Servicing	10
Revised Bloom's Taxonomy Level	L_1 – Remembering, L_2 – Understanding	
Module-4		
Models for Event – Modelling. Interprocess Comp Processes in an App Clear – cut Distenti Semaphores, Shared	g concepts: Program Models, DFG Models, State Machine Programming controlled Program Flow, Modelling of Multiprocessor Systems, UML munication and Synchronization of Processes, Threads and Tasks: Multiple plication, Multiple Threads in an Application, Tasks, Task Status, Task and Data, on Between Functions, ISRS and Tasks by their Characteristics, Concept of d Data, Interprocess Communication, Signal Function, Semaphore Functions, and Data, Interprocess Communication, Signal Function, Semaphore Functions, Mailbox Functions, Pipe Functions, Socket Functions, RPC Functions. ■ L₁ − Remembering, L₂ − Understanding.	10

M.TECH MICROELECTRONICS AND CONTROL SYSTEMS (EMS) 16EMS14 EMBEDDED SYSTEMS (Core Course) (continued) CHOICE BASED CREDIT SYSTEM (CBCS) Module-5 Real - Time Operating Systems: OS Services, Process Management, Timer Functions, Event Functions, Memory management, Device, File and IO Subsystems Management, Interrupt Routines in RTOS Environment and Handling of Interrupt Source Calls, Real – time Operating Systems, Basic Design Using an RTOS, Rtos Task Scheduling Models, Interrupt Latency and Response of the task

Revised Bloom's Taxonomy Level L_1 – Remembering, L_2 – Understanding.

Course outcomes:

At the end of the course the student will be able to:

as performance Metrics, OS Security Issues.

- Describe embedded system, recognize the classification of embedded systems and design process in embedded system.
- Describe processor architecture and memory organization.
- Communicate with processor using serial and parallel devices with the processor and explain interrupt services mechanism.■

Graduate Attributes (As per NBA):

Engineering Knowledge, Problem analysis.

Question paper pattern:

- The question paper will have ten questions.
- Each full question is for 16 marks.
- There will be 2 full questions (with a maximum of four sub questions in one full question) from each module.
- Each full question with sub questions will cover the contents under a module.
- Students will have to answer 5 full questions, selecting one full question from each module. ■

Text Book 1 Embedded Systems: Architecture, Programming and Design Raj Kamal Mc Graw Hill 2nd Edition,2014

	E BASED CREDIT		
NONL	SEMESTER INEAR SYSTEMS		
Course Code	16EMS151		20
Number of Lecture Hours/Week	03		03
Total Number of Lecture Hours	40	Exam Marks	80
	Credits - 0	3	
 Understand the concepts of Phas Understand the concepts of Lyap Understand the Describing func 	ounov stability techni	-	
Module-1			Teaching Hours
-Amplitude dependence, Jump resonance Cycles, Asynchronous quenching. Comm methods of analysis of nonlinear systems nonlinear system. ■ Revised Bloom's L₁ - Remembering, Taxonomy Level Module-2	on Physical Non-line Definition of describ	earities, Classification of nonlinearities,	
Describing Function Method: Introduct function for functions like $x2$, $x3$, $ x x$ and			08
hysteresis, backlash and a combination of enclosure, stable and unstable limit cycle existence of limit cycle and calculation of	f these, Analysis of no s, Review of polar plo f magnitude and frequ	onlinear systems – Concept of ot and Nichols Plot, Evaluation of uency of oscillation. ■	
hysteresis, backlash and a combination of enclosure, stable and unstable limit cycle existence of limit cycle and calculation of	f these, Analysis of no s, Review of polar plo f magnitude and frequ	onlinear systems – Concept of ot and Nichols Plot, Evaluation of	
hysteresis, backlash and a combination of enclosure, stable and unstable limit cycle existence of limit cycle and calculation of Revised Bloom's $ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	f these, Analysis of noise, Review of polar plots, Review and frequency L_2 – Understanding,	onlinear systems – Concept of ot and Nichols Plot, Evaluation of uency of oscillation. ■ L ₃ – Applying, L ₄ – Analysing.	
hysteresis, backlash and a combination of enclosure, stable and unstable limit cycle existence of limit cycle and calculation of $\mathbf{Revised\ Bloom's}$ $\mathbf{L}_1 - \mathbf{Remembering}$,	f these, Analysis of nos, Review of polar plof f magnitude and frequency L ₂ – Understanding, hase plane and phase nalysis of nonlinear sy	onlinear systems – Concept of ot and Nichols Plot, Evaluation of uency of oscillation. ■ L ₃ – Applying, L ₄ – Analysing. trajectory, Singular points –evaluation, ystem using phase trajectories, Limit	08
hysteresis, backlash and a combination of enclosure, stable and unstable limit cycle existence of limit cycle and calculation of the existence of limit cycle and calculation of limit cycle and calculatio	f these, Analysis of no s, Review of polar plo f magnitude and frequency L ₂ – Understanding, hase plane and phase nalysis of nonlinear syphase trajectories - A	onlinear systems – Concept of ot and Nichols Plot, Evaluation of uency of oscillation. ■ L ₃ – Applying, L ₄ – Analysing. trajectory, Singular points –evaluation, ystem using phase trajectories, Limit	08

Lyapunov Stability: Stability Definitions, Some Preliminaries, Lyapunov's Direct Method, Stability of Linear Systems, Lyapunov's Linearization Method, The Lur'e Problem, Krasovskii;s method of stability assessment, Variable gradient method of stability assessment. Stability assessment of discrete time systems. ■

Module-5

Stability Assessment in the Frequency Domain: Circle criteria and its application, Popov's method. Sliding mode control: Introduction An overview of classical sliding mode control, introductory example, Dynamics in sliding mode − Linear Systems, Nonlinear Systems, Chattering Problems, Reachability Condition, Applications of Sliding mode control. ■

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M.TECH MICROELECTRONICS AND CONTROL SYSTEMS (EMS) 16EMS151 NONLINEAR SYSTEMS (Elective Course) (continued) CHOICE BASED CREDIT SYSTEM (CBCS)

Course outcomes:

At the end of the course the student will be able to:

- Identify the nonlinearity present in a system and explain the behavior of nonlinear system.
- Evaluate the describing function for the nonlinearity present in the system and assess the performance of the system using it.
- Analyze the nonlinear system using the Phase Plane Analysis.
- Define the stability of a system and assess the stability using Lyapunov Stability method.
- Assess the stability of nonlinear system using circle criterion and Popov's stability criterion and apply sliding mode control to the linear and nonlinear systems. ■

Graduate Attributes (As per NBA):

Engineering Knowledge, Problem Analysis, Design / development of solutions, Ethics.

Question paper pattern:

- The question paper will have ten questions.
- Each full question is for 16 marks.
- There will be 2 full questions (with a maximum of four sub questions in one full question) from each module.
- Each full question with sub questions will cover the contents under a module.

Students will have to answer 5 full questions, selecting one full question from each module.

Text/Reference Books

1	Advanced Control Theory	A.NagoorKani	RBA Publications	2 nd Edition, 2009
2.	Nonlinear Systems Analysis	M. Vidyasagar	PHI	2 nd Edition. 2002
3	Non Linear Systems	H. K. Khalil	Pearson	2015
4.	Sliding Mode Control in Engineering	Wilfrid Perruquetti & Jean Pierre Barbot	Marcel Dekker	2002

M.TECH MICROELECTRONICS AND CONTROL SYSTEMS (EMS) CHOICE BASED CREDIT SYSTEM (CBCS)					
	SEMESTER - I				
PROCESS CONTROL AND INSTRUMENTATION (Elective Course)					
Course Code 16EMS152 IA Marks 20					
Number of Lecture Hours/Week	Number of Lecture Hours/Week 03 Exam Hours 03				
Total Number of Lecture Hours 40 Exam Marks 80					
	Credits - 03	3			

- To introduce the concepts of process control, the elements in the building blocks, the units for physical measurements, the use of basic electrical and analog electronic circuits
- To provide digital concepts to their applications, measurement of pressure and level in process control.
- To discuss the instruments and sensors for measurement of flow of fluids, temperature and heat, position, force and light.
- To discuss Humidity measuring devices, regulators, valves, motors and the use of PLC for sequential logic control and continuous control.
- To discuss various methods of analog and digital signal conditioning, process control, the terminology used, and the various methods of implementation of the controller functions and the documentation for alarm and trip systems. ■

Module-1		Teaching Hours
Control Loop, Instr Process Facility Co Units and Standar Standards. Basic Electrical Co	ocess Control: Introduction, Process Control, Definition of the Elements in a umentation and Sensors, Control System Evaluation, Analog and Digital Data, nsiderations. ds: Introduction, Basic Units, Units Derived from Base Units, Standard Prefixes, omponents: Introduction, Circuits with R, L, and C, RC Filters, Bridge Circuits. s: Introduction, Analog Circuits, Types of Amplifiers, Amplifier Applications.	08
Revised Bloom's Taxonomy Level	L_1 – Remembering, L_2 – Understanding.	
Module-2		-
Basic Processor. Microelectromech Devices, Microelec Pressure: Introduct	anical Devices and Smart Sensors: Introduction, Basic Sensors, Piezoelectric tromechanical Devices, Smart Sensors Introduction. tion, Pressure Measurement, Measuring Instruments, Application Considerations. Level Measurement, Application Considerations. ■	08
Revised Bloom's Taxonomy Level	L_1 – Remembering, L_2 – Understanding.	
Module-3		· ·
Temperature and Application Consid	Fluid Flow, Flow Measuring Instruments, Application Considerations. Heat: Introduction, Temperature and Heat, Temperature Measuring Devices, erations. Id Light: Introduction, Position and Motion Sensing, Force, Torque, and Load	08
Cells, Light. ■		
	L_1 – Remembering, L_2 – Understanding.	
Cells, Light. Revised Bloom's	L_1 – Remembering, L_2 – Understanding.	

M.TECH MICROELECTRONICS AND CONTROL SYSTEMS (EMS) 16EMS152 PROCESS CONTROL AND INSTRUMENTATION (Elective Course) (continued) CHOICE BASED CREDIT SYSTEM (CBCS)

Module-4 (cont	inued)	Teaching Hours
_	gic Controllers: Introduction, Programmable Controller System, Controller	
Operation, Input/ou	tput Modules, Ladder Diagrams. ■	
Revised Bloom's Taxonomy Level	L_1 – Remembering, L_2 – Understanding.	
Module-5		
Considerations for S Analog Transmission Process Control: I Process Control Tu Documentation and	ng and Transmission: Introduction, General Sensor Conditioning, Conditioning Specific Types of Devices, Digital Conditioning, Pneumatic Transmission, on, Digital Transmission, Wireless Transmission. Introduction, Sequential Control, Discontinuous Control, Continuous Control, ning, Implementation of Control Loops. d P&ID: Introduction, Alarm and Trip Systems, PLC Documentation, Pipe and mbols, P&ID Drawings. ■	08
Revised Bloom's Taxonomy Level	L_1 – Remembering, L_2 – Understanding, L_4 – Analysing.	

Course outcomes:

At the end of the course the student will be able to:

- Explain the concepts of process control, the elements in the building blocks, the units for physical measurements, the use of basic electrical and analog electronic circuits.
- Explain the use of digital concepts to their applications, measurement of pressure and level in process control.
- Explain the use of instruments and sensors for measurement of flow of fluids, temperature and heat, position, force and light.
- Explain use of Humidity measuring devices, regulators, valves, motors and the use of PLC for sequential logic control and continuous control.
- Discuss various methods of analog and digital signal conditioning, process control, the terminology
 used, and the various methods of implementation of the controller functions and the documentation for
 alarm and trip systems. ■

Graduate Attributes (As per NBA):

Engineering Knowledge, Problem analysis.

Question paper pattern:

- The question paper will have ten questions.
- Each full question is for 16 marks.
- There will be 2 full questions (with a maximum of four sub questions in one full question) from each module.
- Each full question with sub questions will cover the contents under a module.

Students will have to answer 5 full questions, selecting one full question from each module.

Text Book

1	Introduction to Instrumentation, Sensors, and Process Control	William C. Dunn	Artech House	2006

M.TECH MICROELECTRONICS AND CONTROL SYSTEMS (EMS) CHOICE BASED CREDIT SYSTEM (CBCS) SEMESTER - I					
CONTROL SYSTEMS FOR HVAC (Elective Course)					
Course Code 16EMS153 IA Marks 20					
Number of Lecture Hours/Week	03	Exam Hours	03		
Total Number of Lecture Hours	40	Exam Marks	80		
	Credits - 03				

- To discuss the elements of a control system, the basic types of control action, and the energy sources commonly used for controls and various types of control elements.
- To discuss formation of combinations control elements used for control of HVAC.
- To discuss formation and analysis of complete control system
- To provide better idea of the electrical problems inherent in the design of control diagrams, stability of and the digital control of HVAC control systems.
- To use Psychrometric chart to control design to study central plant pumping and distribution systems

	ychrometric chart to control design, to study central plant pumping and distribution	systems,
	VAC systems and the tuning of HVAC control loops. ■	T 1.*
Module-1		Teaching Hours
	nd Terminology: Introduction, Elementary Control System, Purposes of Control,	08
	rgy Sources for Control, Systems, Measurement, Symbols and Abbreviations,	
Psychrometrics, Re		
	l Devices: Introduction, Pneumatic Control Devices, Control Cabinets, Air	
Supply.		
	ronic Control: Devices, Electric Control Devices, Electronic Control Devices.	
Revised Bloom's Taxonomy Level	L_1 – Remembering, L_2 – Understanding, L_4 – Analysing.	
Module-2		•
Amplifiers, Radial . Flow Control Devi	evices: Introduction, Wall Attachment Devices, Turbulence Amplifiers, Vortex Jet Amplifier, Fluidic Transducers, Manual Switches. ices: Dampers, Steam and Water Flow, Control Valves. ol Systems: Introduction, Outside Air Controls, Air Stratification, Heating,	08
Cooling Coils, Hun	nidity Control, Dehumidifiers, Static Pressure Control, Electric Heat, Gas-Fired	
Heaters, Oil-Fired I	Heaters, Refrigeration Equipment, Fire and Smoke Control, Electrical Interlocks,	
Location of Sensors	S. ■	
Revised Bloom's	L_1 – Remembering, L_2 – Understanding, L_4 – Analysing.	
Taxonomy Level		
Module-3		
Dual-Duct Systems Induction Systems,	Systems: Introduction, Single-Zone Systems, Multizone Air Handling Systems, Variable-Volume Systems, Reheat Systems, Heat Reclaim, Fan-Coil Units, Unit Ventilators, Packaged Equipment, Other Packaged Equipment, Radiant g, Radiators and Convectors, Heat Exchangers, Solar Heating and Cooling	08
Revised Bloom's Taxonomy Level	L_1 – Remembering, L_2 – Understanding, L_4 – Analysing.	
Module-4		
Electrical Control of Electric Heaters, Re Special Control: In Environment, Roon Digital and Superv Systems, Computer	ystems: Introduction, Electric Control Diagrams, Electrical Control of a Chiller, of an Air Handling Unit, Example: A Typical Small Air- Conditioning System, educed-Voltage Starters, Multispeed Starters, Variable Speed Controllers. Introduction, Close Temperature and/or Humidity Control, Controlled ins for Testing. visory Control Systems: Introduction, Hard-Wired Systems, Multiplexing e-Based Systems for Monitoring and Control, Benefits of the Computer System, enance and Operation. ■ L₁ − Remembering, L₂ − Understanding, L₄ − Analysing.	08

M.TECH MICROELECTRONICS AND CONTROL SYSTEMS (EMS)	
16EMS153 CONTROL SYSTEMS FOR HVAC (Elective Course) (continued)	
CHOICE BASED CREDIT SYSTEM (CBCS)	
Module-5	Teaching
	Hours
Psychrometrics: Introduction, Psychrometric Properties, Psychrometric Tables, Psychrometric	08
Charts, Processes on the Psychrometric Chart, HVAC Cycles on the Chart, Impossible Processes,	
Effects of Altitude.	
Central Plant Pumping and Distribution Systems: Introduction, Diversity, Constant Flow	
Systems, Variable Flow Systems, Distribution Systems, Building Interfaces.	
Retrofit of Existing Control Systems: Introduction, Economic Analysis, Discriminators, Control	
Modes, Economy Cycle Controls, Single-Zone systems, Reheat Systems, Multizone Systems, Dual-	
Duct Systems, Systems with Humidity Control, Control Valves and Pumping Arrangements.	
Dynamic Response And Tuning: Introduction, Dynamic Response, Tuning HVAC Control Loops.	
Revised Bloom's L_1 – Remembering, L_2 – Understanding, L_4 – Analysing.	

Course outcomes:

Taxonomy Level

At the end of the course the student will be able to:

- Discuss the elements of a control system, the basic types of control action, and the energy sources used for controls and various types of control elements.
- Discuss formation of combinations control elements used for control of HVAC.
- Discuss formation and analysis of complete control system for specific application.
- Explain and solve the electrical problems inherent in the design of control diagrams, stability of and the digital control of HVAC control systems.
- Use Psychrometric chart to control design, to study central plant pumping and distribution systems, existing HVAC systems and the tuning of HVAC control loops. ■

Graduate Attributes (As per NBA):

Engineering Knowledge, Problem analysis.

Question paper pattern:

- The question paper will have ten questions.
- Each full question is for 16 marks.
- There will be 2 full questions (with a maximum of four sub questions in one full question) from each module.
- Each full question with sub questions will cover the contents under a module.

Students will have to answer 5 full questions, selecting one full question from each module.

Text Book					
1	Control Systems For Heating, Ventilating, and Air Conditioning	Roger W. Haines	Springer	6 th Edition, 2006	

M.TECH MICROELECTRONICS AND CONTROL SYSTEMS (EMS) CHOICE BASED CREDIT SYSTEM (CBCS)						
	SEMESTER - I					
NANOTECHNOLOGY FOR MICROELECTRONICS AND OPTOELECTRONICS (Elective Course)						
Course Code 16EMS154 IA Marks 20						
Number of Lecture Hours/Week	03	Exam Hours	03			
Total Number of Lecture Hours	40	Exam Marks	80			
	Credits - 03					

- To review the present trends in microelectronic and optoelectronic devices, solid state and semiconductor physics and define nanostructures.
- To explain the behavior of electrons in nanostructures and the transport and optical properties of nanostructures.
- To study the transport properties of electrons in magnetic field and integral and fractional quantum Hall effect.
- To study advanced semiconductor devices based on nanostructures and advanced optoelectronic and photonic devices based on quantum heterostructures. ■

		Teaching Hours
Characteristic leng wires, and dots, De transport. Survey of Solid S solid. Density of sta electrons in bands,	es and Nanotechnologies: Trends in nanoelectronics and Optoelectronics, this in mesoscopic systems, Quantum mechanical coherence, Quantum wells, insity of states and dimensionality, Semiconductor heterostructures, Quantum state Physics: Introduction, review of quantum mechanics, free electron model of a fates function, Bloch theorem, Electrons in crystalline solids, Dynamics of Lattice vibrations, Phonons.	08
Revised Bloom's Taxonomy Level	L_1 – Remembering, L_2 – Understanding.	
Module-2		
and extrinsic semico transport in semico The Physics of Lo dimensional semico triangular quantum	nductor Physics: Introduction, Energy bands in typical semiconductors, Intrinsic onductors, Electron and hole concentrations in semiconductors, Elementary inductors, Degenerate semiconductors, Optical properties of semiconductors. w-Dimensional Semiconductors: Introduction, Basic properties of two-onductor nanostructures, Square quantum well of finite depth, Parabolic and wells, Quantum wires, Quantum dots, Strained layers, Effect of strain on valence are in quantum wells, Excitonic effects in quantum. ■	08
Revised Bloom's Taxonomy Level	L_1 – Remembering, L_2 – Understanding.	
Taxonomy Level		
Module-3		
Module-3 Semiconductor Quaterojunctions, Quantum	nantum Nanostructures and Superlattices: Introduction, MOSFET structures, uantum wells, Superlattices. nsport in Nanostructures: Introduction, Parallel transport, Perpendicular transport in nanostructures. ■	08
Module-3 Semiconductor Qu Heterojunctions, Q Electric Field Tra	uantum wells, Superlattices. nsport in Nanostructures: Introduction, Parallel transport, Perpendicular	08
Module-3 Semiconductor Quaterojunctions, Quantum Control Trainsport, Quantum Revised Bloom's	uantum wells, Superlattices. nsport in Nanostructures: Introduction, Parallel transport, Perpendicular transport in nanostructures. ■	08

M.TECH MICROELECTRONICS AND CONTROL SYSTEMS (EMS) 16EMS154 NANOTECHNOLOGY FOR MICROELECTRONICS AND OPTOELECTRONICS (Elective Course) (continued) CHOICE BASED CREDIT SYSTEM (CBCS)

Module-4 (continued)	Teaching Hours	
Optical and Electro-optical Processes in Quantum Heterostructures: Introduction, Optical properties of quantum wells and superlattices, Optical properties of quantum dots and		
nanocrystals, Electro-optical effects in quantum wells. Quantum confined Stark Effect, Electro-optical effects in superlattices. Stark ladders and Bloch Oscillations. ■		
Revised Bloom's L_1 – Remembering, L_2 – Understanding.	-	
Module-5		
Electronic Devices Based on Nanostructures: Introduction, MODFETs, Heterojunction bipolar transistors, Resonant tunnel effect, Hot electron transistors, Resonant tunneling transistor, Single electron transistor.	08	
Optoelectronic Devices Based on Nanostructures: Introduction, Heterostructure semiconductor lasers, Quantum well semiconductor lasers, Vertical cavity surface emitting lasers (VCSELs),		
Strained quantum well lasers, Quantum dot lasers, Quantum well and superlattice photodetectors, Quantum well modulators. ■		
Revised Bloom's L_1 – Remembering, L_2 – Understanding.		

Course outcomes:

At the end of the course the student will be able to:

- Explain the present trends in microelectronic and optoelectronic devices, solid state and semiconductor physics and define nanostructures.
- Explain behavior of electrons in nanostructures and the transport and optical properties of nanostructures.
- Discuss the transport properties of electrons in magnetic field and integral and fractional quantum Hall effect.
- Discuss advanced semiconductor devices based on nanostructures and advanced optoelectronic and photonic devices based on quantum heterostructures. ■

Graduate Attributes (As per NBA):

Engineering Knowledge, Problem analysis.

Question paper pattern:

- The question paper will have ten questions.
- Each full question is for 16 marks.
- There will be 2 full questions (with a maximum of four sub questions in one full question) from each module.
- Each full question with sub questions will cover the contents under a module.

Students will have to answer 5 full questions, selecting one full question from each module.

1 Nanotechnology for Microelectronics J.M. Martínez-Duart, R.J. Martín- Elsevier 2006 and Optoelectronics Palma, F. Agulló-Rueda	Text	Text Book					
	1			Elsevier	2006		

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M.TECH MICROELECTRONICS AND CONTROL SYSTEMS (EMS) CHOICE BASED CREDIT SYSTEM (CBCS)				
SEMESTER - I				
MICROELECTRONICS AND CONTROL LABORATORY - I				
Course Code	16EMSL16	IA Marks	20	
Number of Practical Hours/Week	03	Exam Hours	03	
Total Number of Practical Hours	40	Exam Marks	80	

Credits - 02

Course objectives:

- Simulation of a second order system to study the output and perform state estimation by pole placement method in MATLAB/Scilab.
- To analyze the stability of the systems in time and frequency domains using MATLAB/Scilab.
- To Design and verification of the frequency response of different compensators.
- To evaluate the performance of different controllers in enhancing the system performance.
- To verify the sampling theorem, design and analyze the FIR filters.
- To impart knowledge on FIS toolbox for control system applications.

Sl.		Experiments			
NO		-			
1	Simulation o	f a typical second order system.			
2	Study of syst	tem stability by using root locus, Bode plot and Nyquist plot.			
3	Frequency re	esponse of lag, lead and lag-lead network.			
4	Performance characteristics of P, PI, PID controller.				
5	DC and AC Servo motor characteristic s.				
6	Verification of Sampling Theorem.				
7	Design and verification of FIR filter.				
8	State estimation using Pole placement method.				
9	Study of MALAB FIS Tool box.				
10	Control system application using FIS Tool box.				
Revis	ed Bloom's	L_1 – Remembering, L_2 – Understanding, L_3 – Applying, L_4 – Analysing, L_5 – Evaluating.			
Taxor	Taxonomy Level				

Course outcomes:

At the end of the course the student will be able to:

- At the end of the course the student will be able to:
- Use MATLAB/Scilab to simulate a second order system to study the output and perform state estimation by pole placement method.
- Analyze the stability of the systems in time and frequency domains
- Design and verify the frequency response of different compensators.
- Evaluate the performance of different controllers in enhancing the system performance
- Verify the sampling theorem, design and analyze the FIR filter
- Gain knowledge on FIS toolbox for control system applications.

Graduate Attributes (As per NBA):

Engineering Knowledge, Problem Analysis, Conduct investigations of complex Problems, Modern Tool Usage, Individual and Team work, Communication.

M.TECH MICROELECTRONICS AND CONTROL SYSTEMS (EMS) CHOICE BASED CREDIT SYSTEM (CBCS) SEMESTER - I SEMINAR

SEMINAR				
Course Code	16EMS17	IA Marks	100	
No. of Lecture Hours/Week		Exam Hours		
Number of contact Hours/week	03	Number of Tutorial Hours/week		
Total No. of contact Hours		Exam Marks		

Credits - 01

The objective of the seminar is to inculcate self-learning, face audience confidently, enhance communication skill, involve in group discussion and present and exchange ideas.

Each student, under the guidance of a Faculty, is required to

- Choose, preferably, a recent topic of his/her interest relevant to the Course of Specialization.
- Carryout literature survey, organize the Course topics in a systematic order.
- Prepare the report with own sentences.
- Type the matter to acquaint with the use of Micro-soft equation and drawing tools or any such facilities.
- Present the seminar topic orally and/or through power point slides.
- Answer the queries and involve in debate/discussion.
- Submit two copies of the typed report with a list of references.

The participants shall take part in discussion to foster friendly and stimulating environment in which the students are motivated to reach high standards and become self-confident.

The Internal Assessment marks for the seminar shall be awarded (based on the relevance of the topic, presentation skill, participation in the question and answer session and quality of report) by the committee constituted for the purpose by the Head of the Department. The committee shall consist of three faculties from the department with the senior most acting as the Chairman. ■

Marks distribution for internal assessment of the course 16EMS17 seminar:

Seminar Report: 30 marks Presentation skill:50 marks Question and Answer:20 marks

Graduate Attributes (As per NBA):

Engineering Knowledge, Problem Analysis, Design / development of solutions, Conduct investigations of complex Problems, Modern Tool Usage, Engineers and society, Environment and sustainability, Ethics, Individual and Team work, Communication.

II SEMESTER

			Teaching Hours /Week			Examination			
Sl. No	Course Code	Title	Theory	Practical/ Field work/ Assignment	Duration in hours	I.A. Marks	Theory/ Practical Marks	Total Marks	Credits
1	16EMS21	Industrial Control Technology - 1	04		03	20	80	100	4
2	16EMS22	Optimal Control Theory	04		03	20	80	100	4
3	16EMS23	High Speed VLSI Design	04		03	20	80	100	4
4	16EMS24	CAD Tools For VLSI Design	04		03	20	80	100	4
5	16EMS25X	Elective - 2	03		03	20	80	100	3
6	16EMSL26	Microelectronics and Control Laboratory - II	-	3	03	20	80	100	2
7	16EMS27	Seminar	ı	3	-	100	-	100	1
	T	OTAL	19	06	18	220	480	700	22

Number of credits completed at the end of II semester: 22+22=44

Elective -1

Course Code under 16EMS25X	Title
16EMS251	Low Power VLSI Design
16EMS252	Robust Control Theory
16EMS253	Digital System Design with VHDL
16EMS254	Real Time Approach to Process Control

Note: Project Phase-1: 6-week duration shall be carried out between 2nd and 3rd Semester vacation. Candidates in consultation with the guide shall carry out literature survey/ visit industries to finalize the topic of Project.

M.TECH MICROELECTRONICS AND CONTROL SYSTEMS (EMS) CHOICE BASED CREDIT SYSTEM (CBCS) **SEMESTER - II** INDUSTRIAL CONTROL TECHNOLOGY - 1 (Core Course) Course Code 16EMS21 IA Marks 20 Number of Lecture Hours/Week Exam Hours 03 04 Total Number of Lecture Hours 50 Exam Marks 80 Credits - 04

- To discuss three types of industrial control systems; embedded control systems, real time control systems and distributed control systems.
- To discuss three types of industrial control engineering; process control, motion control and production automation.
- To explain the working of field elements of industrial control systems; sensors and actuators.
- To discuss working of transducers and valves used in industrial control systems.
- To discuss application of single-core and multi-core microprocessor units in industrial control systems.
- To discuss application of programmable-logic application specific integrated circuits and devices in industrial control systems. ■

Module-1		Teaching Hours
Industrial Contro	Systems: Embedded Control Systems, Real-Time Control Systems, Distributed	10
Control System.		
Industrial Contro	Engineering: Industrial Process Controls, Industrial Motion Controls, Industrial	
Production Automa		
Revised Bloom's Taxonomy Level	L_1 – Remembering, L_2 – Understanding.	
Module-2		
	ators: Industrial Optical Sensors, Industrial Physical Sensors, Industrial ors, Industrial Actuators. ■	10
Revised Bloom's Taxonomy Level	L_1 – Remembering, L_2 – Understanding.	
Module-3		
Module 5		
	Valves: Industrial Switches, Industrial Transducers, Industrial Valves. ■	10
	Valves: Industrial Switches, Industrial Transducers, Industrial Valves. \blacksquare $L_1 - \text{Remembering}, L_2 - \text{Understanding}.$	10
Transducers and Revised Bloom's		10
Transducers and Revised Bloom's Taxonomy Level Module-4		10
Transducers and Revised Bloom's Taxonomy Level Module-4	L_1 – Remembering, L_2 – Understanding.	
Transducers and Revised Bloom's Taxonomy Level Module-4 Microprocessors: Revised Bloom's	L_1 – Remembering, L_2 – Understanding. Single-Core Microprocessor Units, Multicore Microprocessor Units.	
Revised Bloom's Taxonomy Level Module-4 Microprocessors: Revised Bloom's Taxonomy Level Module-5	L_1 – Remembering, L_2 – Understanding. Single-Core Microprocessor Units, Multicore Microprocessor Units.	
Revised Bloom's Taxonomy Level Module-4 Microprocessors: Revised Bloom's Taxonomy Level Module-5 Programmable-Level	$L_1 - Remembering, \ L_2 - Understanding.$ Single-Core Microprocessor Units, Multicore Microprocessor Units. \blacksquare $L_1 - Remembering, \ L_2 - Understanding.$	10
Revised Bloom's Taxonomy Level Module-4 Microprocessors: Revised Bloom's Taxonomy Level Module-5 Programmable-Level	L_1 – Remembering, L_2 – Understanding. Single-Core Microprocessor Units, Multicore Microprocessor Units. L_1 – Remembering, L_2 – Understanding. Ogic and Application-Specific Integrated Circuits (PLASIC): Fabrication	10

M.TECH MICROELECTRONICS AND CONTROL SYSTEMS (EMS) 16EMS21 INDUSTRIAL CONTROL TECHNOLOGY - 1 (Core Course) (continued) CHOICE BASED CREDIT SYSTEM (CBCS)

Course outcomes:

At the end of the course the student will be able to:

- Differentiate between different types of industrial control systems; embedded control systems, real time control systems and distributed control systems.
- Explain three types of industrial control engineering; process control, motion control and production automation.
- Explain the need of sensors and actuators used in industrial control systems.
- Explain the working of transducers and valves used in industrial control systems.
- Explain the need of microelectronic components in industrial control systems
- Explain the use of multi-core microprocessors in industrial control systems.
- Describe programmable peripheral I/O ports, programmable interrupt controllers, programmable timers, and CMOS and DMA controllers, the application specific integrated circuits used in industrial control systems.

Graduate Attributes (As per NBA):

Engineering Knowledge, Problem Analysis.

Question paper pattern:

- The question paper will have ten questions.
- Each full question is for 16 marks.
- There will be 2 full questions (with a maximum of four sub questions in one full question) from each module.
- Each full question with sub questions will cover the contents under a module.
- Students will have to answer 5 full questions, selecting one full question from each module.

Text Book 1 Advanced Industrial Control Technology Peng Zhang Elsevier 2010

M.TECH MICROELECTRONICS AND CONTROL SYSTEMS (EMS) CHOICE BASED CREDIT SYSTEM (CBCS)						
	SEMESTER - II					
OPTIM	OPTIMAL CONTROL THEORY (Core Course)					
Course Code	16EMS22	IA Marks	20			
Number of Lecture Hours/Week 04 Exam Hours 03						
Total Number of Lecture Hours 50 Exam Marks 80						
	Credits - 04	1				

- To discuss modeling of systems.
- To discuss state and control constraints.
- To discuss the performance measures used in control problems.
- To explain determination of control function that minimizes the performance measure.
- To explain development of a dynamic program applicable to a class of control problems.
- To explain some basic ideas of the calculus of variations and to relate the analogy of results in calculus and the results of calculus of variations
- To explain application of variational method to optimal control problems.
- To explain Pontryagin's minimum principle. ■

Module-1		Teaching
<u> </u>		Hours
The Performance Performance Meas Dynamic Prograr principle of Optim	blem Formulation, State Variable Representation of a System. Measure: Performance Measure for Optimal Control Problems, Selecting a ure, Selection of a Performance Measure. Inming: The optimal Control Law, the Principle of Optimality, Application of the ality to Decision- Making, Dynamic Programming applied to a Routing Problem, ol System, Interpolation. L₁ − Remembering, L₂ − Understanding, L₃ − Applying.	10
Taxonomy Level	7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7	
Module-2		
Computational Pro Solution, Analytica Continuous Linear Observations.	nming (continued): A Recurrence Relation of Dynamic Programming, cedure for Solving Control Problems, Characteristics of Dynamic Programming al Results – Linear Regulator Problems, The Hamilton- Jacobi-Bellman Equation, Regulator Problem, The Hamilton- Jacobi-Bellman Equation – Some Wariations: Fundamental Concepts, Functions of a Single Function. ■	10
Revised Bloom's Taxonomy Level	L_1 – Remembering, L_2 – Understanding, L_3 – Applying.	
Module-3		
Piecewise - smoot	Variations (continued): Functionals involving several independent Functions, the Externals, Constrained Extrema. Approach to Optimal Control Problems: Necessary Conditions for Optimal	10
Revised Bloom's	L_1 – Remembering, L_2 – Understanding, L_3 – Applying.	
Taxonomy Level		
		•
Taxonomy Level Module-4 The Variational A	Approach to Optimal Control Problems (continued): Linear regulator problem, mum Principle and state Inequality Constraints, Minimum −Time problems. ■	10

	M.TECH MICROELECTRONICS AND CONTROL SYSTEMS (EMS) 16EMS22 OPTIMAL CONTROL THEORY (Core Course) (continued) CHOICE BASED CREDIT SYSTEM (CBCS)	
Module-5		Teaching Hours
	pproach to Optimal Control Problems (continued): Minimum Control-Effort Intervals in Optimal Control Problems. ■	10
Revised Bloom's Taxonomy Level	L_1 – Remembering, L_2 – Understanding, L_3 – Applying.	

Course outcomes:

At the end of the course the student will be able to:

- Develop mathematical models for systems using state variables.
- Formulate an optimal control problem with constraints.
- Discuss performance of and performance measures used in control problems.
- Evaluate control function that minimizes the performance measure.
- Explain dynamic programming applicable to a class of control problems.
- Explain basic ideas of the calculus of variations.
- Explain application of variational method to optimal control problems.
- Explain Pontryagin's minimum principle used for optimal control systems. ■

Graduate Attributes (As per NBA):

Engineering Knowledge, Problem Analysis, Design / development of solutions, Conduct investigations of complex Problems, Modern Tool Usage, Ethics.

Question paper pattern:

- The question paper will have ten questions.
- Each full question is for 16 marks.
- There will be 2 full questions (with a maximum of four sub questions in one full question) from each module.
- Each full question with sub questions will cover the contents under a module.
- Students will have to answer 5 full questions, selecting one full question from each module.

Text Book

1	Optimal Control Theory An Introduction	Donal E Kirk	Dover Publication	2004

	CHOI	CE BASED CREDIT			
		SEMESTER			
0 0 1	HIGH	SPEED VLSI DESIG		20	2
Course Code	T /337 1	16EMS23	IA Marks	20	
Number of Lecture F		04	Exam Hours	03	
Total Number of Lec	cture Hours	50 Credits - 04	Exam Marks	80)
Course objectives					
	nd electromigration		itances and inductances ated with VLSI intercor		
Module-1					Teachin Hours
of Images, Method of Miller's Theorem, In Propagation Modes in Delays. Parasitic Resistance Considerations, Para	of Moments, Even- nverse Laplace Tran in Micro strip Intereses, Capacitances, a sitic Capacitances:	and Odd-Mode Capaci nsformation, Resistive I connection, Slow-Wave and Inductances: Para	ns, Copper Interconnect tances, Transmission Li Interconnection as Ladd e Mode Propagation, Presitic Resistances: Gener s, Parasitic Inductances	ne Equations, er Network, opagation	10
Revised Bloom's	I Damamhanin				
Taxonomy Level Module-2 Parasitic Resistance	es, Capacitances, a		inued): Green's Function		10
Taxonomy Level Module-2 Parasitic Resistance Using Method of Ima Method, Simplified I Substrates, Inductance	es, Capacitances, a ages, Green's Func Formulas for Interc ce Extraction Using	and Inductances (cont tion Method: Fourier In onnection Capacitances	ntegral Approach, Netw s and Inductances on Sil terconnections: Resistar	ork Analog licon and GaAs	10
Taxonomy Level Module-2 Parasitic Resistance Using Method of Ima Method, Simplified I Substrates, Inductance Electrode Capacitance Revised Bloom's	es, Capacitances, a ages, Green's Func Formulas for Interc ce Extraction Using ces in GaAs MESF	and Inductances (cont tion Method: Fourier In onnection Capacitances g FastHenry, Copper In	ntegral Approach, Netw s and Inductances on Sil terconnections: Resistar	ork Analog licon and GaAs	10
Taxonomy Level Module-2 Parasitic Resistance Using Method of Ima Method, Simplified I Substrates, Inductance Electrode Capacitance Revised Bloom's Taxonomy Level	es, Capacitances, a ages, Green's Func Formulas for Interc ce Extraction Using ces in GaAs MESF	and Inductances (contention Method: Fourier Intention Capacitances FastHenry, Copper Intertion of Programments	ntegral Approach, Netw s and Inductances on Sil terconnections: Resistar	ork Analog licon and GaAs	10
Taxonomy Level Module-2 Parasitic Resistance Using Method of Ima Method, Simplified I Substrates, Inductance Electrode Capacitance Revised Bloom's Taxonomy Level Module-3 Interconnection Del Interconnection, Trai Analysis of Parallel I Interconnections Mo	es, Capacitances, a ages, Green's Function Using Ces in GaAs MESF L ₁ – Remembering Lays: Metal–Insulansmission Line And Multilevel Intercondelled as Multiple	and Inductances (contition Method: Fourier Informection Capacitances grastHenry, Copper Informection of Programmer Informed Infor	ntegral Approach, Netwest and Inductances on Silterconnections: Resistant and IPCSGV.	ork Analog licon and GaAs nce Modeling, mission Line	10
Taxonomy Level Module-2 Parasitic Resistance Using Method of Ima Method, Simplified I Substrates, Inductance Electrode Capacitance Revised Bloom's Taxonomy Level Module-3 Interconnection, Trace Analysis of Parallel I Interconnections Mo Revised Bloom's	es, Capacitances, a ages, Green's Function Using Ces in GaAs MESF L ₁ – Remembering Lays: Metal–Insulansmission Line And Multilevel Intercondelled as Multiple	and Inductances (contition Method: Fourier Inconnection Capacitances FastHenry, Copper In ET:Application of Program, L ₂ – Understanding. tor–Semiconductor Micalysis of Single-Level Innections, Analysis of Continuous Control (Continuous Control (Control	ntegral Approach, Netwest and Inductances on Silterconnections: Resistant and IPCSGV.	ork Analog licon and GaAs nce Modeling, mission Line	
Taxonomy Level Module-2 Parasitic Resistance Using Method of Ima Method, Simplified I Substrates, Inductance Electrode Capacitance Revised Bloom's Taxonomy Level Module-3 Interconnection Del Interconnection, Trai Analysis of Parallel I Interconnections Mo	es, Capacitances, a ages, Green's Function Using Ces in GaAs MESF L ₁ – Remembering Lays: Metal–Insulansmission Line And Multilevel Intercondelled as Multiple	and Inductances (contition Method: Fourier Informection Capacitances grastHenry, Copper Informection of Programmer Informed Infor	ntegral Approach, Netwest and Inductances on Silterconnections: Resistant and IPCSGV.	ork Analog licon and GaAs nce Modeling, mission Line	
Taxonomy Level Module-2 Parasitic Resistance Using Method of Ima Method, Simplified I Substrates, Inductance Electrode Capacitance Revised Bloom's Taxonomy Level Module-3 Interconnection, Trat Analysis of Parallel I Interconnections Mo Revised Bloom's Taxonomy Level Module-4 Interconnection Del Coupled Lumped Di Compact Expression Circuits, Active Inter Crosstalk Analysis:	es, Capacitances, a ages, Green's Function Using Ces in GaAs MESF L ₁ – Remembering lays: Metal–Insulansmission Line And Multilevel Intercondelled as Multiple L ₁ – Remembering lays (continued): Instributed Systems, as for Interconnections.	and Inductances (contition Method: Fourier Informection Capacitances of FastHenry, Copper Informection of Programmers, Laboration of Programmers, Laborator Michael School of Complete Microstrips of Coupled Microstrips. Modelling of Lossy Par Very High Frequency Informection of Coupled Microstrips on Delays, Interconnections of Coupled Microstrips.	ntegral Approach, Netwest and Inductances on Silterconnections: Resistant and IPCSGV.	ork Analog dicon and GaAs ance Modeling, mission Line as, Parallel connections as erconnection, er Integrated	

M.TECH MICROELECTRONICS AND CONTROL SYSTEMS (EMS) 16EMS23 HIGH SPEED VLSI DESIGN (Core Course) (continued) CHOICE BASED CREDIT SYSTEM (CBCS) Module-5 Crosstalk Analysis: Transmission Line Analysis of Parallel Multilevel Interconnections, Analysis of Crossing Interconnections, Compact Expressions for Crosstalk Analysis, Multiconductor Buses in GaAs High-Speed Logic Circuits. Electromigration-Induced Failure Analysis: Electromigration in VLSI Interconnection Metallizations: Overview. Revised Bloom's Taxonomy Level N. T. – Remembering, L₂ – Understanding.

Course outcomes:

At the end of the course the student will be able to:

- Discuss basic techniques and advanced concepts regarding wave propagation in an interconnection, v
- Discuss multilevel, multilayer, and multipath interconnections employed in VLSI applications.
- Discuss copper interconnections and their fabrication techniques.
- Explain numerical techniques that can be used to determine the interconnection resistances, capacitances, and inductances on a high-density VLSI chip.
- Calculate the propagation delays in the single and multilevel parallel and crossing interconnections using numerical algorithms.
- Explain the crosstalk effects in the single and multilevel parallel and crossing interconnections.
- Develop a model of very high speed VLSI circuits for the crosstalk analysis.
- Discuss the degradation of the reliability of an interconnection due to electromigration. ■

Graduate Attributes (As per NBA):

Engineering Knowledge, Problem Analysis, Conduct investigations of complex Problems.

Question paper pattern:

- The question paper will have ten questions.
- Each full question is for 16 marks.
- There will be 2 full questions (with a maximum of four sub questions in one full question) from each module.
- Each full question with sub questions will cover the contents under a module.
- Students will have to answer 5 full questions, selecting one full question from each module. ■

Text Book

	1	High-Speed VLSI Interconnections	Ashok K. Goel	Wiley	2007
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M.TECH MICROELECTRONICS AND CONTROL SYSTEMS (EMS) CHOICE BASED CREDIT SYSTEM (CBCS)					
CAP TO	SEMESTER - II				
CADTO	OOLS FOR VLSI DES	IGN (Core Course)			
Course Code	16EMS24	IA Marks	20		
Number of Lecture Hours/Week 04 Exam Hours 03					
Total Number of Lecture Hours 50 Exam Marks 80					
	Credits - 04				

- To give an overview of the VLSI physical design automation field, including VLSI design cycle, physical design cycle, design styles and packaging styles.
- To explain fabrication process, impact of process innovations on physical design.
- To discuss design rules, yield, delay, and fabrication costs involved in the VLSI process.
- To discuss data structures, algorithms involved in the physical design.
- To explain graphs used to model problems in VLSI design and basic algorithms for these graphs.
- To explain partitioning algorithms, their classification, factors considered in partitioning the VLSI circuits.
- To discuss basic algorithms for floor planning and pin assignment.
- To discuss different techniques for placement such as, simulated annealing, simulated evolution, and force-directed.
- To discuss global routing, detailed routing and routing algorithms.

VLSI Physical Design Automation: VLSI Design Cycle, New Trends in VLSI Design Cycle, Physical Design Cycle, New Trends in Physical Design Cycle, Physical Design Cycle, New Trends in Physical Design Styles. 10			
Physical Design Cycle, New Trends in Physical Design Cycle, Design Styles, System Packaging Styles. Design and Fabrication of VLSI Devices: Fabrication Materials, Transistor Fundamentals, Fabrication of VLSI Circuits, Design Rules, Layout of Basic Devices. Revised Bloom's Taxonomy Level Module-2 Data Structures and Basic Algorithms: Basic Terminology, Complexity Issues and NP-hardness, Basic Algorithms, Basic Data Structures, Graph Algorithms for Physical design. Revised Bloom's Taxonomy Level Module-3 Partitioning: Problem Formulation, Classification of Partitioning Algorithms, Group Migration Algorithms, Simulated Annealing and Evolution, Other Partitioning Algorithms, Performance Driven Partitioning Revised Bloom's Taxonomy Level Module-4 Placement: Problem Formulation, Classification of Placement Algorithms, Simulation Based Placement Algorithms, Partitioning Based Placement Algorithms, Other Placement Algorithms, Performance Driven Placement. Global Routing: Problem Formulation, Classification of Global Routing Algorithms, Maze Routing Algorithms, Line-Probe Algorithms, Shortest Path Based Algorithms, Steiner Tree based Algorithms, Integer Programming Based Approach, Performance Driven Routing. Revised Bloom's L₁ - Remembering, L₂ - Understanding. 10 Placement: Problem Formulation, Classification of Global Routing Algorithms, Maze Routing Algorithms, Line-Probe Algorithms, Shortest Path Based Algorithms, Steiner Tree based Algorithms, Integer Programming Based Approach, Performance Driven Routing. Revised Bloom's L₁ - Remembering, L₂ - Understanding.	Module-1		U
Taxonomy Level Module-2 Data Structures and Basic Algorithms: Basic Terminology, Complexity Issues and NP-hardness, Basic Algorithms, Basic Data Structures, Graph Algorithms for Physical design. ■ Revised Bloom's Taxonomy Level L₁ - Remembering, L₂ - Understanding. Module-3 Partitioning: Problem Formulation, Classification of Partitioning Algorithms, Group Migration Algorithms, Simulated Annealing and Evolution, Other Partitioning Algorithms, Performance Driven Partitioning. Floorplanning and Pin Assignment: Floorplanning, Chip planning, Pin Assignment, Integrated Approach. ■ Revised Bloom's Taxonomy Level L₁ - Remembering, L₂ - Understanding. Placement: Problem Formulation, Classification of Placement Algorithms, Simulation Based Placement Algorithms, Partitioning Based Placement Algorithms, Other Placement Algorithms, Partitioning Based Placement Algorithms, Other Placement Algorithms, Maze Routing Algorithms, Line-Probe Algorithms, Shortest Path Based Algorithms, Steiner Tree based Algorithms, Integer Programming Based Approach, Performance Driven Routing. ■ Revised Bloom's L₁ - Remembering, L₂ - Understanding.	Physical Design Cy Styles. Design and Fabric	cle, New Trends in Physical Design Cycle, Design Styles, System Packaging ation of VLSI Devices: Fabrication Materials, Transistor Fundamentals,	
Data Structures and Basic Algorithms: Basic Terminology, Complexity Issues and NP-hardness, Basic Algorithms, Basic Data Structures, Graph Algorithms for Physical design. ■ 10 Revised Bloom's Taxonomy Level L₁ - Remembering, L₂ - Understanding. 10 Module-3 Partitioning: Problem Formulation, Classification of Partitioning Algorithms, Group Migration Algorithms, Simulated Annealing and Evolution, Other Partitioning Algorithms, Performance Driven Partitioning. 10 Floorplanning and Pin Assignment: Floorplanning, Chip planning, Pin Assignment, Integrated Approach. ■ Revised Bloom's Taxonomy Level L₁ - Remembering, L₂ - Understanding. Module-4 Placement: Problem Formulation, Classification of Placement Algorithms, Simulation Based Placement Algorithms, Partitioning Based Placement Algorithms, Other Placement Algorithms, Performance Driven Placement. 10 Global Routing: Problem Formulation, Classification of Global Routing Algorithms, Maze Routing Algorithms, Line-Probe Algorithms, Shortest Path Based Algorithms, Steiner Tree based Algorithms, Integer Programming Based Approach, Performance Driven Routing. ■ Revised Bloom's L₁ - Remembering, L₂ - Understanding.	Taxonomy Level	L_1 – Remembering, L_2 – Understanding.	
Basic Algorithms, Basic Data Structures, Graph Algorithms for Physical design. ■ Revised Bloom's Taxonomy Level Module-3 Partitioning: Problem Formulation, Classification of Partitioning Algorithms, Group Migration Algorithms, Simulated Annealing and Evolution, Other Partitioning Algorithms, Performance Driven Partitioning. Floorplanning and Pin Assignment: Floorplanning, Chip planning, Pin Assignment, Integrated Approach. ■ Revised Bloom's Taxonomy Level Placement: Problem Formulation, Classification of Placement Algorithms, Simulation Based Placement Algorithms, Partitioning Based Placement Algorithms, Other Placement Algorithms, Performance Driven Placement. Global Routing: Problem Formulation, Classification of Global Routing Algorithms, Maze Routing Algorithms, Line-Probe Algorithms, Shortest Path Based Algorithms, Steiner Tree based Algorithms, Integer Programming Based Approach, Performance Driven Routing. Revised Bloom's L₁ – Remembering, L₂ – Understanding. Revised Bloom's L₁ – Remembering, L₂ – Understanding.	Module-2		
Taxonomy Level Module-3 Partitioning: Problem Formulation, Classification of Partitioning Algorithms, Group Migration Algorithms, Simulated Annealing and Evolution, Other Partitioning Algorithms, Performance Driven Partitioning. Floorplanning and Pin Assignment: Floorplanning, Chip planning, Pin Assignment, Integrated Approach. ■ Revised Bloom's Taxonomy Level L₁ – Remembering, L₂ – Understanding. Module-4 Placement: Problem Formulation, Classification of Placement Algorithms, Simulation Based Placement Algorithms, Partitioning Based Placement Algorithms, Other Placement Algorithms, Performance Driven Placement. 10 Global Routing: Problem Formulation, Classification of Global Routing Algorithms, Maze Routing Algorithms, Line-Probe Algorithms, Shortest Path Based Algorithms, Steiner Tree based Algorithms, Integer Programming Based Approach, Performance Driven Routing. ■ Revised Bloom's L₁ – Remembering, L₂ – Understanding.			10
Partitioning: Problem Formulation, Classification of Partitioning Algorithms, Group Migration Algorithms, Simulated Annealing and Evolution, Other Partitioning Algorithms, Performance Driven Partitioning. Floorplanning and Pin Assignment: Floorplanning, Chip planning, Pin Assignment, Integrated Approach. ■ Revised Bloom's Taxonomy Level Placement: Problem Formulation, Classification of Placement Algorithms, Simulation Based Placement Algorithms, Partitioning Based Placement Algorithms, Other Placement Algorithms, Performance Driven Placement. Global Routing: Problem Formulation, Classification of Global Routing Algorithms, Maze Routing Algorithms, Line-Probe Algorithms, Shortest Path Based Algorithms, Steiner Tree based Algorithms, Integer Programming Based Approach, Performance Driven Routing. ■ Revised Bloom's L₁ − Remembering, L₂ − Understanding.		L_1 – Remembering, L_2 – Understanding.	
Algorithms, Simulated Annealing and Evolution, Other Partitioning Algorithms, Performance Driven Partitioning. Floorplanning and Pin Assignment: Floorplanning, Chip planning, Pin Assignment, Integrated Approach. Revised Bloom's Taxonomy Level Module-4 Placement: Problem Formulation, Classification of Placement Algorithms, Simulation Based Placement Algorithms, Partitioning Based Placement Algorithms, Other Placement Algorithms, Performance Driven Placement. Global Routing: Problem Formulation, Classification of Global Routing Algorithms, Maze Routing Algorithms, Line-Probe Algorithms, Shortest Path Based Algorithms, Steiner Tree based Algorithms, Integer Programming Based Approach, Performance Driven Routing. Revised Bloom's L₁ − Remembering, L₂ − Understanding.	Module-3		
Module-4 Placement: Problem Formulation, Classification of Placement Algorithms, Simulation Based Placement Algorithms, Partitioning Based Placement Algorithms, Other Placement Algorithms, Performance Driven Placement. Global Routing: Problem Formulation, Classification of Global Routing Algorithms, Maze Routing Algorithms, Line-Probe Algorithms, Shortest Path Based Algorithms, Steiner Tree based Algorithms, Integer Programming Based Approach, Performance Driven Routing. Revised Bloom's L₁ − Remembering, L₂ − Understanding.	Algorithms, Simula Partitioning. Floorplanning and	ted Annealing and Evolution, Other Partitioning Algorithms, Performance Driven	10
Placement: Problem Formulation, Classification of Placement Algorithms, Simulation Based Placement Algorithms, Partitioning Based Placement Algorithms, Other Placement Algorithms, Performance Driven Placement. Global Routing: Problem Formulation, Classification of Global Routing Algorithms, Maze Routing Algorithms, Line-Probe Algorithms, Shortest Path Based Algorithms, Steiner Tree based Algorithms, Integer Programming Based Approach, Performance Driven Routing. Revised Bloom's L₁ − Remembering, L₂ − Understanding.		L_1 – Remembering, L_2 – Understanding.	
Placement Algorithms, Partitioning Based Placement Algorithms, Other Placement Algorithms, Performance Driven Placement. Global Routing: Problem Formulation, Classification of Global Routing Algorithms, Maze Routing Algorithms, Line-Probe Algorithms, Shortest Path Based Algorithms, Steiner Tree based Algorithms, Integer Programming Based Approach, Performance Driven Routing. Revised Bloom's L₁ − Remembering, L₂ − Understanding.	Module-4		
Taxonomy Level	Placement Algorith Performance Driver Global Routing: P Algorithms, Line-P Integer Programmin Revised Bloom's	ms, Partitioning Based Placement Algorithms, Other Placement Algorithms, in Placement. roblem Formulation, Classification of Global Routing Algorithms, Maze Routing robe Algorithms, Shortest Path Based Algorithms, Steiner Tree based Algorithms, in Based Approach, Performance Driven Routing.	10
	Taxonomy Level		

	1.TECH MICROELECTRONICS AND CONTROL SYSTEMS (EMS) 6EMS24 CAD TOOLS FOR VLSI DESIGN (Core Course) (continued) CHOICE BASED CREDIT SYSTEM (CBCS)	
Module-5		Teaching Hours
Routing Algorithms	Problem Formulation, Classification of Routing Algorithms, Single-Layer at Two-Layer Channel Routing Algorithms, Three-Layer Channel Routing Layer Channel Routing Algorithms, Switchbox Routing Algorithms.	10
Revised Bloom's Taxonomy Level	L_1 – Remembering, L_2 – Understanding.	

Course outcomes:

At the end of the course the student will be able to:

- Discuss design automation field including the VLSI design cycle, physical design cycle, design styles and packaging styles.
- Discuss the fabrication process for VLSI devices, process innovations, design rules and costs involved in fabrication process. .
- Explain data structures for layout and algorithms involved in the physical design.
- Explain graphs used to model problems in VLSI design and algorithms for the graphs.
- Explain partitioning, partitioning algorithms, their classification and the factors that must be considered in partitioning the VLSI circuits.
- Discuss algorithms for floorplanning and pin assignment and techniques for placement.
- Discuss global routing, routing algorithms and routing of multi-terminal nets
- Discuss detailed routing, routing algorithms and their classification. ■

Graduate Attributes (As per NBA):

Engineering Knowledge, Problem Analysis, Design / development of solutions.

Question paper pattern:

- The question paper will have ten questions.
- Each full question is for 16 marks.
- There will be 2 full questions (with a maximum of four sub questions in one full question) from each module.
- Each full question with sub questions will cover the contents under a module.
- Students will have to answer 5 full questions, selecting one full question from each module.

Text Books

1 Algorithms for VLSI Physical Design Naveed A. Sherwani Kluwer Academic Automation Naveed A. Sherwani Publishers

M,TECH MICROELECTRONICS AND CONTROL SYSTEMS (EMS) CHOICE BASED CREDIT SYSTEM (CBCS) SEMESTER - II					
LOW POWER VLSI DESIGN (Elective Course)					
Course Code	16EMS251	IA Marks	20		
Number of Lecture Hours/Week	03	Exam Hours	03		
Total Number of Lecture Hours	40	Exam Marks	80		
Credits - 03					

- To explain the necessity of low power VLSI, the charging and discharging capacitances, short circuit and leakage currents in CMOS circuits and basic principles of low power design.
- To explain simulation of VLSI chips using modeling techniques to estimate power dissipation.
- To explain probabilistic power analysis for VLSI circuits.
- To discuss the optimization and trade-off techniques that involve power dissipation for digital circuits.
- To explain gate reorganization, signal gating, logic encoding and low power techniques for reduction in power consumption in VLSI circuits.
- Explain power and performance management, switching activity reduction for VLSI circuits.
- To explain the architecture for reduction in the power consumption of VLSI circuits.
- To explain the advanced techniques in the design of VLSI circuits; adiabatic computation, pass transistor logic synthesis and asynchronous circuits. ■

Module-1		Teaching Hours	
Low Power VLSI Chips: Introduction, Needs for Low Power VLSI Chips, Charging and Discharging Capacitance, Short-circuit Current in CMOS Circuit, CMOS Leakage Current, Static Current, Basic Principles of Low Power Design, Low Power Figure of Merits. Simulation Power Analysis: SPICE Circuit Simulation, Discrete Transistor Modelling and Analysis, Gate-level Logic Simulation, Architecture-level Analysis, Data Correlation Analysis in DSP Systems, Monte Carlo Simulation. ■			
Revised Bloom's Taxonomy Level	L_1 – Remembering, L_2 – Understanding.		
Module-2			
	er Analysis: Random Logic Signals, Probability and Frequency, Probabilistic Chniques, Signal Entropy. ■	08	
Revised Bloom's Taxonomy Level	L_1 – Remembering, L_2 – Understanding.		
Module-3			
Circuit: Transistor and Gate Sizing, Equivalent Pin Ordering, Network Restructuring and Reorganization, Special Latches and Flip-flops, Low Power Digital Cell Library, Adjustable Device Threshold Voltage. ■			
Revised Bloom's Taxonomy Level	L_1 – Remembering, L_2 – Understanding.		
Module-4			
 Logic: Gate Reorganization, Signal Gating, Logic Encoding, State Machine Encoding, Precomputation Logic. Special Techniques: Power Reduction in Clock Networks, CMOS Floating Node, Low Power Bus, Delay Balancing, Low Power Techniques for SRAM. ■ 		08	
Revised Bloom's Taxonomy Level	L_1 – Remembering, L_2 – Understanding.		
Module-5			
Architecture and System: Power and Performance Management, Switching Activity Reduction, Parallel Architecture with Voltage Reduction, Flow Graph Transformation. Advanced Techniques: Adiabatic Computation, Pass Transistor Logic Synthesis, Asynchronous Circuits. ■		08	
Circuits.			

M.TECH MICROELECTRONICS AND CONTROL SYSTEMS (EMS) 16EMS251 LOW POWER VLSI DESIGN (Elective Course) (continued) CHOICE BASED CREDIT SYSTEM (CBCS)

Course outcomes:

At the end of the course the student will be able to:

- Explain the needs for low power VLSI, the charging and discharging capacitances, short circuit and leakage currents in CMOS circuits.
- Explain basic principles of low power design.
- Simulate VLSI chips using modeling techniques to estimate power dissipation.
- Perform probabilistic power analysis for VLSI circuits.
- Discuss the optimization and trade-off techniques that involve power dissipation for digital circuits.
- Explain gate reorganization, signal gating, logic encoding and low power techniques for reduction in power consumption in VLSI circuits.
- Explain power and performance management switching activity reduction and the architecture for reduction in the power consumption of VLSI circuits.
- Explain the advanced techniques in the design of VLSI circuits; adiabatic computation, pass transistor logic synthesis and asynchronous circuits. ■

Graduate Attributes (As per NBA):

Engineering Knowledge, Problem Analysis, Modern Tool Usage.

Question paper pattern:

- The question paper will have ten questions.
- Each full question is for 16 marks.
- There will be 2 full questions (with a maximum of four sub questions in one full question) from each module.
- Each full question with sub questions will cover the contents under a module.
- Students will have to answer 5 full questions, selecting one full question from each module.

Text Book 1 Practical Low Power Digital VLSI Design Gary Yeap Springer 1998

M.TECH MICROELECTRONICS AND CONTROL SYSTEMS (EMS) CHOICE BASED CREDIT SYSTEM (CBCS) SEMESTER - II						
ROBUST CONTROL THEORY (Elective Course)						
Course Code	16EMS252	IA Marks	20			
Number of Lecture Hours/Week	03	Exam Hours	03			
Total Number of Lecture Hours	40	Exam Marks	80			
Credits - 03						

- To present a broad range of well worked out, theoretical and application studies in the field of robust control system analysis and design that include robust PID, H-infinity, sliding mode, fault tolerant, fuzzy and QFT based control systems.
- To explain the current progress in the field robust control, motivate and encourage new ideas and solutions in the robust control area. ■

Module-1		Teaching Hours
Introduction: Systems and Control, Modern Control Theory, Stability, Optimal Control, Optimal Control Approach, Kharitonov Approach, H _∞ and H ₂ Control, Applications. Optimal Control and Optimal Observers: Optimal Control Problem, Principle of Optimality, Hamilton–Jacobi–Bellman Equation, Linear Quadratic Regulator Problem, Kalman Filter. ■		
Revised Bloom's Taxonomy Level	L_1 – Remembering, L_2 – Understanding.	
Module-2		
Robust Control of Linear Systems: Introduction, Matched Uncertainty, Unmatched Uncertainty, Uncertainty in the Input Matrix. ■		
Revised Bloom's Taxonomy Level	L_1 – Remembering, L_2 – Understanding.	
Module-3		
Uncertainty, Uncert	Nonlinear Systems: Introduction, Matched Uncertainty, Unmatched ainty in the Input Matrix. Sach: Introduction, Preliminary Theorems, Kharitonov Theorem, Control Design Theorem.	08
Revised Bloom's Taxonomy Level	L_1 – Remembering, L_2 – Understanding, L_3 – Applying, L_4 – Analysing.	
Module-4		
\mathbf{H}_{∞} and \mathbf{H}_2 Control: Introduction, Function Space, Computation of \mathbf{H}_{∞} and \mathbf{H}_2 Norms, Robust Control Problem as \mathbf{H}_{∞} and \mathbf{H}_2 Control Problem, \mathbf{H}_{∞} / \mathbf{H}_2 Control Synthesis.		
Revised Bloom's Taxonomy Level	L_1 – Remembering, L_2 – Understanding, L_3 – Applying, L_4 – Analysing.	
Module-5		
Active Vehicle Susp Robust Control of Simulations.	Manipulators: Robot Dynamics, Problem Formulation, Robust Control Design, Control: Modelling and Problem Formulation, Control Design for Jet-borne	08
Revised Bloom's Taxonomy Level	L_1 – Remembering, L_2 – Understanding, L_3 – Applying, L_4 – Analysing.	

M.TECH MICROELECTRONICS AND CONTROL SYSTEMS (EMS) 16EMS252 ROBUST CONTROL THEORY (Elective Course) (continued) CHOICE BASED CREDIT SYSTEM (CBCS)

Course outcomes:

At the end of the course the student will be able to:

- Explain properties of linear time-invariant systems including controllability, observability, stability, stabilizability, and detectability.
- Synthesize linear time-invariant systems by pole placement and observer design.
- Discuss optimal control and the Kalman filter.
- Explain H_{∞} and H_2 robust control design.
- Use optimal control approach to robust control design of linear and nonlinear systems
- Assess robust control of parametric systems using the Kharitonov theorem.
- Design robust active damper for vibration systems, robust controller for robot manipulators.
- Design controller for Jet-borne Hovering.

Graduate Attributes (As per NBA):

Engineering Knowledge, Problem Analysis, Design / development of solutions, Conduct investigations of complex Problems, Modern Tool Usage.

Question paper pattern:

- The question paper will have ten questions.
- Each full question is for 16 marks.
- There will be 2 full questions (with a maximum of four sub questions in one full question) from each module.
- Each full question with sub questions will cover the contents under a module.
- Students will have to answer 5 full questions, selecting one full question from each module. ■

Text Book 1 Robust Control Design; An Optimal Control Approach Feng Lin Wiley 2007

M.TECH MICROELECTRONICS AND CONTROL SYSTEMS (EMS) CHOICE BASED CREDIT SYSTEM (CBCS)							
	SEMESTER - II						
DIGITAL SYSTEM DESIGN WITH VHDL (Elective Course)							
Course Code	16EMS253	IA Marks	20				
Number of Lecture Hours/Week	Number of Lecture Hours/Week 03 Exam Hours 03						
Total Number of Lecture Hours 40 Exam Marks 80							
	Credits - 03	3					

- To discuss the design of digital systems, CMO technology, programmable logic and engineering problems of noise margins and fan-out.
- To discuss the principles of Boolean algebra, combinational logic design, timing diagrams and basic number systems.
- To explain modeling of combinational logic and synchronous sequential logic systems in VHDL.
- To explain modeling of sequential logic blocks and complex sequential systems in VHDL.
- To describes event-driven simulation and specific features of a VHDL simulator.
- To discuss synthesis tool for RTL synthesis, fault modeling and design-for-test principles.
- To explain the designing of asynchronous sequential circuits.
- To explain simulation of digital to analog and analog to digital converters using VHDL-AMS simulator.

Module-1		Teachi Hours
Combinational log Number codes. Combinational log	ern digital design, CMOS technology, Programmable logic, Electrical properties. ic design: Boolean algebra, Logic gates, Combinational logic design, Timing, ic using VHDL gate models: Entities and architectures, Identifiers, spaces and Signal assignments, Generics, Constant and open ports, Testbenches,	08
Revised Bloom's Taxonomy Level	L_1 - Remembering, L_2 - Understanding, L_3 - Applying, L_4 - Analysing.	
Module-2		
Adders, Parity chec Synchronous sequ sequential systems,	ilding blocks: Three-state buffers, Decoders, Multiplexers, Priority encoder, ker, Testbenches for combinational blocks. ential design: Synchronous sequential systems, Models of synchronous Algorithmic state machines, Synthesis from ASM charts, State machines in benches for state machines. ■ L₁ - Remembering, L₂ - Understanding, L₃ – Applying, L₄ – Analysing.	08
Module-3		
shift registers, Cour Complex sequentia	equential logic blocks: Latches, Flip-flops, JK and T flip-flops, Registers and neers, Memory, Sequential multiplier, Testbenches for sequential building blocks. al systems: Linked state machines, Datapath /controller partitioning, Instructions, ressor, VHDL model of a simple microprocessor. ■ L₁ - Remembering, L₂ - Understanding, L₃ – Applying.	08
Module-4		I
issues, File operation VHDL synthesis: I Verifying synthesis Testing digital systematics. Fault simulation, Fa	RTL synthesis, Constraints, Synthesis for FPGAs, Behavioural synthesis,	08
Revised Bloom's		

M.TECH MICROELECTRONICS AND CONTROL SYSTEMS (EMS) 16EMS253 DIGITAL SYSTEM DESIGN WITH VHDL (Elective Course) (continued) CHOICE BASED CREDIT SYSTEM (CRCS)

	CHOICE BASED CREDIT SYSTEM (CBCS)	
Module-5		Teaching Hours
Design for testabil Boundary scan (IEI	ity: Ad hoc testability improvements, Structured design for test, Built-in self-test, EE 1149.1).	08
Asynchronous sequential design: Asynchronous circuits, Analysis of asynchronous circuits, Design of asynchronous sequential circuits, Asynchronous state machines, Setup and hold times and metastability.		
_	ne analogue world: Digital to analogue converters, Analogue to digital AMS, Phase-locked loops, VHDL-AMS simulators. ■	
Revised Bloom's Taxonomy Level	L_1 - Remembering, L_2 - Understanding, L_3 - Applying, L_4 - Analysing, L_5 - Evaluating.	

Course outcomes:

At the end of the course the student will be able to:

- Discuss the design digital systems using VHDL, the technology of CMO integrated circuits programmable logic, engineering problems of noise margins and fan-out.
- Explain the principles of Boolean algebra, combinational logic design, timing, hazards and basic number systems.
- Model combinational logic and synchronous sequential logic systems in VHDL.
- Develop models for sequential logic blocks and complex sequential systems in VHDL.
- Describes idea of event-driven simulation and specific features of a VHDL simulator.
- Discuss synthesis tool for RTL synthesis, fault modeling and design-for-test principles.
- Design asynchronous sequential circuits.
- Explain simulation of digital to analog and analog to digital converters using VHDL-AMS simulator.■

Graduate Attributes (As per NBA):

Engineering Knowledge, Problem Analysis, Design / development of solutions, Conduct investigations of complex Problems, Modern Tool Usage, Ethics, Communication.

Question paper pattern:

- The question paper will have ten questions.
- Each full question is for 16 marks.
- There will be 2 full questions (with a maximum of four sub questions in one full question) from each module.
- Each full question with sub questions will cover the contents under a module.
- Students will have to answer 5 full questions, selecting one full question from each module.

Text Book

1	1	Digital System Design with VHDL	Mark Zwoli´nski	Pearson	2 nd Edition, 2004

M.TECH MICROELECTRONICS AND CONTROL SYSTEMS (EMS) CHOICE BASED CREDIT SYSTEM (CBCS)						
SEMESTER - II REAL TIME APPROACH TO PROCESS CONTROL (Elective Course)						
Course Code	16EMS254	IA Marks	20			
Number of Lecture Hours/Week	03	Exam Hours	03			
Total Number of Lecture Hours 40 Exam Marks 80						
	Credits - 03					

- To give an overview of process control.
- To introduce the instrumentation used in the process control.
- To explain basics of single input single output systems, Feedback control, the elements of control loops, system dynamics including capacitance and dead time, and system modeling.
- To highlight the various PID control modes and provide a framework for understanding control-loop design and tuning.
- To introduce advanced control configurations including feed-forward, cascade, and override control.
- To explain practical rules of thumb for designing and tuning the more common control loops found in industry.
- To explain control of distillation columns.
- To introduce the concept of multiple loop controllers and issues relating to the plant-wide control problem. ■

Module-1		Teaching Hours			
,	n and Process control hardware fundamentals: Control, Simulation, Control, Primary elements, Final control elements. ■	08			
Revised Bloom's Taxonomy Level	L_1 – Remembering, L_2 – Understanding.				
Module-2					
control overview, F	single input—single output systems: Open-loop control, Disturbances, Feedback eedback control: a closer look, Process attributes: capacitance and dead time, sponse, Process modelling and simulation. ■	08			
Revised Bloom's Taxonomy Level	L_1 – Remembering, L_2 – Understanding.				
Module-3					
Proportional plus in controller, Proportion hardware.	es: On-off control, Proportional (P-only) control, Integral (I-only) control, Integral (PI) control, Derivative action, Proportional plus derivative (PD) contail integral derivative (PID) control, Choosing the correct controller, Controller controllers: Quality of control and optimisation, Tuning methods.	08			
Revised Bloom's Taxonomy Level	Revised Bloom's L_1 – Remembering, L_2 – Understanding, L_3 – Applying, L_4 – Analysing.				
Module-4					
control, Override co	n classical automatic control: Cascade control, Feedforward control, Ratio ontrol (auto selectors). cops: Flow loops, Liquid pressure loops, Liquid level control, Gas pressure loops, loops, Pump control, Compressor control, Boiler control. ■	08			
Revised Bloom's Taxonomy Level	L_1 – Remembering, L_2 – Understanding.				

M.TECH MICROELECTRONICS AND CONTROL SYSTEMS (EMS) 16EMS254 REAL TIME APPROACH TO PROCESS CONTROL (Elective Course) (continued) CHOICE BASED CREDIT SYSTEM (CBCS)

Module-5	Teaching Hours
Distillation column control: Basic terms, Steady-state and dynamic degrees of freedom, Control system objectives and design considerations, Methodology for selection of a controller structure, Level, pressure, temperature and composition control, Optimizing control, Distillation control scheme design using steady-state models, Distillation control scheme design using dynamic models. Using steady-state methods in a multi-loop control scheme: Variable pairing, The relative gain array, Niederlinski index, Decoupling control loops, Tuning the controllers for multi-loop systems, Practical examples. Plant-wide control: Short-term versus long-term control focus, Cascaded units, Recycle streams, General considerations for plant-wide control. ■	08

Course outcomes:

At the end of the course the student will be able to:

- Discuss process control and the instruments used in the process control
- Explain basics of single input single output systems, Feedback control, elements of control loops, system dynamics including capacitance and dead time, and system modeling.
- Discuss various PID control modes.
- Understand control-loop design and tuning.
- Explain advanced control configurations including feed-forward, cascade, and override control.
- Explain thumb rules for designing and tuning the more common control loops found in industry.
- Control distillation columns.
- Explain the concept of multiple loop controllers and issues relating to the plant-wide control problem. ■

Graduate Attributes (As per NBA):

Engineering Knowledge, Problem Analysis, Design / development of solutions, Conduct investigations of complex Problems.

Question paper pattern:

- The question paper will have ten questions.
- Each full question is for 16 marks.
- There will be 2 full questions (with a maximum of four sub questions in one full question) from each module.
- Each full question with sub questions will cover the contents under a module.
- Students will have to answer 5 full questions, selecting one full question from each module.

Text Book

1	A Real-Time Approach to Process Control	William Y. Svrcek	Wiley	2 nd Edition, 2006

M.TECH MICROELECTRONICS AND CONTROL SYSTEMS (EMS) CHOICE BASED CREDIT SYSTEM (CBCS) SEMESTER - II					
MICROELECTRONICS AND CONTROL LABORATORY - II					
Course Code	16EMSL26	IA Marks	20		
Number of Practical Hours/Week 03 Exam Hours 03					
Total Number of Practical Hours	40	Exam Marks	80		

Credits - 02

Course objectives:

- To develop Verilog code for verification of the functionality of CMOS inverter, buffer, transmission gate, Boolean expressions, adders, flip-flops and shift registers.
- To draw the transfer characteristics of CMOS inverter and compute noise margins, critical input and output.
- To design Mod-16 synchronous and asynchronous counters, draw truth table and waveform diagram. ■

Sl. NO		Experiments		
Note:	Note: Cadence Layout software to be used for Schematic and Layout.			
1		function of CMOS inverter by Verilog code. he voltage transfer characteristics to determine critical input and output voltages and low and pargins.		
2	Write a Veri	log code for a buffer and verify its functionality.		
3	Write a Veri	log code for a Transmission gate and verify its functionality.		
4	Using the Verilog code verify the functionality of a Boolean expression using Basic gates like NAND, NOR, AND, XOR.			
5	Design a 16 bit parallel adder (carry select, carry look ahead adder and ripple carry adder) using Verilog code and verify its functionality. Compare the area and power utilisation.			
6	Write a Veri	log code for a 3 input Boolean expression using 8:1 multiplexor and verify its functionality.		
7	Design the for flip flop, JK	ollowing Flip flops using Verilog code and verify the functionality: SR flip flop, D flip flop, T flip-flop.		
8	Write a Veri	log code for a universal shift register and verify its functionality.		
9	Design a MOD-16 Synchronous counter using synchronous reset. Draw the truth table and waveform diagram.			
10	Design a MOD-16 Asynchronous counter using T-flip flop. Draw the truth table and waveform diagram.			
	ed Bloom's nomy Level	L_3 – Applying, L_4 – Analysing, L_5 – Evaluating, L_6 – Creating		

Course outcomes:

At the end of the course the student will be able to:

- Write Verilog code to verify the functionality of CMOS inverter and buffer.
- Write Verilog code to verify the functionality of Basic gates, transmission gates and universal shift register.
- Write Verilog codes for verifying the functionality of 3 input Boolean expression using 8:1 multiplexer.
- Determine critical input and output voltages of CMOS inverter and noise margins of CMOS inverter.
- Use Verilog code to design a 16 bit parallel adder, flip flops.
- Design MOD -16 synchronous counter using synchronous set.
- Design MOD -16 asynchronous counter using T flip flop.

Graduate Attributes (As per NBA):

Engineering Knowledge, Problem Analysis, Conduct investigations of complex Problems, Modern Tool Usage, Individual and Team work, Communication.

M.TECH MICROELECTRONICS AND CONTROL SYSTEMS (EMS) **CHOICE BASED CREDIT SYSTEM (CBCS)**

SEMESTER - II

SEMINAR					
Course Code	16EMS27	IA Marks	100		
No. of Lecture Hours/Week		Exam Hours			
Number of contact Hours/week	03	Number of Tutorial Hours/week			
Total No. of contact Hours		Exam Marks			

Credits - 01

The objective of the seminar is to inculcate self-learning, face audience confidently, enhance communication skill, involve in group discussion and present and exchange ideas.

Each student, under the guidance of a Faculty, is required to

- Choose, preferably, a recent topic of his/her interest relevant to the Course of Specialization.
- Carryout literature survey, organize the Course topics in a systematic order.
- Prepare the report with own sentences.
- Type the matter to acquaint with the use of Micro-soft equation and drawing tools or any such facilities.
- Present the seminar topic orally and/or through power point slides.
- Answer the queries and involve in debate/discussion.
- Submit two copies of the typed report with a list of references.

The participants shall take part in discussion to foster friendly and stimulating environment in which the students are motivated to reach high standards and become self-confident.

The Internal Assessment marks for the seminar shall be awarded (based on the relevance of the topic, presentation skill, participation in the question and answer session and quality of report) by the committee constituted for the purpose by the Head of the Department. The committee shall consist of three faculties from the department with the senior most acting as the Chairman.

Marks distribution for internal assessment of the course 16EMS27 seminar:

Seminar Report: 30 marks Presentation skill:50 marks Ouestion and Answer:20 marks

Graduate Attributes (As per NBA):

Engineering Knowledge, Problem Analysis, Design / development of solutions, Conduct investigations of complex Problems, Modern Tool Usage, Engineers and society, Environment and sustainability, Ethics, Individual and Team work, Communication.

VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI SCHEME OF TEACHING AND EXAMINATION - 2016-17 M.Tech MICROELECTRONICS AND CONTROL SYSTEMS (EMS) CHOICE BASED CREDIT SYSTEM (CBCS)

III SEMESTER

			Teaching l	Hours /Week	Examination				
Sl. No	Course Code	Title	Theory	Practical/ Field work/ Assignment	Duration in hours	I.A. Marks	Theory/ Practical Marks	Total Marks	Credits
1	16EMS31	Seminar / Presentation on Internship (After 8 weeks from the date of commencement)				25		25	20
2	16EMS32	Report on Internship				25		25	
3	16EMS33	Evaluation and Viva- Voce of Internship			I	-	75	75	
4	16EMS34	Evaluation of Project phase -1				50		50	1
	ŗ	ГОТАL				100	75	175	21

Number of credits completed at the end of III semester: 22+22+21=65

Note:

Internship of 16 weeks shall be carried out during III semester.

Major part of the Project work shall also be carried out during the III semester in consultation with the Guide/s.

VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI SCHEME OF TEACHING AND EXAMINATION - 2016-17 M.Tech MICROELECTRONICS AND CONTROL SYSTEMS (EMS) CHOICE BASED CREDIT SYSTEM (CBCS)

IV SEMESTER

			Teaching Hours /Week		Examination				
Sl. No	Course Code	Title	Theory	Practical/ Field work/ Assignment	Duration in hours	I.A. Marks	Theory/ Practical Marks	Total Marks	Credits
1	16EMS41	Industrial Control Technology - 2	04		03	20	80	100	4
2	16EMS42X	Elective - 3	03		03	20	80	100	3
3	16EMS43	Evaluation of Project phase - 2				50	-	50	3
4	16EMS44	Evaluation of Project and Viva-Voce			03	-1	100 + 100	200	10
		TOTAL	07		09	90	360	450	20

Number of credits completed at the end of IV semester: 22+22+21+20=85

Elective -1				
Course Code under 16EMS42X Title				
16EMS421	Industrial Control - Software and Routines			
16EMS422	Digital System Design with FPGA			
16EMS423	Microelectronic Fabrication			
16EMS424	Reset Control Systems			

Note: 1. Project Phase-1: 6-week duration shall be carried out between 2nd and 3rd Semester vacation. Candidates in consultation with the guide shall carry out literature survey/ visit industries to finalize the topic of Project.

- **2. Project Phase-2:** 16-week duration during 4th semester. Evaluation shall be done by the committee comprising of HoD as Chairman, Guide and Senior faculty of the department.
- **3. Project Evaluation**: Evaluation shall be taken up at the end of 4th semester. Project work evaluation and Viva-Voce examination shall conducted
- 4. Project evaluation:
 - a. Internal Examiner shall carry out the evaluation for 100 marks.
 - b. External Examiner shall carry out the evaluation for 100 marks.
 - c .The average of marks allotted by the internal and external examiner shall be the final marks of the project evaluation.
 - d. Viva-Voce examination of Project work shall be conducted jointly by Internal and External examiner for 100 marks.

M.TECH MICROELECTRONICS AND CONTROL SYSTEMS (EMS) CHOICE BASED CREDIT SYSTEM (CBCS) **SEMESTER - IV** INDUSTRIAL CONTROL TECHNOLOGY - 2 (Core Course) Course Code 20 16EMS41 IA Marks Number of Lecture Hours/Week 04 **Exam Hours** 03 Total Number of Lecture Hours 50 Exam Marks 80 Credits - 04

- To explain the industrial intelligent controllers necessary for both industrial production control and industrial process control; PLC controllers, CNC controllers, and fuzzy-logic controllers.
- To explain industrial process controllers, including PID controllers, batch process controllers and servo motion controllers.
- To explain industrial motherboards, industrial personal computers, computer peripherals and accessories.
- To introduces the layer model, architectures, components, functions and applications of several primary industrial control networks: CAN, SCADA, Ethernet, Device Net, LAN, and other enterprise networks.
- To explain networking devices, including networking hubs, switches, routers, bridges, gateways, repeaters and key techniques used in these networking devices. ■

Module-1		Teaching Hours
Industrial Intellige	ent Controllers: PLC (Programmable Logic Control) Controllers, CNC	10
(Computer Numeric	cal Control) Controllers, FLC (Fuzzy Logic Control) Controllers.	
Revised Bloom's	L_1 – Remembering, L_2 – Understanding.	
Taxonomy Level		
Module-2		
Industrial Process	Controllers: PID (Proportional-Integral-Derivative) Controllers, BPC (Batch	10
Process Control) Co	ontrollers, SMC (Servo Motion Control) Controllers.	
Industrial Compu	ters: Introduction, Industrial Computer Classes and Configurations, Industrial	
_	als and Accessories. ■	
Revised Bloom's	L_1 – Remembering, L_2 – Understanding.	
Taxonomy Level	5, - 5	
Module-3		L
3Industrial Contro	ol Networks: Controller Area Network (CAN), Supervisory Control and Data	10
Acquisition (SCAE	A) Network, Industrial Ethernet Network, Industrial Enterprise Networks.	
Acquisition (SCAL	A) Network, maustral Ethernet Network, maustral Enterprise Networks.	
Revised Bloom's	•	
• `	L_1 – Remembering, L_2 – Understanding.	
Revised Bloom's	•	
Revised Bloom's Taxonomy Level Module-4	•	10
Revised Bloom's Taxonomy Level Module-4	L_1 – Remembering, L_2 – Understanding.	10
Revised Bloom's Taxonomy Level Module-4 Networking Devic Revised Bloom's	L ₁ – Remembering, L ₂ – Understanding. es: Hubs and Switches, Network Routers, Bridges, Gateways and Repeaters. ■	10
Revised Bloom's Taxonomy Level Module-4 Networking Devic Revised Bloom's Taxonomy Level Module-5	L ₁ – Remembering, L ₂ – Understanding. es: Hubs and Switches, Network Routers, Bridges, Gateways and Repeaters. ■	
Revised Bloom's Taxonomy Level Module-4 Networking Devic Revised Bloom's Taxonomy Level Module-5 Human-machine in	es: Hubs and Switches, Network Routers, Bridges, Gateways and Repeaters. ■ L ₁ − Remembering, L ₂ − Understanding. Interfaces: Human–Machine Interactions, User–Machine Interfaces, Industrial	10
Revised Bloom's Taxonomy Level Module-4 Networking Devic Revised Bloom's Taxonomy Level Module-5 Human-machine in Application Examp	es: Hubs and Switches, Network Routers, Bridges, Gateways and Repeaters. ■ L ₁ − Remembering, L ₂ − Understanding. Interfaces: Human–Machine Interactions, User–Machine Interfaces, Industrial	
Revised Bloom's Taxonomy Level Module-4 Networking Devic Revised Bloom's Taxonomy Level Module-5 Human-machine in Application Examp	es: Hubs and Switches, Network Routers, Bridges, Gateways and Repeaters. L₁ – Remembering, L₂ – Understanding. L₁ – Remembering, L₂ – Understanding. Interfaces: Human–Machine Interactions, User–Machine Interfaces, Industrial les. In Interfaces: Data Transmission Basics, Data Transmission I/O Devices, Data	
Revised Bloom's Taxonomy Level Module-4 Networking Devic Revised Bloom's Taxonomy Level Module-5 Human-machine is Application Examp Data Transmission	es: Hubs and Switches, Network Routers, Bridges, Gateways and Repeaters. L₁ – Remembering, L₂ – Understanding. L₁ – Remembering, L₂ – Understanding. Interfaces: Human–Machine Interactions, User–Machine Interfaces, Industrial les. In Interfaces: Data Transmission Basics, Data Transmission I/O Devices, Data	

M.TECH MICROELECTRONICS AND CONTROL SYSTEMS (EMS) 16EMS41 INDUSTRIAL CONTROL TECHNOLOGY - 2 (Core Course) (continued) CHOICE BASED CREDIT SYSTEM (CBCS)

Course outcomes:

At the end of the course the student will be able to:

- Explain the industrial intelligent controllers necessary for both industrial production control and industrial process control.
- Explain industrial process controllers, including PID controllers, batch process controllers and servo motion controllers.
- Explain industrial motherboards, industrial personal computers, computer peripherals and accessories.
- Discuss the layer model, architectures, components, functions.
- Discuss applications of several primary industrial control networks: CAN, SCADA, Ethernet, DeviceNet, LAN, and other enterprise networks.
- Explain networking devices, including networking hubs, switches, routers, bridges, gateways, repeaters and key techniques used in these networking devices.
- Describe interfaces existing in industrial control systems namely human machine interfaces and data transmission interfaces.

Graduate Attributes (As per NBA):

Engineering Knowledge, Problem Analysis.

Question paper pattern:

- The question paper will have ten questions.
- Each full question is for 16 marks.
- There will be 2 full questions (with a maximum of four sub questions in one full question) from each module.
- Each full question with sub questions will cover the contents under a module.
- Students will have to answer 5 full questions, selecting one full question from each module.

Text Book 1 Advanced Industrial Control Technology Peng Zhang Elsevier 2010

M.TECH MICROELECTRONICS AND CONTROL SYSTEMS (EMS) CHOICE BASED CREDIT SYSTEM (CBCS) **SEMESTER - IV** INDUSTRIAL CONTROL - SOFTWARE AND ROUTINES (Elective Course) Course Code 20 16EMS421 IA Marks Number of Lecture Hours/Week 03 **Exam Hours** 03 Total Number of Lecture Hours 40 Exam Marks 80 Credits - 03

Course objectives:

- To explain the firmware of a microprocessor chipset.
- To explain all the details of real-time operating systems, which are the platforms needed for a control system to satisfy real-time criteria.
- To explain the distributed operating system, the necessary platform for distributed control systems.
- To explain industrial system operation routines, including the self-test routines at power-on and power-down, installation and configuration routines, diagnostic routines, and calibration routines.
- To discuss the identification principles and techniques for model-based control.

		m 1.
Module-1		Teaching Hours
Microprocessor B	oot Code: Code Structures, Single-Processor Boot Sequences, Multiprocessor	08
Boot Sequences.		
	ing Systems: Introduction, Task Controls, Input /Output Device Drivers. ■	
Revised Bloom's Taxonomy Level	L_1 – Remembering, L_2 – Understanding.	
Module-2		
Real-Time Operat	ing Systems (continued): Interrupts, Memory Management, Event Brokers,	08
Message Queue, Se	maphores, Timer.	
Revised Bloom's	L_1 – Remembering, L_2 – Understanding.	
Taxonomy Level		
Module-3		
Distributed Opera	ting Systems: Multiprocessor Operating Systems, Multicomputer Operating	08
Systems, Distributed and Parallel Facilities. ■		
Revised Bloom's	L_1 – Remembering, L_2 – Understanding.	
Taxonomy Level		
Module-4		
Industrial Control	System Operation Routines: Self-Test Routines, Install and Configure Routines,	08
Diagnosis Routines	, Calibration Routines. ■	
Revised Bloom's Taxonomy Level	L_1 – Remembering, L_2 – Understanding.	
Module-5		•
Industrial Contro	System Simulation Routines: Modelling and Identification, Simulation and	08
Control, Software and Simulator. ■		
Revised Bloom's	L_1 – Remembering, L_2 – Understanding.	
Taxonomy Level		
	·	

Course outcomes:

At the end of the course the student will be able to:

- Explain the Microprocessor boot code, one of the key component of Embedded software for control purpose.
- Explain in detail the real-time operating systems, which are the platforms needed for a control system to satisfy real-time criteria.
- Explain the distributed operating system, the necessary platform for distributed control systems.
- Explain industrial system operation routines, including the self-test routines at power-on and power-down, installation and configuration routines, diagnostic routines, and calibration routines.
- Discuss the identification principles and techniques for model-based control.

M.TECH MICROELECTRONICS AND CONTROL SYSTEMS (EMS) 16EMS421 INDUSTRIAL CONTROL - SOFTWARE AND ROUTINES (Elective Course) (continued) CHOICE BASED CREDIT SYSTEM (CBCS)

Graduate Attributes (As per NBA):

Engineering Knowledge, Problem Analysis, Modern Tool Usage, Engineers and society, Environment and sustainability, Ethics.

Question paper pattern:

- The question paper will have ten questions.
- Each full question is for 16 marks.
- There will be 2 full questions (with a maximum of four sub questions in one full question) from each module.
- Each full question with sub questions will cover the contents under a module.
- Students will have to answer 5 full questions, selecting one full question from each module.

Text	Book			
1	Advanced Industrial Control Technology	Peng Zhang	Elsevier	2010

M.TECH MICROELECTRONICS AND CONTROL SYSTEMS (EMS) CHOICE BASED CREDIT SYSTEM (CBCS) SEMESTER - IV					
DIGITAL SYSTEM DESIGN WITH FPGA (Elective Course)					
Course Code	16EMS422	IA Marks	20		
Number of Lecture Hours/Week 03 Exam Hours 03					
Total Number of Lecture Hours 40 Exam Marks 80					
Cradits - 03					

- To introduce the programmable logic devices, their differing architectures, and their use within electronic system design.
- To explain the terminology used, design methods and tools.
- To discuss programming languages that can be used to develop digital designs for implementation in either a processor or in programmable logic.
- To discuss electronic systems design, the types of solutions that can be developed, and the decisions that will need to be made in order to identify the right technology choice for the design implementation.
- To introduce VHDL as hardware description language to describe digital circuit and system designs in an ASCII text-based format.
- To explain the testing of the electronic system.
- To discuss interfacing of programmable logic to the analogue world and power electronics circuits.
- To explain with a case study the necessity to develop programmable logic—based designs at a high level of abstraction using behavioral descriptions of the system functionality. ■

M.TECH MICROELECTRONICS AND CONTROL SYSTEMS (EMS)	
16EMS422 DIGITAL SYSTEM DESIGN WITH FPGA (Elective Course) (continued)	
CHOICE BASED CREDIT SYSTEM (CBCS)	
	<i>a</i> 1.
Module-4	Teaching
	Hours
Introduction to Digital Logic Design with VHDL (continued): Sequential Logic Design, Memories	08
Unsigned versus Signed Arithmetic - Adder Example. Multiplier Example.	
Testing the Design: Introduction, Integrated Circuit Testing, Printed Circuit Board Testing, Boundary	
Scan Testing, Software Testing. ■	
Scali Testing, Software Testing.	
Revised Bloom's L_4 – Remembering L_2 – Understanding L_3 – Applying L_4 – Analysing	
El Remembering, Ez Gracistanding, E3 Tippijing, E4 Thaijing.	
Taxonomy Level	
Module-5	
Digital-to-Analogue Conversion, and Power Electronics: Introduction, Digital-to-Analogue	08
Conversion, Analogue-to-Digital Conversion, Power Electronics, Heat Dissipation and Heat sinks.	
Operational Amplifier Circuits.	

Course outcomes:

Revised Bloom's

Taxonomy Level

At the end of the course the student will be able to:

• Discuss programmable logic devices that are available today, their architectures, their use within electronic system design and the terminology used.

 L_1 – Remembering, L_2 – Understanding, L_3 – Applying, L_4 – Analysing.

- Discuss different programming languages that are used to develop digital designs for implementation in either a processor or in programmable logic.
- Explain designing of electronic systems, the types of solutions that can be developed, and the decisions that will need to be made in order to identify the right technology choice for the design implementation.
- Describe digital circuit and system designs in an ASCII text-based format using VHDL.
- Test the electronic systems for failure mechanisms in hardware and software.
- Interface programmable logic devices to the analogue world.

System-Level Design: Introduction, Case Study-DC Motor Control. ■

• Explain with a case study the necessity to develop programmable logic—based designs at a high level of abstraction using behavioral descriptions of the system functionality. ■

Graduate Attributes (As perNBA):

Engineering Knowledge, Problem Analysis, Design / development of solutions, Conduct investigations of complex Problems, Modern Tool Usage, Ethics, Communication.

Question paper pattern:

- The question paper will have ten questions.
- Each full question is for 16 marks.
- There will be 2 full questions (with a maximum of four sub questions in one full question) from each module.
- Each full question with sub questions will cover the contents under a module.
- Students will have to answer 5 full questions, selecting one full question from each module.

Text Book 1 Digital Systems Design with FPGAs and CPLDs Ian Grout Elsevier 2008

M.TECH MICROELECTRONICS AND CONTROL SYSTEMS (EMS) CHOICE BASED CREDIT SYSTEM (CBCS) SEMESTER - IV					
MICROELECTRONIC FABRICATION (Elective Course)					
Course Code 16EMS423 IA Marks 20					
Number of Lecture Hours/Week 03 Exam Hours 03					
Total Number of Lecture Hours 40 Exam Marks 80					
Cradits - 03					

- To explain the basic processes of fabrication of monolithic integrated –circuit and steps in lithographic process, including mask fabrication, photoresist process and etching.
- To explain the theory of oxide growth, techniques for selective oxidation of silicon, methods to determine the thickness of oxide film and process simulation.
- To explain theoretical and practical aspects of diffusion process and diffusion systems, the characterization of diffused layer sheet resistance and determination of junction depth.
- To explain the process of ion implementation, mathematical modelling of the impurity distributions, and the removal of crystal damage due to implantation process.
- To explain deposition processes, including evaporation, chemical vapour deposition and sputtering.
- To discuss interconnections and the problems associated with making good contacts between metal and silicon.
- To discuss the liftoff process, multilevel metallization, copper interconnects, and Damascene process.
- To discuss testing, die separation, attachment, wire bonding, packages used with integrated circuits and MOS process design.
- To discuss interconnections between fabrication processes, bipolar device design and layout.
- To discuss processes for fabrication of microelectromechanical elements in silicon.

- 10 discuss	processes for fabrication of interoelectronic flaments in sincon.			
Module-1		Teaching Hours		
Introduction: Histo	orical Perspective, Overview of Monolithic Fabrication, Metal – Oxide	08		
Semiconductor (MOS) Process, Basic Bipolar Process, Safety.				
Lithography: The Photolithographic Process, Etching Techniques, Photomask Fabrication,				
Exposure Systems, Exposure Sources, Optical and Electron Microscopy.				
	n of Silicon: The Oxidation Process, Modelling Oxidation, Factors Influencing			
	pant Redistribution during Oxidation, Masking Properties of Silicon Dioxide,			
	lation, Oxide Quality, Selective Oxidation and Shallow Trench Formation, Oxide			
	rization, Process Simulation. ■			
Revised Bloom's Taxonomy Level	L_1 – Remembering, L_2 – Understanding.			
Module-2				
Diffusion: The Diff	fusion Process, Mathematical Model for Diffusion, The Diffusion Coefficient,	08		
Successive Diffusion	ons, Solid – Solubility Limits, Junction Formation and Characterization, Sheet			
Resistance, Generat	tion – Depth and Impurity Profile Measurement, Diffusion Simulation, Diffusion			
Systems, Gettering. ■				
Revised Bloom's	L_1 – Remembering, L_2 – Understanding.	1		
Taxonomy Level				
Module-3		l		
Ion Implantation:	Implantation Technology, Mathematical Model for Ion Implantation, Selective	08		
Implantation, Juncti Shallow Implantation	ion Depth and Sheet Resistance, Channeling, Lattice, Damage and Annealing,			
	Evaporation, Sputtering, Chemical Vapour Deposition, Epitaxy.			
	nd Contacts: Interconnections in Integrated Circuits, Metal Interconnections and			
Contact Technology, Diffused Interconnections, Polysilicon Interconnections and Buried Contacts,				
Silicides and Multilayer – Contact Technology, The Liftoff Process, Multilevel Metallization, Copper				
Interconnects and Damascene Process. ■				
Revised Bloom's Taxonomy Level	L_1 – Remembering, L_2 – Understanding.			
		•		

1,100001	16EMS423 MICROELECTRONIC FABRICATION (Elective Course) (continued) CHOICE BASED CREDIT SYSTEM (CBCS)	Teaching
Packages, Flip – Chip and tape – Automated – Bonding Process, Yield. MOS Process Integration: Basic MOS Device Considerations, MOS Transistor Layout and Design Rules, Complementary MOS (CMOS) Technology, Silicon on Insulator. ■ Revised Bloom's Taxonomy Level L₁ – Remembering, L₂ – Understanding. Module-5 Bipolar Process Integration: The Junction – Isolated Structure, Current Gain, Transit Time, Base Width, Breakdown Voltages, Other Elements in SBC Technology, Layout Considerations, Advanced Bipolar Structure, Other Bipolar Insulation Techniques, BICMOS. Process for Microelectromechanical Systems (MEMS): Mechanical Properties of Silicon, Bulk Micromachining, Silicon Etchants, Surface Micromachining, High – Aspect – Ratio	Module-4	Hours
Module-5 Bipolar Process Integration: The Junction – Isolated Structure, Current Gain, Transit Time, Base Width, Breakdown Voltages, Other Elements in SBC Technology, Layout Considerations, Advanced Bipolar Structure, Other Bipolar Insulation Techniques, BICMOS. Process for Microelectromechanical Systems (MEMS): Mechanical Properties of Silicon, Bulk Micromachining, Silicon Etchants, Surface Micromachining, High – Aspect – Ratio	Packages, Flip – Chip and tape – Automated – Bonding Process, Yield. MOS Process Integration: Basic MOS Device Considerations, MOS Transistor Layout and Design Rules, Complementary MOS (CMOS) Technology, Silicon on Insulator. ■ Revised Bloom's L₁ – Remembering, L₂ – Understanding.	08
Width, Breakdown Voltages, Other Elements in SBC Technology, Layout Considerations, Advanced Bipolar Structure, Other Bipolar Insulation Techniques, BICMOS. Process for Microelectromechanical Systems (MEMS): Mechanical Properties of Silicon, Bulk Micromachining, Silicon Etchants, Surface Micromachining, High – Aspect – Ratio		
Revised Bloom's L_1 – Remembering, L_2 – Understanding.	Width, Breakdown Voltages, Other Elements in SBC Technology, Layout Considerations, Advanced Bipolar Structure, Other Bipolar Insulation Techniques, BICMOS. Process for Microelectromechanical Systems (MEMS): Mechanical Properties of Silicon, Bulk Micromachining, Silicon Etchants, Surface Micromachining, High – Aspect – Ratio Micromachining, Silicon Wafer Bonding, IC Process Compatibility.	08

Course outcomes:

Taxonomy Level

At the end of the course the student will be able to:

- Explain the basic processes of fabrication of monolithic integrated –circuit and basic steps in lithographic process.
- Discuss the theory of oxide growth, oxide growth processes, factors affecting the growth rate, impurity redistribution during oxidation.
- Explain techniques for selective oxidation of silicon, methods to determine the thickness of oxide film and process simulation.
- Explain theoretical and practical aspects of diffusion process and diffusion systems, the characterization of diffused layer sheet resistance and determination of junction depth.
- Discuss ion implementation technology, mathematical modelling of the impurity distributions, and the removal of crystal damage due to implantation process.
- Explain deposition processes and interconnections.
- Discuss packaging and associated processes with integrated circuits and MOS process integration.
- Discuss bipolar process integration and processes for fabrication of microelectromechanical elements in silicon.

Graduate Attributes (As per NBA):

Engineering Knowledge, Problem Analysis, Conduct investigations of complex Problems, Communication.

Question paper pattern:

- The question paper will have ten questions.
- Each full question is for 16 marks.
- There will be 2 full questions (with a maximum of four sub questions in one full question) from each module.
- Each full question with sub questions will cover the contents under a module.
- ▶ Students will have to answer 5 full questions, selecting one full question from each module. ■

Text Book 1 Introduction to Microelectronic Fabrication Richard C Jaeger Prentice Hall 2nd Edition, 2002

M.TECH MICROELECTRONICS AND CONTROL SYSTEMS (EMS) CHOICE BASED CREDIT SYSTEM (CBCS) SEMESTER - IV					
RESET CONTROL SYSTEMS (Elective Course)					
Course Code	16EMS424	IA Marks	20		
Number of Lecture Hours/Week 03 Exam Hours 03					
Total Number of Lecture Hours 40 Exam Marks 80					
Credits - 03					

- To give basics and fundamental design concepts of Reset Control Systems.
- To derive the describing function of reset systems.
- To explain how the reset matrix affects the frequency domain property of HDD system.
- To explain stability analysis of Reset Control Systems.
- To discuss robust stability of RCSs with uncertainties, Quadratic stability and affine quadratic stability for systems with time-varying and constant uncertainties.
- To study robust stability for RCSs with time-delays.
- To study stability of RCSs with discrete-time reset conditions.
- To study stability of RCS with fixed reset time instants both moving horizon optimization and fixed horizon optimization.
- To discuss the application of optimal reset law design to HDD systems and PZT-positioning stage respectively.

• To discuss passivity and finite L2 gain stability of RCSs with conic jump sets. ■

Module-1		Teachin Hours		
Introduction: Mot	ivation of reset control, Basic concepts of RCSs, Fundamental theory of	08		
traditional reset design. ■				
Revised Bloom's Taxonomy Level	L_1 – Remembering, L_2 – Understanding.			
Module-2				
Describing function analysis of reset systems: Sinusoid input response, Describing function, Application to HDD systems. ■				
Revised Bloom's Taxonomy Level	Remembering, L_2 - Understanding, L_3 - Applying, L_4 - Analyzing.			
Module-3				
Stability of reset control systems: Preliminaries, Quadratic stability, Stability of RCSs with timedelay, Reset times-dependent stability, Passivity of RCSs. ■				
•				
Revised Bloom's Taxonomy Level	Remembering, L_2 - Understanding, L_3 - Applying, L_4 - Analyzing.			
	Remembering, L_2 - Understanding, L_3 - Applying, L_4 - Analyzing.			
Taxonomy Level Module-4 Robust stability of quadratic stability, RCSs with discret	Remembering, L₂ - Understanding, L₃ - Applying, L₄ - Analyzing. f reset control systems: Definitions and assumptions, Quadratic stability, Affine Robust stability of RCS with time-delay, Examples. e-time reset conditions: Preliminaries and problem setting, Stability analysis, A thod, Application to track-seeking control of HDD systems.	08		
Taxonomy Level Module-4 Robust stability of quadratic stability, RCSs with discret	f reset control systems: Definitions and assumptions, Quadratic stability, Affine Robust stability of RCS with time-delay, Examples. e-time reset conditions: Preliminaries and problem setting, Stability analysis, A	08		
Module-4 Robust stability of quadratic stability, RCSs with discret heuristic design me Revised Bloom's	f reset control systems: Definitions and assumptions, Quadratic stability, Affine Robust stability of RCS with time-delay, Examples. e-time reset conditions: Preliminaries and problem setting, Stability analysis, A thod, Application to track-seeking control of HDD systems. ■	08		
Taxonomy Level Module-4 Robust stability of quadratic stability, RCSs with discret heuristic design me Revised Bloom's Taxonomy Level Module-5 Reset control system Optimal reset law of the re	f reset control systems: Definitions and assumptions, Quadratic stability, Affine Robust stability of RCS with time-delay, Examples. e-time reset conditions: Preliminaries and problem setting, Stability analysis, A thod, Application to track-seeking control of HDD systems. ■	08		

M.TECH MICROELECTRONICS AND CONTROL SYSTEMS (EMS) 16EMS424 RESET CONTROL SYSTEMS (Elective Course) (continued) CHOICE BASED CREDIT SYSTEM (CBCS)

Course outcomes:

At the end of the course the student will be able to:

- Explain design concepts of Reset Control Systems.
- Explain the describing function of reset systems and the effects of reset matrix on the frequency domain property of HDD system.
- Perform stability analysis of Reset Control Systems.
- Explain robust stability, Quadratic stability and affine quadratic stability for reset control systems.
- Perform stability study of RCSs with discrete-time reset conditions.
- Perform stability study stability of RCS with fixed reset time instants both moving horizon optimization and fixed horizon optimization
- Discuss the application of optimal reset law design to HDD systems and PZT-positioning stage.
- Discuss passivity and finite L_2 gain stability of RCSs with conic jump sets. \blacksquare

Graduate Attributes (As per NBA):

Engineering Knowledge, Problem Analysis, Conduct investigations of complex Problems.

Question paper pattern:

- The question paper will have ten questions.
- Each full question is for 16 marks.
- There will be 2 full questions (with a maximum of four sub questions in one full question) from each module.
- Each full question with sub questions will cover the contents under a module.
- Students will have to answer 5 full questions, selecting one full question from each module.

Text Book						
1	Analysis and Design of Reset Control Systems	Yuqian Guo et al	IET	2015		